



SVM PANEL FACEPLATE

Within the HSDCU the grounding is S&EA's responsibility, and the formal specifications are at its external I/Fs but the unit shall not emit more CM noise than the grounding partitioning shown would imply

All the RED lettered items have digital drives. Except for BiasD/As they are linked to BOTH prime and redundant FPGAs

**HERSCHEL SPIRE
GROUNDING SCHEME**
JD 16th September 2002
Bolometer analogue chassis
links omitted pending Review

