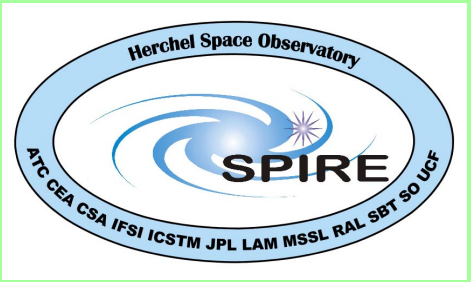


GROUNDING REVIEW

Introduction

Dr. John **Delderfield**

SPIRE SYSTEMS ENGINEER

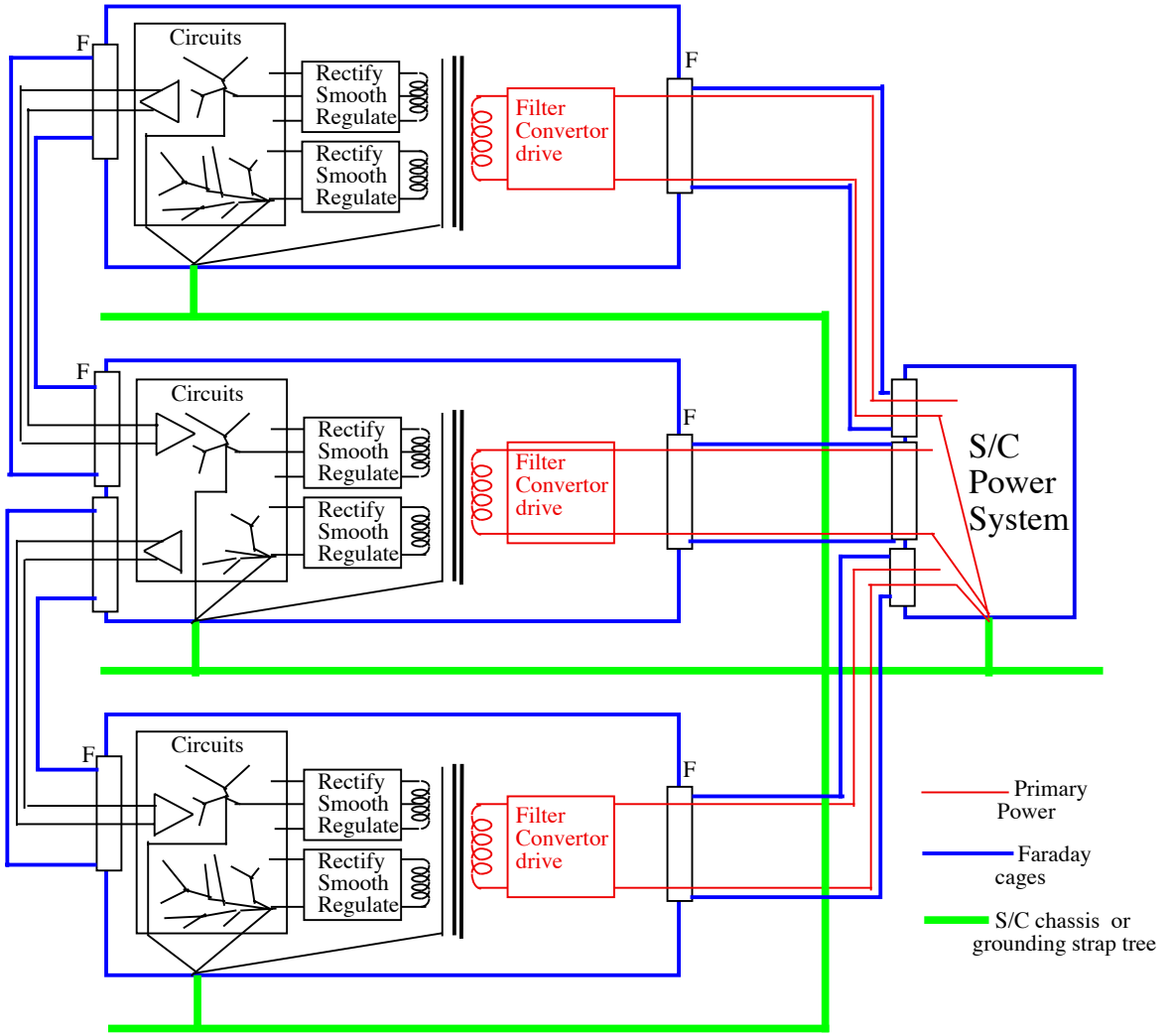
- Grounding and EMC have always been recognised as critical areas for the correct operation of SPIRE.
- A top level controlled instrument document, SPIRE Grounding Philosophy, **SPIRE-RAL-PRJ-00624** include discussion and reasons rather than just being a list of tabulated requirements.
- This document contains the SPIRE System grounding diagram, which is repeated in the IID-B.
- The process of optimising the grounding/screening has involved discussions between JPL, CEA & RAL, plus inputs from the Herschel Plank Working Group (linked by Doug Griffin).
- The requirements and to some extent the implementation have been confirmed, reviewed and agreed at SPIRE's major milestone ESA reviews.

- Overview of SPIRE Project Progress
- Summary of SPIRE grounding

SPIRE Project Progress

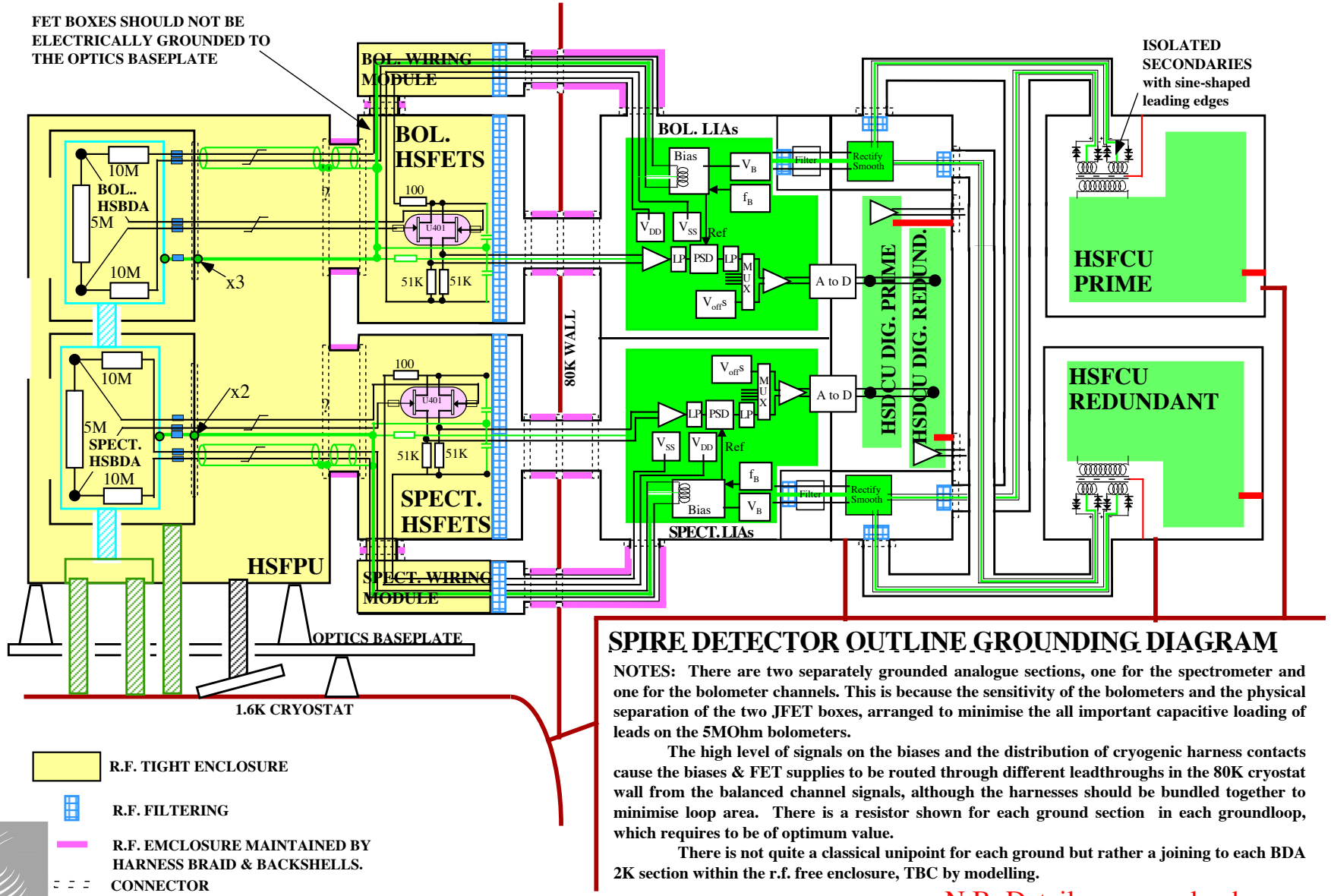
Position at Instrument Intermediate Design Review, April 2001

SIMPLISTIC GROUNDING



Electrical Design and Grounding Scheme

Dr. John Delderfield



SPIRE DETECTOR OUTLINE GROUNDING DIAGRAM

NOTES: There are two separately grounded analogue sections, one for the spectrometer and one for the bolometer channels. This is because the sensitivity of the bolometers and the physical separation of the two JFET boxes, arranged to minimise the all important capacitive loading of leads on the 5MOhm bolometers.

The high level of signals on the biases and the distribution of cryogenic harness contacts cause the biases & FET supplies to be routed through different leadthroughs in the 80K cryostat wall from the balanced channel signals, although the harnesses should be bundled together to minimise loop area. There is a resistor shown for each ground section in each groundloop, which requires to be of optimum value.

There is not quite a classical unipoint for each ground but rather a joining to each BDA 2K section within the r.f. free enclosure, TBC by modelling.

N.B. Details now evolved

Electrical Design and Grounding Scheme

Dr. John Delderfield

- Grounding and EMC are design drivers for Spire.
- Bolometers must not receive wire or field-coupled stray energy
- FPU and JFETs form closed isolated Faraday cage
- DCU analogue sections very carefully coupled to this with attention to cryoharness detail: differential, screened, separate chassis and signal grounds, non-standard power-supply config., control of imbalances injected into signal ground/digital noise.
- Decided by discussion last November, but recently written up in SPIRE-RAL-PRJ-00624 to avoid ambiguities, etc.
- Details of system still to be tied down: DCU seals and screens, JFET backharness, power filter detail, etc.
- Approach: rigorous design, computer modelling, test.

Assumed EMI and Spurious Signal Culprits

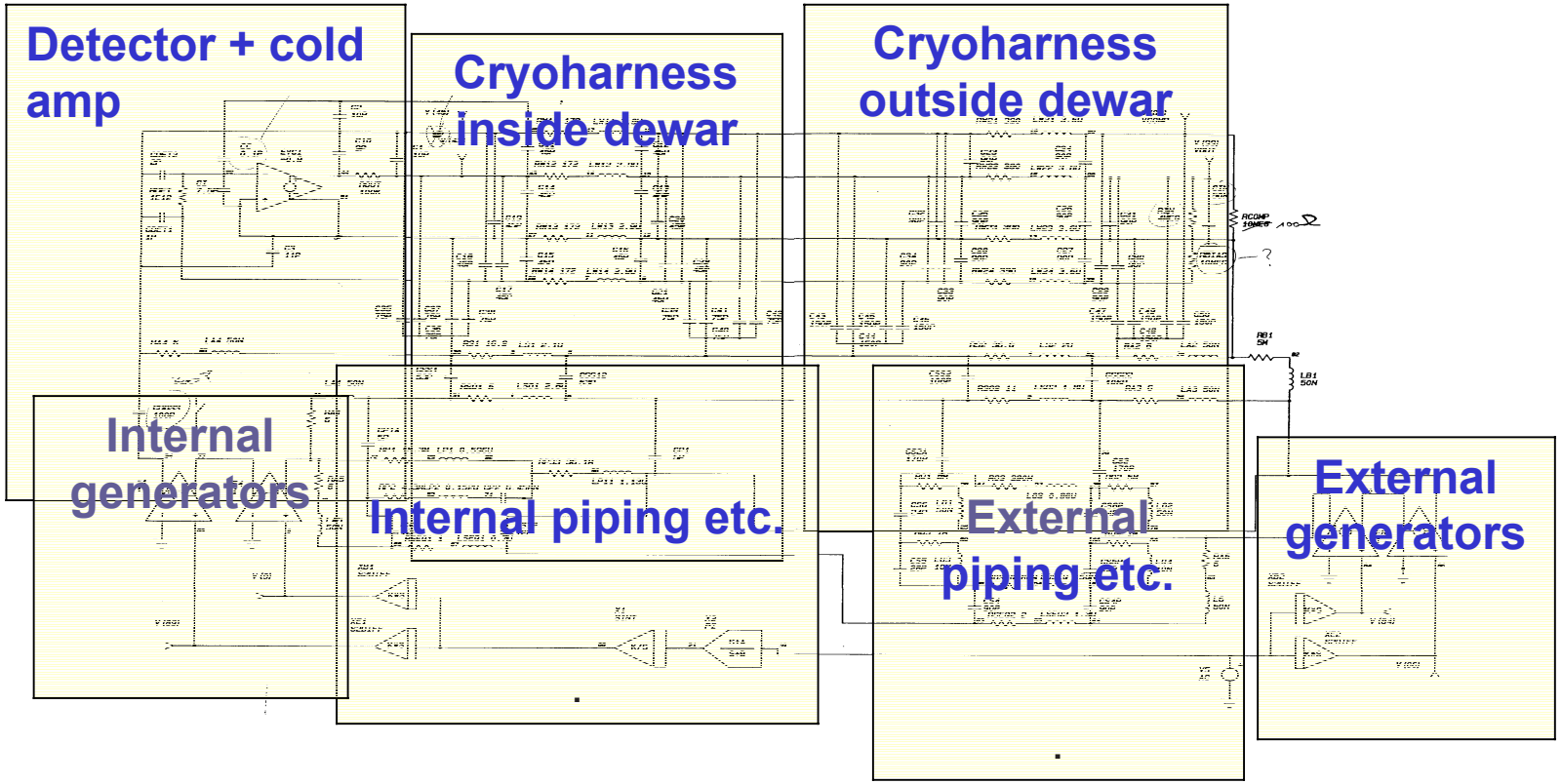
1. Radiated EM power reaching inside the CVV
   - Radio frequency E-fields
   - Low frequency B-fields
   - Sub-mm photons (straylight)
2. Conducted spurious currents and voltages
   - Direct signal corruption on to signal wires
   - RF capacitive couplings, e.g. between inner and outer braids
   - Indirect signal corruption via ohmic heating of the 5 MΩ bolometers
3. Microphonic disturbances to bolometer circuit
   - P/F and other P/L induced vibrations
   - SMEC
   - BSM
4. Bolometers and Harnesses
   - Inter-Channel Crosstalk !

Blue text added to slide for this grounding review, but not new info.

"Three Pronged" Analysis Approach

- Modelling
  - ***orcad*** model of the bolometer biasing and detection circuit
- Testing within RAL EMC facility
  - Detector harness shielding tightness
  - Detector harness microphonic susceptibility
  - Attenuation of FPU structure
  - Need for "chicken wire" filter at FPU entrance
- Testing of FPU structure in a representative CVV at ESTEC EMC Testing Facility

orcad modelling (3)
CVV Modelling



Testing within RAL EMC facility

- Facility
  - Constructed to MIL STD 461/462
  - 10 KHz to 1 GHz (10-30 V/m)
  - E-Fields and B-Fields
  - 1m x 1m x 1m space envelope
- A simple mock-up of the SPIRE Optical Bench and Photometer cover to be fabricated
  - Welded photometer cover
  - Cover screwed to optical bench
  - Internal light baffles to be included
- A receiving antenna is to be placed at the location of the photometer detector box.
- Representative detector harnesses are tested to determine level of signal pick-up.
- Wire mesh (“Chicken wire”) placed at the entrance to the FPU to determine need for and/or the effectiveness of extra shielding.

Future of SPIRE EMC

- Complete ***orcad*** simulations
- Complete EMC testing at RAL
- Complete ESTEC EMC testing in representative CVV

- High priority from systems view

  Science impact

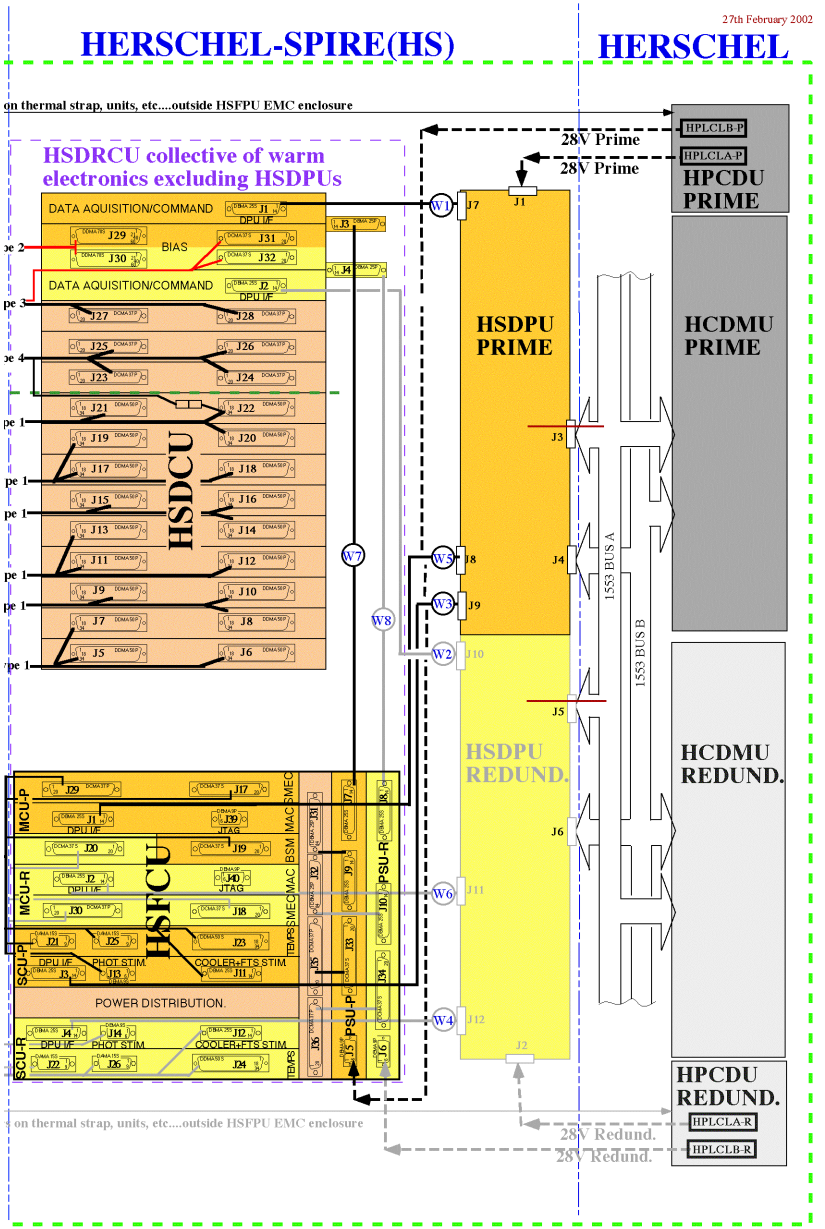
Schedule and budget implications

- To summarise, for SPIRE's IBDR in April 2001 there was a Baseline Grounding / EMC design in place, reviewed and agreed.
- This was fed down into sub-system requirements, for instance agreeing that the bolometers would be conditioned by SPIRE with chassis to analogue grounds joined at the cold end in JPL's SubSystem Specification Document.

- What progress had been made at the Instrument Baseline Design Review, March 2002?
- The SPIRE Harness Definition document (which includes the Cryoharness) and Instrument Block Diagram had been detailed almost to the state that they are in today.
- The Spire Grounding Philosophy document was further evolved after meetings with CEA to work through how the DRCU was being implemented, and discussed with JPL. Its issues were dated 24th August, 10th September and 24th September, & the last issue expanded the Grounding Diagram to include the CVV system and the HSFCU.

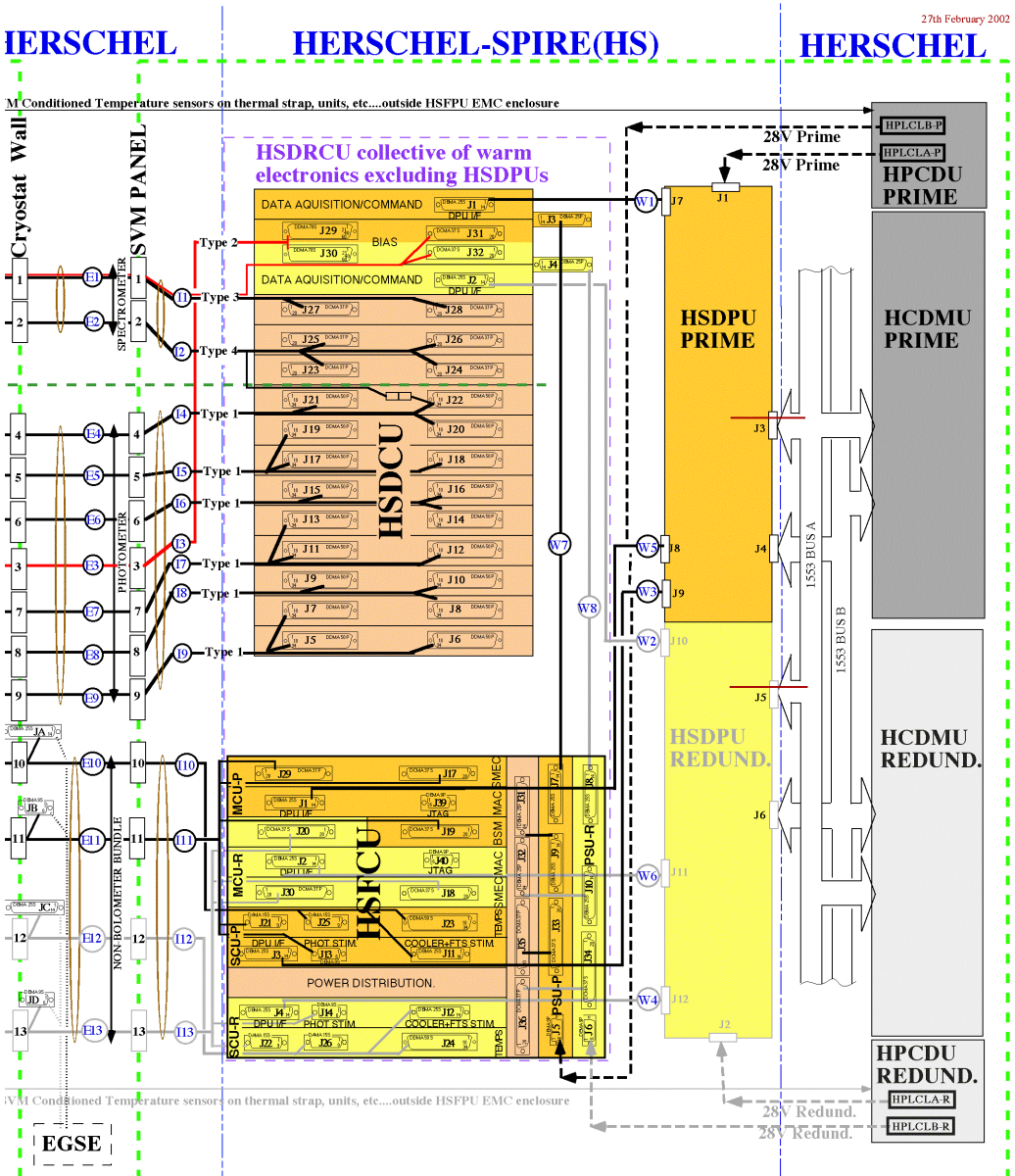
Warm Electronics

- HSDRCU=:
  - HSFCU with power supply is Prime and Redundant, only to be powered by Herschel to match the active HSDPU.
  - HSDCU has P/R bias generators and interfaces to HSDPU, but the remainder of the bolometer system is non-redundant.
- Supplied [with "W" harnesses] by CEA Saclay; SVM routings needed.
- HSDCU runs bolometers, baselined as either photometer or spectrometer. HSFCU runs the remainder of the SPIRE cryogenic sub-systems.
- Implementation subject to detailed design, particularly w.r.t. the power supply.
- Sizes now worked through but mass budget issues, see next presentation.

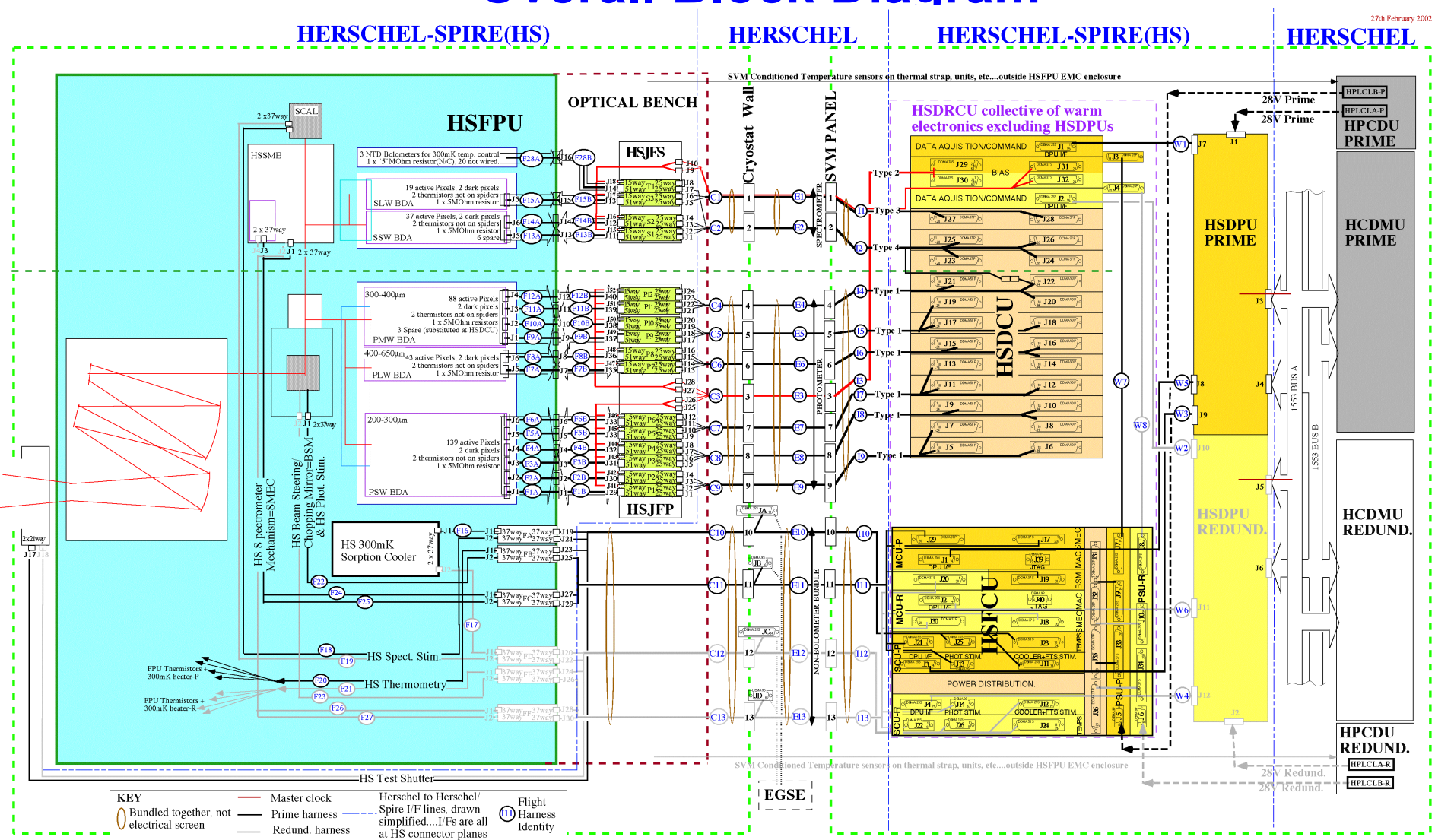


Harness Outside CVV

- Warm electronics+Herschel harness from HSDRCU to connectors on CVV.
- SPIRE instrument pin-out details now all sorted.
- “I” harness definition little changed from issue 8, but now copper (as for ground-test harness being made).
- “E” harness inserted to finish on SVM panel . 13off, mechanically simple links.
- Launch latch confirmation and shutter operation conns. moved to CVV skin position.
- Note brown bundling of wire groups to minimise R.F. loops



Overall Block Diagram

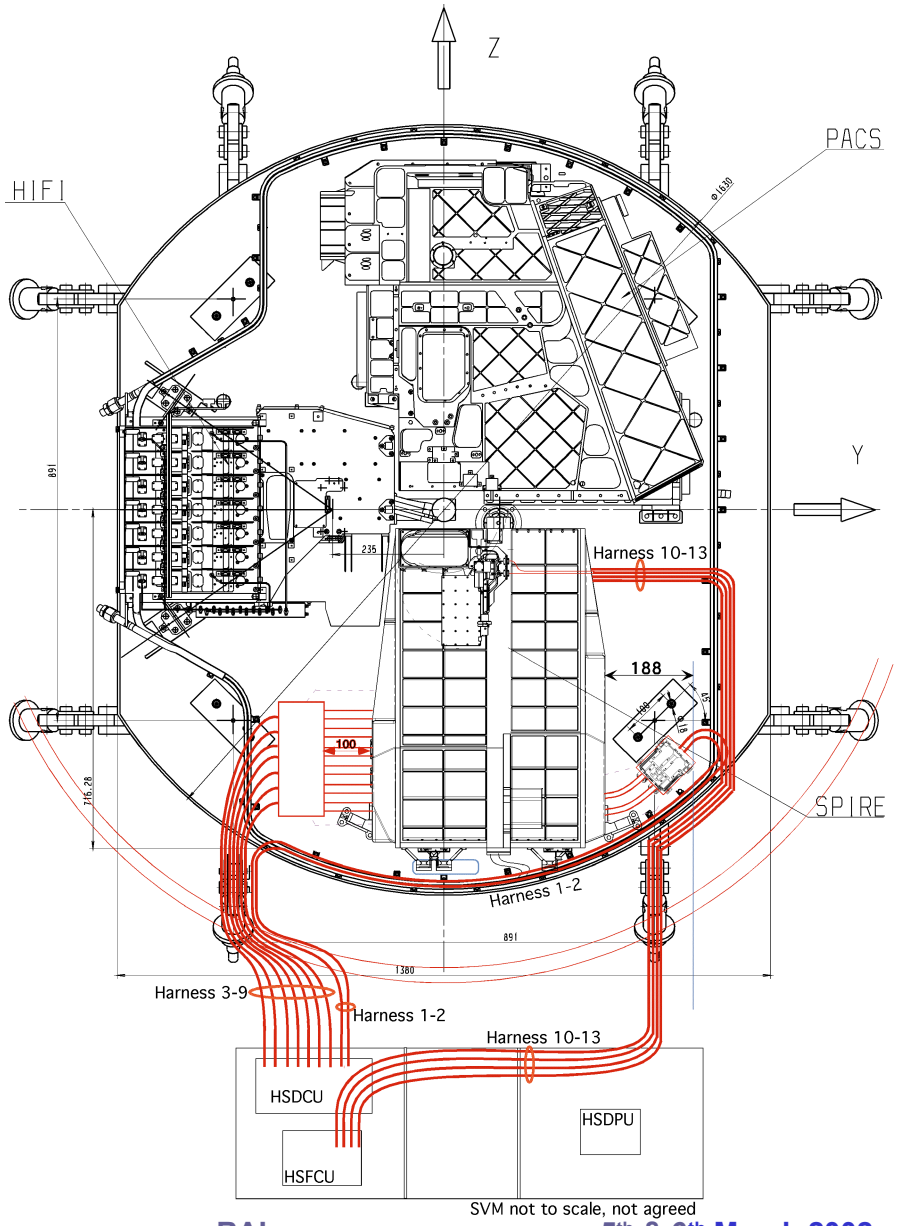


Electrical I/F Comments

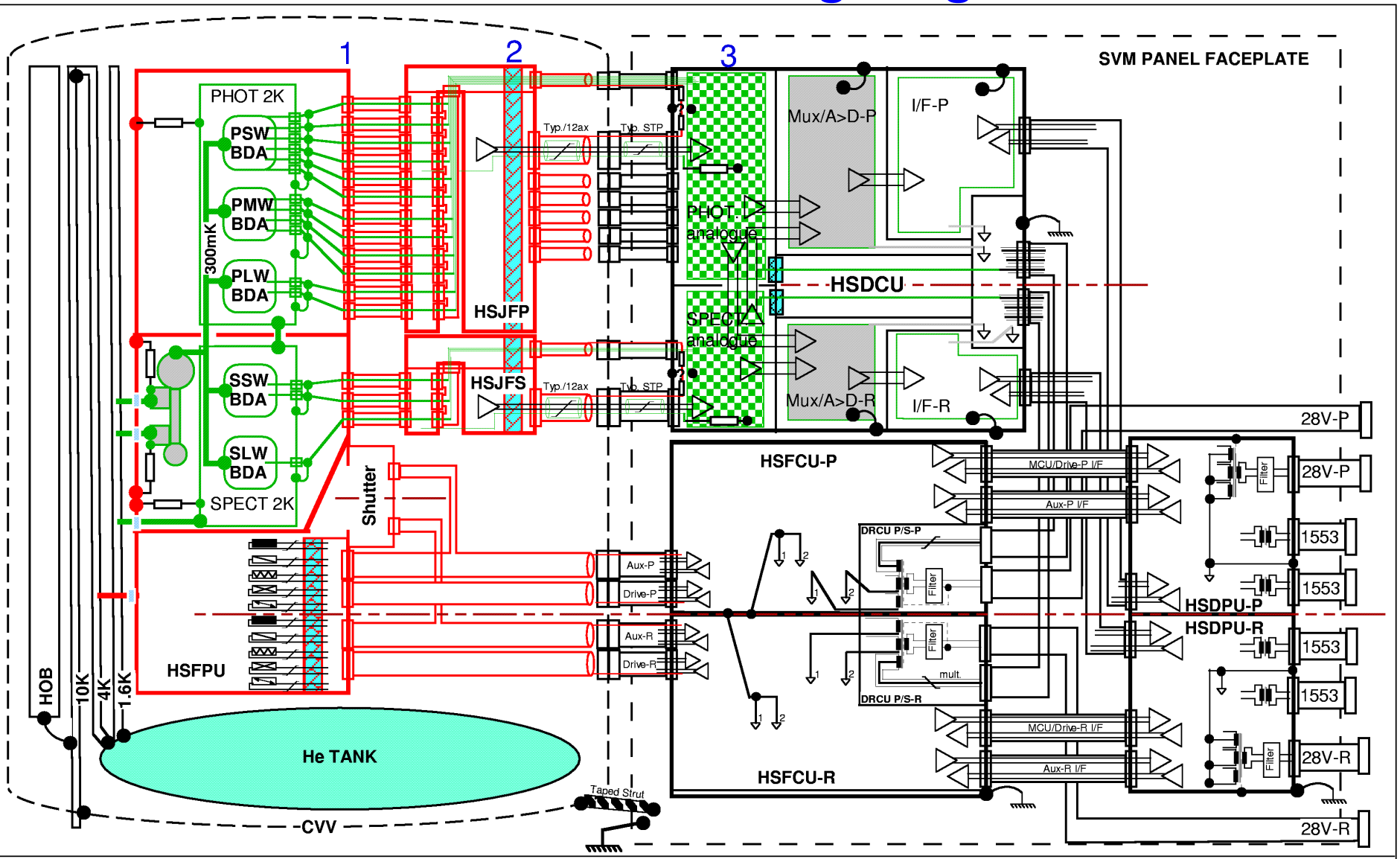
- Herschel/Spire interfaces now simplified by removal of multiple sync. signals and RTU launch-lock readout.
- HSFCU/HSFPU interfaces simple in that [excepting SMEC preamplifiers] they are all circuits in the warm electronics driving passive loads in the cryogenic.
- HSFPU BDAs / HSJFS & HSJFP essentially under JPL internal control except for the need to finish harness routing details. JPL provide this harness.
- HSJFS & HSJFP to HSDRCU signal I/Fs are critical to SPIRE's noise performance, with low cross-talk, and so are validated as early as possible in the programme.
- HSJFS & HSJFP to HSDRCU bias interfaces now sorted and compatible with CEA's FMECA conclusions. The bias outputs are cross-linked for robustness in the module.

Harness Routings

- RAL suggestion 25/10/01
- The HSFPU J19-J30 now linearly disposed in a single filter unit some 75 mm above HOB's surface.
- Overall routings inside SPIRE, from HSFPU to JFETS, and by Herschel still subject to detail design.
- Designed to optimise thermal loads, impedances, screens, dissipation in harness, whilst being reliable / providing low enough Rs for actuators, etc.



Instrument Grounding Diagram



HERSCHEL SPIRE GROUNDING SCHEME

JD 1st march 2002

RF shielded cable joined to connector backshells both ends and so closing FaradayCage

Join

Sapphire Break

Secondary ground or ground plane

To S/C chassis

RF Filtering, sealed to wall of Faradaycage

Transformer coupled I/F, no signal ground line.

Differential Transmitter, no signal ground line.

Differential Receiver, no signal ground line.

Power Transformer with Electrostatic Screen

Resistance

Winding (e.g. Motor)

Relay coil

Heater

Sensor

Temperature Sensor

Cal/Stim.

Grounding Comments

- All HSFPU electrical items isolated from chassis. Together with the JFETs, the HSFPU forms a Faraday cage aimed at preventing the bolometers receiving wire or field-coupled stray energy.
- Conventional grounding of HSFCU, HSDPU, and other than the analogue front-ends of HSDCU. All non-bolometer loads in HSFPU are driven balanced.
- Analogue photometer and spectrometer front-end grounds are split so as to minimise loop areas caused by having two JFET units.
- All bolometer systems, bias and amplifiers, are run differentially, but note potential imbalance in R.F. filters.
- Still to decide on grounding at 1, 2 or 3, and to confirm open shields inside CVV connectors/need for internal shields. More detail to follow in EMC presentation.

So at the Instrument Baseline Design review in March 2002, from which the consortium went forward to implement detailed designs, we had sorted a many things out, including the harness, but:

i. the link between bolometer bias ground and chassis was still to be at a choice of 3 positions, but the hardware maintained low temperature hardware ground links
ii. I had just removed question marks on the DRCU power supply grounds for the review!

Let us consider an overview of SPIRE grounding,

I will extract some points from **SPIRE-RAL-PRJ-00624**:

- In general terms SPIRE shall conform to an ESA classical unit-by-unit secondary power configuration.
- It has a chassis/box that is closed to form a conductive Faraday cage, with all apertures including vents and joints having controlled geometry with adequately small maximum dimensions.
- Primary power is "isolated" from chassis
- Each unit is powered with secondary (or conditioned) power which is isolated from the primary power buses and unipoint grounded via a link to unit chassis.
- All signal inputs and outputs are differential and ideally pass through filter connectors. Signal ground lines do not pass between units. Inputs are normally high impedance and are required to maintain a defined high impedance w.r.t. chassis. Outputs are required to have controlled slew rates, with minimum skew to limit common mode spikes and little ringing.

- The secondary grounds within each unit are carefully configured in a documented way and if multiple supplies are used the grounds for each supply are separately controlled with a minimum of joins between the supplies, classically just one at the unit unipoint.
- Theoretically there should be no current flow in any ground wire, which should only be used for signal voltage reference. This is just one example of the general requirement that any device taking a.c. current shall have adequate local decoupling/filtering, obviously to ensure its own correct operation, but also adequately to inhibit noise propagation to other elements in the unit; logic or digital functions can be the most troublesome with their a.c. components taking the form of switching noise.
- Depending on the susceptibility of circuits, logic signals that travel a distance across a unit may need to be slowed down with series resistors and squared up again on receipt by Schottky buffers such that excessive dV/dT noise is not broadcast.

- The whole arrangement so far described is prefixed by "in general terms".
- The configuration is best suited to systems in which each unit operates over a restricted range of signal level. In Spire this would apply to the HSDPU.
- Otherwise isolation of noise from high level circuits such as power convertors to sensitive analogue elements get more and more impossible to achieve. Considering the front-end signal source in Spire, we have an noise spec. of 7nV/√Hz at about 2.5MΩ and 300mK.
- There comes a point when the need to control noise requires separate preamplifier unit(s), preferably with an electrostatic screen separating it (them) from any digital functions such as multiplexors or A-D convertors, with the signals then transferring to a conventional unit via balanced digital I/Fs.

•The power needs to be fed to this system's analogue sections extremely quietly, prefiltered and actively regulated with external sensing in an external unit. It must then be filtered in a separate compartment within the analogue unit that has bulkhead connectors feeding to the analogue system.
•Grounding has to be very carefully configured as secondary grounds are implicitly distributed outside of one unit. If one considers the whole volume of the various units in this supply system as if it were joined into one by the harness screens that join them, the grounding it should look like a unipoint tree as if it were still within one unit.
•Multichannel operation requires adequate interchannel screening and a configuration that keeps any designed-in signal cross-talk to below specified levels.

The essential features of SPIRE's implementation are:

- signal power gain from external JFET amplifiers
- separate analogue ground paths, without loops, between spectrometer and photometer systems
- maintenance of single point ground joins to S/C chassis
- analogue power, quiet and regulated, supplied from a unit external to the one that houses the sensitive analogue systems, without ground switching.
- ground-plane option invoked to keep a large area of analogue signal ground quiet in each of the spectrometer and photometer parts
- the detectors to be in a Faraday cage with full filtering on all wires entering it (non-bolometer ones not shown) extended with full shielding into the JFET boxes.
- a separate compartment division is introduced in the JFET boxes with ceramic feed-through filtering to close the Faraday cage..*now connectors are filtered.*

The essential specifications are (contd.):

- unipoint analogue ground for the 300mK BDA system with minimised voltages between the bolometers and their local chassis.
- information transfer out of the digital part of the HSDCU via normal balanced ESA-type digital interfaces, both fast and slow, to the HSDPU (not shown but having its own separate conventional grounding scheme).
- The need to bundle together groups of long harnesses between HSJFETs and HSDCU (not shown here but see instrument block diagram) to minimise loop area between bias routed analogue ground lines and differential signal lines.
- An optimised multiplexing/transfer of data from the analogue sections of the DCU to the back-end digital ones to minimise current injection back into the analogue ground and hence potentially back to the detectors.

There's a great deal more detailed discussion in SPIRE-RAL-PRJ-00624 with which anyone critiquing the situation in detail should acquaint themselves. The extracts I have just presented are all very long-standing.

The document has recently been extended to include some coverage of the Tiger Team exchanges, which we will come to later in this Review.

So why does SPIRE need a Grounding Review at all?

Comparing the IBDR grounding diagram with the earlier IIBR version shows evolution of the HSDCU grounding. The option of grounding the bolometer analogue grounding to a chassis unipoint one at the warm end is shown. This was included as a request from CEA as a link that could be tried/considered as SPIRE designed/tested out its system; it had stated it could not be a design driver forcing changes on the cold SPIRE units.

CEA made a first cut at some of the HSFCU boards to be populated by JPL as per the IBDR grounding approach.

Moving towards a DRCU Power Supply specification, pressed by SPIRE System to complete a baseline design with power supply grounds, secondaries, filtering, prime/redundant drawn out as whole scheme, CEA stated that warm-end sourced Common Mode noise (best thought of as charge or current injection) had to be returned via warm end loops and not loops that went to the cold-end and back.

Given that there are at least three factors in this budget {how much noise is generated to start with, how it is filtered and the loops this uses, and the analogue circuits' susceptibility}, localising noise to near its source was an approach that could not be disagreed with and this was written up within an Addendum to the Grounding Philosophy Document issued 5th June 2002.

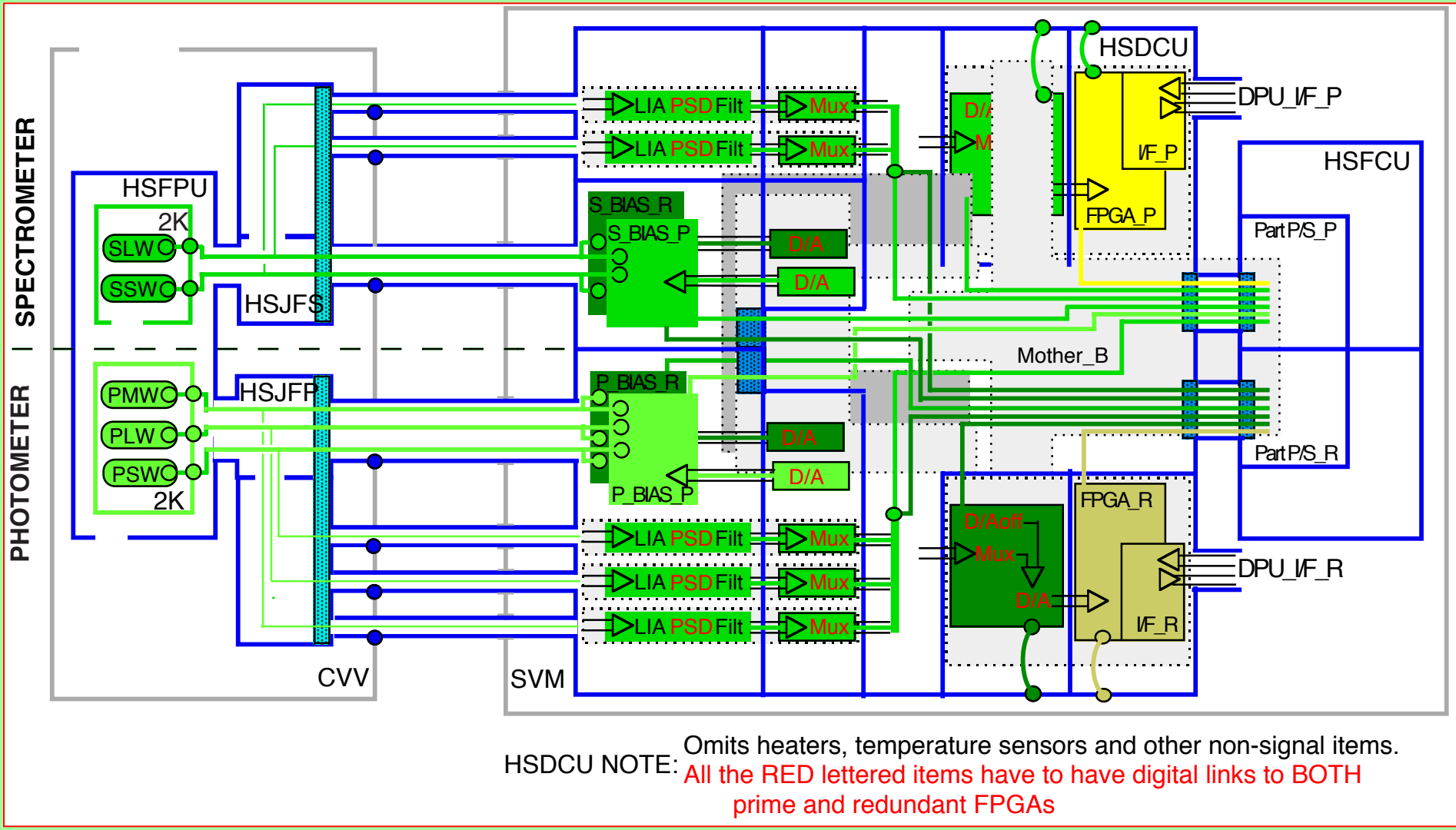
So, again, why are we needing a Grounding Review at all?

CEA further suggested that the warm-end grounding of the bolometer analogue grounds was mandatory, a position that I initially rebuffed by requesting we keep to the IBDR baseline. However it then became clear that the next generation of HSDCU PCBs had already been designed non-compliantly.

A detector summit minuted that any analogue ground PCB links to chassis should be removable **not** solid groundplane. However there was some delay before I realised that this had not been actioned….possibly because CEA were not informed officially!

So the first way of sorting this out was to set up a directed activity to work the grounding through, a decision minuted as forming a Tiger Team. We held numerous three party telephone conferences and exchanged notes/analyses etc. These resulted in my issuing a document called SPIRE Grounding on 16th July which proposed a way forward (now added to the top level document). It describes a way to proceed, and may still be the outcome of this review, but not all parties felt able to sign up to it with a good level of confidence in July. So here we are, after a delay to get presentation material together, at a review.

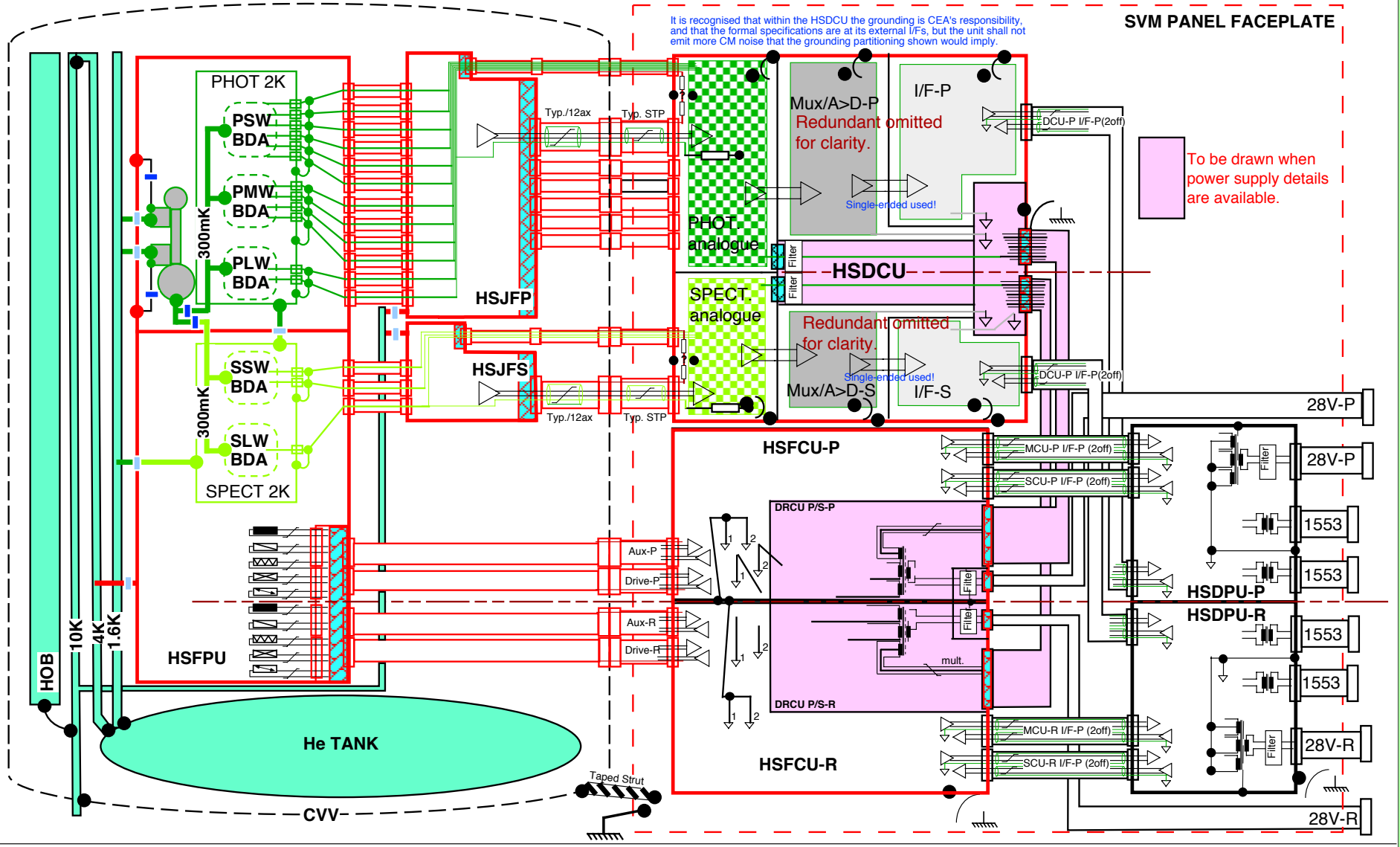
Consider a grounding overview,based on recent DDR documents.



HSDCU NOTE: Omits heaters, temperature sensors and other non-signal items.
All the RED lettered items have to have digital links to BOTH prime and redundant FPGAs

The agenda now calls for JPL, CEA the Review Team each to present their perspectives on the situation. I will then try and pull together something, starting from my proposal of 14th July

I will work up the slides after this point when I am in receipt of other inputs



HERSCHEL SPIRE GROUNDING SCHEME

JD 15th July 2002

RF shielded cable joined to connector backshells both ends and so closing Faraday Cage

Join | Sapphire Break | Other Break

Secondary ground or ground plane

To S/C chassis

Cristek etc. R.F Filter Connectors, sealed to walls of Faraday cages

Transformer coupled I/F, no signal ground line.

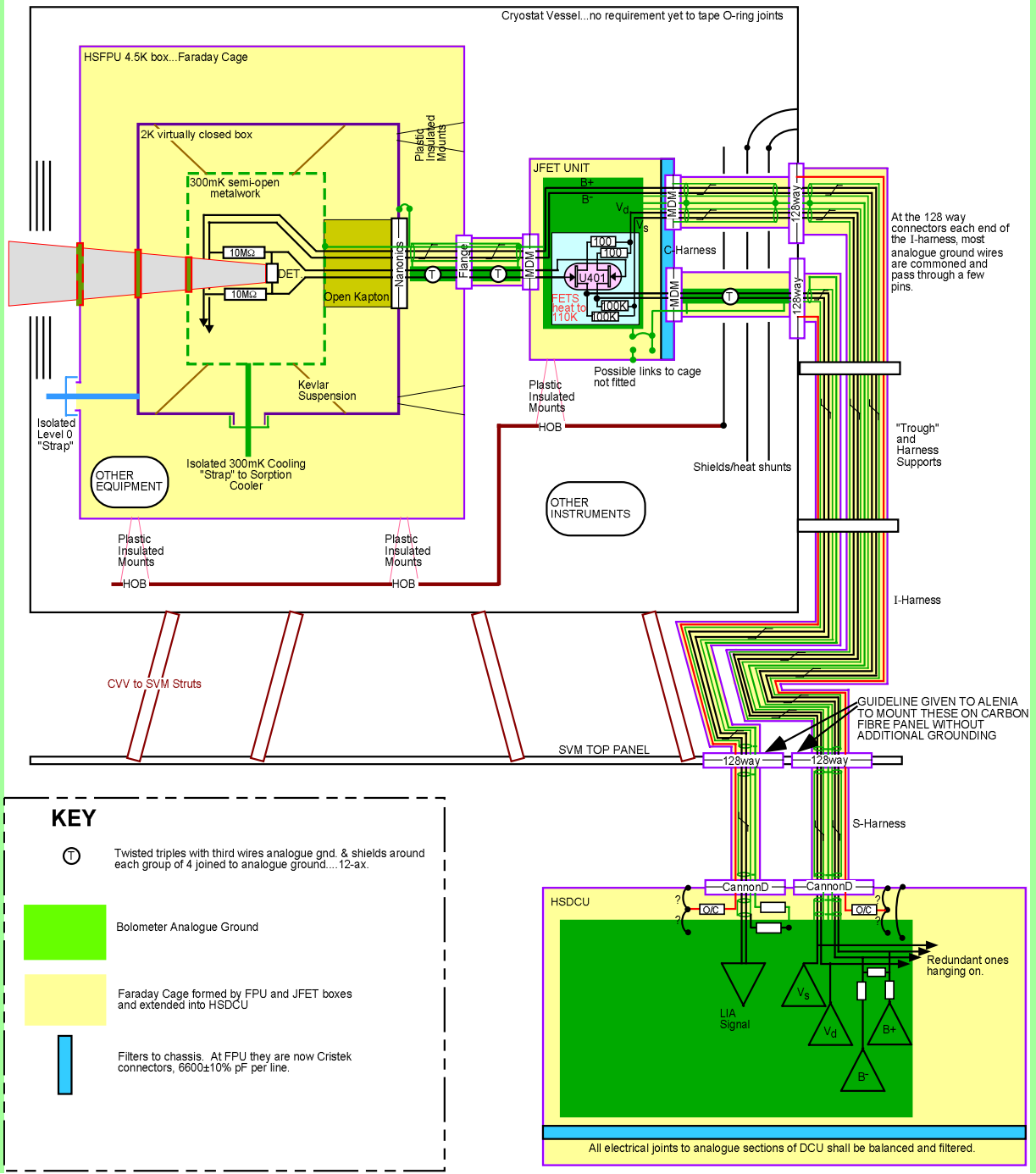
Differential Transmitter, no signal ground line.

Differential Receiver, no signal ground line.

Power Transformer with Electrostatic Screen

Resistance
Winding (e.g. Motor)
Relay coil
Heater
Sensor
Temperature Sensor
Cal/Stim.

SINGLE DETECTOR DETAIL GROUNDING



Changes since Overall grounding scheme version of 5th June.

•Shutter removed.

•Joined up instrument Faraday cage, see increase in red lines, by re-connecting shields at CVV wall.

•Made resistors in Faraday shield link wires very narrow line because they would not be fitted in this scheme. I am assuming that the wire's fractional contribution to heatleak is small and that just running totally inside a Faraday cage they cannot be a source of pickup. Besides the test harness layup is made.

•Removed all grounding option numbers as we are being forced at this stage to define one baseline.

•Remove 2K detector box resistances to HSFPU chassis. This scheme requires the

•mountings be "isolated". Put isolation in 2K box link...would separate S/C strap be easier?

•Reposition 300mK pump in drawing to show it more correctly on the Photometer side.

•Put in 300mK ground breaks, distinguishing between sapphire and other ground breaks.

•Simplify way backharness with bias grounds is drawn.

•Add ground LINKS from LIA analogue ground to HSDCU chassis, previously only a "can we include as an option to try" link.

•Change Spectrometer ground colour so no-one can assume it's the same as the Photometer!

•Remove cross-feeds from Spectrometer LIA to Photometer, and visa versa, which where a left-over from old ideas.

•Add note giving CEA flexibility within HSDCU.

TRADE_OFF TABLE

Route Forward	Tech	Herit	Progr	Risk	
Cold end only grounding	Poor PS CM	JPL	Delay	?	
Warm end only grounding	Poor Bol.	CEA	OK	?	
Warm end link and closed analogue shields	OK	?	OK	?	