SPIRE-SAP-REP-001348

Work Package: Management & System

1. Subsystem Progress This Month	
Meetings	
13/05/2002	Herschel project internal review
24/05/2002	SAp / LAM MCU coordination meeting
28/05/2002	DRCU System meeting (SPIRE System / SAp / JPL)
Management act.	
Project control	➢ SPIRE master schedule updated. ➢ DCU EM QM1 detailed schedule. ➢ SPIRE FPU simulator detailed schedule update. ➢ SCU QM1 detailed schedule update. ➢ Action list update. ➢ SPIRE reporting.
CEA/JPL MoU	➢ Signed by SPIRE PI.
PA	➢ PA / QA internal audit near to completion. ➢ Jean Fontignie has joined the QA team. He is in charge of electronics PA.
SAp / JPL	➢ F. Pinsard stay at Caltech : • 11/04 to 10/06: DAQ IF + BIAS board test • 24/06 to 12/07: LIA-P board test • 22/07 to 16/08: LIA-S test board + functional system test • 09/09 to 18/10: performances system test

2. Problem Areas	**Remedial Actions**
➢ Potential risk on DRCU FM delivery: Grounding scheme issue prevents (among else) to send out the PSU call for tender.	➢ See DRCU workpackage section.

3. Actions

Still Opened

Ref.	*Meeting*	*Actionnee*	*Due date*	*Action*
/	/	/	/	/

Closed

Ref.	*Meeting*	*Actionnee*	*Due date*	*Action*
/	/	/	/	/

4. Project Milestones

Main Delivery Milestones	*Resp.*	*Baseline*	*Current*
DRCU QM1 delivery to RAL	SAp	03/03/2003	03/03/2003
DRCU QM2 delivery to RAL	SAp	05/01/2004	05/01/2004
DRCU FM delivery to RAL	SAp	30/07/2004	30/07/2004

Work Package: DRCU

1. Subsystem Progress Since Project Inception	
DRCU	
DCU/QM1	➢ BIAS PCB, LIA-P PCB, LIA-S PCB fabrication files sent to JPL ➢ Test plans: LIA-P, LIA-s, BIAS, DAQ-IF available in draft form. ➢ Back planes in fabrication ➢ **DAQ IF** • Fabrication file send to JPL 18/01/2002 • 2 boards available for test at JPL • DAQ IF test achieved ➢ **BIAS** • Components sent • BIAS board assembly achieved 29/05 ➢ **LIA-P** • PCB fabrication achieved • LIA-P Board assembly: wait for components ➢ **LIA-S** • PCB fabrication achieved • LIA-S board assembly: wait for components
SCU/QM1	➢ Draft Specification and preliminary (H/W & VHDL) design available. ➢ Draft DPU/SCU ICD issued. (Internal) Writing of Issue 0.3 ➢ Preliminary command list available ➢ Heaters: prototype test in preparation ➢ Temperature sensors: test successful ➢ DPU I/F command and data I/F achieved. ➢ **Functions** • Heater & temperature function implementation achieved • Calibrator function implementation in progress. • HSK function: prototype board in fabrication, 2 people were added for a few month's to study it, the test software and a FPGA to convert different communication protocols. • SCU logic function (pinout) study: achievement • SCU logic function (logic) study started ➢ **Boards** • Temperature board: design PCB achieved. • Cchkif board: design PCB started. • Back plane board: design PCB started. ➢ Analog port study achievement ➢ Analog port software primitive started. ➢ Test plan started.
MCU I/F	➢ Design available at LAM & SAp ➢ MCU QM1 delivery to SAp confirmed 12/12/2003.
PSU	➢ Separated power bench will be used for QM1 and QM2. ➢ Draft Specification available. ➢ Call for tender process in progress (Call for Application completed) ➢ Contractual specification writing in progress
DRCU Boxes	➢ Modeling completed. ➢ DCU board front panel design achieved **DCU Box.** ➢ STM: detailed design achieved, ready for fabrication. ➢ QM1: detailed design update in progress ➢ QM2 & FM: / **FCU Box.** ➢ STM: detailed design achieved, ready for fabrication. ➢ QM1: detailed design update in progress. ➢ QM2 & FM: /

Test Equipments	
LTU #1	➢ Specifications available ➢ Hardware & software architecture definition near to completion. ➢ Software development in progress. I/F started. ➢ Hardware procurement in progress ➢ Power bench specification writing in progress.
FPU Simulator #1	➢ Specification available ➢ Electronics prototyping ongoing ➢ S/W evaluation on going ➢ **PXI TRIG IO** Hardware test achieved. Second fabrication achieved. ➢ **PXI BOLO SPIRE** Electronic & design Achieved. VHDL soft studies. Test software specification writing achievement. Test board configuration study & realisation achievement. Functional test over at 80% ➢ **PXI heater/Supply** Design modification achieved after specifications were updated (17/12/2001). design achieved. Manufacturing file writing,. Test software specifications achievement. test board configuration study & realization achievement. Onboard VHDL software study achievement. PXI part fabrication started week 21 (sub-contractor SPCI & ERTE). ➢ **PXI Cernox DC & AC** Analogue studies & design achieved. Complementary tests achieved. Manufacturing file writing achieved, Test software specifications achievement. Test board configuration study & realisation over at 50%. Onboard VHDL software study over at 50%. PXI part fabrication started week 21 (sub-contractor SPCI & ERTE). ➢ **Software** Supervision software specification writing. Output & input file configuration specification writing. PXI BOLO SPIRE test software development over at 80%. ➢ Rack study started.
Part Procurement	
	➢ Declared components list update: edition 13 ➢ OP400 qualification review 12/02/02 ➢ Harnesses connector estimation carried out. ➢ ATP update with Technologica
Other	
Containers	➢ Specification available.
AIV	
➢ DRCU development tree available (last version 30/11/2001) ➢ Test plan writing in progress.	

2. Subsystem Progress This Month	
Documentation	
➢ /	/
Meeting	
24/05/2002	Meeting at LAM: discussion on MCU AIV and Mechanism Simulator specification and I/F (incl. LTU).
28/05/02	DRCU System meeting at SAp
30/05/02	Grounding scheme telecon
DRCU	
DCU/QM1	➢ Tests on DAQ IF ➢ BIAS board assembly ➢ LIA-P PCB fabrication ➢ LIA-S PCB fabrication ➢ Backplanes in fabrication
SCU/QM1	➢ HSK function: prototype board in fabrication, 2 people were added for a few months to study it, the test software and a FPGA to convert different communication protocols. ➢ SCU logic function (pinout) study: achievement ➢ SCU logic function (logic) study started ➢ Temperature board design PCB achievement. ➢ Cchkif board: design PCB started ➢ Analog port study achievement ➢ Analog port software primitive started. ➢ Test plan started. ➢ Writing of issue 0.3 of "generic DPU I/F"
MCU I/F	➢ MCU AIV meeting May.24th Keep on doing.
PSU	➢ Contractual specification writing.
DRCU Boxes	➢ DRCU/QM1 Board front panels fabrication. ➢ DCU/QM1 box design update, fabrication in stand by. Ready for July (not critical yet) ➢ FCU/QM1 box design update, fabrication in stand by. Not critical yet
Test Equipments	
LTU	➢ Work on Software development, I/F started. ➢ Hardware procurement progress. (OS, development system.) ➢ Power bench specification writing started. Wait for PSU specification to be achieved
FPU Simulator	➢ PXI BOLO SPIRE: test board configuration study & realisation achievement. Functional test over at 80% ➢ PXI Cernox DC & AC: test board configuration study & realisation over at 50%. Onboard VHDL software study over at 50%. PXI part fabrication started week 21 (sub-contractor SPCI & ERTE). ➢ PXI heater/supply: test board configuration study & realisation achievement. Onboard VHDL software study achievement. PXI part fabrication started week 21 (sub-contractor SPCI & ERTE). ➢ Software: Supervision software specification writing. Output & input file configuration specification writing. PXI BOLO SPIRE test software development over at 80%. ➢ Rack study started.
Others	
	➢ /
Part Procurement	
	➢ Components sent to JPL ➢ ATP (authorisation to Proceed) update with Technologica. ➢ Contact with sub-contractors. ➢ Components list update. Issue 13
AIV	
➢ Test plan writing.	
PA / QA Activities	
Mechanic	➢ /
Electronics	➢ /

3. Problem Areas	Remedial Actions
Grounding scheme: The grounding scheme is questioned by JPL, but boards are under test and PSU specifications await decision.	DRCU system meeting (28/05/02). Grounding scheme telecon (30/05/02) Tiger team set up.
Test harness responsibility to be clarified.	
FPU harness	Proposal made by RAL to include the Cooler harness in the SPIRE FPU harness spec.
The SCU development does not progress at the expected pace. The person in charge of the analog part moved to another department.	A new person has been appointed to take over the analog activity of the SCU.

4. Milestones		Status
DCU EM QM1 delivery to SAp from JPL	06/11/2002	On schedule
DRCU QM1 harnesses need date	06/11/2002	On schedule
LTU DRCU need date	06/11/2002	On schedule
SPIRE FPU simulator #1 need date delivery to SAp	06/11/2002	On schedule
Detector test cryostat delivery to SAp by JPL	25/11/2002	On schedule
MCU QM1 + simulator need date delivery to SAp	10/12/2002	On schedule
SCU QM1 delivery by SEDI need date	24/12/2002	On schedule
DRCU QM1 delivery to RAL	**03/03/2003**	**On schedule**
SPIRE FPU simulator #2 need date	28/07/2003	On schedule
SCU QM2 need date	27/08/2003	On schedule
MCU QM2 delivery to SAp need date	27/08/2003	On schedule
DRCU QM2 delivery to RAL	05/01/2004	On schedule
MCU FM delivery to SAp need date	26/04/2004	On schedule
SCU FM need date	05/05/2004	On schedule
DRCU FM ready for delivery to RAL	30/07/2004	On schedule

Documentation status

1.Documentation List		
Title	**Reference**	**Version, date**
Reference documentation		
➢ SPIRE Instrument Development Plan IIDR	/	Issue 1.1 12/4/2001 IIDR
➢ SPIRE Major Milestone List issue 1.3 IIDR	SPIRE-RAL-PRJ-000455	Issue 1.3
➢ SPIRE Instrument Requirements	34	Issue 1.0 23/11/00
➢ SPIRE System Budget	/	Issue 3.4 24/07/2001
➢ Cryo-cooler Control Specification	/	/
➢ Calibrator SSSD: SCAL ➢ Calibrator SSSD : PCAL	HSO-CDF-SP-001 HSO-CDF-SP-003	Issue 1.0 10/9/2001 Issue 1.0 11/9/2001
➢ Detector SSSD	/	Issue 3.1 – draft
➢ Shutter SSSD	Not yet	/
➢ Instrument Interface Document part A	SCI-PT-IIDA-04624	2.0, 31/07/2001
➢ Instrument Interface Document part A	SCI-PT-IIDA-04624	3.0, draft 03/05/2002
➢ Instrument Interface Document part B	SCI-PT-IIDB/SPIRE-02124	2.0, 31/07/2001
➢ SPIRE configurable document tree	SPIRE-RAL-PRJ-00033	3.1 03/05/2001
➢ SPIRE product tree	SPIRE-RAL-PRJ-00455	1.0 09/11/1999
➢ SPIRE instrument development plan	SPIRE-RAL-PRJ-0035	1.0 20/05/2000
➢ SPIRE management plan	SPIRE-RAL-PRJ-00029	01/01/2001
➢ SPIRE Data ICD	SPIRE-RAL-DOC-001078	1.0 draft1 15/01/2002
➢ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1 29/03/2001
Management		
➢ Management plan for the Herschel project.	SAp-FIRST-JLA-0038-01	3.0 23/11/2001
➢ Actions list	SAp-FIRST-DR-0050-01	
➢ DRCU & WIH Development Plan	SAp-SPIRE-JLA-0047-01	3.0 27/11/2001
➢ SPIRE product tree	SAp-FIRST-DR-0071-02	1.2
➢ WBS Herschel	SAP-FIRST-DR-0043-01	2.1
➢ WBS SPIRE	SAP-FIRST-DR-0045-01	2.1
➢ SPIRE master schedule	SAp-SPIRE-DR-0053-02	2.9 28/05/2002
➢ DCU EM QM1 at JPL detailed schedule	SAP-FIRST-DR-0050-01	4.4 28/05/2002
➢ SPIRE FPU simulator detailed schedule	SIG-FIRST-PdA-0052-01	10.0 28/05/2002
➢ SCU QM1 detailed schedule	SEI-SPIRE-MM-0049-01	8.0 28/05/2002
➢ LTU & power bench detailed schedule	SAp-FIRST-DR-0069-02	2.5 25/05/2002
DRCU		
➢ DRCU Specifications document	SAp-SPIRE-Cca-0025-00	Issue 0.91 01/03/2002
➢ DRCU Development Tree	H0030	30/11/2001
➢ DRCU ICD	SAp-SPIRE-Cca-0075-02	0.6 01/03/2002
➢ DCU design document	SAp-SPIRE-FP-0063-02	0.1 04/03/2002
➢ Test plan DAQ IF	SAp-SPIRE-FP-0067-02	0.1 draft
➢ Test plan BIAS	SAp-SPIRE-FP-0066-02	0.1 draft
➢ Test plan LIA P	SAp-SPIRE-FP-0064-02	0.1 draft
➢ Test plan LIA S	SAp-SPIRE-FP-0065-02	0.1 draft
➢ SPIRE test configuration,	SAp-SPIRE-LD-0015-01	3.0 08/2001
➢ FPU simulator specifications for DCU / SCU test	SIG-SPIRE-PdA-0030-01	19/03/2001
➢ SPIRE LTU specifications	SAp-SPIRE-FD-0071-02	1.0 22/04/2002
QA		
➢ Standard product assurance plan	SAp-GERES-Flo-436-00	1.0 09/11/2000
➢ SPIRE liste des documents à produire	SAp-SPIRE-Flo-0028-00	0.2 15/12/2000
➢ Organisation de la gestion documentaire sur Herschel au SAp	SAp-FIRST-DR-0053-01	1.1 06/12/2001
➢ Gestion des documents sur la base Herschel	SAp-FIRST-DR-0072-02	1.3 15/04/2002
➢ Procédures de contrôle projet sur Herschel	SAp-FIRST-DR-0125-02	1.0 15/04/2002
➢ DRCU FMECA Report		Issue 1.0 25/10/2001
➢ Analyse de fiabilité du DRCU	SAp-SPIRE-Flo-0039-01	21/08/2001
➢ DRCU processor board product assurance specification	SAp-SPIRE-Flo-0020-00	10/01/2001