Work Package: **Management & System** **SPIRE-SAP-REP-001282**

1. Subsystem Progress This Month	
Meetings	
5-6 /03	SPIRE IBDR
Management act.	
Project control	➢ SPIRE master schedule updated. ➢ DCU EM QM1 detailed schedule updated before Frederic's mission to the USA at JPL. ➢ SPIRE FPU simulator detailed schedule update. ➢ SCU QM1 detailed schedule update. ➢ Action list update. ➢ SPIRE reporting.
CEA/JPL MoU	➢ Signed by JPL, to be signed by SPIRE PI
DCU QM1 dev. schedule	➢ Agreed with JPL

2. Problem Areas	**Remedial Actions**
➢ SPIRE/CEA MoU not yet signed	➢ CEA to send a new proposal legally acceptable by CEA
➢ S/C I/F not yet frozen	➢ SPIRE Project action on ESA/Alcatel

3. Actions

Still Opened

Ref.	***Meeting***	***Actionnee***	***Due date***	***Action***
/	/	/	/	/

Closed

Ref.	***Meeting***	***Actionnee***	***Due date***	***Action***
/	/	/	/	/

4. Project Milestones

Main Delivery Milestones	***Resp.***	***Baseline***	***Current***
DRCU QM1 delivery to RAL	SAp	03/03/2003	03/03/2003
DRCU QM2 delivery to RAL	SAp	05/01/2004	05/01/2004
DRCU FM delivery to RAL	SAp	30/07/2004	30/07/2004

Work Package: DRCU

1. Subsystem Progress Since Project Inception	
DRCU	
DCU	➢ Board PCB re-design ➢ IBDR documentation writing achieved ➢ FPGA achieved. ➢ DAQ IF fabrication file send to JPL 18/01 ➢ BIAS PCB fabrication file send to JPL ➢ LIA-P PCB fabrication file send to JPL ➢ LIA-S PCB fabrication file send to JPL ➢ Test plan LIA-P, LIA-s, BIAS, DAQ-IF writing achieved ➢ DCU box realization file achieved
SCU	➢ Draft Specification and preliminary (H/W & VHDL) design available. ➢ Draft DPU/SCU ICD issued. (Internal) ➢ Preliminary command list available ➢ Heaters: prototype test in preparation ➢ Temperature sensors: test successful ➢ Heater & temperature function implementation finalisation ➢ Analog ports in progress ➢ Calibrator function implementation in progress ➢ HSK function implementation in progress. ➢ Temperature card: design PCB in progress. ➢ DPU I/F command and data I/F achieved. ➢ SCU QM1 box design & manufacturing file finalisation. ➢ Dynamic studies of FCU box finalisation.
MCU I/F	➢ Design defined and available at LAM & SAp ➢ MCU QM1 delivery to SAp confirmed 12/12/2003.
PSU	➢ Separated power bench will be used for QM1 and QM2. ➢ Draft Specification available. ➢ Call for tender process started (Call for Application completed) ➢ Specification writing: finalisation
DRCU Boxes	➢ Modeling ➢ DCU board front panel design achieved ➢ Board front panels fabrication in progress.
Test Equipments	
LTU	➢ Specification writing in progress ➢ Hardware & software architecture definition in progress ➢ Detailed schedule updated
FPU Simulator	➢ Specification available ➢ Electronics prototyping ongoing ➢ S/W evaluation on going ➢ PXI TRIG IO: Hardware test achieved. Second fabrication achieved. ➢ PXI BOLO SPIRE: Electronic & design Achieved. Test software specification writing in progress. Fabrication in progress. ➢ PXI heater/Supply: Design modification achieved after specifications were updated (17/12/2001). ➢ PXI Cernox DC & AC: Analogue studies & design achieved. Complementary tests achieved ➢ Software: Supervision software specification writing in finalisation. Input & output files specification writing in progress.
Part Procurement	
	➢ Declared components list update: edition 12 ➢ OP400 qualification review 12/02/02 ➢ Harness's connectors estimation
Other	
Containers	➢ Specification available.
AIV	
➢ DRCU development tree available (last version 30/11/2001)	

2. Subsystem Progress This Month		
Documentation		
➢ DCU design document	SAp-SPIRE-FP-0063-02	Issue 0.1, 04/03/2002
➢ DCU LIA-P test plan	SAp-SPIRE-FP-0064-02	Issue 0.1 draft
➢ DCU LIA-S test plan	SAp-SPIRE-FP-0065-02	Issue 0.1 draft
➢ DCU BIAS test plan	SAp-SPIRE-FP-0066-02	Issue 0.1 draft
➢ DCU DAQ IF test plan	SAp-SPIRE-FP-0067-02	Issue 0.1 draft

Meeting	
13/03	LAM: Mechanics on DCU, MCU
19/03	Start of fabrication review boards LIA-S
DRCU	
DCU	➢ LIA-S: PCB layout modification achieved. Quality review before fabrication, file sent to JPL ➢ FPGA achievement ➢ Test plan LIA-P, LIA-S, BIAS, DAQ IF writing ➢ Sorting out of DAQ-IF board fabrication issues ➢ DCU box realization file
SCU	➢ Heater function implementation achievement. ➢ Temperature function implementation finalisation. ➢ Calibrator function implementation ➢ HSK function implementation. ➢ Temperature card: design PCB. ➢ DPU I/F command and data I/F achievement. ➢ Analog ports. ➢ SCU QM1 dedicated box design & manufacturing file finalisation.
MCU I/F	➢ MCU QM1 delivery to SAp confirmed 12/12/2003.
PSU	➢
DRCU Boxes	➢ Board front panels fabrication.
Test Equipments	
LTU	➢ Specification writing ➢ Hardware & software architecture definition ➢ Detailed schedule update.
FPU Simulator	➢ PXI BOLO SPIRE: Electronic & design Achieved. Fabrication beginning. Test software specification writing ➢ PXI Cernox DC & AC: Analogue studies & design achievement. Complementary tests done ➢ PXI heater/supply: Design achievement. ➢ Software: Supervision software specification writing. Input & output files specification writing
Others	
	➢ /
Part Procurement	
	➢ Harness‘ connectors estimation.
AIV	
➢ /	
PA / QA Activities	
LIA-S board	➢ Fabrication file review (non conformances check, electrical scheme & mechanical drawing check, equipment file, mounting procedure check…).

3. Problem Areas	**Remedial Actions**
FRB components, LIA-P, LIA-S, BIAS capacities not available	JPL looks for these components

4. Milestones		Status
DCU EM QM1 delivery to SAp	08/11/2002	On schedule
DRCU QM1 harnesses need date	18/11/2002	On schedule
LTU DRCU need date	19/11/2002	On schedule
SPIRE FPU simulator #1 delivery to SAp	19/11/2002	On schedule
Detector test cryostat delivery to SAp by JPL	26/11/2002	On schedule
MCU QM1 + simulator need date delivery to SAp	10/12/2002	On schedule
SCU QM1 delivery by SEDI need date	24/12/2002	On schedule
DRCU QM1 delivery to RAL	03/03/2003	On schedule
SPIRE FPU simulator #2 need date	28/07/2003	On schedule
SCU QM2 need date	27/08/2003	On schedule
MCU QM2 delivery to SAp need date	27/08/2003	On schedule
DRCU QM2 delivery to RAL	05/01/2004	On schedule
MCU FM delivery to SAp need date	26/04/2004	On schedule
SCU FM need date	05/05/2004	On schedule
DRCU FM ready for delivery to RAL	30/07/2004	On schedule
F.Pinsard missions at JPL for the DCU EM/QM1	11/04→1/06/2002; 24/06→12/07; 22/07→16/08; 09/09→18/10	

Documentation status

1.Documentation List		
Title	**Reference**	**Version, date**
Reference documentation		
➢ SPIRE Instrument Development Plan IIDR	/	Issue 1.1 12/4/2001 IIDR
➢ SPIRE Major Milestone List issue 1.3 IIDR	SPIRE-RAL-PRJ-000455	Issue 1.3
➢ SPIRE Instrument Requirements	34	Issue 1.0 23/11/00
➢ SPIRE System Budget	/	Issue 3.4 24/07/2001
➢ Cryo-cooler Control Specification	/	/
➢ Calibrator SSSD: SCAL ➢ Calibrator SSSD : PCAL	HSO-CDF-SP-001 HSO-CDF-SP-003	Issue 1.0 10/9/2001 Issue 1.0 11/9/2001
➢ Detector SSSD	/	Issue 3.1 – draft
➢ Shutter SSSD	Not yet	/
➢ Instrument Interface Document part A	SCI-PT-IIDA-04624	2.0, 31/07/2001
➢ Instrument Interface Document part B	SCI-PT-IIDB/PACS-02126	2.0, 31/07/2001
➢ SPIRE configurable document tree	SPIRE-RAL-PRJ-00033	3.1 03/05/2001
➢ SPIRE product tree	SPIRE-RAL-PRJ-00455	1.0 09/11/1999
➢ SPIRE instrument development plan	SPIRE-RAL-PRJ-0035	1.0 20/05/2000
➢ SPIRE management plan	SPIRE-RAL-PRJ-00029	01/01/2001
➢ SPIRE Data ICD	SPIRE-RAL-DOC-001078	1.0 draft1 15/01/2002
➢ SPIRE instrument AIV plan	SPIRE-RAL-PRJ-000410	2.1 29/03/2001
Management		
➢ Management plan for the Herschel project.	SAp-FIRST-JLA-0038-01	3.0 23/11/2001
➢ Actions list	SAp-FIRST-DR-0050-01	1.6
➢ DRCU & WIH Development Plan	SAp-SPIRE-JLA-0047-01	3.0 27/11/2001
➢ SPIRE product tree	SAp-FIRST-DR-0071-02	1.2
➢ WBS Herschel	SAP-FIRST-DR-0043-01	2.1
➢ WBS SPIRE	SAP-FIRST-DR-0045-01	2.1
➢ SPIRE master schedule	SAp-SPIRE-DR-0053-02	2.4 25/03/2002
➢ DCU EM QM1 at JPL detailed schedule	SAP-FIRST-DR-0050-01	4.2 22/03/2002
➢ SPIRE FPU simulator detailed schedule	SIG-FIRST-PdA-0052-01	8.0 28/03/2002
➢ SCU QM1 detailed schedule	SEI-SPIRE-MM-0049-01	7.0 28/03/2002
➢ LTU & power bench detailed schedule	SAp-FIRST-DR-0069-02	2.3 22/03/2002
➢ Milestones list update	SAp-FIRST-DR-0068-02	1.3 28/03/2002
DRCU		
➢ DRCU Specifications document	SAp-SPIRE-CCa-0025-00	Issue 0.91 01/03/2002
➢ DRCU Development Tree	H0030	30/11/2001
➢ DRCU ICD	SAp-SPIRE-CCa-0025-00	0.6 01/03/2002
➢ DCU design document	SAp-SPIRE-FP-0063-02	0.1 04/03/2002
➢ Test plan DAQ IF	SAp-SPIRE-FP-0067-02	0.1 draft
➢ Test plan BIAS	SAp-SPIRE-FP-0066-02	0.1 draft
➢ Test plan LIA P	SAp-SPIRE-FP-0064-02	0.1 draft
➢ Test plan LIA S	SAp-SPIRE-FP-0065-02	0.1 draft
➢ SPIRE test configuration,	SAp-SPIRE-LD-0015-01	3.0 08/2001
➢ FPU simulator specifications for DCU / SCU test	SIG-SPIRE-PdA-0030-01	19/03/2001
QA		
➢ Standard product assurance plan	SAp-GERES-Flo-436-00	1.0 09/11/2000
➢ SPIRE liste des documents à produire	SAp-SPIRE-Flo-0028-00	0.2 15/12/2000
➢ Organisation de la gestion documentaire sur Herschel au SAp	SAp-FIRST-DR-0053-01	1.1 06/12/2001
➢ Gestion des documents sur la base Herschel	SAp-FIRST-DR-0072-02	1.2 draft 25/03/2002
➢ DRCU FMECA Report		Issue 1.0 25/10/2001
➢ Analyse de fiabilité du DRCU	SAp-SPIRE-Flo-0039-01	21/08/2001
➢ DRCU processor board product assurance specification	SAp-SPIRE-Flo-0020-00	10/01/2001