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To:SPIRE Hardware People

From: John Delderfield

cc: Doug, Dave Smith, Hoorst Faas SPIRE-RAL-COM-001265

SPIRE CRYO-HARNESS CONSIDERATIONS.

First let's summarise the present progress. The production of the calibration/test harness has been underway for some while based on Harness Definition 0.9. The HERSCHEL contractors are now getting into useful levels of detail. The SVM harness routing is pretty well fixed. SPIRE has issued ECR29, which includes the IID-B type of reduced harness specification listing. Could SPIRE Hardware People please respond if their mean/peak currents when operating are significantly wrong in the ECR29. Doug is now concentrating on issuing 1.0 of the Harness Specification which will be in line with this and reflect other details that have been worked through.

There are still items to be tidied up. For instance exactly how the harness bundles proceed from the SVM brackets to the HOB mounted units is still I believe only a proposal, and the order in which connectors leave the FPU is yet to be defined in its I/F diagram and this may cause re-ordering of the JFET rack connector numbers.

With this as the general situation, would SPIRE hardware people please be very aware of the two following issues:

i. Harness thermal optimisation.

We have specified the maximum impedances for "wires" in flight operating conditions consistent with SPIRE performance. This was to minimise harness conduction. In one or two cases these impedances are actually lower than sub-system designers have in their ICDs (e.g. the sorption cooler) because of the currents that the wires have to carry.

However, Astrium are finding that the maximum impedance solution may not be the optimum thermal one because some of the higher current lines then have high dissipation. So as I am not aware of any electrical problem in reducing harness impedances, I have given Astrium the OK to explore the option of lowering some impedances. Please would SPIRE Hardware People shout if they know of any electrical problems that would be induced by too low a harness impedance. I expect that tables in a later issue of the Harness Definition, maybe 1.1, will have columns for Astrium's estimated actual impedances.

ii Harness impedance variation.

There are four causes of such variatioin: differences calibration/test to flight; I-series warm to 80K harness impedance variation with FM CVV environment; local heating of harness due to our own currents; an increase of 25% in cases of robustness in our wiring if one wire breaks. It's clearly important that the DRCU circuits should not be sensitive to these factors, such as for instance by using the technique of monitoring currents. The bolometer a.c. bias and JFET supply systems would seem particularly relevant as they seek to provide operating conditions at the JFET rack I/Fs to JPL systems conducive to an extreme stability of gain. The analysis of how the design achieves this will be need to be a major element in the DRCU DDR. A similar, but possibly less demanding, issue

is how the DRCU controls the recycling power to meet Lionel's aim of it only needing the energy that was required for the 4 litre device.

Cheers

John