
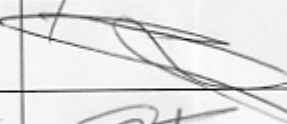
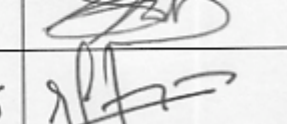
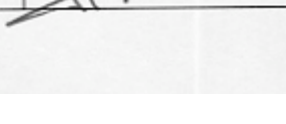




SPIRE-SAP-PRJ-001243

HERSCHEL/SPIRE
DETECTOR CONTROL UNIT
DESIGN DOCUMENT

SPIRE Project ref : SPIRE-SAP-PRJ-001243

	Function	Name	Date	Visa
Prepared by	DCU Designer	PINSARD	11/7/2005	
Verified by	Elect. Syst. Ing.	C.CARA	11/07/05	
Approved by	PA Manager	J. FONTIGNIE	11/07/05	
Approved by	Projet Manager	J-L.AUGUERES	11/07/05	

	DCU Design document	 SAp-SPIRE- FP-0063-02 Issue : 1.0 Date : 11/07/2005
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DOCUMENT STATUS and CHANGE RECORD

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List of Acronyms

ADC	Analog to Digital Converter
AMUX	Analog Multiplexer
DPU	Data Processing Unit
DCU	Detector Control Unit
DMUX	Digital Multiplexer
DRCU	Detector Readout & Control Unit
FPU	Focal Plane Unit
JFET	Junction Field Effect Transistor
LIA	Lock-in amplifier
BPF	Band Pass Filter
LPF	Low Pass Filter
NA	Not Applicable
SCU	Sub-system Control Unit
PSU	Power Supply Unit
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
WIH	Warm Interconnect Harnesses
PSW	Photometer Short Wavelength
PMW	Photometer Medium Wavelength
PLW	Photometer Long Wavelength
SSW	Spectrometer Short Wavelength
PSW	Spectrometer Long Wavelength
TC	Temperature Control
BDA	Bolometric Detector Assembly

1 INTRODUCTION

1.1 PURPOSE

The purpose of this document is to show how the DCU electronics is designed and implemented to comply with the DCU subsystem requirements.

1.2 SCOPE

This document deals only with the electronics of the Detector Control Unit. It covers neither the mechanical nor the thermal aspects of the DCU box.

1.3 OVERALL DOCUMENT DESCRIPTION

First, functions and their interfaces are described: functions are split into sub-functions as necessary and are related to the corresponding functional requirements.

Next, function overall implementations are described.

Then, function implementations are detailed and demonstrations of the capabilities to cover the performance requirements are provided.

Finally, a verification cross table summarizes the compliance to the electronics requirements.

1.4 APPLICABLES DOCUMENTS

AD1	DRCU Interface Control DOCUMENT	Sap-SPIRE-CCA- 075-02	1.0
AD2	DRCU Subsystem Specification	Sap-SPIRE-CCA-25-00	1.0
AD3			
AD4	Spire harness definition	SPIRE-RAL-PRJ-000608	1.0
AD5	Spire instrument block diagram	SPIRE-RAL-DWG-000646	5.1
AD6	DRCU/DPU Interface Control DOCUMENT	Sap-SPIRE-CCA- 076-02	0.7

1.5 REFERENCES DOCUMENTS

RD1	MAT02 data sheet		REV.C
RD2	OP-400 data sheet		
RD3			
RD4			
AD5			

2 GENERAL DESCRIPTION

2.1 DCU FUNCTIONAL DESCRIPTION

The DCU functional diagram is shown here after:

This DCU diagram represents functions as well as communication between them.

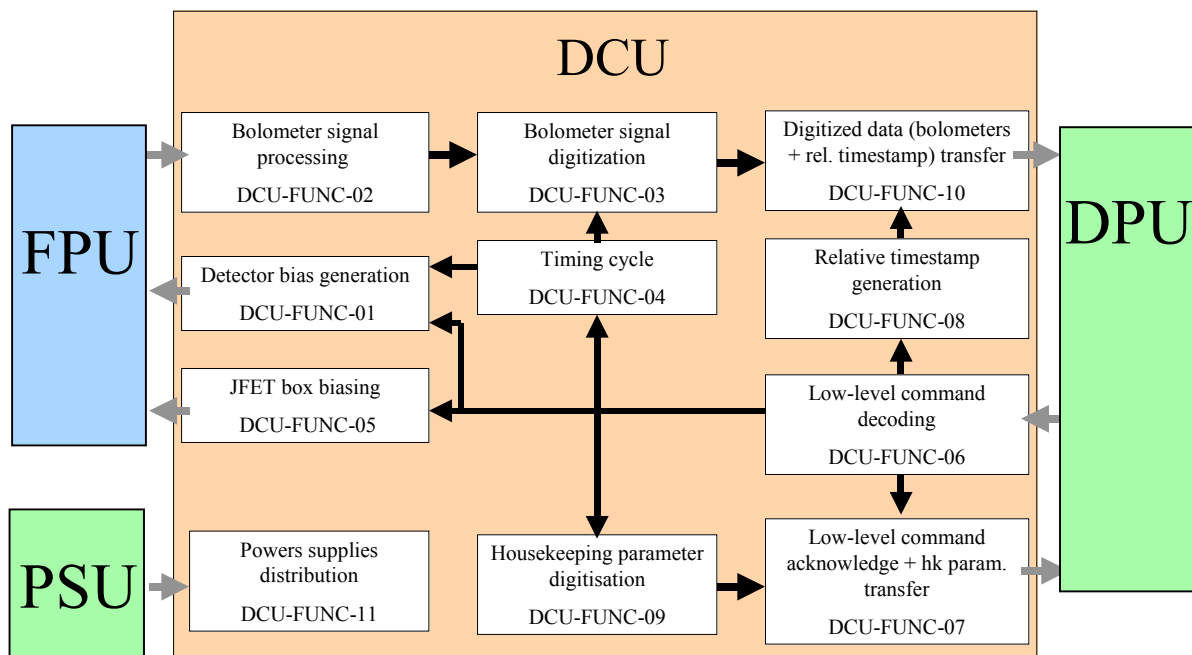


Figure 2-1: DCU Functional diagram

In the following paragraphs each function is detailed into elementary functions.

NOTE: DCU-FUN-xx and DRCU REQ-yy come from AD2

2.1.1 DCU-FUNC-01 (Detector bias generation)

2.1.1.1 Diagram

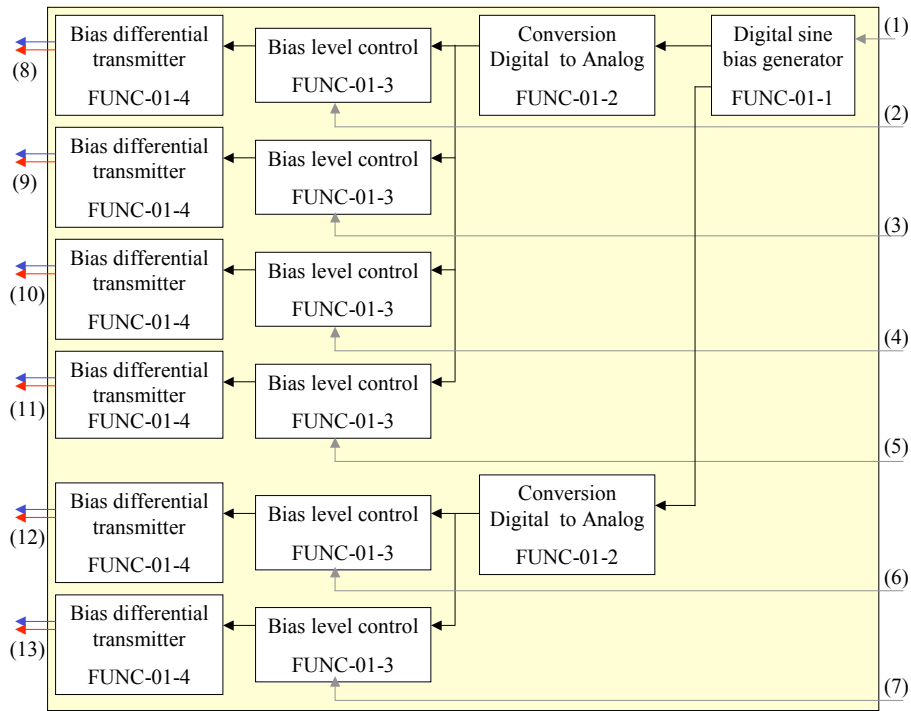


Figure 2-2: DCU-FUNC-01 diagram

2.1.1.2 Interface list

- (1) Interface **SINE_GENERATOR**: carries the sine wave clock and the generator mode for the spectrometer and the photometer
- (2) Interface **AMPL_BIAS_PSW**: commands the first bias level.
- (3) Interface **AMPL_BIAS_PMW**: commands the second bias level.
- (4) Interface **AMPL_BIAS_PLW**: commands the third bias level.
- (5) Interface **AMPL_BIAS_TC**: commands the fourth bias level.
- (6) Interface **AMPL_BIAS_SSW**: commands the fifth bias level.
- (7) Interface **AMPL_BIAS_SLW**: commands the sixth bias level.
- (8) Interface **BIAS_PSW**: biases the BDA PSW.
- (9) Interface **BIAS_PMW**: biases the BDA PMW.
- (10) Interface **BIAS_PLW**: biases the BDA PLW.
- (11) Interface **BIAS_TC**: biases the BDA TC.
- (12) Interface **BIAS_SSW**: biases the BDA SSW.
- (13) Interface **BIAS_SLW**: biases the BDA SLW.

2.1.1.3 Functional requirement list

DRCU REQ-17: The DCU-FUNC-01 has 6 bias channels.

DRCU REQ-18: Each channel level is individually adjustable by a low-level command:

SetPhotoBiasAmplSW* set the PSW bias level.
 SetPhotoBiasAmplMW* set the PMW bias level.
 SetPhotoBiasAmplLW* set the PLW bias level.
 SetPhotoBiasAmplTC* set the TC bias level.
 SetSpectroBiasAmplSW* set the SSW bias level.
 SetSpectroBiasAmplLW* set the SLW bias level.

DRCU REQ-19: The two following commands set the frequency of the photometer and the spectrometer:

SetPhotoBiasFreq* and SetSpectroBiasFreq*

Two commands switch the bias generators between a sine waveform and an adjustable DC level, independently for both photometer and spectrometer:

SetPhotoBiasMode* and SetSpectroBiasMode*

Note: The temperature channels are considered as part of the photometer

*see AD6

2.1.1.4 Physical implementation

The two FUNC-01-2 functions, the six FUNC-01-3 functions and the six FUNC-01-4 functions are implemented on the BIAS BOARD.

The function FUNC-01-1 is implemented in the FPGA of the DAQ+IF BOARD.

The interfaces AMPL_BIAS_PSW, AMPL_BIAS_PMW, AMPL_BIAS_PLW, AMPL_BIAS_TC, AMPL_BIAS_SSW, AMPL_BIAS_SLW and the data transmission between FUNC-01-1 and the two functions FUNC-01-2 is made by two serials links (one for the photometer and one for the spectrometer).

The performance and the implementation of the functions FUNC-01-2, FUNC-01-3, FUNC-01-4 and the serial link bias board side are described in the BIAS BOARD section.

The FUNC-01-1 and the other end of the serial link are described in the DAQ+IF board section.

2.1.2 DCU-FUNC-02 (Bolometer signal processing)

2.1.2.1 Diagram

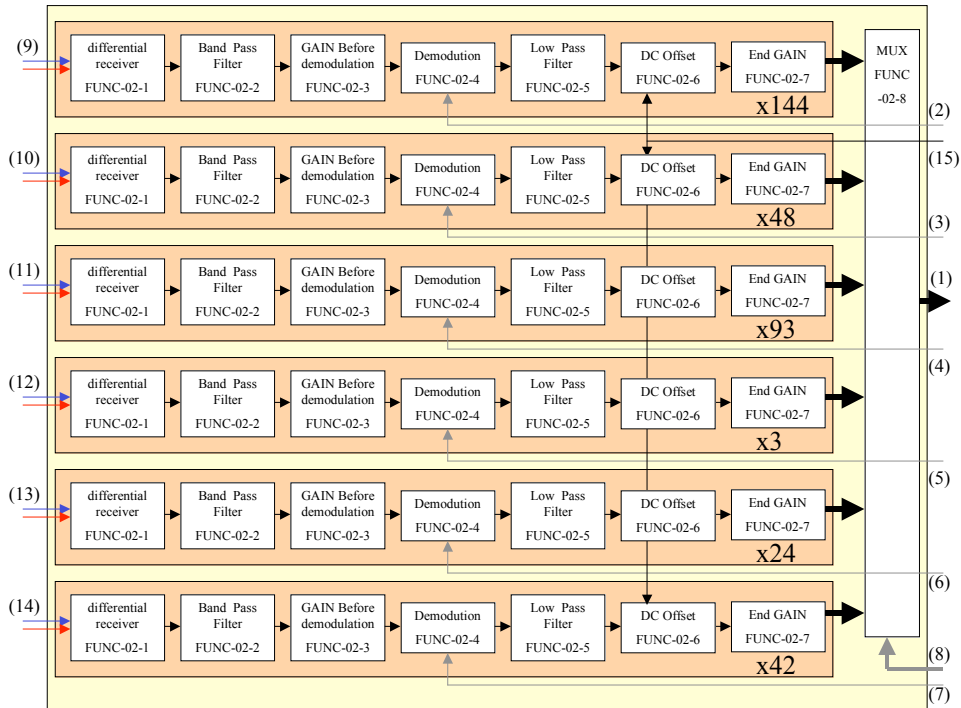


Figure 2-3: DCU-FUNC-02 diagram

2.1.2.2 Interface list

- (1) Interface **INPUT_ADC**: multiplexed channels to be digitized.
- (2) Interface **DEMOD_PSW**: demodulation signal for PSW BDA.
- (3) Interface **DEMOD_PLW**: demodulation signal for PLW BDA.
- (4) Interface **DEMOD_PMW**: demodulation signal for PMW BDA.
- (5) Interface **DEMOD_TC**: demodulation signal for TC BDA.
- (6) Interface **DEMOD_SLW**: demodulation signal for SLW BDA.
- (7) Interface **DEMOD_SSW**: demodulation signal for SSW BDA.
- (8) Interface **CMD_MUX**: commands mux positions.
- (9) Interface **IN_PSW**: modulated signals from BDA PSW.
- (10) Interface **IN_PLW**: modulated signals from BDA PLW.
- (11) Interface **IN_PMW**: modulated signals from BDA PMW.
- (12) Interface **IN_TC**: modulated signals from BDA TC.
- (13) Interface **IN_SLW**: modulated signals from BDA SLW.
- (14) Interface **IN_SSW**: modulated signals from BDA SSW.
- (15) Interface **CMD_OFFSET**: commands offsets.

2.1.2.3 Functional and performance requirement list

DRCU REQ-15:

The DCU-FUNC-02 has 48 PLW channels, 93 PMW channels, 3 TC channels, 144 PSW channels, 24 SLW channels and 48 SSW channels.

DRCU REQ-32-6

To achieve a noise level of 7nVrms/rtHz as seen in the post demodulation after digitization:

The noise level for ADC with 5V full scale is about 58 μVrms (*adc_noise* value found by test). In order to have this noise equivalent to less than 5nVrms/√Hz (*in_noise*) at the input of the bolometer signal processing function, the gain should be:

- for the photometer greater than $\frac{adc_noise}{in_noise \cdot \sqrt{photo_BW}} = 5187$ (0)
- for the spectrometer greater than $\frac{adc_noise}{in_noise \cdot \sqrt{spectro_BW}} = 2320$

As such the noise level allocated to the bolometer signal processing is 5nVrms/rtHz.

DRCU REQ-32-1

In order to not saturate at an input voltage of 11mVrms (at photometer inputs) and 17mVrms (at spectrometer inputs) the gains limits are going to be set as following:

The absolute maximum gain for a photometer signal before demodulation (FUNC-02-3) is:

$$\frac{5}{0,011 \cdot \sqrt{2}} = 321 \quad (1)$$

The absolute maximum gain for a spectrometer signal before demodulation (FUNC-02-3) is:

$$\frac{5}{0,017 \cdot \sqrt{2}} = 207 \quad (2)$$

The absolute maximum gain for a complete photometer channel before offset subtraction (FUNC-02-6) is:

$$\frac{5}{0,011} = 454 \quad (3)$$

The absolute maximum gain for a complete spectrometer channel before offset subtraction (FUNC-02-6) is:

$$\frac{5}{0,017} = 294 \quad (4)$$

Photometer LPF functions (FUNC-02-5) are 4 poles Bessel filters. Their structural gain is:

$$1.93 \quad (5)$$

Spectrometer LPF functions (FUNC-02-5) are 6 poles Bessel filters. Their structural gain is:

$$3.03 \quad (6)$$

So, in order to have the maximum gain (4), the photometer gain before demodulation (FUNC-02-3) shall be:

$$\frac{454.\pi}{1.93 \times 2\sqrt{2}} = 261$$

This value is compliant with (1) (ie less than 321)

So, in order to have the maximum gain (5), the spectrometer gain before demodulation (FUNC-02-3) shall be:

$$\frac{294.\pi}{3.03 \times 2\sqrt{2}} = 107$$

This value is compliant with (2) (ie less than 207)

From previous calculation (0), the end gain (FUNC-02-7) shall not be less than:

- 11.4 for the photometer.
- 8 for the spectrometer.

2.1.2.4 Physical implementation

The functions FUNC-02-1, FUNC-02-2, FUNC-02-3, FUNC-02-4, FUNC-02-5 and a part of FUNC-02-8 are implemented on the 9 LIA_P boards and 3 LIA_S boards.

The functions FUNC-02-6, FUNC-02-7 and the second part of FUNC-02-8 are implemented on the DAQ+IF BOARD.

The performance and the implementation of the functions FUNC-02-1, FUNC-02-2, FUNC-02-3, FUNC-02-4, FUNC-02-5 and the first part of FUNC-02-8 are described in the LIAs sections.

The functions FUNC-02-6, FUNC-02-7 and the second part of FUNC-02-8 are described in the DAQ+IF board section.

2.1.3 DCU-FUNC-03 (Bolometer signal digitization)

This function is made by six 16 bit ADC. Their acquisition timing is driven by the function DCU-FUNC-04 (timing cycle). They digitize the six analog signals provided by the function DCU-FUNC-02 (bolometer signal processing).

The function DCU-FUNC-03 is described in the DAQ+IF board section.

2.1.4 DCU-FUNC-04 (Timing cycle)

2.1.4.1 Diagram

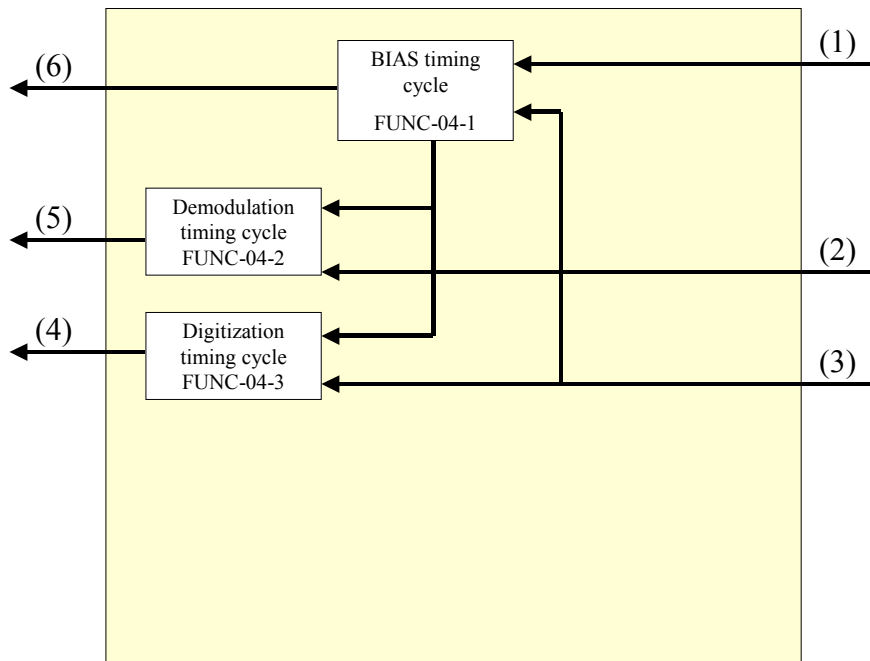


Figure 2-4: DCU-FUNC-04 diagram

2.1.4.2 Interface list

- (1) Interface **CMD_FREQUENCY**: commands the bias frequency and the sample frequency.
- (2) Interface **CMD_DEMOD**: commands the phase shift for each demodulation signals.
- (3) Interface **CMD_MODE**: selects the different modes.
- (4) Interface **CONTROL**: operates the MUXs, the offsets, the ADCs.
- (5) Interface **DEMOD_SIGNALS**: gives 6 demodulation signals.
- (6) Interface **BIAS_CLK**: is the bias clock for the bias generator.

2.1.4.3 Functional requirement list

DRCU REQ-25:

In FUNC-04-1, the 10MHz main clock is divided by the parameter `PhotoMClkDiv` when `DataMode` is in Photometer, and by the parameter `SpectroMClkDiv` when `DataMode` is in Spectrometer to give a clock 256 times the bias frequency.

The bias frequency is divided by $1 + \text{PhotoBiasDiv}$ when `DataMode` is in Photometer, or by $1 + \text{SpectroBiasDiv}$ when `DataMode` is in Spectrometer to give a clock at the sampling frequency.

DRCU REQ-26:

The number of blocks to be transferred is selected by the command `SetFrameCounter`

DRCU REQ-38:

In FUNC-04-3, a cycle takes less than 6.2ms for a complete picture of the photometer and less than 1.2ms for the spectrometer one.

The FUNC-04-2 generates the demodulation signals at the bias frequency:

Each BDA group signal has its own demodulation signal adjustable in phase by a low-level command:

`SetPhotoDemodSW*` set the PSW demodulation signal phase shift.
`SetPhotoDemodMW*` set the PMW demodulation signal phase shift.
`SetPhotoDemodLW*` set the PLW demodulation signal phase shift.
`SetPhotoDemodTC*` set the TC demodulation signal phase shift.
`SetSpectroDemodSW*` set the SSW demodulation signal phase shift.
`SetSpectroDemodLW*` set the SLW demodulation signal phase shift.

**see AD1*

2.1.4.4 Physical implementation

All the functions are implemented in the FPGA. See the FPGA section of the DAQ+IF board.

2.1.5 DCU-FUNC-05 (JFET box biasing)

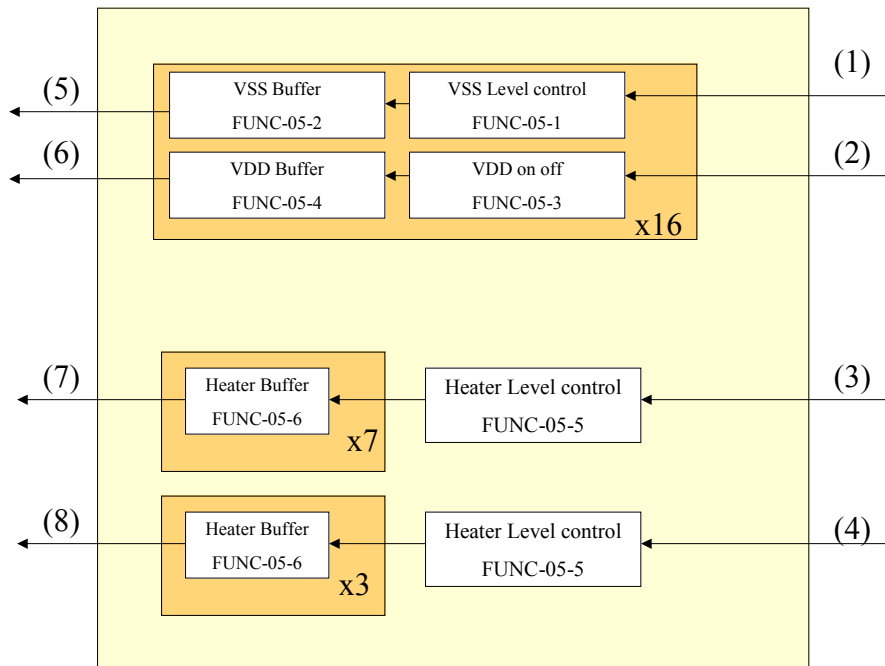


Figure 2-5: DCU-FUNC-05 diagram

2.1.5.1 Interface list

- (1) Interface **CMD_VSS**: commands VSS levels.
- (2) Interface **CMD_VDD**: commands VDD ON/OFF.
- (3) Interface **CMD_HEATER_PH**: commands heater photometer level.
- (4) Interface **CMD_HEATER_SP**: commands heater spectrometer level.
- (5) Interface **VSS**: is the group of VSS signals.
- (6) Interface **VDD**: is the group of VDD signals.
- (7) Interface **HEATER_PH**: is the group of heater photometer signals.
- (8) Interface **HEATER_SP**: is the group of heater spectrometer signals.

2.1.5.2 Functional requirement list

DRCU REQ-20: The DCU-FUNC-05 has 16 JFET bias channels and 2 JFET heater bias channels

DRCU REQ-21:

Each VSS channel level is individually adjustable by a low-level command from 0V (OFF) to -5V:

SetPhSWJfetVSS1* set the PSW VSS1 level.
 SetPhSWJfetVSS2* set the PSW VSS2 level.
 SetPhSWJfetVSS3* set the PSW VSS3 level.
 SetPhSWJfetVSS4* set the PSW VSS4 level.
 SetPhSWJfetVSS5* set the PSW VSS5 level.
 SetPhSWJfetVSS6* set the PSW VSS6 level.

SetPhMWJfetVSS1* set the PMW VSS1 level.
 SetPhMWJfetVSS2* set the PMW VSS2 level.
 SetPhMWJfetVSS3* set the PMW VSS3 level.
 SetPhMWJfetVSS4* set the PMW VSS4 level.

SetPhLWJfetVSS1* set the PLW VSS1 level.
 SetPhLWJfetVSS2* set the PLW VSS2 level.

SetTCJfetVSS1* set the TC VSS1 level.

SetSpSWJfetVSS1* set the SSW VSS1 level.
 SetSpSWJfetVSS2* set the SSW VSS2 level.

SetSpLWJfetVSS1* set the SLW VSS1 level.

Each VDD channel level is individually switched ON or OFF by a low-level command:

SetPhSWJfetPwr* with the parameter PSW_JFET_1* switch On/Off the PSW VDD1 level.
 SetPhSWJfetPwr* with the parameter PSW_JFET_2* switch On/Off the PSW VDD2 level.
 SetPhSWJfetPwr* with the parameter PSW_JFET_3* switch On/Off the PSW VDD3 level.
 SetPhSWJfetPwr* with the parameter PSW_JFET_4* switch On/Off the PSW VDD4 level.
 SetPhSWJfetPwr* with the parameter PSW_JFET_5* switch On/Off the PSW VDD5 level.
 SetPhSWJfetPwr* with the parameter PSW_JFET_6* switch On/Off the PSW VDD6 level.

SetPhMLTCWJfetPwr* with the parameter PMW_JFET_1* switch On/Off the PMW VDD1 level.
 SetPhMLTCWJfetPwr* with the parameter PMW_JFET_2* switch On/Off the PMW VDD2 level.
 SetPhMLWTCJfetPwr* with the parameter PMW_JFET_3* switch On/Off the PMW VDD3 level.
 SetPhMLWTCJfetPwr* with the parameter PMW_JFET_4* switch On/Off the PMW VDD4 level.

SetPhMLWTCJfetPwr* with the parameter PLW_JFET_1* switch On/Off the PLW VDD1 level.

SetPhMLWTCJfetPwr* with the parameter PLW_JFET_2* switch On/Off the PLW VDD2 level.

SetPhMLWTCJfetPwr* with the parameter TC_JFET* switch On/Off the TC VDD1 level.

SetSpSLWJfetPwr* with the parameter SLW_JFET_1* switch On/Off the SLW VDD1 level.

SetSpSLWJfetPwr* with the parameter SSW_JFET_1* switch On/Off the SSW VDD1 level.

SetSpSLWJfetPwr* with the parameter SSW_JFET_2* switch On/Off the SSW VDD2 level.

DRCU REQ-22:

Each heater channel level is individually adjustable by a low-level command from 0V (OFF) to -5V:

SetPhotoHeaterBias* set the photometer heater level.

SetSpectroHeaterBias* set the spectrometer heater level.

2.1.5.3 Physical implementation

The complete FUNC-05 is implemented on the BIAS BOARD.

The same two serials links described with the FUNC-02 realize the interfaces CMD_VSS, CMD_VDD, CMD_HEATER_PH and CMD_HEATER_SP.

The performance and the implementation of the function FUNC-05 are described in the BIAS BOARD section.

2.1.6 DCU-FUNC-06 (Low-level command decoding)

See FPGA section.

2.1.7 DCU-FUNC-07 (Low-level command acknowledge + hk parameter transfer)

See FPGA section.

2.1.8 DCU-FUNC-08 (Relative timestamp generation)

See FPGA section.

2.1.9 DCU-FUNC-09 (Housekeeping parameter digitization)

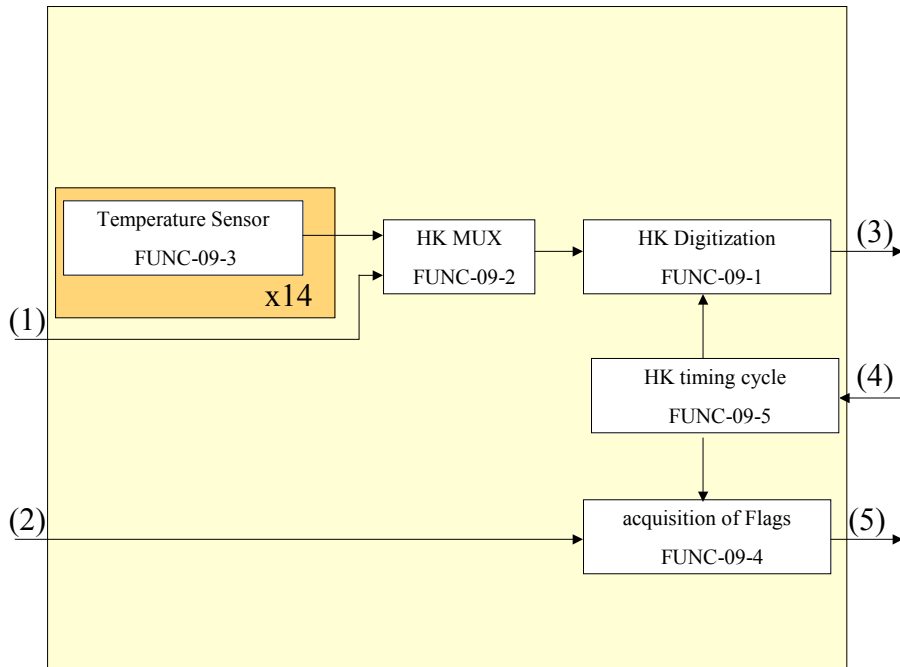


Figure 2-6: DCU-FUNC-09 diagram

2.1.9.1 Interface list

- (1) Interface **SUPPLIES**: power supplies signals.
- (2) Interface **FLAGS**: flags signals.
- (3) Interface **D_HK**: hk values.
- (4) Interface **CMD_HK**: commands the HK digitization.
- (5) Interface **D_FLAG**: flags values.

2.1.9.2 Functional requirement list


DRCU REQ-28: Each board has an AD590 temperature sensor.

2.1.9.3 Physical implementation

The functions FUNC-09-1, FUNC-09-2 and FUNC-09-4 are implemented on the DAQ+IF BOARD.

The performances and the implementations of these functions are described in the DAQ+IF BOARD section.

Function FUNC-09-3, each board has its temperature sensor.

	<p>DCU Design document</p>	 <p>SAP-SPIRE- FP-0063-02 Issue: 1.0 Date : 11/07/2005</p>
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2.1.10 DCU-FUNC-10 (Digitized data transfer)

See FPGA section.

2.1.11 DCU-FUNC-11 (Powers supplies distribution)

See DCU Power Supply section.

3 PERFORMANCE

3.1 PHYSICAL REPARTITION OF THE DCU FUNCTIONS

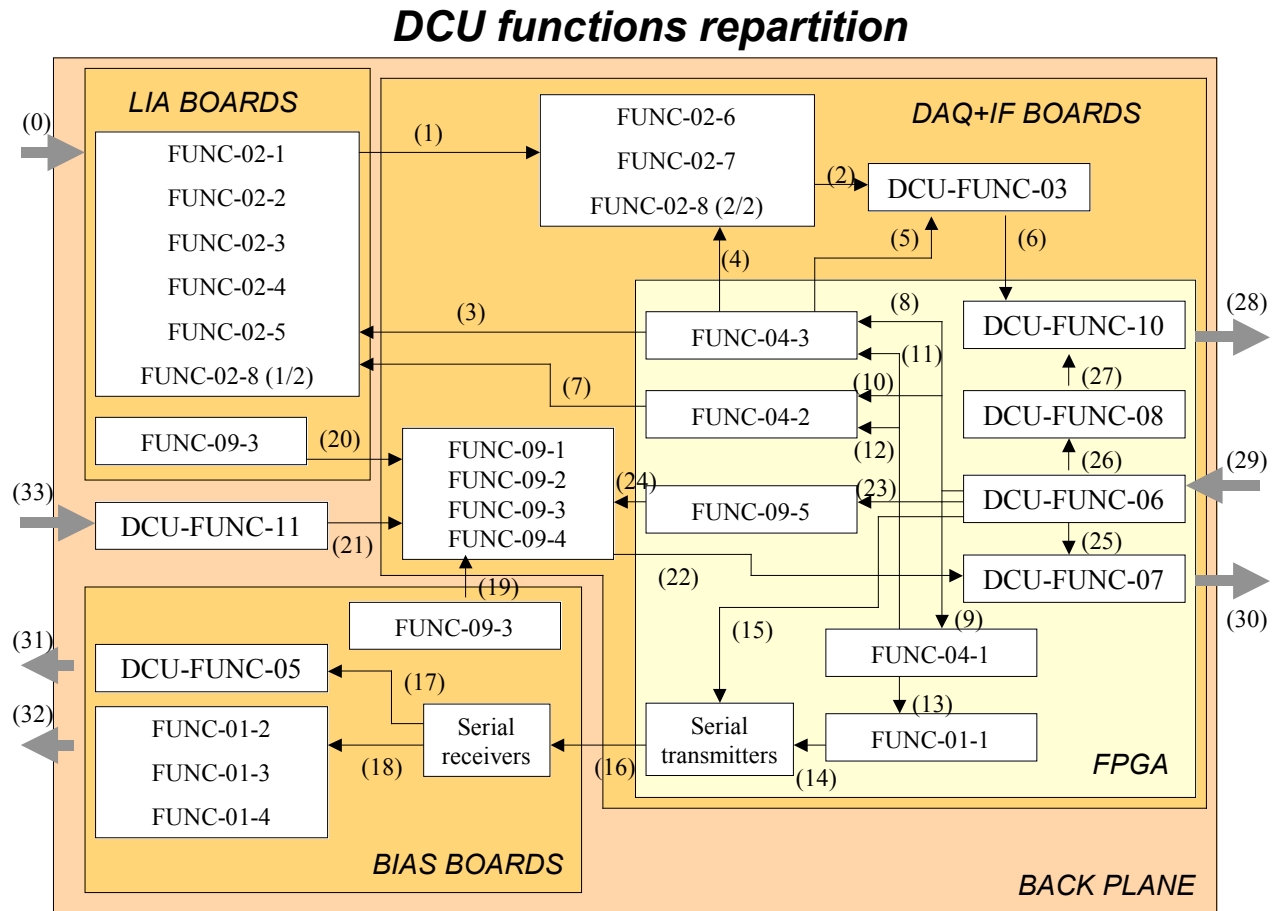














Figure 3-1: DCU functions repartition

3.1.1 INTERFACE LIST

Number	Link	Description
(0)	IN_PSW	Modulated signals from BDA PSW.
	IN_PLW	Modulated signals from BDA PLW.
	IN_PMW	Modulated signals from BDA PMW.
	IN_TC	Modulated signals from BDA TC.
	IN_SLW	Modulated signals from BDA SLW.
	IN_SSW	Modulated signals from BDA SSW.
(1)	MUX_CHANNELS	Multiplexed channels after the first mux stage.
(2)	INPUT_ADC	Multiplexed channels after the second mux stage.
(3)	CMD_MUX_L	Mux LIA commands
(4)	CMD_MUX_H	Mux DAQ+IF commands
	CMD_OFFSET	Offset commands
(5)	CMD_ADC	ADC commands
(6)	DATA_ADC	ADC data
(7)	DEMOD_PLW	Demodulation signal for PLW BDA.
	DEMOD_PMW	Demodulation signal for PMW BDA.
	DEMOD_TC	Demodulation signal for TC BDA.
	DEMOD_SLW	Demodulation signal for SLW BDA.
	DEMOD_SSW	Demodulation signal for SSW BDA.
	DEMOD_PLW	Demodulation signal for PLW BDA.
(8)(9)	CMD_MODE	Modes commands
(9)	CMD_FREQUENCY	Bias frequency and Sample frequency commands
(10)	CMD_DEMOD	Phases shift demodulation commands
(11)	SAMPLE_CLK	Sample clock
(12)(13)	BIAS_CLK	BIAS clock
(14)(17)(16)	SINE_WAVE_D	Data of the sine wave
(15)(17)(16)	AMPL_BIAS_PSW	First bias level command
	AMPL_BIAS_PMW	Second bias level command
	AMPL_BIAS_PLW	Third bias level command
	AMPL_BIAS_TC	Fourth bias level command
	AMPL_BIAS_SSW	Fifth bias level command
	AMPL_BIAS_SLW	Sixth bias level command
(15)(18)(16)	CMD_VSS	VSS levels commands
	CMD_VDD	VDD ON/OFF commands.
	CMD_HEATER_PH	Heater photometer level commands.
	CMD_HEATER_SP	Heater spectrometer level commands.
(19)	BIAS_TEMPERATURE	BIAS board temperature
(20)	LIA_TEMPERATURE	LIA boards temperature
(21)	SUPLIES	Powers supplies signals
	FLAGS	Flags signals
(22)	D_HK	HK values
	D_FLAG	Flags values
(23)	CMD_HK	HK commands
(24)	HK_CYCLE_SIG	HK cycle signals
(25)	CMD_ACK&STATUS	Commands acknowledge and DCU status
(26)	TIME_RST	Timestamp reset
(27)	TIME_DATA	Timestamp data
(28)	DATA	Instrument data
(29)	CMD	DPU commands
(30)	HK_ACK	HK and acknowledge
(31)	VSS/VDD/HEATER	JFET DC bias
(32)	BIAS	Bolometer bias
(33)	POWER	Powers supplies

3.1.2 FUNCTIONS LIST

Function	Detail	Description	Note	Pictogram
DCU-FUNC-01 Detector bias generation	FUNC-01-1	Digital sine generator	1 prime / 1 redundant	
	FUNC-01-2	Conversion digital to analog	2 prime / 2 redundant	
	FUNC-01-3	Bias Level control	6 prime / 6 redundant	
	FUNC-01-4	Bias differential transmitter	6 prime / 6 redundant	
DCU-FUNC-02 Bolometer signal processing	FUNC-02-1	Differential receiver	288 photo / 72 spectro	
	FUNC-02-2	Band pass filter	288 photo / 72 spectro	
	FUNC-02-3	Gain before demodulation	288 photo / 72 spectro	
	FUNC-02-4	Demodulation	288 photo / 72 spectro	
	FUNC-02-5	Low pass filter	288 photo / 72 spectro	
	FUNC-02-6	DC offset	288 photo / 72 spectro for prime and redundant	
	FUNC-02-7	End gain	6 prime / 6 redundant	
	FUNC-02-8	Mux N to M	(1/2) 18 mux 16 to 1 photo 6 mux 16 to 1 spectro (2/2) 6 mux 3 to 1 photo 6 mux 1 to 1 spectro For prime and redundant	
DCU-FUNC-03	x	Bolometer signal digitization	1 prime / 1 redundant	
DCU-FUNC-04 Timing cycle	FUNC-04-1	Bias timing cycle	1 prime / 1 redundant	
	FUNC-04-2	Demodulation timing cycle	1 prime / 1 redundant	
	FUNC-04-3	Digitization timing cycle	1 prime / 1 redundant	
DCU-FUNC-05 JFET box biasing	FUNC-05-1	Vss control level	16 prime / 16 redundant	
	FUNC-05-2	VSS buffer	16 prime / 16 redundant	
	FUNC-05-3	VDD on / off	16 prime / 16 redundant	
	FUNC-05-4	VDD buffer	16 prime / 16 redundant	
	FUNC-05-5	Heater control level	2 prime / 2 redundant	
	FUNC-05-6	Heater buffer	10 prime / 10 redundant	
DCU-FUNC-06	x	Low-level command decoding	1 prime / 1 redundant	
DCU-FUNC-07	x	Low-level command acknowledge + HK parameter transfer	1 prime / 1 redundant	
DCU-FUNC-08	x	The relative timestamp generation	1 prime / 1 redundant	
DCU-FUNC-09 JFET box biasing	FUNC-09-1	HK digitization	1 prime / 1 redundant	
	FUNC-09-2	HK mux	1 prime / 1 redundant	
	FUNC-09-3	Temperature sensor	14 prime / 14 redundant	
	FUNC-09-4	Flags acquisition	1 prime / 1 redundant	
	FUNC-09-5	HK timing cycle	1 prime / 1 redundant	
DCU-FUNC-10	x	Digitized data transfer	1 prime / 1 redundant	
DCU-FUNC-11	x	Powers supplies distribution		

3.2 PHYSICAL OVERVIEW

The following drawing shows:

- How the DCU is connected to the FPU.
- The different harness types and their location.
- That the DCU power supply is provided by the PSU.
- The data exchange link with the DPU PRIME and REDUNDANT.

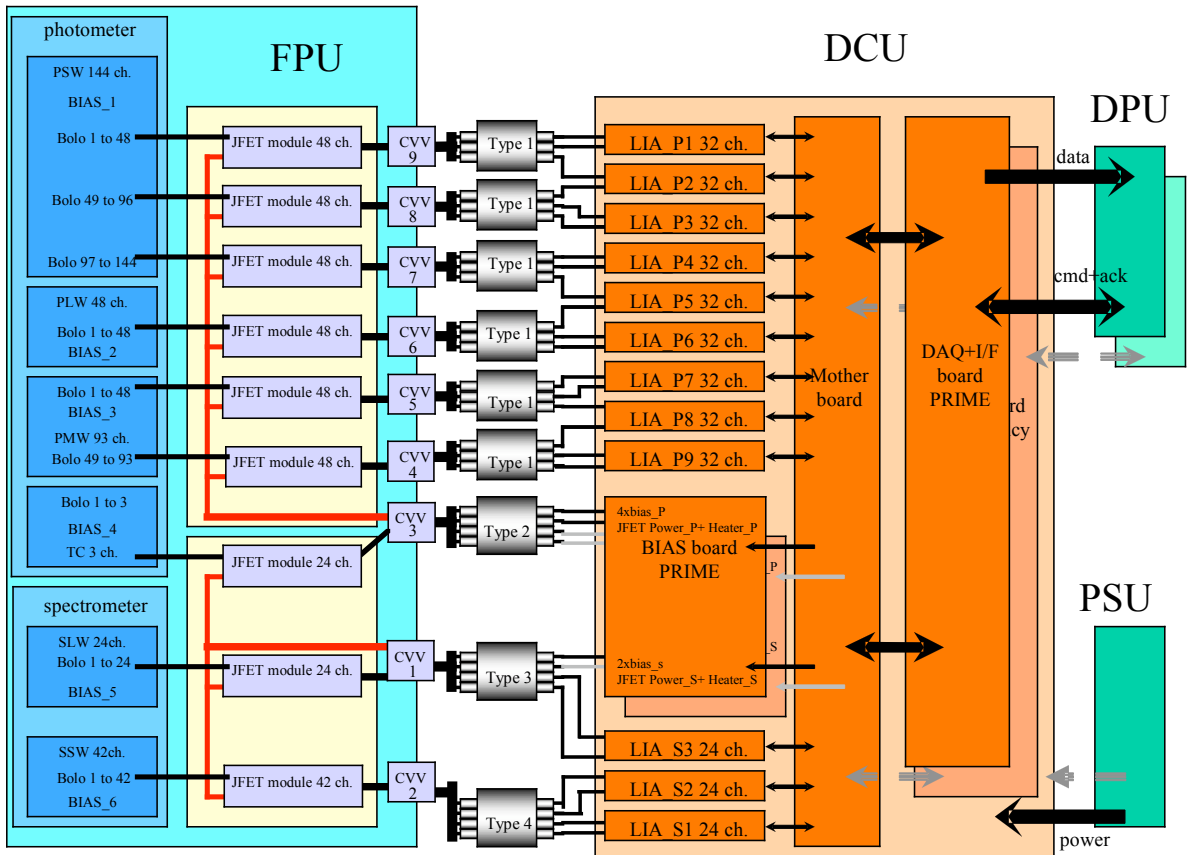


Figure 3-2: DCU Overview

Harness Type 1, 2, 3 and 4 compliant with Spire harness definition document.

3.3 PHOTOMETER

Nine LIA_P boards make up the LIA photometer section.

1. LIA_P1 to LIA_P4 and the first 16 channels of LIA_P5 will receive and process the signals from 144 “PSW bolometers.”

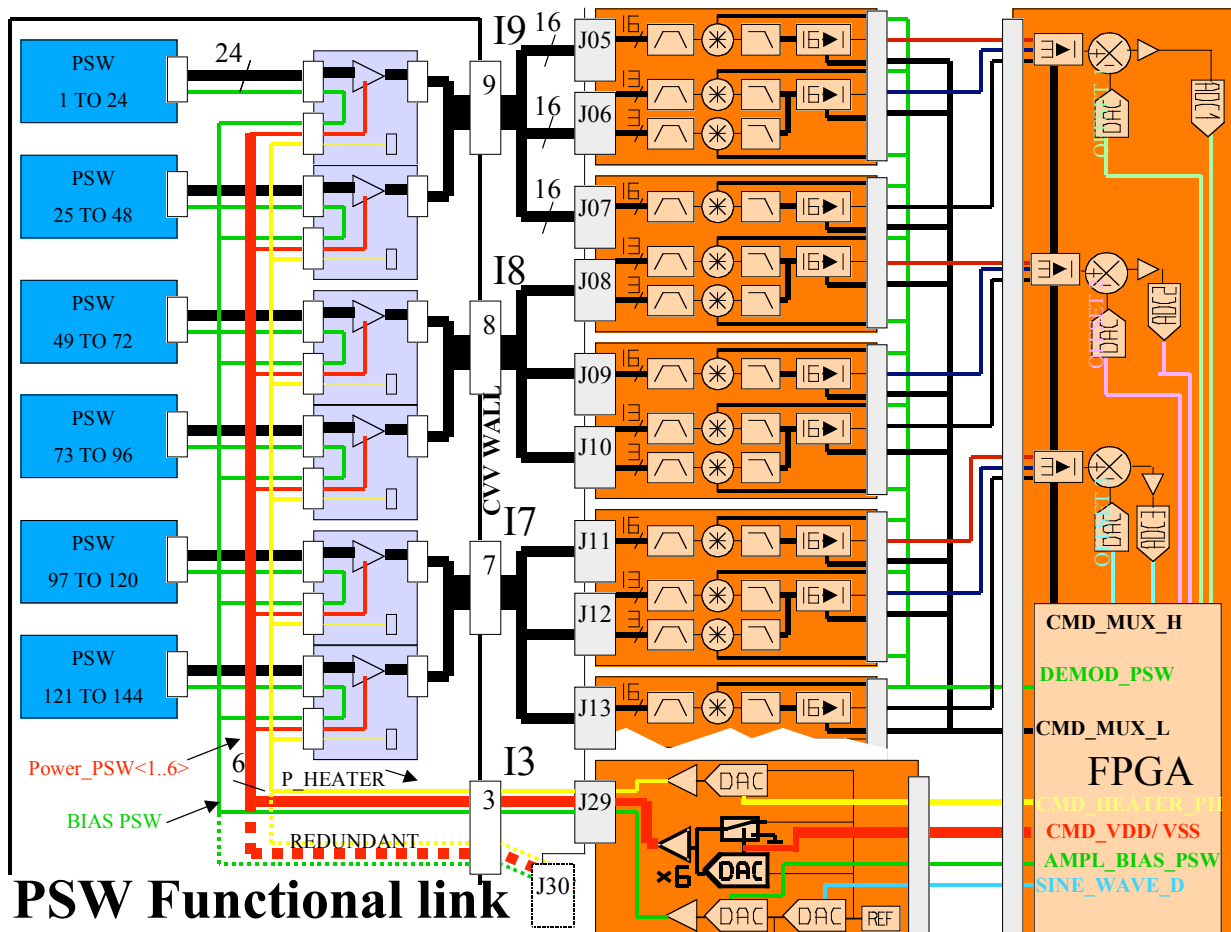


Figure 3-3 PSW Photometer Functional Links

- The 144 PSW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_PSW.)
- All of the 144 channels are sent to the DAQ+IF board through 9 differential links that are digitized by 3 ADCs.

- The other 16 channels from LIA_P5 and LIA_P6 receive and process signals from 48 “PLW bolometers.”

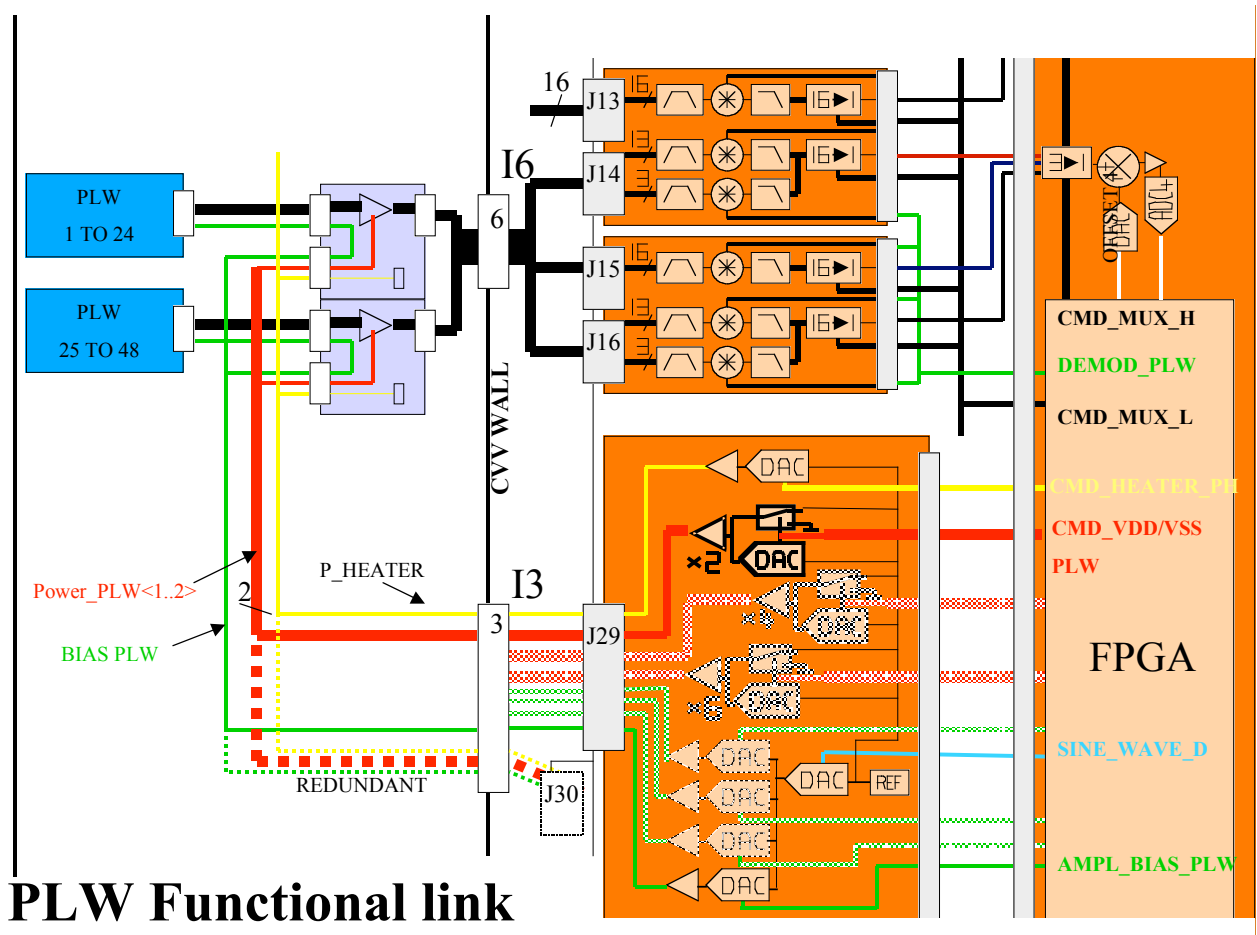


Figure 3-4 PLW Photometer Functional Links

- The 48 PLW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_PLW.)
- All of the 48 channels are sent to the DAQ+IF board through 3 differential links that are digitized by one ADC.

3. LIA_P7 to LIA_P8 and the first 29 channels of the LIA_P9 receive and process the signals from 93 “PMW bolometers.”

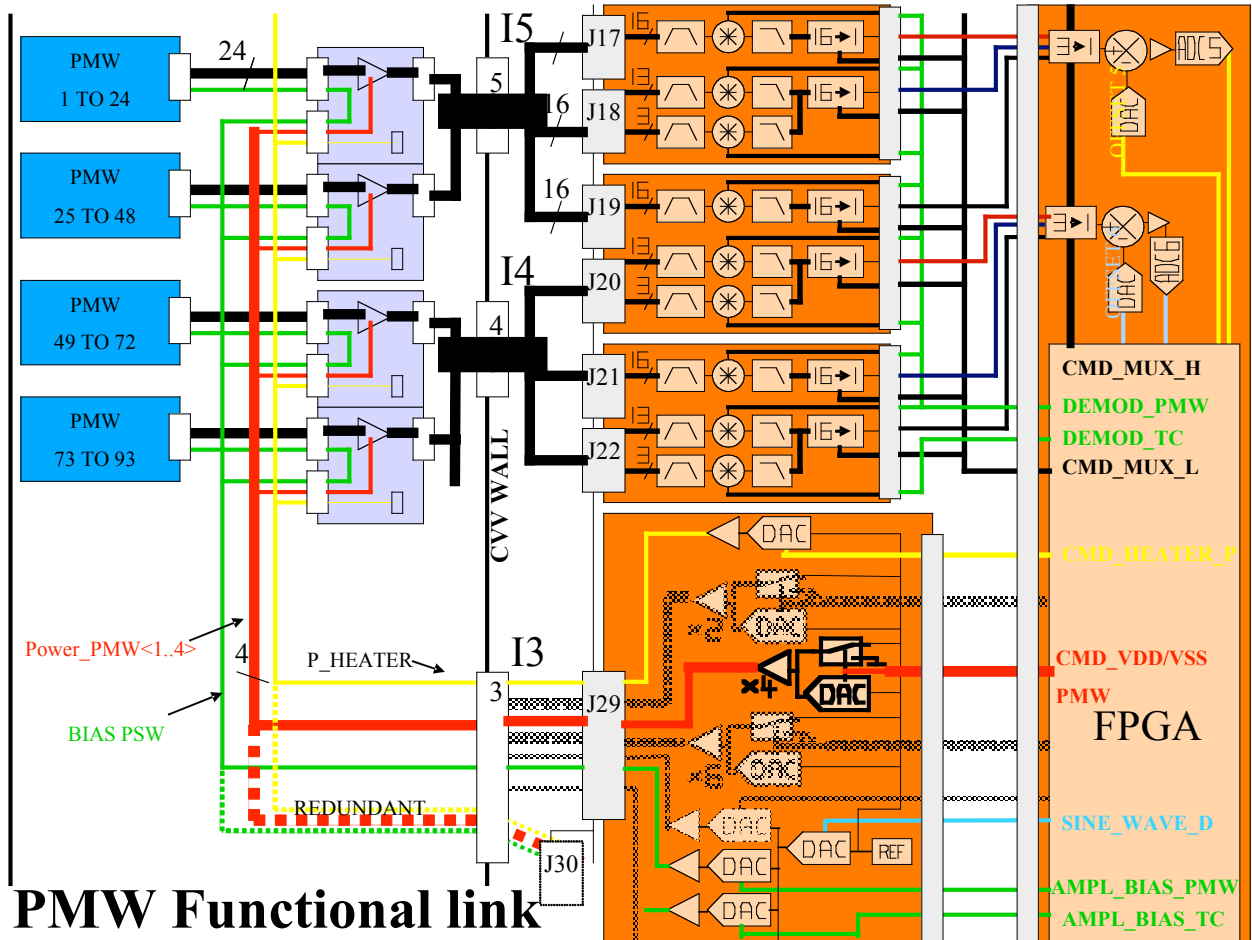


Figure 3-5 PMW Photometer Functional Links

- The 93 PMW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOM_PMW.)
- All of the 93 channels are sent to the DAQ+IF board through 6 differential links that are digitized by 2 ADCs.

4. The last 3 channels of the LIA_P9 receive and process signals from 3 “T/C bolometers.”

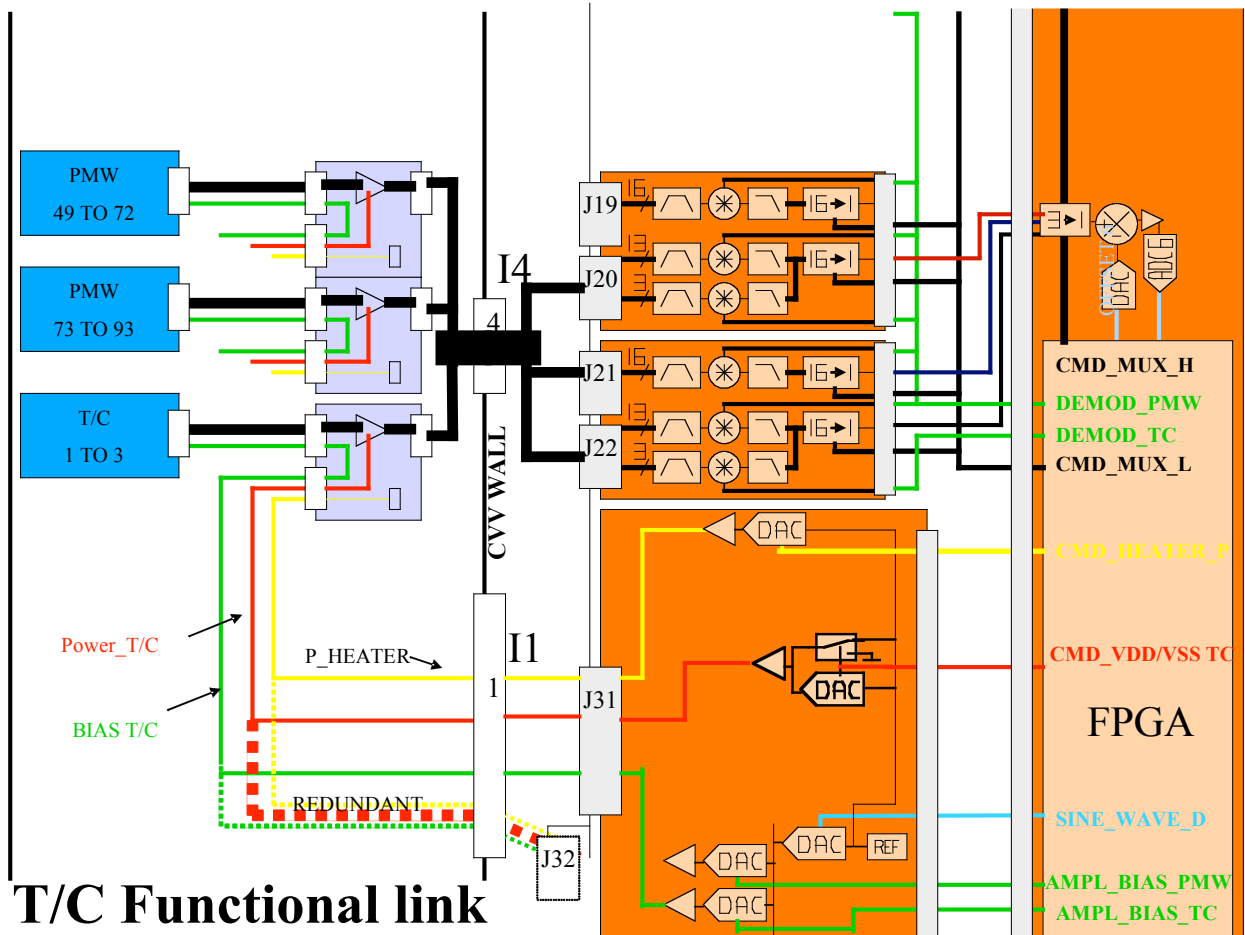


Figure 3-6 T/C Photometer Functional Links

- The 3 T/C channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_T/C)
- All 3 channels are sent to the DAQ+IF board through one differential link that is digitized by one ADC.
- Note: The T/C bias signals go through connectors J31 and J32 as well as harness I1 that are mainly used to carry the spectrometer signals. However, these T/C signals always refer to the photometer's ground.

3.3.1 LIA channel allocation

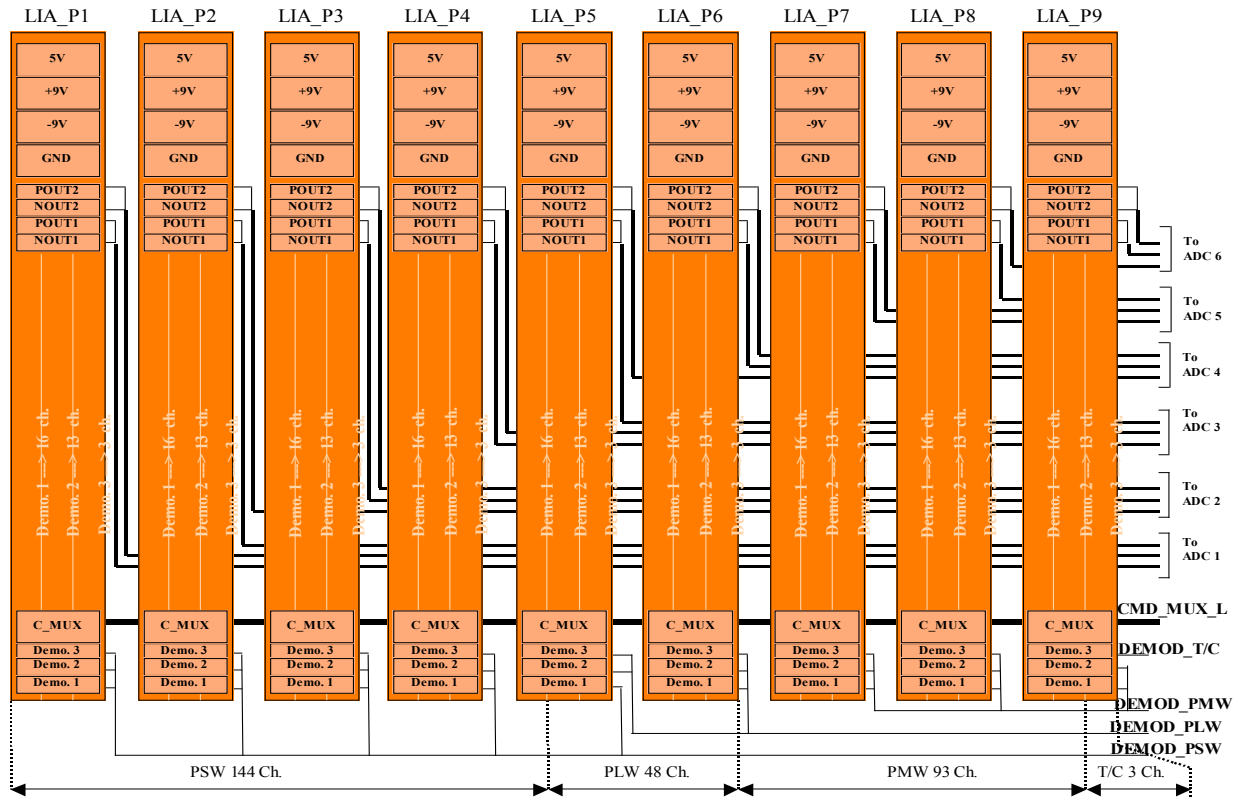


Figure 3-7 LIA Photometer Section

Each group receive its own respective demodulation signal: DEMOD_PSW, DEMOD_PMW, DEMOD_PLW and DEMOD_T/C. Each of these signals can have a different phase shift.

The LIA photometer is supplied only when the SPIRE instrument is running in the photometer mode.

Each LIA photometer board receives its own group of 3 supply lines (-9V, +9V and 5V), which will be automatically shutdown if an error occurs on one of these three lines.

3.4 SPECTROMETER

Three LIA_S boards make up the LIA spectrometer section.

- LIA_S1 and LIA_S2 receive and process signals from forty-two “S-SW bolometers.”
- LIA_S3 receive and process signals from twenty-four “S-LW bolometers.”

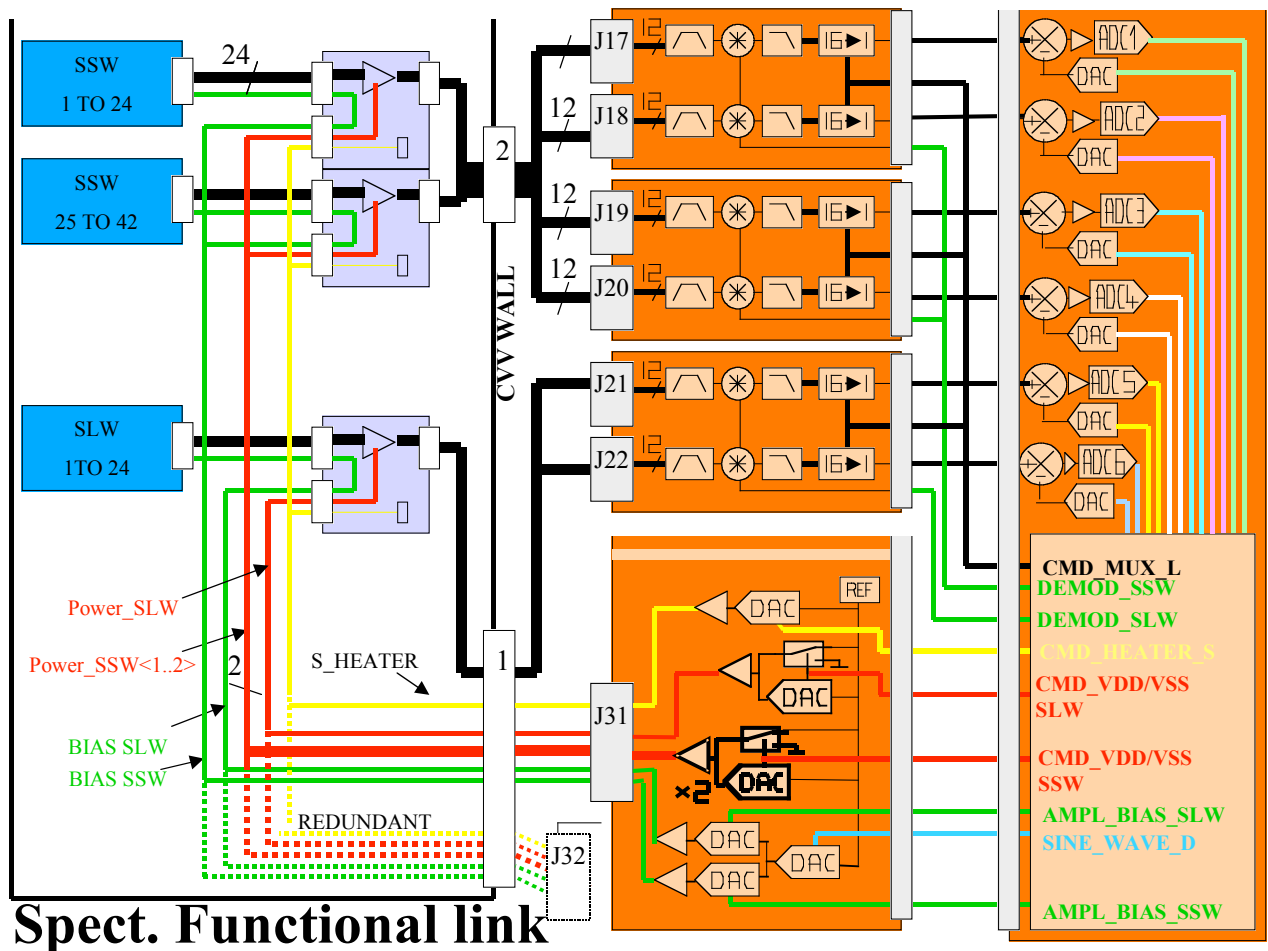


Figure 3-8 Spectrometer Functional Links

The 24 SLW channels receive the same sinus bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_SLW.)

All of the 24 channels are sent to the DAQ+IF board through two differential links that are digitized by two ADCs.

The 42 SSW channels + six spare channels receive the same sinus bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_SSW.)

All of the 42 channels are sent to the DAQ+IF board through four differential links that are digitized by four ADCs.

3.4.1 LIA channel allocation

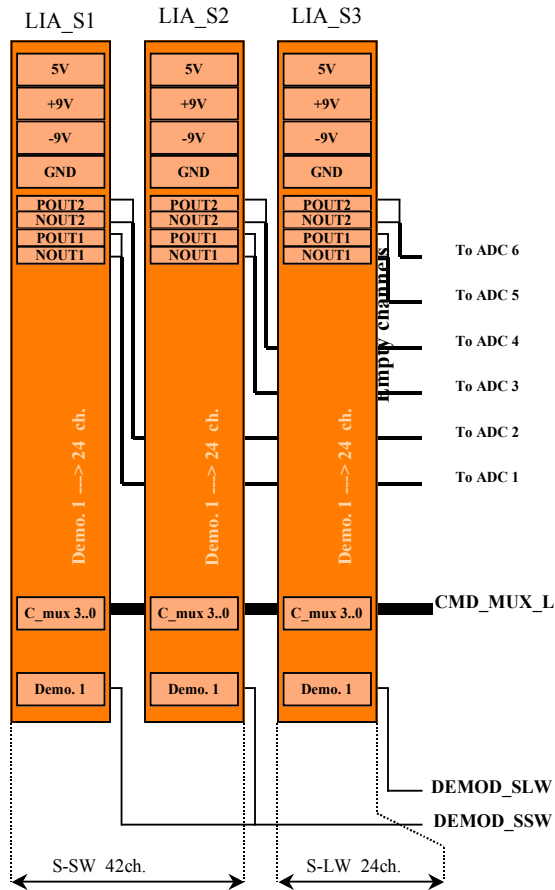


Figure 3-9 LIA Spectrometer Section

Each group receive its own respective demodulation signal: DEMOD_SSW and DEMOD_SLW. These signals can each have a different phase shift.

The LIA spectrometer is supplied only when the SPIRE instrument is running in spectrometer mode.

Each LIA spectrometer board receives its own group of 3 supply lines (-9V, +9V and 5V), which are automatically shutdown if an error occurs in on one of these three lines.

3.5 LIA PHOTOMETER BOARD

3.5.1 LIA Photometer Board Overview

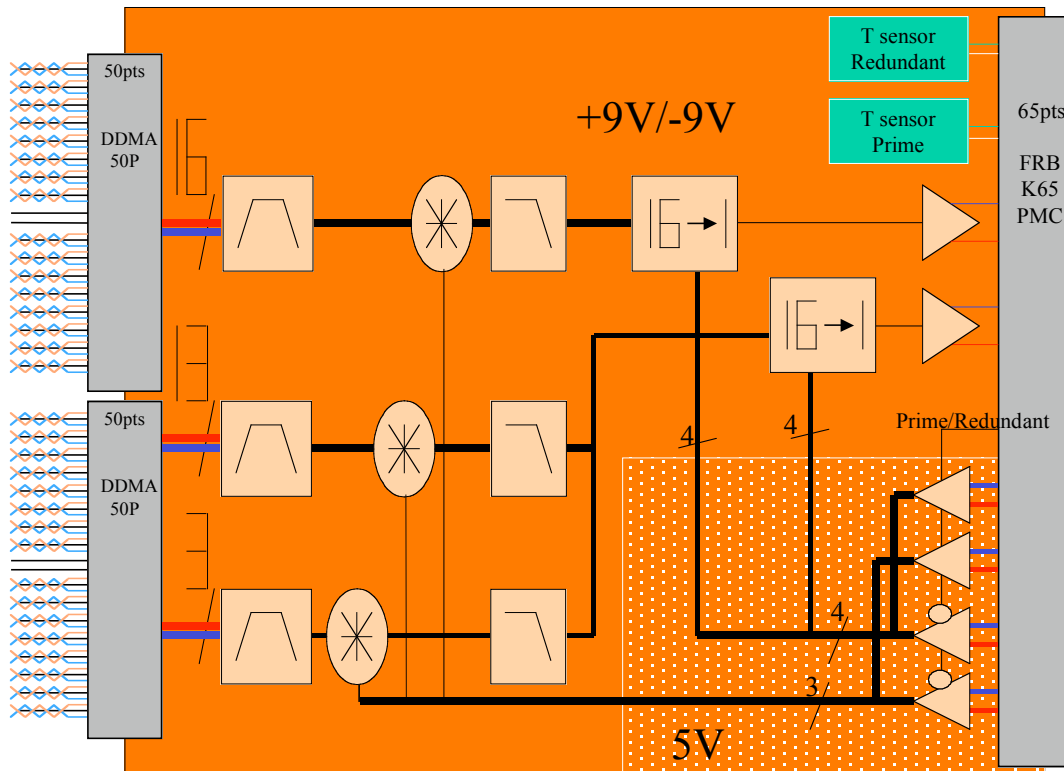


Figure 3-10 LIA Photometer Board Overview

- **The LIA_P board has thirty-two channels that are divided into three groups:**
 - A group of sixteen channels which go to the first multiplexer.
 - A group of thirteen channels, which go to the second multiplexer.
 - A group of three channels, which also go to the second multiplexer.
- **Each of the three groups can receive its own demodulation signal.**
- **The receivers that relay the multiplexer command signals as well as the demodulation signals are redundant:**
 - A PRIME/REDUNDANT signal from the PSU activates the PRIME receivers when the PRIME power supply turns on and the REDUNDANT receivers when the REDUNDANT power supply turns on.
 - The LIA PRIME receivers are connected to the PRIME DAQ+IF board.
 - The LIA REDUNDANT receivers are connected to the REDUNDANT DAQ+IF board.
- **The two multiplexers receive the same command signals.**

3.5.2 LIA Photometer Board Interface

Interface	Signal Name	Description	Type	Level	In/Out	Frequency
IN_PSW IN_PLW IN_PMW IN_TC	IN+ <i>xx</i>	Bolometer Differential Signal JEFT output	Analogic	11mVrms (AC) <i>photo</i> (31mVrms TC) + 15mV (DC) 1V Common mode offset	IN	50-300Hz
	IN- <i>xx</i>					
MUX_CHANNEL	POUT <i>x</i>	sixteen LIA_P channels multiplexed in one differential signal	Analogic	0 to 5V	OUT	0-5Hz at mux freq. ~10kHz
	NOUT <i>x</i>					
CMD_MUX_H	PA <i>x</i> -	BIT Command Mux (PRIME) Differential Signal	Digital (LVDS)	-0,3Vto 0,3V	IN	~10kHz
	PA <i>x</i> +					
	RA <i>x</i> -	BIT Command Mux (REDUNDANT) Differential Signal	Digital (LVDS)	-0,3Vto 0,3V	IN	~10kHz
	RA <i>x</i> +					
DEMOD_PLW/PMW PSW	PDEM0D1-	Demodulation Differential Signal (PRIME) for Channels One to Sixteen	Digital (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	PDEM0D1+					
	PDEM0D2-	Demodulation Differential Signal (PRIME) for Channels Seventeen to Twenty-nine	Digital (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	PDEM0D2+					
DEM0D_PLW/PMW PSW/TC	PDEM0D3-	Demodulation Differential Signal for Channels Thirty to Thirty two	Digital (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	PDEM0D3+					
DEM0D_PLW/PMW PSW	RDEM0D1-	Demodulation Differential signal (REDUNDANT) for Channels One to Sixteen	Digital (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	RDEM0D1+					
	RDEM0D2-	Demodulation Differential Signal (REDUNDANT) for Channels Seventeen to Twenty-nine	Digital (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	RDEM0D2+					
DEM0D_PLW/PMW PSW/TC	RDEM0D3-	Demodulation Differential Signal for (REDUNDANT) Channels Thirty to Thirty two	Digital (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	RDEM0D3+					
LIA_TEMPERATURE	PT_P9V	Sensor PRIME Bias	Analogic	9V	IN	DC
	PT	Output Sensor PRIME	Analogic	2 to 4V	OUT	-
	RT_P9V	Sensor REDUNDANT Bias	Analogic	9V	IN	DC
	RT	Output Sensor REDUNDANT	Analogic	2 to 4V	OUT	-
POWER	P9V	9V Power Supply	Power	9V	IN	DC
	N9V	-9V Power Supply	Power	-9V	IN	DC
	P9V_P	PRIME/REDUNDANT Signal	Analogic	0 to 9V	IN	DC
	P5V	5V Power Supply	Power	5V	IN	DC
	GND	Grounding	Power	0V	-	DC

3.5.3 LIA PHOTOMETER and TC FUNCTIONS

3.5.3.1 LIA Photometer or TC Channel Overview

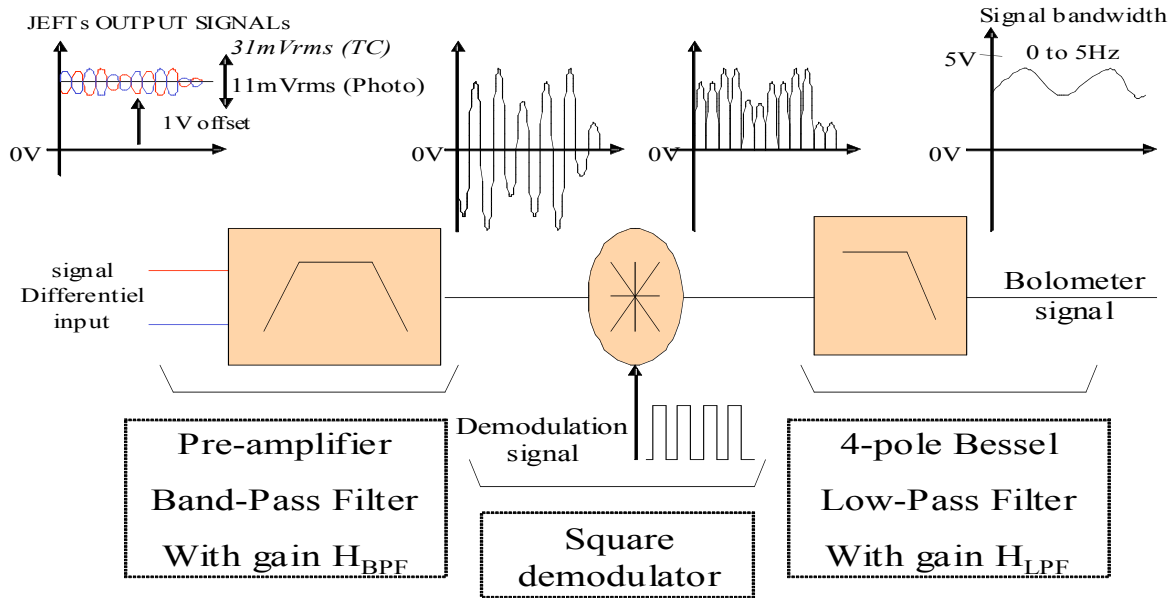


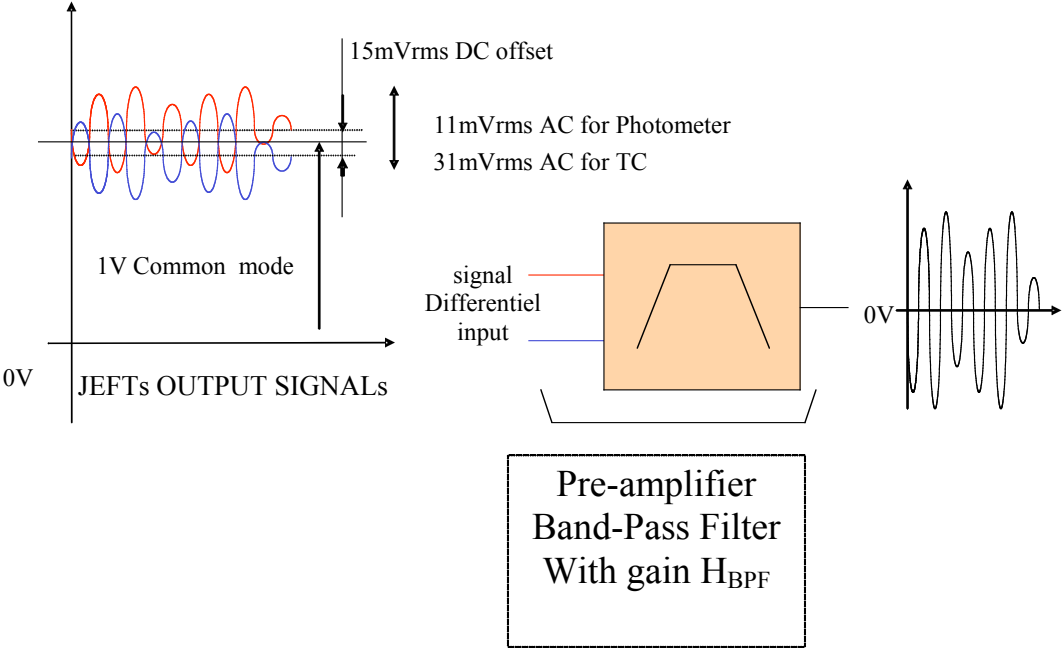
Figure 3-11 LIA Photometer or TC Board Channel

The input differential signal that comes from a bolometer is amplified and its DC component is eliminated by the pre-amplifier BPF. Then, it is demodulated by a squared signal. Afterwards, a four-pole Bessel LPF filters it.

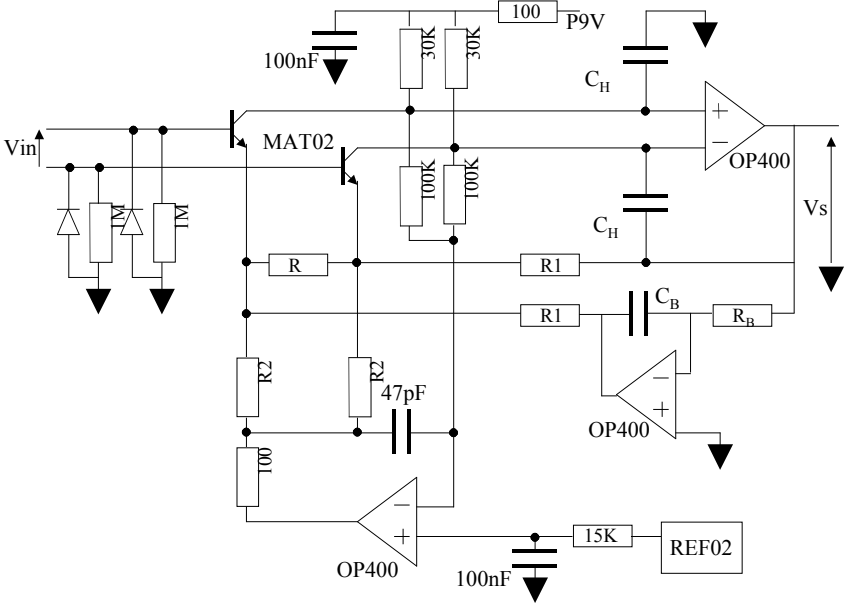
3.5.3.2 LIA Photometer or TC Pre-amplifier BPF (FUNC-02 –1, FUNC-02 –2 and FUNC-02 –3)

The pre-amplifier BPF does the three following functions:

- FUNC-02-1 Differential receiver.
- FUNC-02-2 Band pass filter.
- FUNC-02-3 Gain before demodulation.



3.5.3.2.1 Preamplifier circuit



The differential input of the pre-amplifier use MAT02 and OP400 to provide a good common mode rejection

The MAT02 are chosen in order to make an every low noise differential input.

The integrator in the feedback loop removes the differential offset. The maximum differential DC offset removed is 19mV.

3.5.3.2.2 Preamplifier transfer function

$$\frac{V_S}{V_{in}} = H_{BPF} = G \cdot \left(\frac{R_B \cdot C_B \cdot R}{1 + (R_B \cdot C_B) p + \left(\frac{R}{G} + R1 \right) C_H \cdot R_B \cdot C_B \cdot p^2} \right) \text{ with } G = \left(+ \frac{R1}{R2} + \frac{2R1}{R} \right)$$

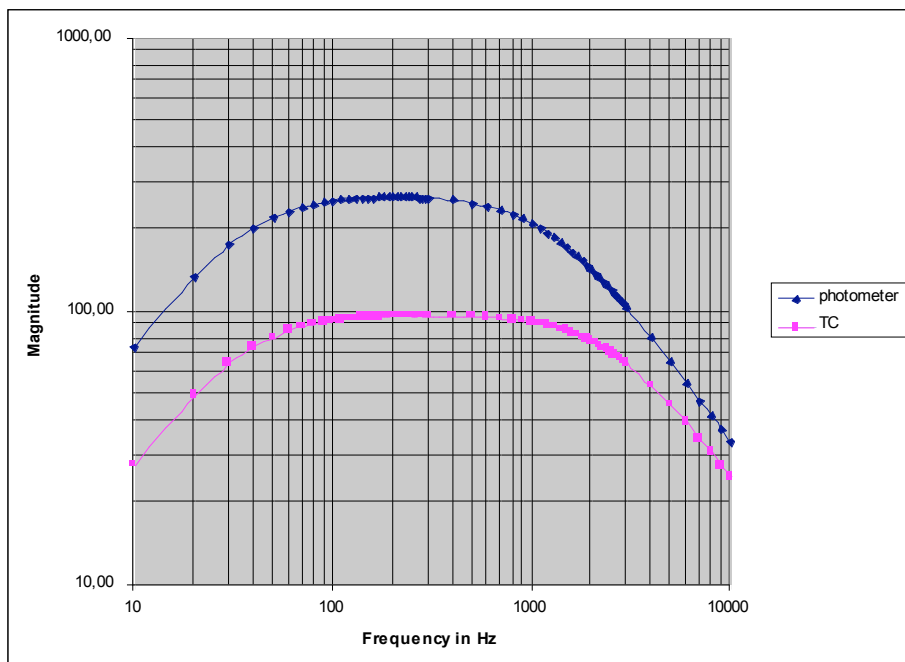
R1=R2=15K; R=115 (for photometer channels) or R=316 (For TC channels); R_B=100K; C_B=47nF; C_H=1.5nF;

Mat02 Transconductance: S=3.868x10⁻³ for T=300K

So $H_{BPF} = 262.8 \cdot \left(\frac{4.7 \cdot 10^{-3} \cdot p}{1 + 4.7 \cdot 10^{-3} p + 5.85 \cdot 10^{-7} \cdot p^2} \right)$ for photometer channels

$H_{BPF} = 96.9 \cdot \left(\frac{4.7 \cdot 10^{-3} \cdot p}{1 + 4.7 \cdot 10^{-3} p + 5.85 \cdot 10^{-7} \cdot p^2} \right)$ For TC channel

	Photometer		TC	
	frequency	magnitude	frequency	magnitude
max	208,11	262,8	299,48	96,9
Low cut of	33,01	189,64	33,44	68,5
High cut of	1311,98		2681,97	



3.5.3.2.3 Preamplifier Common mode Rejection simulation result

The following simulation result shows the common mode transfer function. It shows that we have at least -80dB common mode rejection between 50Hz and 300Hz.

In other words, there is some leeway with the -60dB requirement.

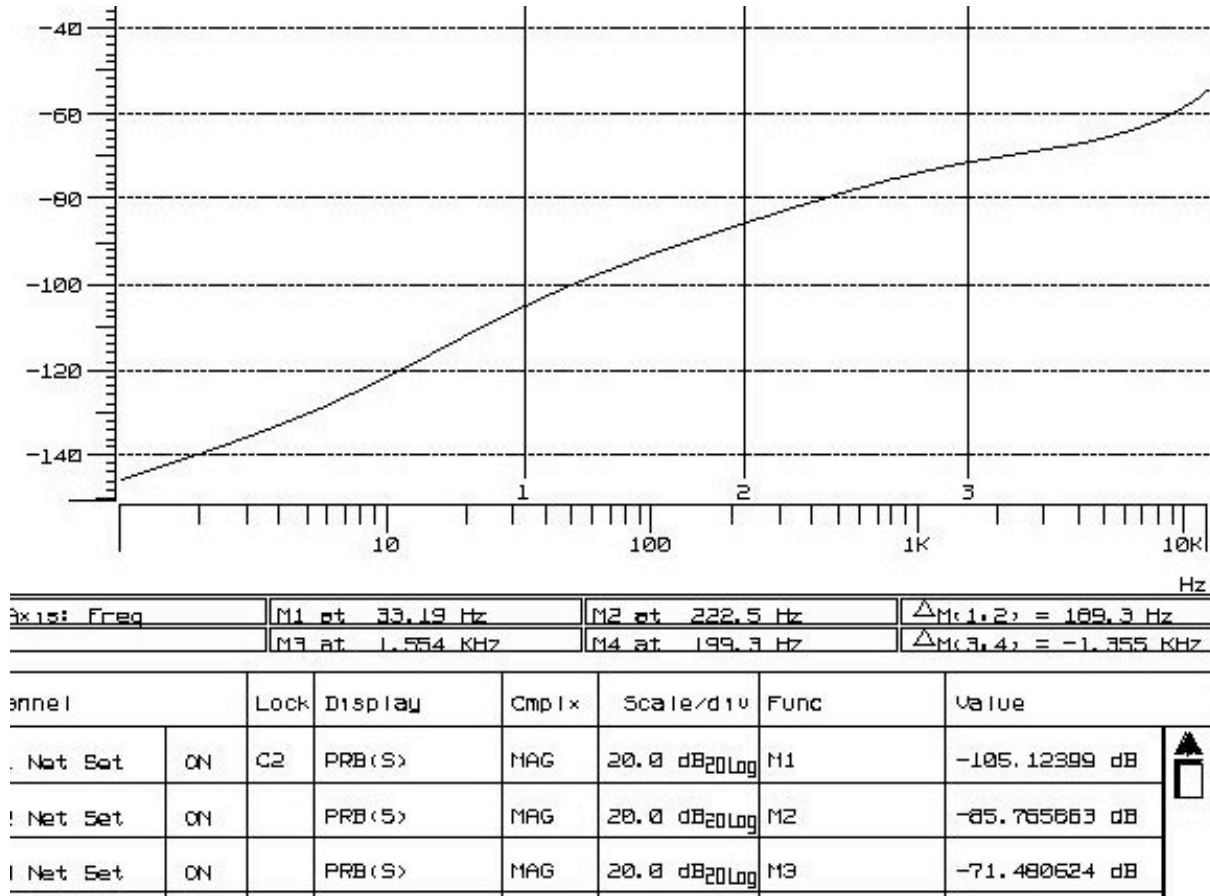
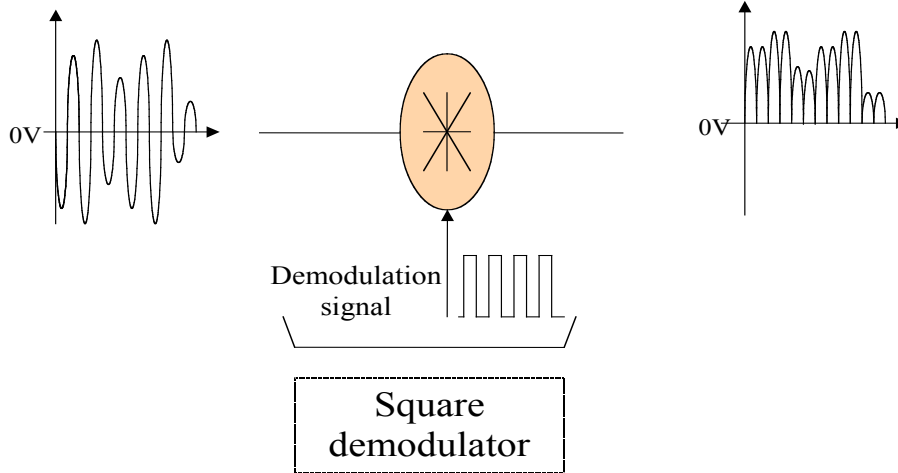


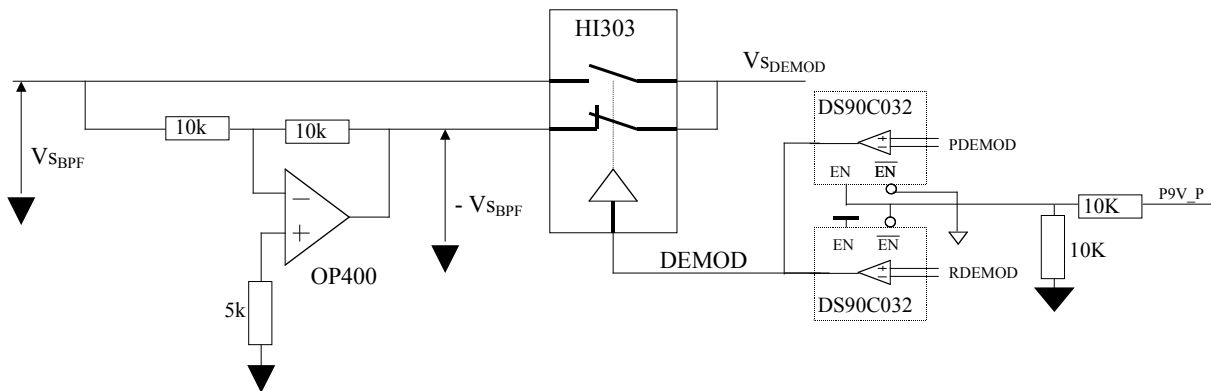
Figure 3-12 LIA Photometer Pre-amplifier BPF Common Mode Rejection

3.5.3.3 LIA Photometer demodulation (FUNC-02 –4)



Switching between the signal and his opposite does the demodulation of the signal coming for the pre-amplifier. This switching is command by the signal DEMOD_PSW for PSW channels, DEMOD_PMW for PMW ones, DEMOD_PLW for PLW ones, and DEMOD_TC for TC ones. The analog switch HI303 does the switch. The opposite signal is done by an OP400 in inverter circuit.

3.5.3.3.1 Demodulation circuit



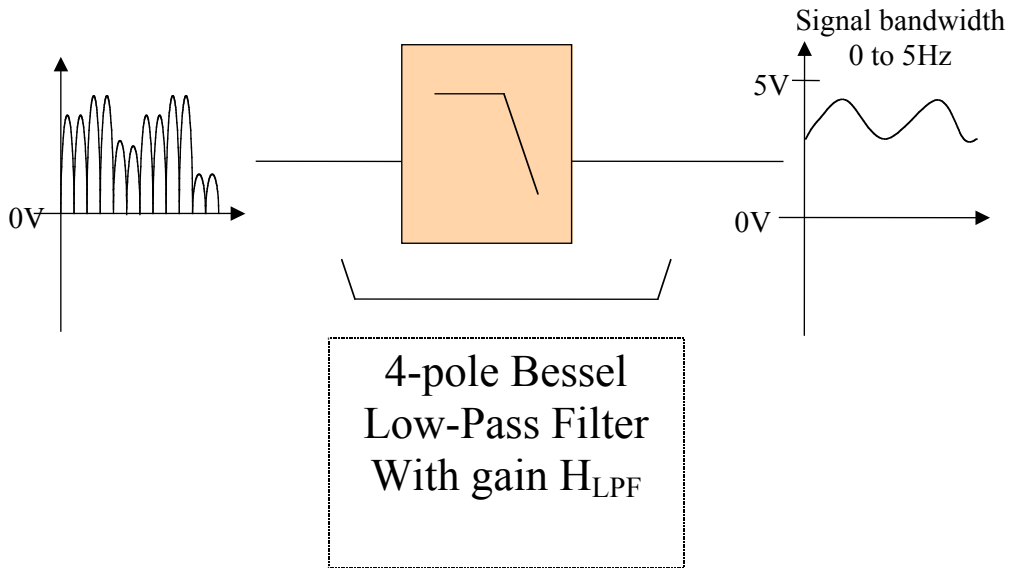
3.5.3.3.2 Output expression

$$V_{SBPF} = V_{in} \cdot H_{BPF}$$

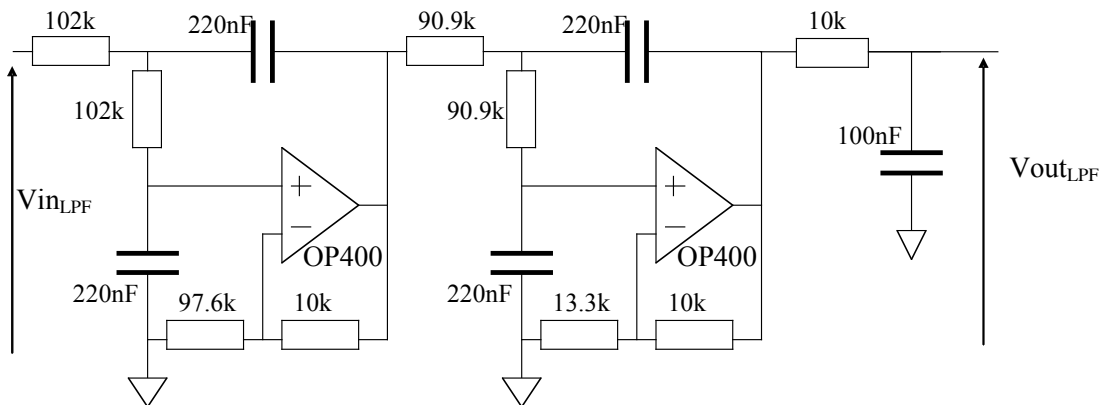
$$V_{SDEMOD}(\omega t) = V_{SBPF} \sum_{n=0}^{\infty} \frac{4}{(1+2n)\pi} \sin[(1+2n)\omega t]$$

3.5.3.4 LIA Photometer LPF (FUNC-02 -5)

The photometer low pass filters are 4 pole Bessel low pass filters.



3.5.3.4.1 LPF circuit



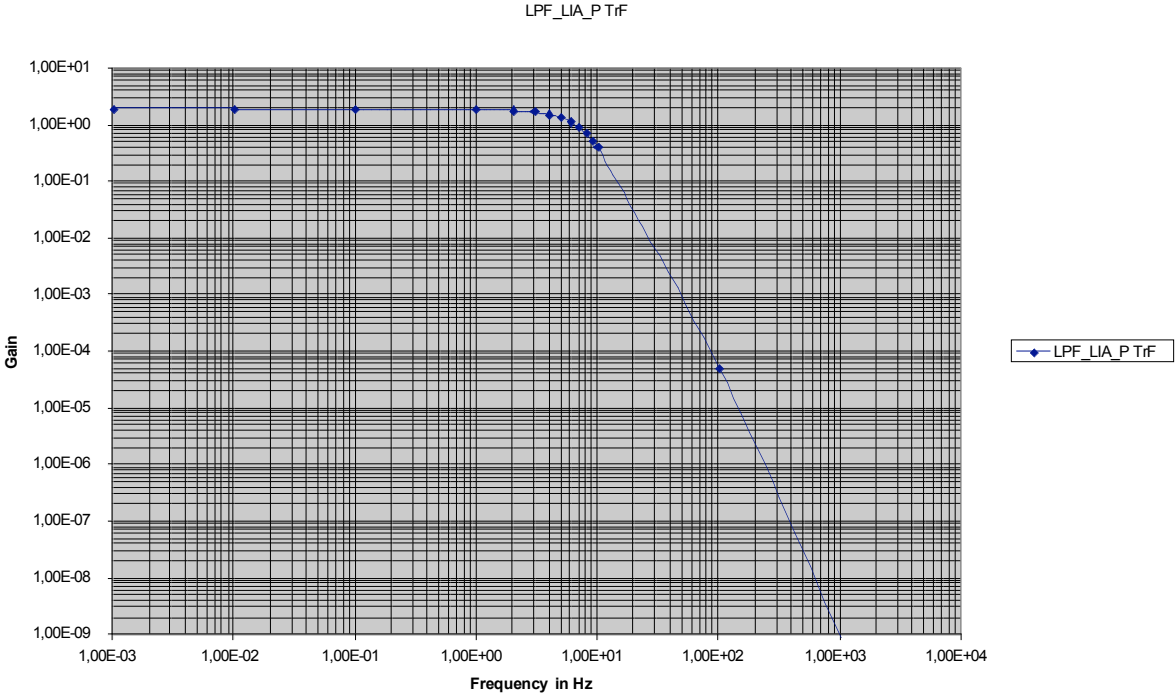
3.5.3.4.2 LPF transfer function

Transfer function:

$$H_{LPF} = \frac{V_{out\ LPF}}{V_{in\ LPF}} = 1.93 \times \frac{1}{1 + 42.58 \cdot 10^{-3} p + 503 \cdot 10^{-6} p^2} \times \frac{1}{1 + 24,96 \cdot 10^{-3} p + 400 \cdot 10^{-6} p^2} \times \frac{1}{1 + 10^{-3} p}$$

(p=j2πf)

Cut off frequency -3dB: Fc = 4,98Hz



3.5.3.5 LIA Photometer Channel Input Noise

MAT02 : BW 50 –300Hz : $V_n=1nV/\sqrt{Hz}$

Resistors noise : $I_n=\sqrt{\frac{4kT}{R}}$; T=295K ; $4kT=1.63\times 10^{-20}$

Input preamplifier noise: $V_{n_{preamp}}=\sqrt{2\times(V_{n_{MAT02}})^2+115^2(I_{n_{15k}}^2+4I_{n_{5k}}^2)}=2nV/\sqrt{Hz}$

OP400 at 0.1Hz: $V_n=66nV/\sqrt{Hz}$; $I_n=1.6pV/\sqrt{Hz}$

LPF Stage 1: $V_{n_{LPF1}}=\sqrt{(V_{n_{OP400}})^2+(213\times 10^3\times I_{n_{OP400}})^2+2V_{n_{02k}}^2}=352nV/\sqrt{Hz}$

LPF Stage 2: $V_{n_{LPF1}}=\sqrt{(V_{n_{OP400}})^2+(188\times 10^3\times I_{n_{OP400}})^2+V_{n_{188k}}^2}=313nV/\sqrt{Hz}$

Input noise LPF: $V_{n_{LPF}}=\sqrt{(V_{n_{LPF1}})^2+\left(\frac{V_{n_{LPF2}}}{1.1}\right)^2}=452nV/\sqrt{Hz}$

Total noise at the photometer LPF output:

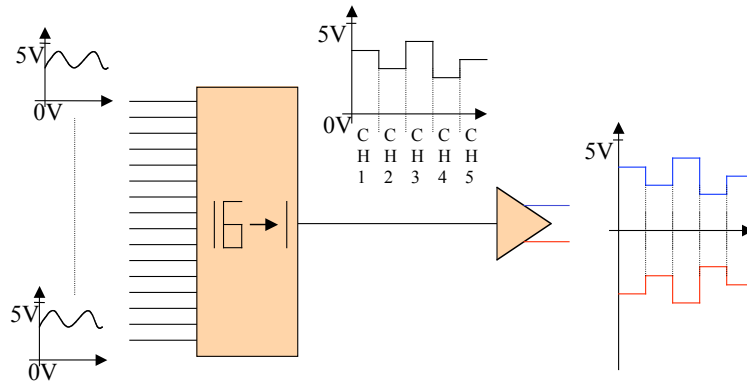
$$V_{n_{LPFout}}=\sqrt{\left[(V_{n_{preamp}}\times H_{BPF})^2\times\left(\frac{4}{X}\right)\times\left[1+\left(\frac{1}{5}\right)+\left(\frac{1}{5}\right)+\left(\frac{1}{7}\right)+\left(\frac{1}{9}\right)\right]+(V_{n_{LPF}})^2\right]\times H_{LPF}^2}=1646nV/\sqrt{Hz}$$

Band pass filter gain $H_{BPF}=261$; Low pass filter gain $H_{LPF}=1.93$ and Total channel gain $H_{TOT}=454$

So the input noise equivalent for a photometer channel is:

$$V_{n_{in}}=\frac{V_{n_{LPFout}}}{H_{TOT}}=3.62nV/\sqrt{Hz}$$

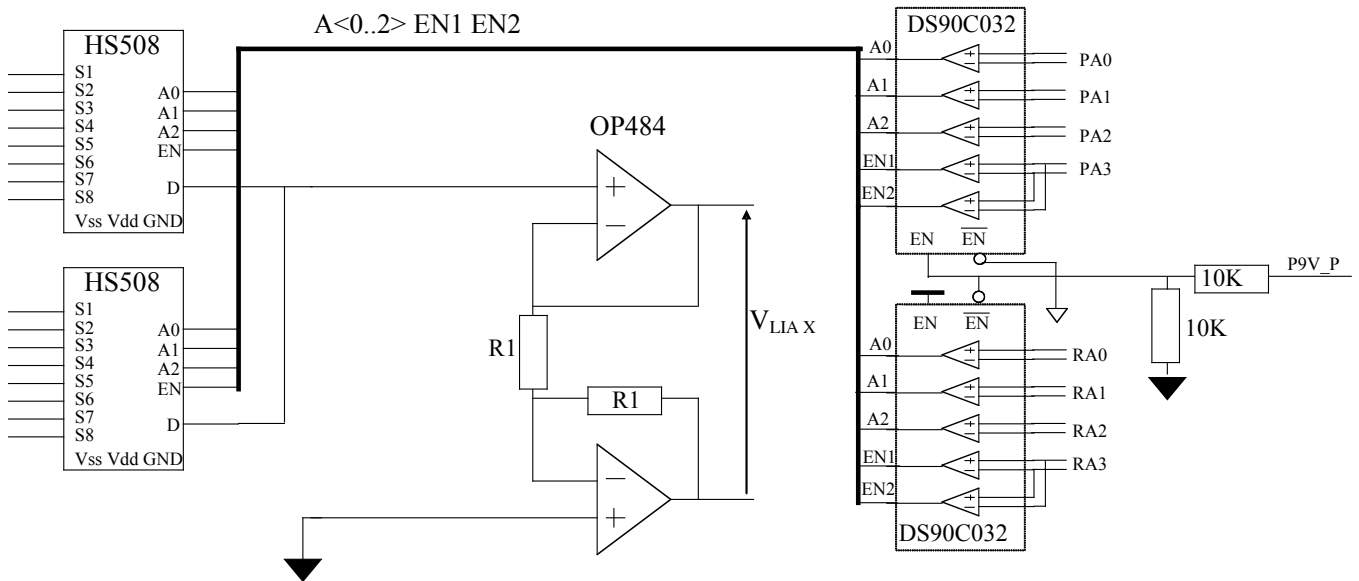
3.5.3.6 LIA Photometer MUX FUNC-02-8 (1/2) and LIA outputs



The first multiplexing stage FUNC-02-8 (1/2) is done by analog mux HS508. The differential output is done by two OP484.

See circuit.

3.5.3.6.1 Circuit



Channels address:

A3 A2 A1 A0	Output 1	Output 2
0000	CH1	CH17
0001	CH3	CH19
0010	CH5	CH21
0011	CH7	CH23
0100	CH9	CH25
0101	CH11	CH27
0110	CH13	CH29
0111	CH15	CH31
1000	CH2	CH18
1001	CH4	CH20
1010	CH6	CH22
1011	CH8	CH24
1100	CH10	CH26
1101	CH12	CH28
1110	CH14	CH30
1111	CH16	CH32

CH1 to CH32 refer to input connectors pinning

3.5.3.6.2 Noise

See noise synthesis section (on DAQ+IF).

3.5.3.6.3 Timing

See FPGA section.

3.5.3.6.4 LIA Channel Gain

$$Gain_{LIA} = \frac{V_{out_{LPF}}}{V_{in}} = H_{BPF} \times \frac{2 \cdot \sqrt{2}}{\pi} \times H_{LPF}$$

Modulation Frequency	Photometer channel gain	TC channel gain
50	385,04	140,69
60	405,67	148,10
70	419,76	153,18
80	429,66	156,76
90	436,79	159,36
100	442,02	161,30
110	445,92	162,77
120	448,87	163,90
130	451,11	164,80
140	452,81	165,51
150	454,10	166,08
160	455,06	166,54
170	455,77	166,92
180	456,25	167,24
190	456,56	167,49
200	456,73	167,70
210	456,76	167,88
220	456,69	168,02
230	456,52	168,13
240	456,27	168,22
250	455,94	168,30
260	455,55	168,35
270	455,10	168,39
280	454,59	168,42
290	454,03	168,43
300	453,42	168,44

3.6 LIA SPECTROMETER BOARD

3.6.1 LIA Spectrometer Board Overview

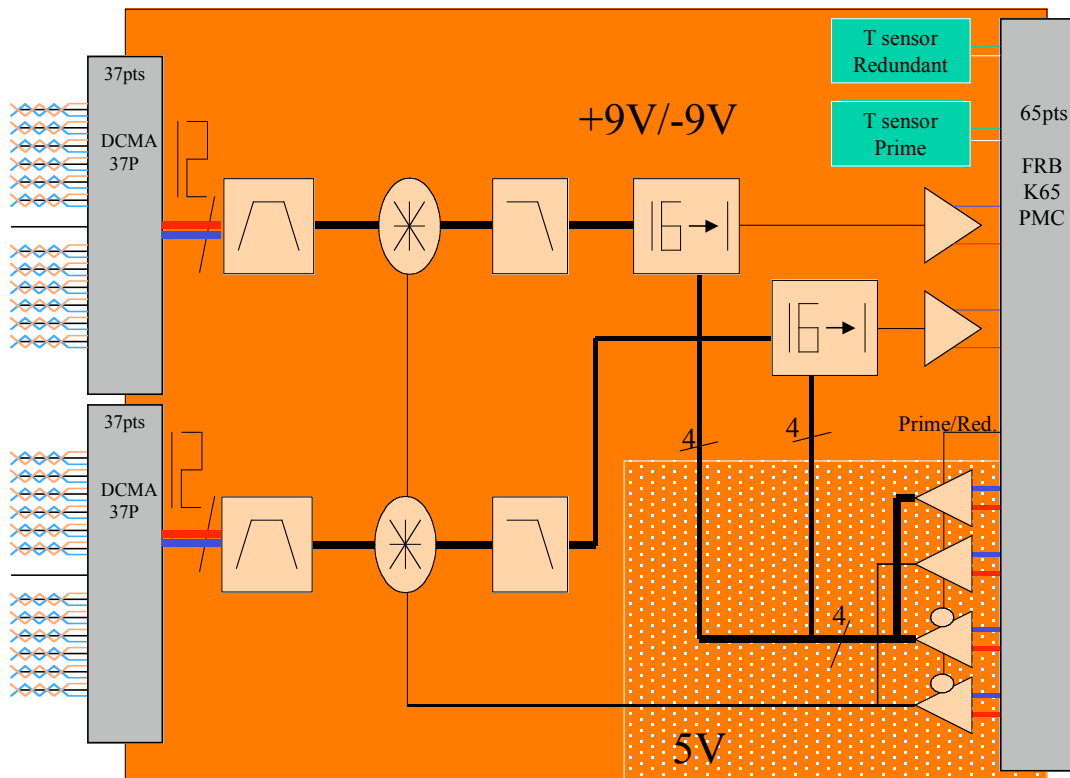


Figure 3-13 LIA Spectrometer Board Overview

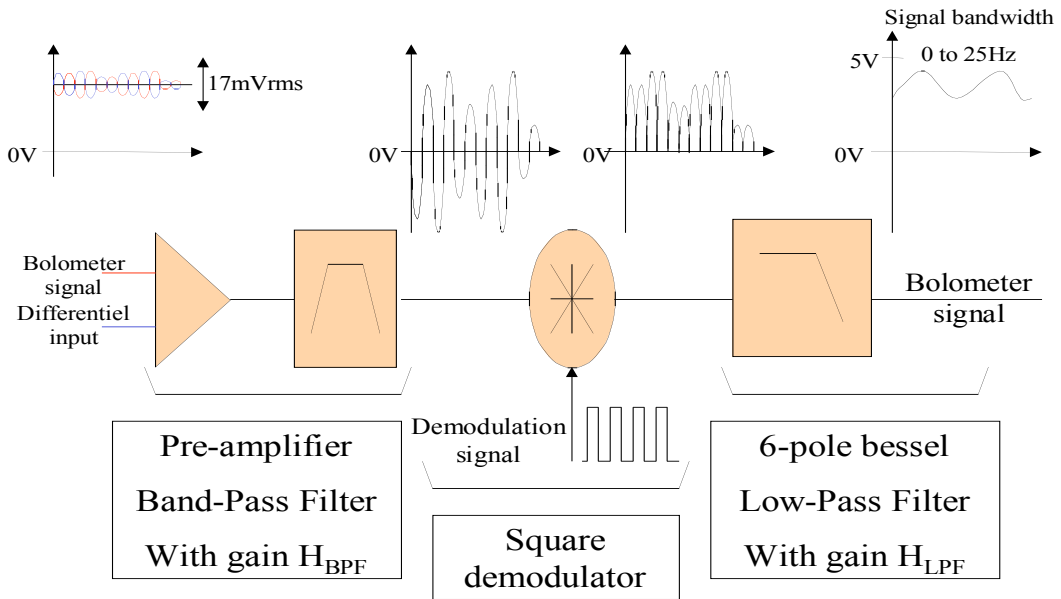
- Each LIA_S board has twenty-four channels, which are divided into two groups.
Each group of 12 channels goes to a multiplexer.
- The two groups receive the same demodulation signal.
- The receivers that relay the multiplexers command signal and demodulation signal are redundant as they are on the LIA photometer boards.
- The two multiplexers receive the same command signals.

3.6.2 LIA Spectrometer Board Interface

Interface	Name	Description	Type	Level	In/Out	Frequency
IN_SSW IN_SLW	IN+ <i>xx</i>	Bolometer Differential Signal	Analogic	11mVrms (AC) + 1.5V (DC)	IN	50-300Hz
	IN- <i>xx</i>					
MUX_CHANNEL	POUT <i>x</i>	The twelve LIA_S channels Multiplexed in a Differential Signal	Analogic	0 to 5V	OUT	0-25Hz at mux freq.
	NOUT <i>x</i>					
CMD_MUX_H	PAX-	BIT Command Mux (PRIME) Differential Signal	Digital (LVDS)	-0,3Vto 0,3V	IN	~10kHz
	PAX+					
	RAX-	BIT Command Mux (REDUNDANT) Differential Signal	Digital (LVDS)	-0,3Vto 0,3V	IN	~10kHz
	RAX+					
DEMOD_SSW DEMOD_SLW	PDEM0D1-	Demodulation Differential Signal (PRIME) for Channels One to Twenty-four	Digital (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	PDEM0D1+					
	RDEM0D1-	Demodulation Differential Signal (REDUNDANT) for Channels One to Twenty-four	Digital (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	RDEM0D1+					
LIA_TEMPERATURE	PT_P9V	Sensor PRIME Bias	Analogic	9V	IN	DC
	PT	Output Sensor PRIME	Analogic	2 to 4V	OUT	-
	RT_P9V	Sensor REDUNDANT Bias	Analogic	9V	IN	DC
	RT	Output Sensor REDUNDANT	Analogic	2 to 4V	OUT	-
POWER	P9V	9V Power Supply	Power	9V	IN	DC
	N9V	-9V Power Supply	Power	-9V	IN	DC
	P9V_P	PRIME/REDUNDANT Signal	Analogic	0 to 9V	IN	DC
	P5V	5V Power Supply	Power	5V	IN	DC
	GND	Grounding	Power	0V	-	DC

3.6.3 LIA SPECTROMETER FUNCTIONS

3.6.3.1 LIA Spectrometer Channel Overview

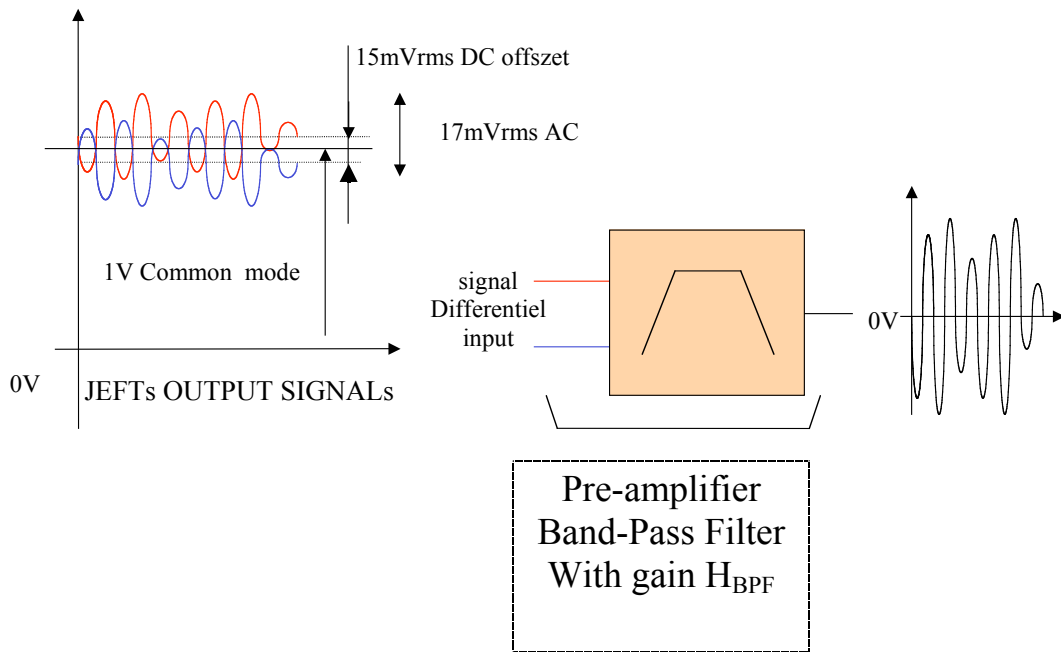


The input differential signal that comes from a bolometer is amplified and its DC component is eliminated by the pre-amplifier BPF. Then, it is demodulated by a squared signal. Afterwards a six-pole Bessel LPF filters it.

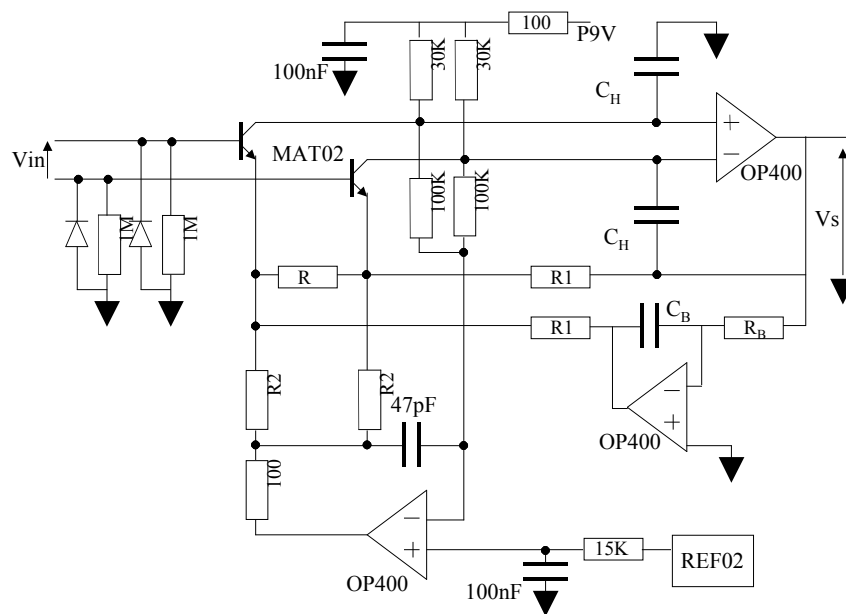
3.6.3.2 LIA Spectrometer Pre-amplifier BPF (FUNC-02 –1, FUNC-02 –2 and FUNC-02 –3)

The pre-amplifier BPF does the three following functions:

- FUNC-02-1 Differential receiver.
- FUNC-02-2 Band pass filter.
- FUNC-02-3 Gain before demodulation.



3.6.3.2.1 Circuit



The differential input of the pre-amplifier use MAT02 and OP400 to provide a good common mode rejection

The MAT02 are chosen in order to make an every low noise differential input.

The integrator in the feedback loop removes the differential offset. The maximum differential DC offset removed is 19mV.

3.6.3.2.2 Preamplifier transfer function

Transfer function:

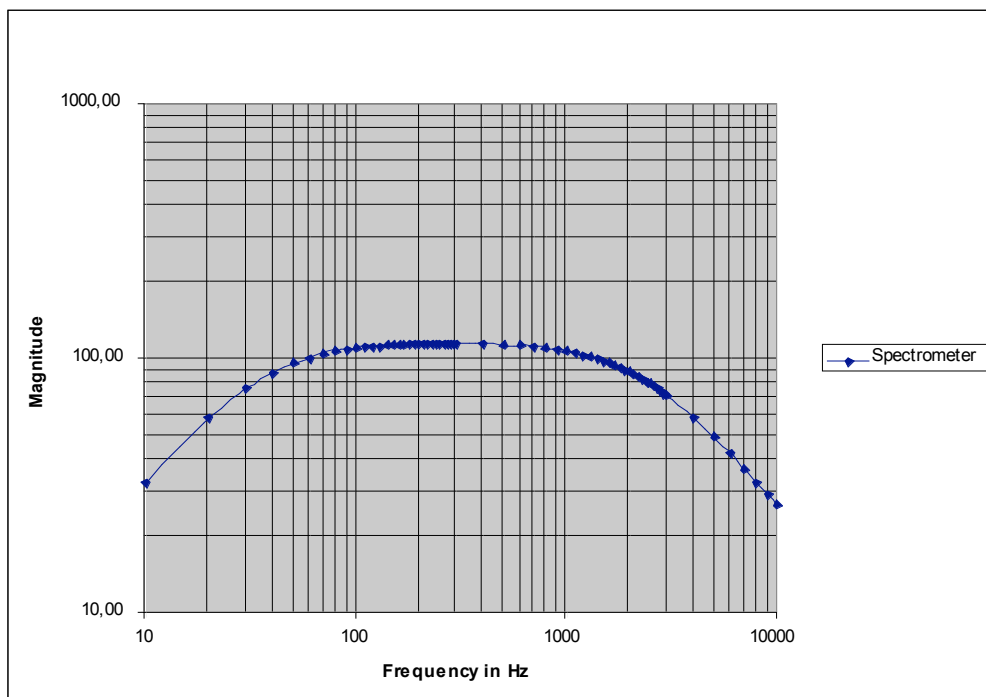
$$\frac{V_S}{V_{in}} = H_{BPF} = G \cdot \left(\frac{R_B \cdot C_B \cdot R}{1 + (R_B \cdot C_B) p + \left(\frac{G}{S} + R1 \right) C_H \cdot R_B \cdot C_B \cdot p^2} \right) \text{ with } G = \left(+ \frac{R1}{R2} + \frac{2R1}{R} \right)$$

R1=R2=15K; R=267; R_B=100K; C_B=47nF; C_H=1.5nF;

Mat02 Tran conductance: S=3.868x10⁻³ for T=300k

$$\text{So } H_{BPF} = 114.4 \cdot \left(\frac{4.7 \cdot 10^{-3} \cdot p}{1 + 4.7 \cdot 10^{-3} p + 3.14 \cdot 10^{-7} \cdot p^2} \right)$$

	Spectrometer	
	frequency	magnitude
max	283,94	114,4
Low cut of	33,39	80,9
High cut of	2414,23	



3.6.3.2.3 Preamplifier Common Mode Rejection simulation result

The following simulation result shows the common mode transfer function. It shows that we have at least -80dB common mode rejection between 50Hz and 300Hz . In other words, there is some leeway with the -60dB requirement.

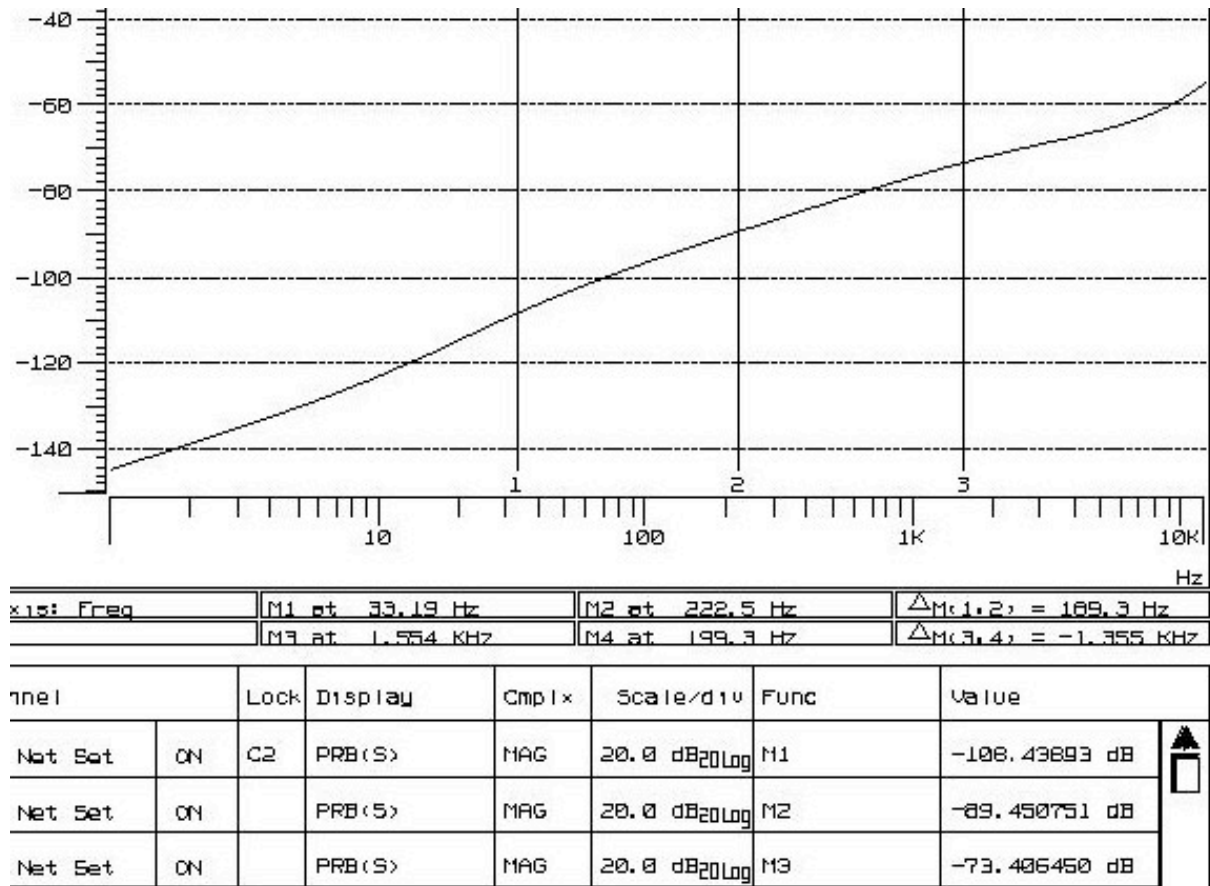
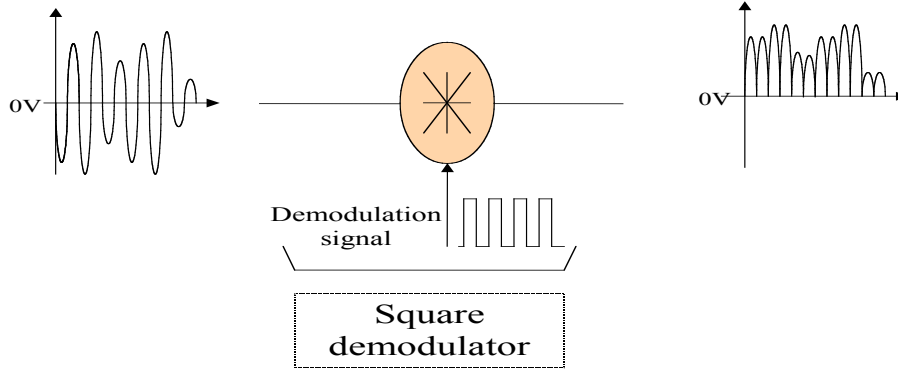


Figure 3-14 LIA Spectrometer Pre-amplifier BPF Common Mode Rejection

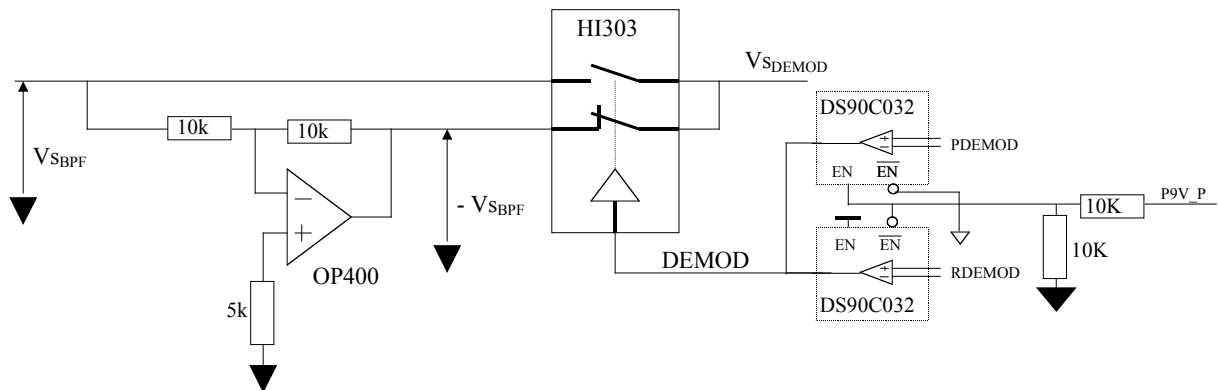
3.6.3.3 LIA Spectrometer demodulation (FUNC-02 –4)



Switching between the signal and his opposite does the demodulation of the signal coming for the pre-amplifier. This switching is command by the signal DEMOD_SSW for SSW channels, and DEMOD_SLW for SLW ones.

The analog switch HI303 does the switch.
The opposite signal is done by an OP400 in inverter circuit.

3.6.3.3.1 Demodulation circuit



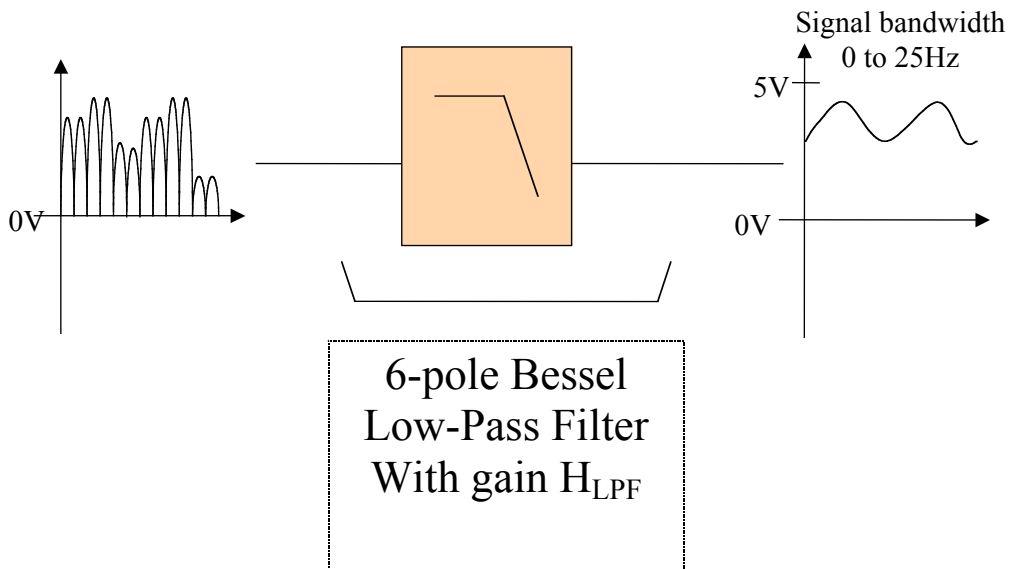
3.6.3.3.2 Output expression

$$V_{SBPF} = V_{in} \cdot H_{BPF}$$

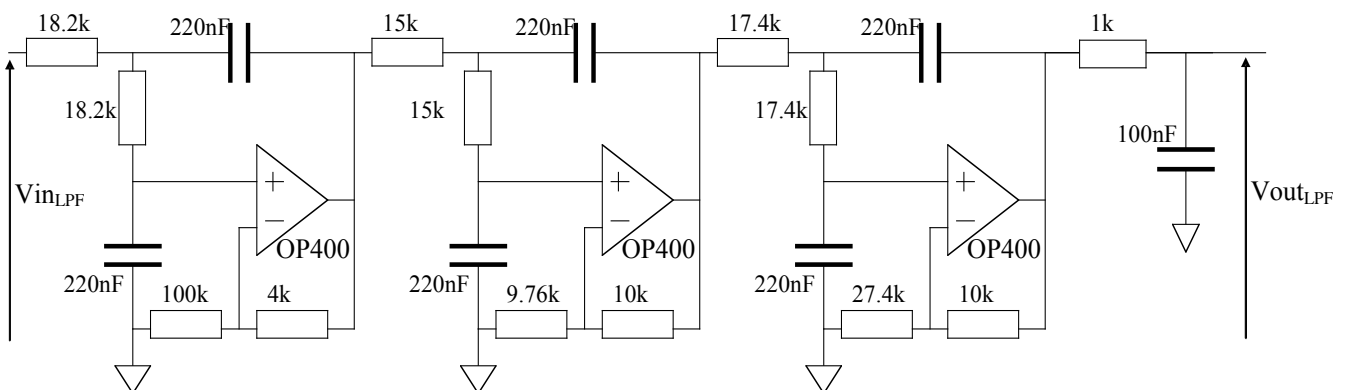
$$V_{SDEMODO}(\omega t) = V_{SBPF} \sum_{n=0}^{\infty} \frac{4}{(1+2n)\pi} \sin[(1+2n)\omega t]$$

3.6.3.4 LIA Spectrometer LPF (FUNC-02 –5)

The photometer low pass filters are 6 pole Bessel low pass filters.



3.6.3.4.1 LPF circuit



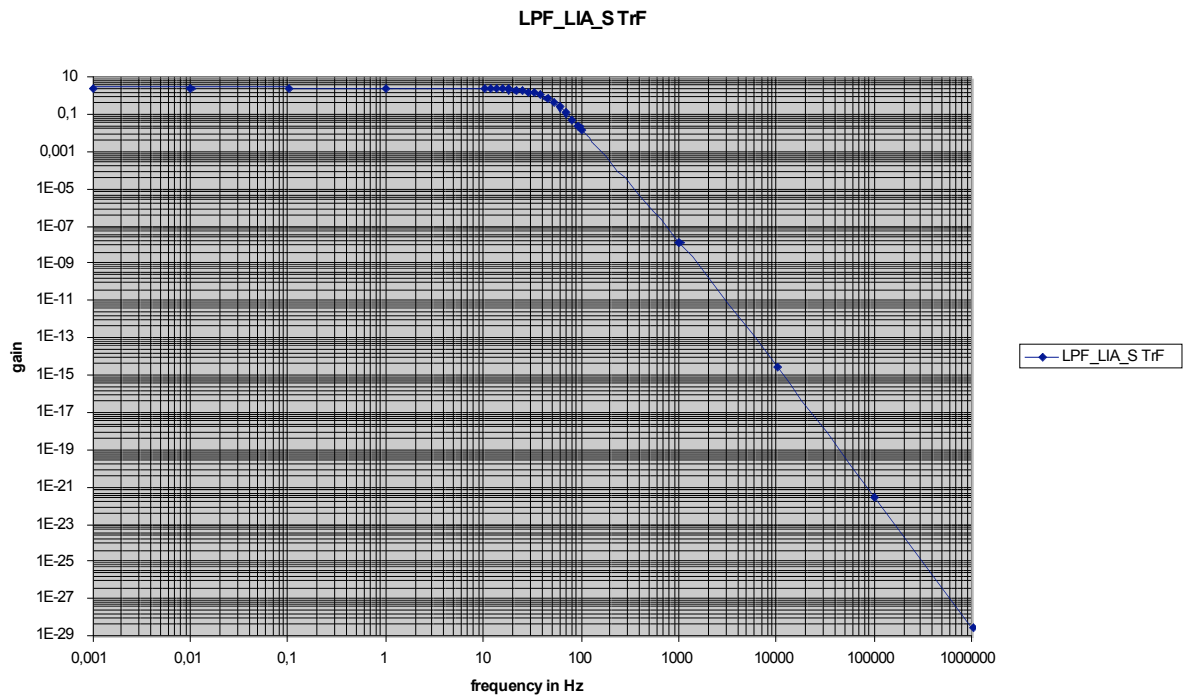
3.6.3.4.2 LPF transfer function

Transfer function:

$$H_{LPF} = \frac{V_{out\ LPF}}{V_{in\ LPF}} = 2,86 \times \frac{1}{1 + 7.85 \cdot 10^{-3} p + 16 \cdot 10^{-6} p^2} \times \frac{1}{1 + 3.25 \cdot 10^{-3} p + 10.9 \cdot 10^{-6} p^2} \times \frac{1}{1 + 6.26 \cdot 10^{-3} p + 14.65 \cdot 10^{-6} p^2} \times \frac{1}{1 + 10^{-4} p}$$

($p=j2\pi f$)

Cut off frequency -3dB: $F_c = 24,44\text{Hz}$



3.6.3.5 LIA Spectrometer Channel Noise

MAT02 : BW 50 –300Hz : $V_n=1nV/\sqrt{Hz}$

Resistors noise : $I_n=\sqrt{\frac{4kT}{R}}$; T=295K ; $4kT=1.63\times 10^{-20}$

Input preamplifier noise: $V_{n_{preamp}}=\sqrt{2\times(V_{n_{MAT02}})^2+264^2(I_{n_{264}}^2+4I_{n_{5k}}^2)}=2.57nV/\sqrt{Hz}$

OP400 at 0.1Hz: $V_n=66nV/\sqrt{Hz}$; $I_n=1.6pV/\sqrt{Hz}$

LPF Stage 1: $V_{n_{LPF1}}=\sqrt{(V_{n_{OP400}})^2+(45\times 10^3\times I_{n_{OP400}})^2+V_{n_{45k}}^2}=101nV/\sqrt{Hz}$

LPF Stage 2: $V_{n_{LPF2}}=\sqrt{(V_{n_{OP400}})^2+(35\times 10^3\times I_{n_{OP400}})^2+V_{n_{35k}}^2}=90nV/\sqrt{Hz}$

LPF Stage 3: $V_{n_{LPF3}}=\sqrt{(V_{n_{OP400}})^2+(42\times 10^3\times I_{n_{OP400}})^2+V_{n_{42k}}^2}=98nV/\sqrt{Hz}$

Input noise LPF: $V_{n_{LPF}}=\sqrt{(V_{n_{LPF1}})^2+\left(\frac{V_{n_{LPF2}}}{1.1}\right)^2+\left(\frac{V_{n_{LPF3}}}{2.2}\right)^2}=137nV/\sqrt{Hz}$

Total noise at the photometer LPF output:

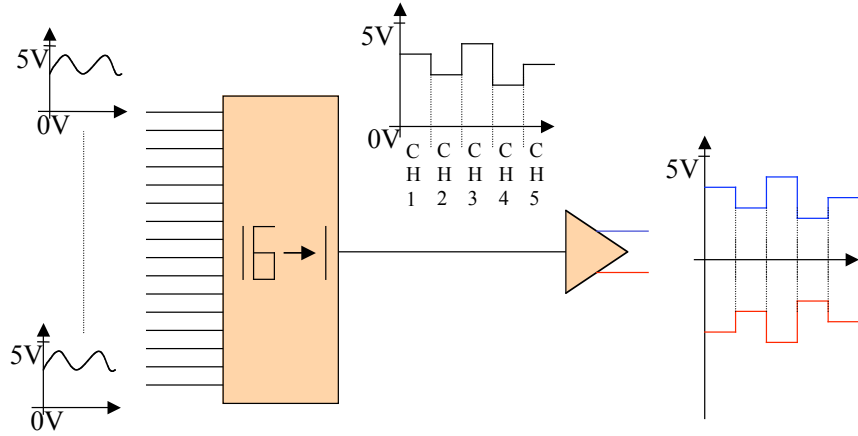
$$V_{n_{LPFout}}=\sqrt{\left[(V_{n_{preamp}}\times H_{BPF})^2\times\left(\frac{4}{\sqrt{\pi}}\right)\times\left[1+\left(\frac{1}{9}\right)+\left(\frac{1}{9}\right)+\left(\frac{1}{9}\right)+\left(\frac{1}{9}\right)\right]+(V_{n_{LPF}})^2\right]\times H_{LPF}^2}=1226nV/\sqrt{Hz}$$

Band pass filter gain $H_{BPF}=107$; Low pass filter gain $H_{LPF}=3.03$ and Total channel gain $H_{TOT}=294$

So the input noise equivalent for a photometer channel is:

$$V_{n_{in}}=\frac{V_{n_{LPFout}}}{H_{TOT}}=4.13nV/\sqrt{Hz}$$

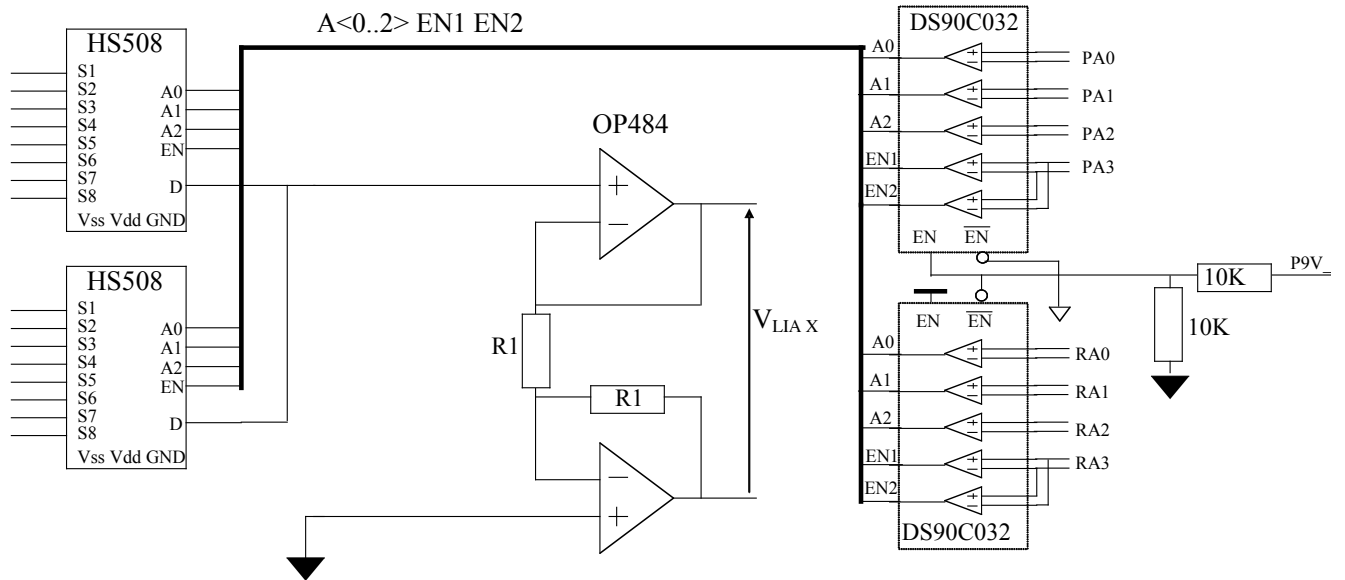
LIA Spectrometer MUX FUNC-02-8 (1/2) and LIA outputs



The first multiplexing stage FUNC-02-8 (1/2) is done by analog mux HS508. The differential output is done by two OP484.

See circuit.

3.6.3.5.1 Circuit



Channels address:

A3 A2 A1 A0	Output 1	Output 2
0000	CH1	CH13
0001	CH3	CH15
0010	CH5	CH17
0011	CH7	CH19
0100	CH9	CH21
0101	CH11	CH23
0110	GND	GND
0111	GND	GND
1000	CH2	CH14
1001	CH4	CH16
1010	CH6	CH18
1011	CH8	CH20
1100	CH10	CH22
1101	CH12	CH24
1110	GND	GND
1111	GND	GND

CH1 to CH24 refer to input connectors pinning

3.6.3.5.2 Noise

See noise synthesis section (on DAQ+IF).

3.6.3.5.3 Timing

See FPGA section.

3.6.3.5.4 LIA Channel Gain

$$Gain_{LIA} = \frac{V_{out_{LPF}}}{V_{in}} = H_{BPF} \times \frac{2 \cdot \sqrt{2}}{\pi} \times H_{LPF}$$

Modulation Frequency	Spectrometer channel gain
50	246,19
60	259,19
70	268,09
80	274,37
90	278,92
100	282,31
110	284,88
120	286,86
130	288,42
140	289,65
150	290,64
160	291,44
170	292,09
180	292,62
190	293,05
200	293,40
210	293,68
220	293,91
230	294,09
240	294,23
250	294,33
260	294,40
270	294,44
280	294,46
290	294,46
300	294,44

3.7 BIAS BOARD

3.7.1 BIAS Board Overview

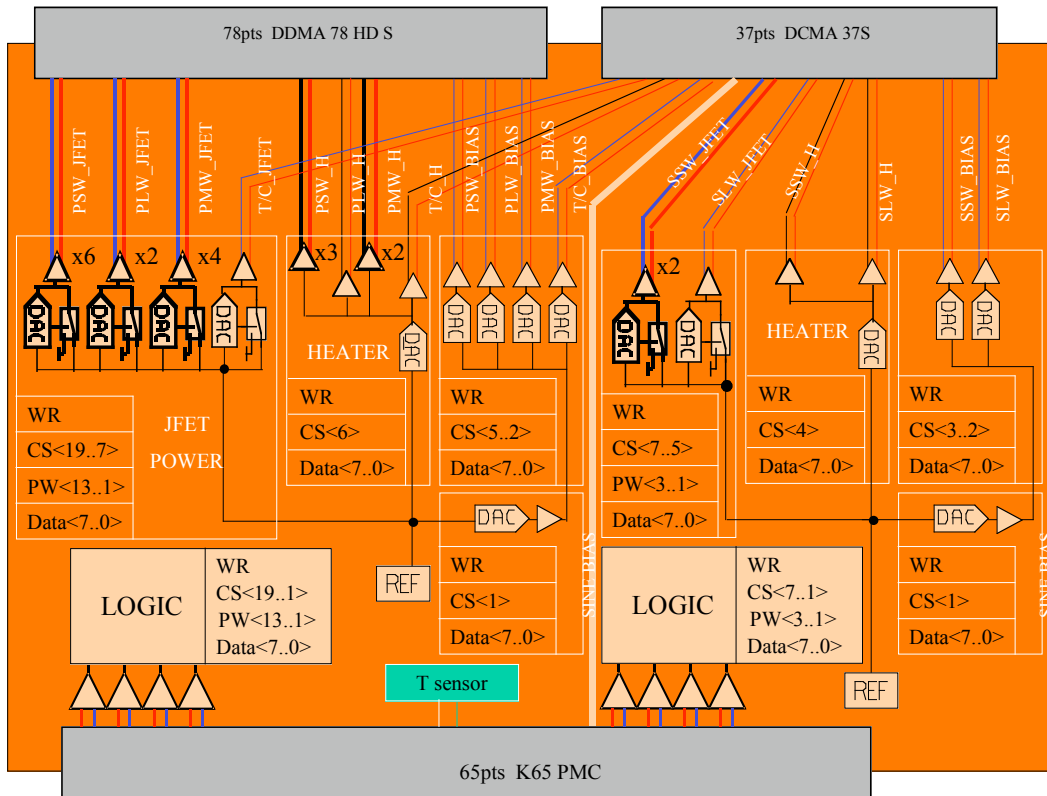


Figure 3-15 BIAS Board Overview

The BIAS board generates sine biases for the bolometers and DC biases for JFETs and heaters.

- Adjustable sine biases:
 - Photometer: 1sine generator/ 4 channels with independent amplitudes
 - Spectrometer: 1sine generator/ 2 channels with independent amplitudes
 - Voltage range: 0 to 100 mVrms for the photometers; 0 to 140 mVrms for the spectrometers and 0 to 200 mVrms for the temperature readout
 - Accuracy: 256 levels
 - Frequency range: 50 to 300Hz
- Adjustable DC JFET biases:
 - Photometer: 13 generators for JFET
 - Spectrometer: 3 generators for JFET
 - Voltage range: 0 to –5V for VSS with 256 levels and VDD is set between 0 and 4V by two resistors
 - Output currents: 5mA max
- Adjustable DC heater biases:
 - Photometer: 1heater generator and 7 buffers
 - Spectrometer: 1 heater generator and 3 buffers
 - Voltage range: 0 to –5V with 256 levels
 - Output currents: 5mA max for each buffer

Note: Each buffer biases at most 2 JFET module* heaters. (*JFETmodule = 24 channels)

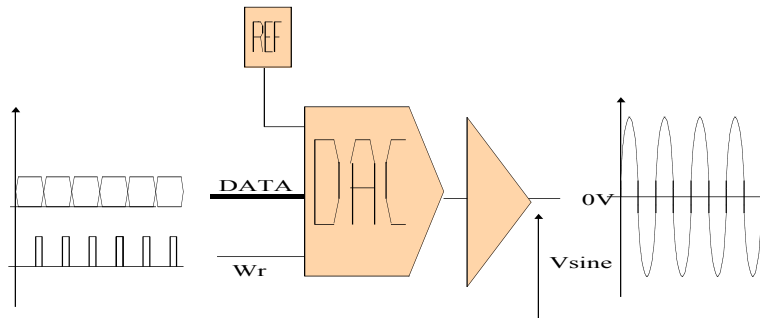
3.7.2 BIAS Board Interface

Interface	Name	Description	Type	Level	In/Out	Frequency
BIAS	PBIAS_Pxx	photometer BIAS	Analogic	100mVrms	OUT	50-300Hz
	NBIAS_Pxx	Differential Signal		to 0v		
	PBIAS_Sxx	spectrometer BIAS	Analogic	140mVrms		
	NBIAS_Sxx	Differential Signal		to 0v		
	PBIAS_TC	Bolometer TC BIAS	Analogic	200mVrms		
	NBIAS_TC	Differential Signal		to 0v		
VSS/VDD/HEATER	VSS_xx	JFET source voltage	Analogic	0 to-5V	OUT	DC
	VDD_xx	JFET Drain voltage	Analogic	2.5V	OUT	DC
	NHEATER_xx	Heaters bias	Analogic	0 to-5V	OUT	DC
	PHEATER_xx		Analogic	0V	OUT	DC
SERIAL LINK PHOTOMETER	CLK_P+	Serial link clock	Digital (LVDS)	-0,3Vto 0,3V	IN	0-10MHz
	CLK_P-	Differential Signal				
	SDATA_P+	Serial link data	Digital (LVDS)	-0,3Vto 0,3V	IN	0-10MHz
	SDATA_P-	Differential Signal				
	WR_DATA_P+	Serial link data write	Digital (LVDS)	-0,3Vto 0,3V	IN	0-768kHz
	WR_DATA_P-	Differential Signal				
	WR_ADRESS_P+	Serial link address write	Digital (LVDS)	-0,3Vto 0,3V	IN	0-48kHz
	WR_ADRESS_P-	Differential Signal				
SERIAL LINK SPECTROMETER	CLK_S+	Serial link clock	Digital (LVDS)	-0,3Vto 0,3V	IN	0-10MHz
	CLK_S-	Differential Signal				
	SDATA_S+	Serial link data	Digital (LVDS)	-0,3Vto 0,3V	IN	0-10MHz
	SDATA_S-	Differential Signal				
	WR_DATA_S+	Serial link data write	Digital (LVDS)	-0,3Vto 0,3V	IN	0-768kHz
	WR_DATA_S-	Differential Signal				
	WR_ADRESS_S+	Serial link address write	Digital (LVDS)	-0,3Vto 0,3V	IN	0-48kHz
	WR_ADRESS_S-	Differential Signal				
BIAS_TEMPERATURE	PT_P9V	Sensor PRIME Bias	Analogic	9V	IN	DC
	PT	Output Sensor PRIME	Analogic	2 to 4V	OUT	-
	RT_P9V	Sensor REDUNDANT Bias	Analogic	9V	IN	DC
	RT	Output Sensor REDUNDANT	Analogic	2 to 4V	OUT	-
POWER	P9V_P	9V Power Supply photometer	Power	9V	IN	DC
	N9V_P	-9V Power Supply photometer	Power	-9V	IN	DC
	P9V_S	9V Power Supply spectrometer	Power	9V	IN	DC
	N9V_S	-9V Power Supply spectrometer	Power	-9V	IN	DC

3.7.3 BIAS BOARD FUNCTIONS

3.7.3.1 BIAS sine conversion digital to analog (FUNC-01-2)

The function DCU-FUNC-01-2 generates a sinusoidal signal with amplitude of 5V and a 0V center from a digital sine wave.



This function is implemented twice on the BIAS board (1 for the photometer and 1 for the spectrometer.)

3.7.3.1.1 circuit

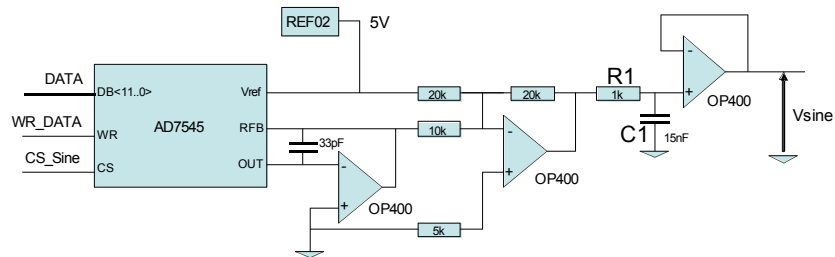


Figure 3-16 Sine Generator

3.7.3.1.2 Sine expression

$$V_{\text{sine}} = REF02 \cdot \frac{\left(1 - 2 \frac{DATA}{4095}\right)}{\left(1 + R_1 C_1 \cdot p\right)} = \frac{5(4095 - 2DATA)}{\left(1 + \frac{p}{2\pi \cdot 10610}\right) \cdot 4095} \quad (p=j2\pi f)$$

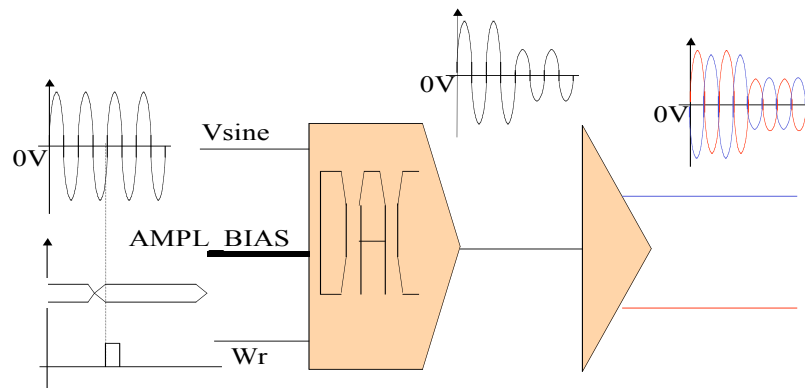
Note: DATA is an integer between 0 and 4095

To generate sinusoidal signal with frequency **F_{sine}** the 256 integers, which describe a sine, should be wrote in the digital to analog converter with a frequency of **256.F_{sine}**.

The 256 values of the sine are given in a table in the FPGA section of this document.

3.7.3.2 BIAS sine attenuator (FUNC-01-3 and FUNC-01-4)

The functions FUNC-01-3 and FUNC-01-4 determinate the sinusoidal signal amplitude for each BDA group.



Each bolometer group has its own bias attenuator.

- The 4 bias attenuators of the photometer receive at their input the signal coming from the photometer BIAS sine conversion digital to analog.
- As well as The 2 bias attenuators of the spectrometer receive at their input the signal coming from the spectrometer BIAS sine conversion digital to analog.

3.7.3.2.1 Circuit

The bias attenuator circuit is as follow:

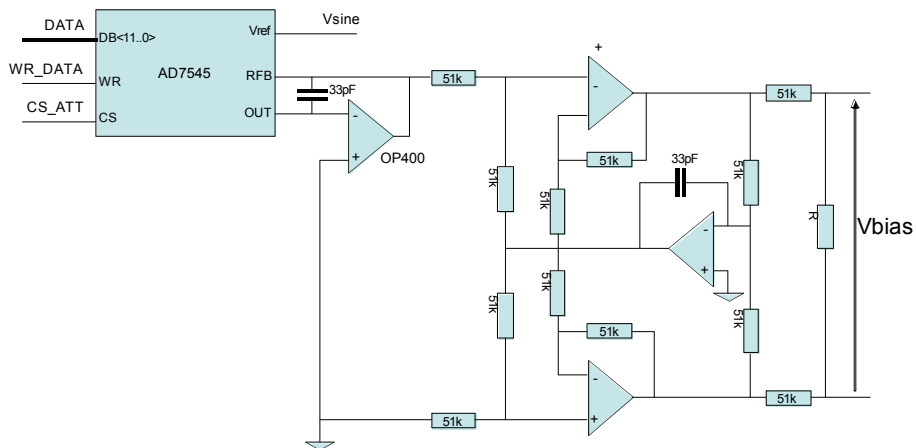


Figure 3-17 Bias Attenuator

3.7.3.2.2 BIAS expression

- FOR PSW, PMW, PLW: R=6,04K
- FOR SSW and SLW: R=8,45K
- FOR TC: R=12,7K

If the redundant and prime bias boards are connected together:

$$BIAS = \frac{AMPL_BIAS}{4095} \cdot \frac{R/2}{102k + R/2} \cdot Vsine$$

If not:

$$BIAS = \frac{AMPL_BIAS}{4095} \cdot \frac{R}{102k + R} \cdot Vsine$$

BIAS in sine mode

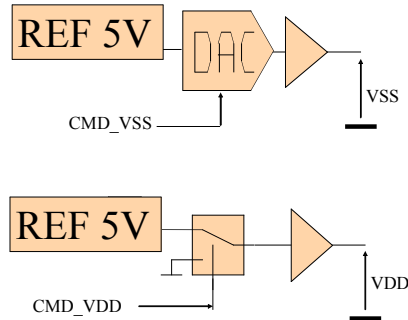
BIAS MODE =255	Photometer		spectro		TC	
	1 bias board	2 bias board	1 bias board	2 bias board	1 bias board	2 bias board
Frequency in Hz	bias in Vrms	bias in Vrms	bias in Vrms	bias in Vrms	bias in Vrms	bias in Vrms
40	0,182	0,094	0,249	0,130	0,361	0,191
50	0,182	0,094	0,249	0,130	0,361	0,191
60	0,182	0,094	0,249	0,130	0,361	0,191
70	0,182	0,094	0,249	0,130	0,361	0,191
80	0,182	0,094	0,249	0,130	0,361	0,191
90	0,182	0,094	0,249	0,130	0,361	0,191
100	0,182	0,094	0,249	0,130	0,361	0,191
110	0,182	0,094	0,249	0,130	0,361	0,191
120	0,182	0,094	0,249	0,130	0,361	0,191
130	0,182	0,094	0,249	0,130	0,361	0,191
140	0,182	0,094	0,249	0,130	0,361	0,191
150	0,182	0,094	0,249	0,130	0,361	0,191
160	0,182	0,094	0,249	0,130	0,361	0,191
170	0,182	0,094	0,249	0,130	0,361	0,191
180	0,182	0,094	0,249	0,130	0,361	0,191
190	0,182	0,094	0,249	0,130	0,361	0,191
200	0,182	0,094	0,249	0,130	0,361	0,191
210	0,182	0,094	0,249	0,130	0,361	0,191
220	0,182	0,094	0,249	0,130	0,361	0,191
230	0,182	0,094	0,249	0,130	0,361	0,191
240	0,182	0,094	0,249	0,130	0,361	0,191
250	0,182	0,094	0,249	0,130	0,361	0,191
260	0,182	0,094	0,249	0,130	0,361	0,191
270	0,182	0,094	0,249	0,130	0,361	0,191
280	0,182	0,094	0,249	0,130	0,361	0,191
290	0,182	0,094	0,249	0,130	0,361	0,191
300	0,182	0,094	0,249	0,130	0,361	0,191

BIAS in DC mode

BIAS MODE	Photometer		spectro		TC	
	1 bias board	2 bias board	1 bias board	2 bias board	1 bias board	2 bias board
	bias in Vpp	bias in Vpp	bias in Vpp	bias in Vpp	bias in Vpp	bias in Vpp
0	0,278	0,143	0,380	0,198	0,551	0,291
1	0,276	0,142	0,377	0,196	0,546	0,289
127	0,002	0,001	0,003	0,001	0,004	0,002
128	0,000	0,000	0,000	0,000	0,000	0,000
129	-0,002	-0,001	-0,003	-0,002	-0,004	-0,002
130	-0,004	-0,002	-0,006	-0,003	-0,009	-0,005
252	-0,269	-0,139	-0,369	-0,192	-0,534	-0,282
253	-0,272	-0,140	-0,372	-0,193	-0,538	-0,285
254	-0,274	-0,141	-0,375	-0,195	-0,542	-0,287

3.7.3.3 JFET VSS and VDD (FUNC-05-1, FUNC-05-2, FUNC-05-3 and FUNC-05-4)

Each JFET module has its own JFET bias generator. A JFET bias generator provide a negative DC tension VSS (DCU-FUNC-05-1 and DCU-FUNC-05-2) and a positive DC tension VDD (DCU-FUNC-05-3 and DCU-FUNC-05-4)



3.7.3.3.1 Circuit

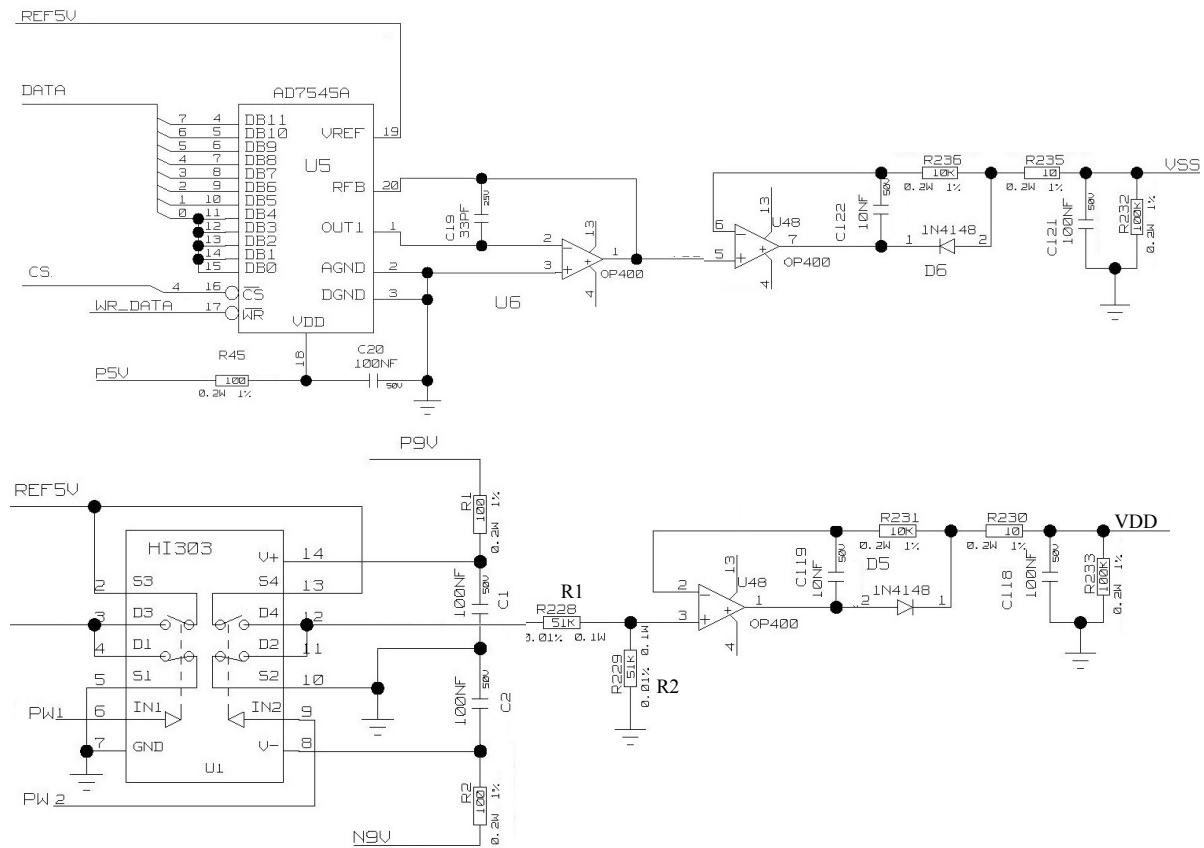


Figure 3-18 JFET Bias Generator

3.7.3.3.2 Characteristic

- VSS generator:

Function DCU-FUNC-05-1:

- From a +5V precision voltage reference, the DAC and the first OP generate a tension proportional to the digital 8 bits DATA: $VSS = -REF5V(DATA \times 256)$.

Function DCU-FUNC-05-2:

- The second OP and its following components are there to:
 - Avoid overshoot when VSS is set ON from OFF or the other way
 - Allow connection with unpower redundant bias board
 - Provide the 5mA required.

- VDD generator:

Function DCU-FUNC-05-3:

- When the switch is **ON** a +5V precision voltage reference is applied on two resistors R1 and R2 so $VDD = REF5V \cdot R2 / (R1 + R2)$.
- When the switch is **OFF** the ground is applied on two resistors R1 and R2 so $VDD = 0V$.

Function DCU-FUNC-05-4:

- The second OP and his following components are there to:
 - Avoid overshoot when VDD is set ON from OFF or the other way
 - Allow connection with unpower redundant bias board
 - Provide the 5mA required.

3.7.3.3.3 ON/OFF Simulation

The following simulation shows the switching ON and OFF of VSS, VDD.

- VSS switched ON 0V to -5V. (A=5V)
- VSS switched OFF -5V to 0V. (A=0V)
- VDD switched ON 0V to 2.5V. (A=5V)
- VDD switched OFF 2.5V to 0V. (A=0V)

The prime generators are powered, the redundant ones are not.
 The load resistor is set for a nominal generator output current of 5mA.

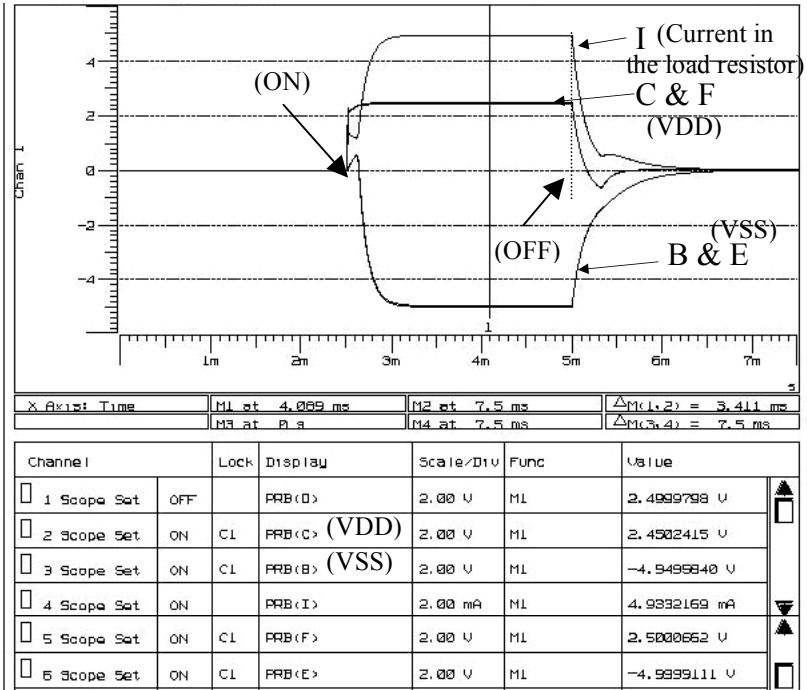
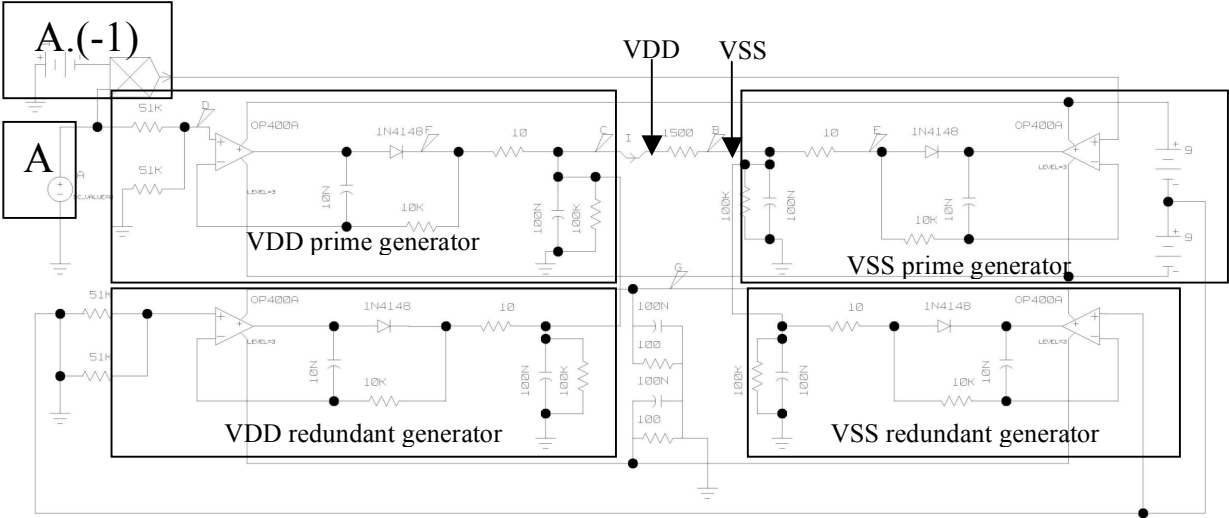


Figure 3-19 JFET Bias Generator Simulation

3.7.3.4 Heater (FUNC-05-5 and FUNC-05-6)

To bias the photometer heaters there are:

- A bias generator FUNC-05-5 and 7 buffers FUNC-05-6 (the buffer heater is similar to a VSS buffer) of which:
 - o each 6 buffers bias each 2 JFET module heaters
 - o 1 buffer biases only the T/C JFET module

To bias the spectrometer heaters there are:

- A bias generator FUNC-05-5 and 2 buffers FUNC-05-6 (the buffer heater is similar to a VSS buffer) of which:
 - o 1 buffer biases 2 JFET module heaters
 - o 1 buffer biases only 1 JFET module heater

3.7.3.4.1 Circuit

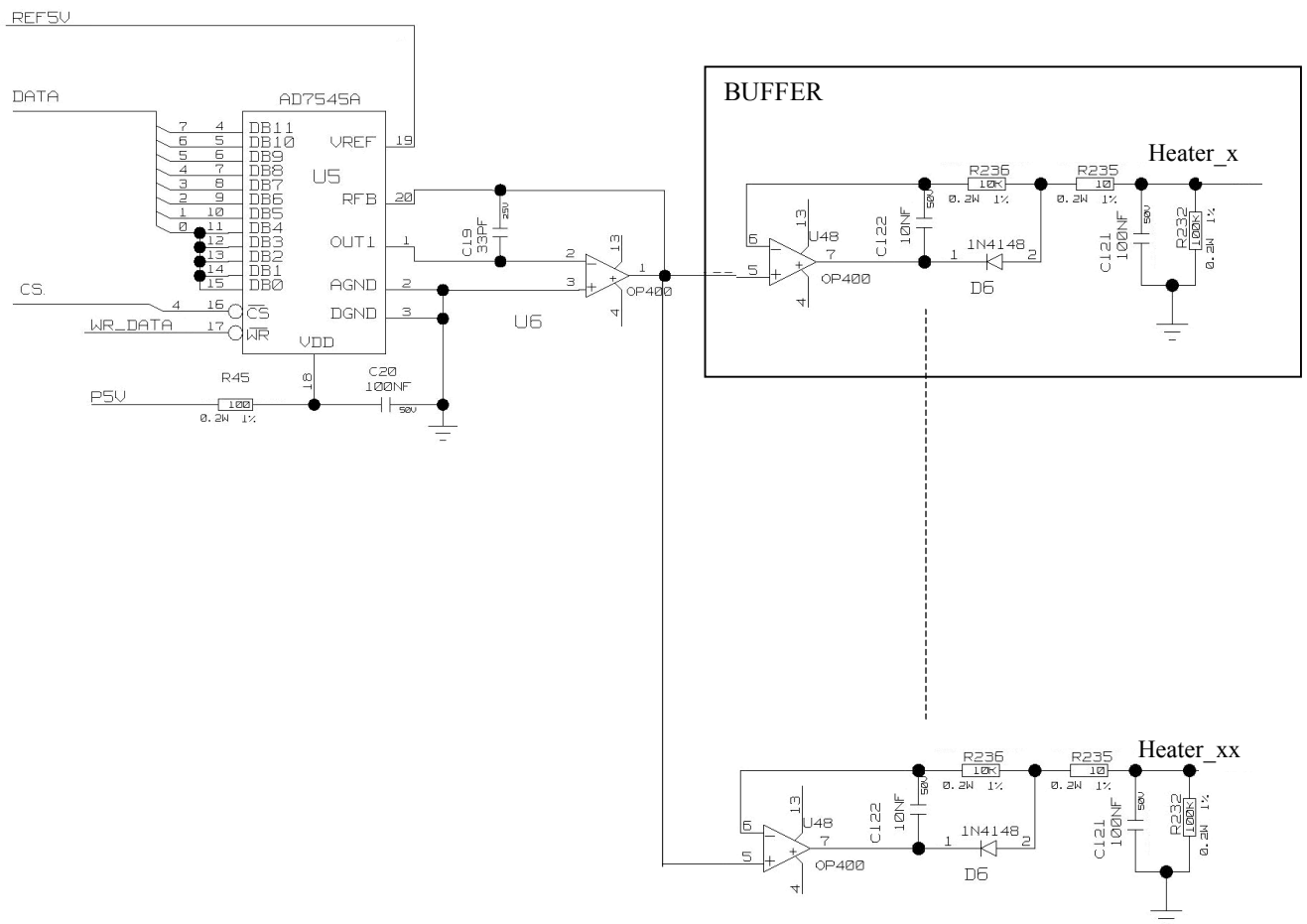


Figure 3-20 Heater Bias Generator

3.7.3.5 Serial receiver

- All of the photometer DACs CS (chips select) and ON/OFF switches are connected to four 8-bit latched SIPO (Serial Input to Parallel Output) shift registers.
- The 17 photometer DACs are connected to the same write signal WR_DATA_P.
- The four 8-bit latch SIPO shift registers are connected to the same latch signal WR_ADRESS_P
- The photometer 12-bit* parallel DATA_P bus is provided by one SIPO shift register.

DAC address map is:

BIT number	Command	BIT number	Command
A1	CS Sine bias generator	A17	CS VSS12_P
A2	CS PSW bias attenuator	A18	CS HEATER_P
A3	CS PLW bias attenuator	A19	ON/OFF VDD1_P
A4	CS T/C bias attenuator	A20	ON/OFF VDD2_P
A5	CS PMW bias attenuator	A21	ON/OFF VDD3_P
A6	CS VSS1_P	A22	ON/OFF VDD4_P
A7	CS VSS2_P	A23	ON/OFF VDD5_P
A8	CS VSS3_P	A24	ON/OFF VDD6_P
A9	CS VSS4_P	A25	ON/OFF VDD7_P
A10	CS VSS5_P	A26	ON/OFF VDD8_P
A11	CS VSS6_P	A27	ON/OFF VDD9_P
A12	CS VSS7_P	A28	ON/OFF VDD10_P
A13	CS VSS8_P	A29	ON/OFF VDD11_P
A14	CS VSS9_P	A30	ON/OFF VDD12_P
A15	CS VSS10_P	A31	ON/OFF VDD_TC
A16	CS VSS11_P	A32	CS VSS_TC

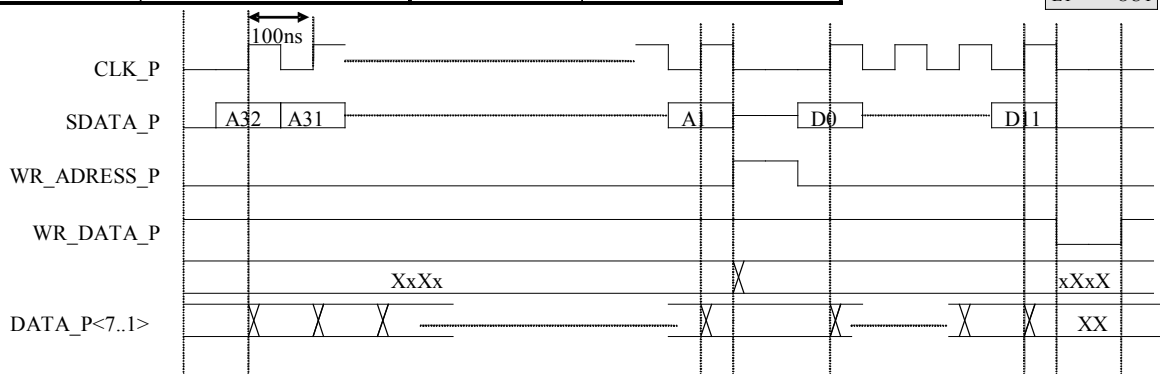
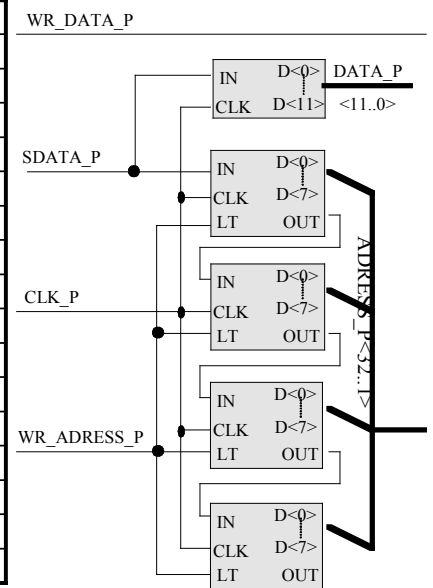


Figure 3-21 Photometer Bias serial link timing

*The seven MSB (DATA_P<7..0>) are connected to all the DAC and the four LSB (DATA_P_LSB<3..0>) are connected only on Sine bias DAC generator

- All of the spectrometer DACs chips select and ON/OFF switches are connected to two 8-bit latch SIPO (Serial Input to Parallel Output) shift registers.
- The 7 spectrometer DACs are connected to the same write signal WR_DATA_S.
- The two 8-bit latch SIPO shift registers are connected to the same latch signal WR_ADDRESS_S
- The spectrometer 12-bit* parallel DATA_S bus is provided by SIPO shift register.

DAC address map is:

BIT number	Command	BIT number	Command
A1	CS Sine bias generator spectro	A9	ON/OFF VDD1_S
A2	CS SLW bias attenuator	A10	ON/OFF VDD2_S
A3	CS SSW bias attenuator	A11	ON/OFF VDD3_S
A4	CS VSS1_S	A12	-
A5	CS VSS2_S	A13	-
A6	CS VSS3_S	A14	-
A7	CS HEATER_S	A15	-
A8	-	A16	-

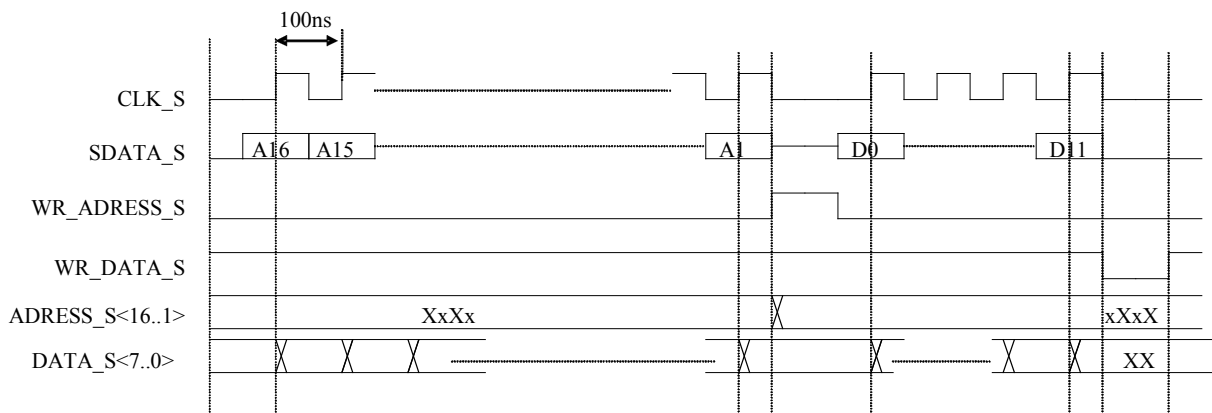
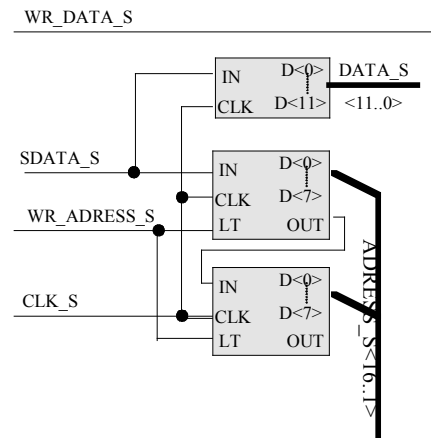


Figure 3-22 Spectrometer Bias serial link timing

*The seven MSB (DATA_P<7..0>) are connected to all the DAC and the four LSB (DATA_P_LSB<3..0>) are connected only on Sine bias DAC generator

3.7.3.6 JFET BIAS Noise

See DCU BIAS Test plan result.

3.8 DAQ+IF BOARD

3.8.1 DAQ+IF Board Overview

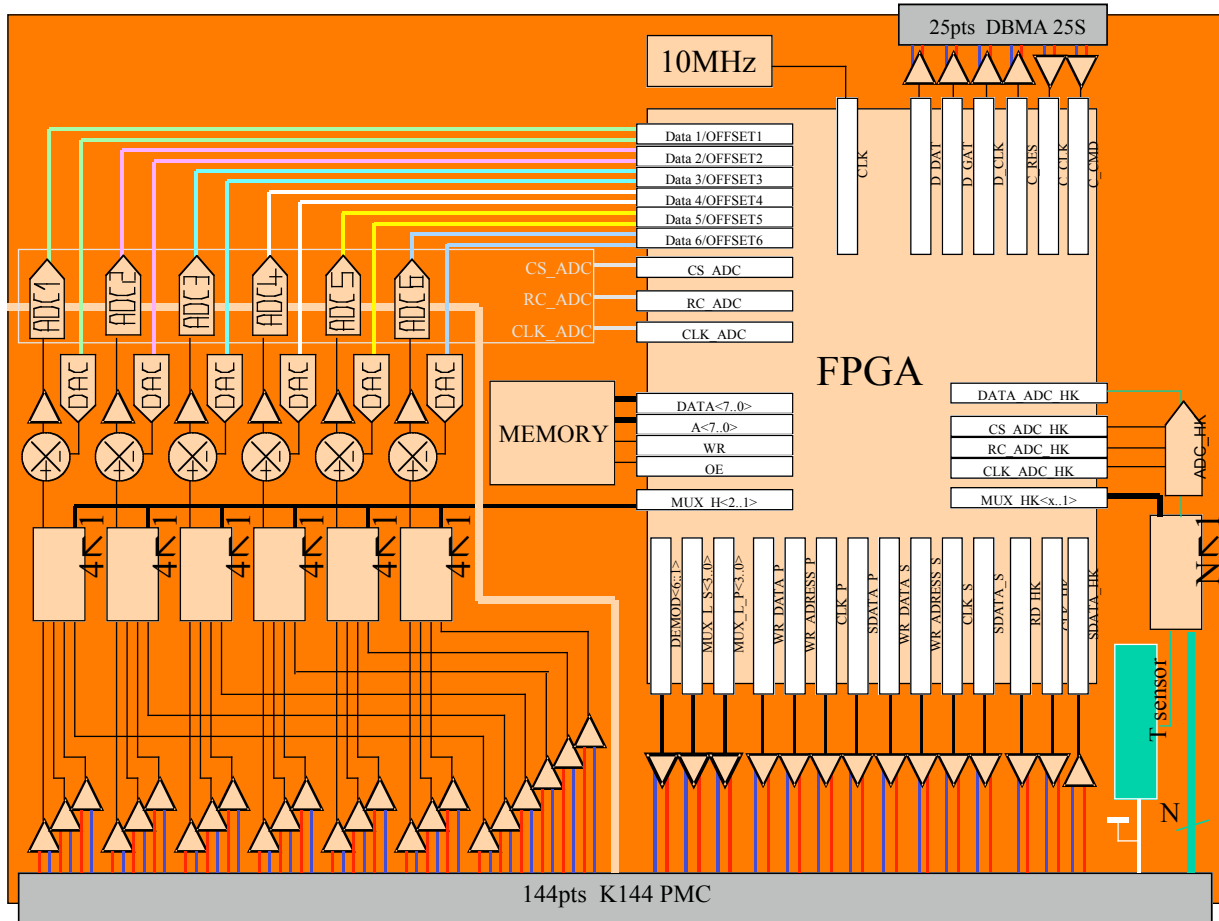


Figure 3-23 DAQ+IF Board Overview

- The DAQ+IF boards receive the bolometer analog signal for all LIA boards output, apply an offset on each bolometer signal, amplify them a last time, and then digitize them.

-The digitized data are embedded in a frame sent to the DPU through the fast link.

-The FPGA carries digital functions like:

- Low level command decoding
- Low level command acknowledge + HK parameters transfer
- The timestamp generation

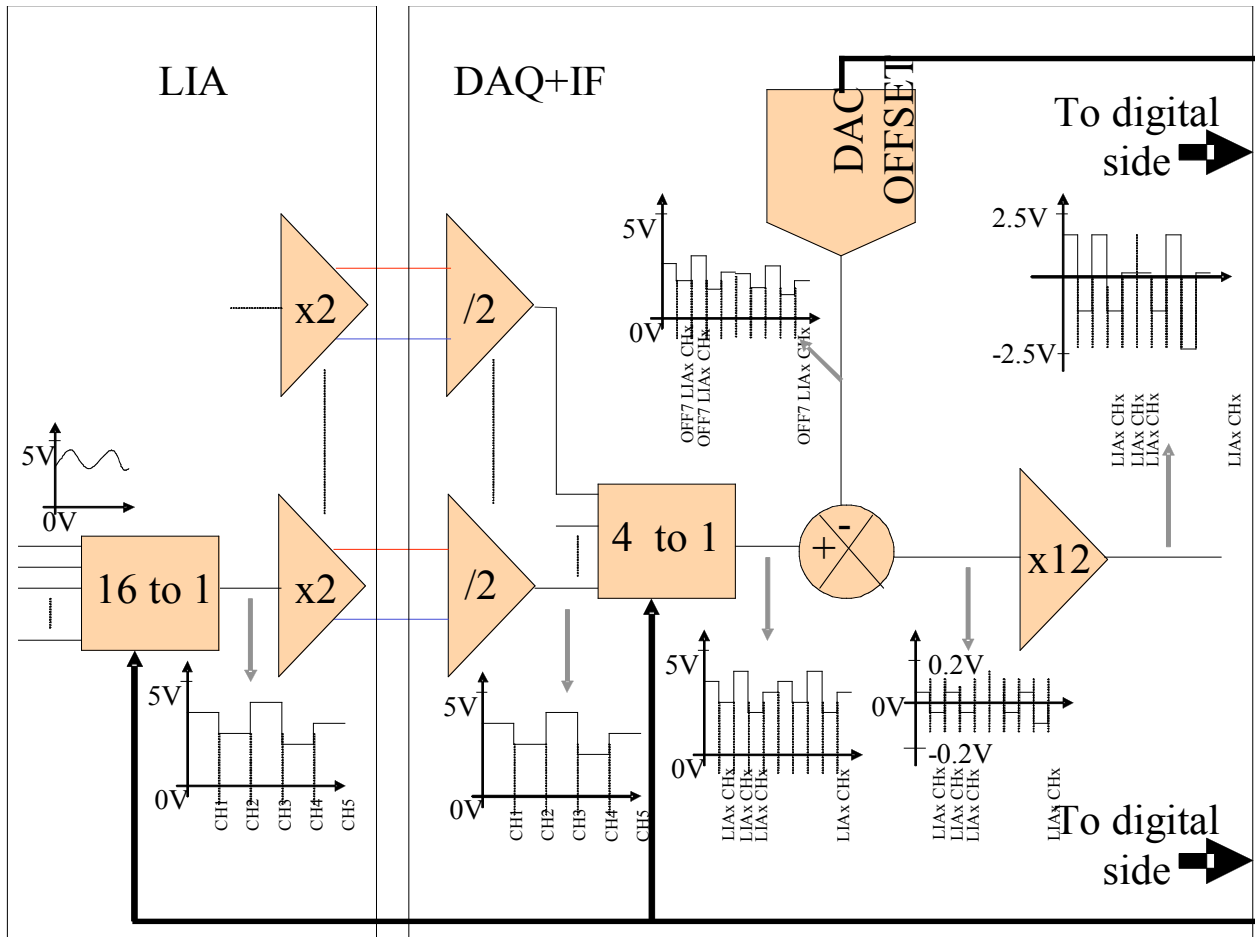
-It provides all the digital signals needed by LIA and BIAS boards, and as well as the internal DAQ+IF board signals.

3.8.2 DAQ+IF Board Interface

Interface	Name	Description	Type	Level	In/Out	Frequency
DATA	D_CLK_DCU_P+	Data clock	Digital	-0,3Vto 0,3V	OUT	2.5MHz
	D_CLK_DCU_P-	Differential Signal				
	D_GAT_DCU_P+	Data gate	Digital	-0,3Vto 0,3V	OUT	2.5MHz
	D_GAT_DCU_P-	Differential Signal				
	D_DAT_DCU_P+	Data	Digital	-0,3Vto 0,3V	OUT	2.5MHz
	D_DAT_DCU_P-	Differential Signal				
CMD_ACK&STATUS	C_RES_DCU_P+	Commands response	Digital	-0,3Vto 0,3V	OUT	3.125 kHz
	C_RES_DCU_P-	Differential Signal				
CMD	C_CMD_DCU_P+	Commands	Digital	-0,3Vto 0,3V	IN	3.125 kHz
	C_CMD_DCU_P-	Differential Signal				
	C_CLK_DCU_P+	Commands clock	Digital	-0,3Vto 0,3V	IN	3.125 kHz
	C_CLK_DCU_P-	Differential Signal				
MUX_CHANNEL	POUT_x	channels Multiplexed in a Differential Signal	Analogic	0 to 5V	IN	0-25Hz at mux freq.
	NOUT_x					
CMD_MUX_H LIA_P & LIA_S	Ax-	BIT Command Mux (PRIME) Differential Signal	Digital	-0,3Vto 0,3V	OUT	~10kHz
	Ax+					
DEMOD_x	DEMODx-	Demodulation Differential Signal (PRIME) for Channels One to Twenty-four	Digital	-0,3Vto 0,3V	OUT	50-300Hz
	DEMODx+					
SERIAL LINK PHOTOMETER	CLK_P+	Serial link clock	Digital	-0,3Vto 0,3V	OUT	0-10MHz
	CLK_P-	Differential Signal				
	SDATA_P+	Serial link data	Digital	-0,3Vto 0,3V	OUT	0-10MHz
	SDATA_P-	Differential Signal				
	WR_DATA_P+	Serial link data write	Digital	-0,3Vto 0,3V	OUT	0-768kHz
	WR_DATA_P-	Differential Signal				
	WR_ADRESS_P+	Serial link address write	Digital	-0,3Vto 0,3V	OUT	0-48kHz
	WR_ADRESS_P-	Differential Signal				
SERIAL LINK SPECTROMETER	CLK_S+	Serial link clock	Digital	-0,3Vto 0,3V	OUT	0-10MHz
	CLK_S-	Differential Signal				
	SDATA_S+	Serial link data	Digital	-0,3Vto 0,3V	OUT	0-10MHz
	SDATA_S-	Differential Signal				
	WR_DATA_S+	Serial link data write	Digital	-0,3Vto 0,3V	OUT	0-768kHz
	WR_DATA_S-	Differential Signal				
	WR_ADRESS_S+	Serial link address write	Digital	-0,3Vto 0,3V	OUT	0-48kHz
	WR_ADRESS_S-	Differential Signal				
SERIAL LINK HK	CLK_HK+	Serial link clock	Digital	-0,3Vto 0,3V	OUT	0-xMHz
	CLK_HK-	Differential Signal				
	SDATA_HK+	Serial link data	Digital	-0,3Vto 0,3V	OUT	0-xMHz
	SDATA_HK-	Differential Signal				
	RD_HK+	Serial link data read	Digital	-0,3Vto 0,3V	OUT	0-xkHz
	RD_HK-	Differential Signal				
BIAS&LIA_ TEMPERATURE	T_P9V	Sensor PRIME Bias	Analogic	9V	OUT	DC
	T	Output Sensor PRIME	Analogic	1 to 2V	IN	-
POWER	P9V	9V Power Supply	Power	9V	IN	DC
	N9V	-9V Power Supply	Power	-9V	IN	DC
	P5V	5V Power Supply	Power	5V	IN	DC
POWER_LIA_P	P9V_LIA_P	9V Power Supply	Power	9V	IN	DC
	N9V_LIA_P	-9V Power Supply	Power	-9V	IN	DC
	P5V_LIA_P	5V Power Supply	Power	5V	IN	DC
POWER_LIA_S	P9V_LIA_S	9V Power Supply	Power	9V	IN	DC
	N9V_LIA_S	-9V Power Supply	Power	-9V	IN	DC
	P5V_LIA_S	5V Power Supply	Power	5V	IN	DC

3.8.3 DAQ+IF BOARD FUNCTIONS

3.8.3.1 LIA Channel Digitization Overview



Channel way to digitization:

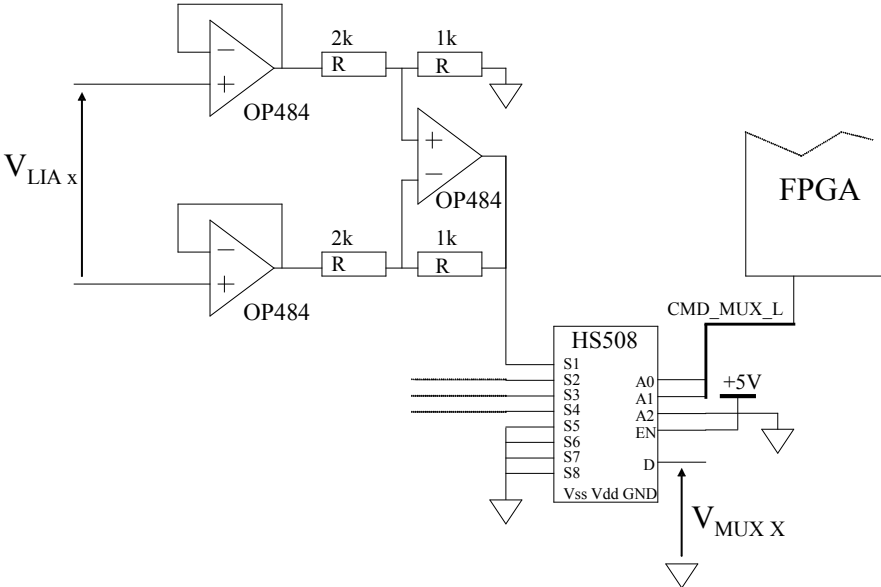
1. After the LIA_P (or LIA_S) channel processing, a bolometer signal is multiplexed with 15 (or 11) other bolometer signals on the same board.
2. Then the multiplexed signal goes out the LIA board through a differential amplifier with one unit gain.
3. The differential multiplexed signal goes into the DAQ+IF board through a differential receiver with one unit gain.
4. DAQ+IF board multiplexing stage:
 - If this multiplexed signal comes from the photometer it is then multiplexed with 2 other signals which come from 2 other LIA_P multiplexers. There are 48 photometer bolometer signals that are multiplexed.
 - If this multiplexed signal comes from the spectrometer then it goes straight through the multiplexer.
5. For each bolometer signal a predetermined offset signal is subtracted.
6. Afterwards, the signal is amplified by 12 and digitized.

3.8.3.2 Analog Receiver and Multiplexer FUNC-02-8

On a DAQ+IF board there are:

- 18 photometer analog receivers for the 18 LIA_P board output.
- 6 “Spectrometer” Analog receivers for the 6 LIA_S board output.
- 6 multiplexers
- Each multiplexer handles
 - o 1 spectrometer analog receiver output.
 - o 3 photometer analog receiver output.

3.8.3.2.1 Circuit



3.8.3.2.2 Noise

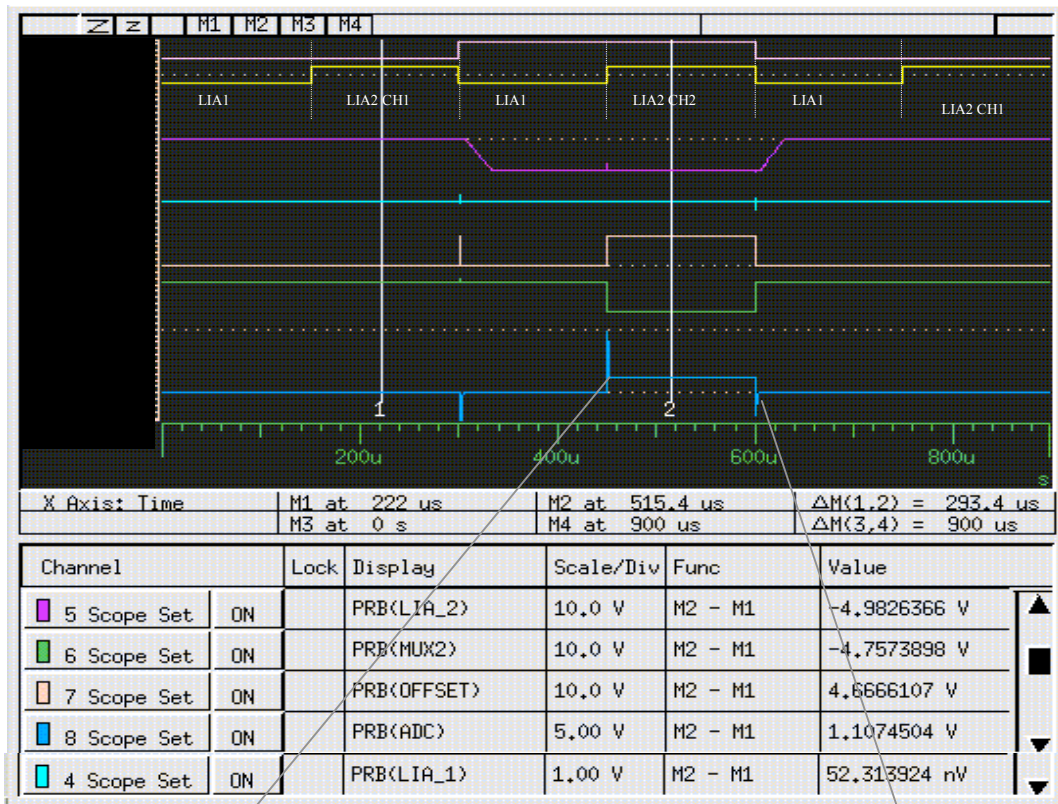
See noise synthesis section (on DAQ+IF).

3.8.3.2.3 Timing

See FPGA section.

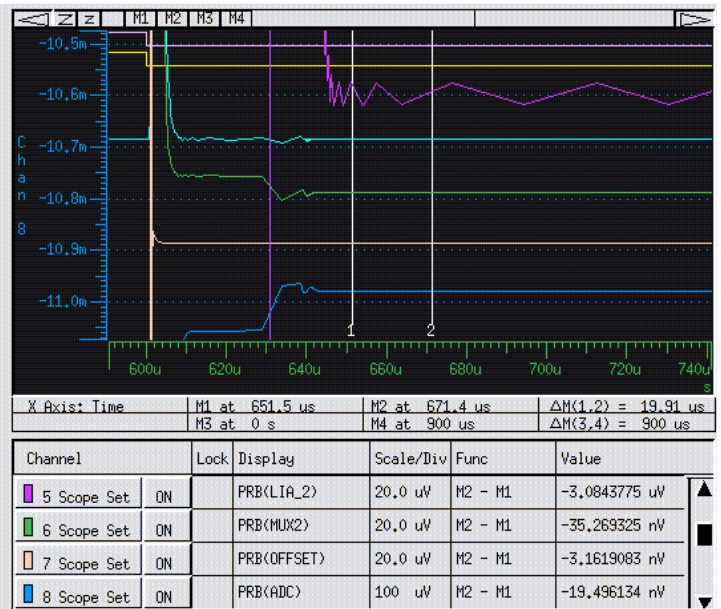
3.8.3.2.4 Simulation

The following simulation determines the maximum time that an input ADC signal needs to be stabilized after different kinds of multiplexer switching:



DETAIL N°1

DETAIL N°2



- When the LIA multiplexer and the DAQ multiplexer are switched at the same time:
 - o The ADC input signal is established and stabilized after 50 μ s. (DETAIL N°2)
- When only the DAQ multiplexer is switched:
 - o The ADC input signal is established and stabilized after 20 μ s. (DETAIL N°1)

3.8.3.3 Offset and Gain FUNC-02-6 and FUNC-02-7

After each multiplexer the channel signals that are going to be digitized are added with their 4-bit predetermined offset signal and the result is multiplied by -12 before to be digitized. Each ADC is associated to one offset generator and gain amplifier. 2 multiplexers with an OP as follower build the 4-bit offset generators.

Note: In reality the output signal of a receiver is negative between 0v and -5V. So we have $(-channel + offset) \times (-12)$ which is equivalent to $(channel - offset) \times (12)$.

3.8.3.3.1 Circuit

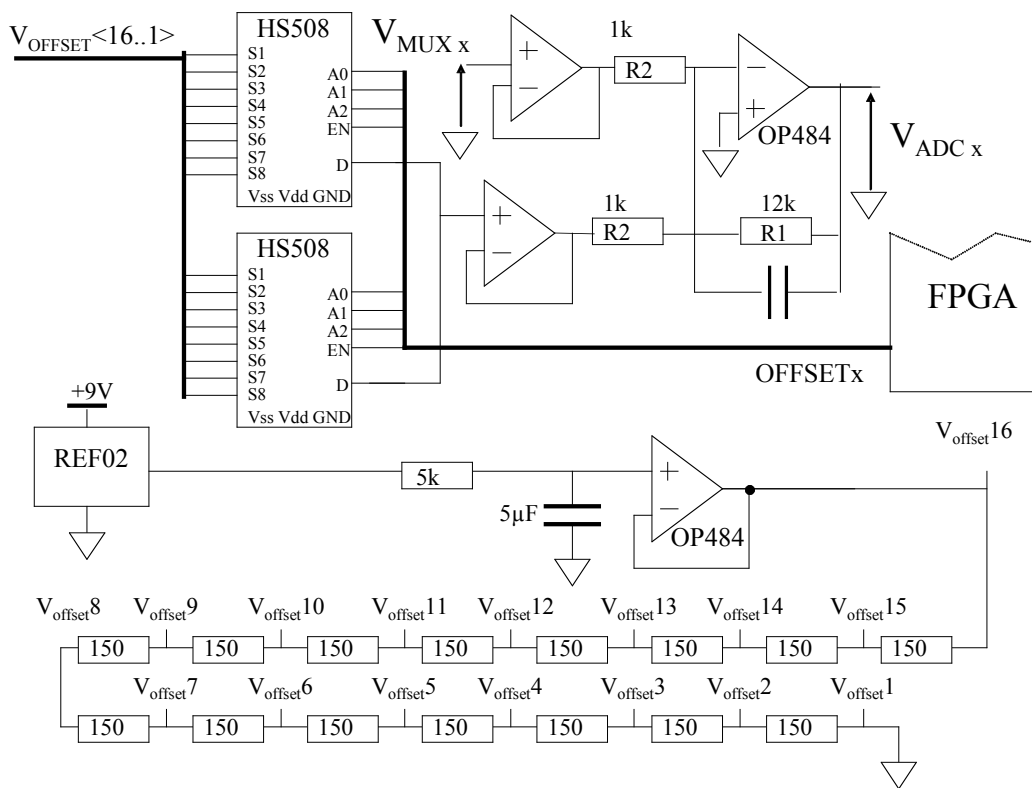


Figure 3-24 Offset and Gain Circuit

3.8.3.3.2 Noise

See noise synthesis section (on DAQ+IF).

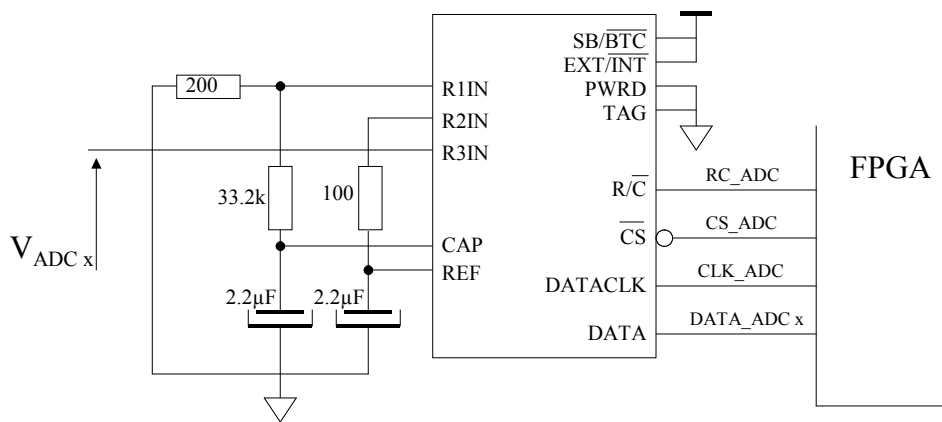
3.8.3.3.3 Timing

See FPGA section.

3.8.3.4 ADCs FUNC-03

6 ADC make the function FUNC-03. There are ADS7809 from SEI on a -1.25 to 3.75 V scale and an external clock.

3.8.3.4.1 Circuit



3.8.3.4.2 Noise

See noise synthesis section (on DAQ+IF).

3.8.3.4.3 Timing

See FPGA section.

3.8.3.5 End to End Gains

3.8.3.5.1 Gain Table

Modulation frequency in Hz	Photometer gain	TC gain	Spectrometer gain
50	4620,49	1688,22	2954,24
60	4868,03	1777,23	3110,28
70	5037,18	1838,16	3217,09
80	5155,97	1881,15	3292,43
90	5241,45	1912,34	3347,07
100	5304,24	1935,55	3387,69
110	5351,09	1953,18	3418,51
120	5386,45	1966,83	3442,32
130	5413,32	1977,55	3460,99
140	5433,75	1986,09	3475,81
150	5449,22	1992,96	3487,69
160	5460,77	1998,53	3497,29
170	5469,18	2003,09	3505,08
180	5475,03	2006,82	3511,42
190	5478,77	2009,90	3516,59
200	5480,72	2012,43	3520,79
210	5481,16	2014,50	3524,19
220	5480,28	2016,20	3526,91
230	5478,27	2017,58	3529,06
240	5475,25	2018,69	3530,71
250	5471,33	2019,56	3531,94
260	5466,61	2020,22	3532,80
270	5461,17	2020,70	3533,32
280	5455,05	2021,02	3533,56
290	5448,33	2021,21	3533,53
300	5441,04	2021,26	3533,27

3.8.3.5.2 Conversion formula

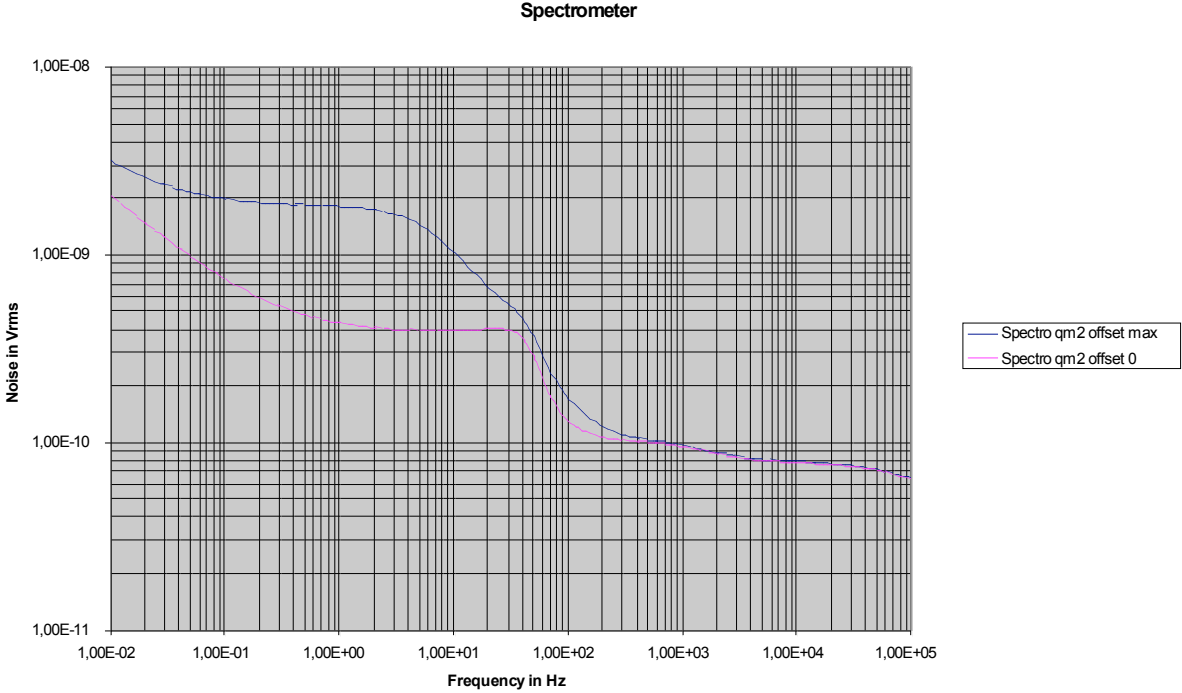
$$V_{in_{RMS}} = \frac{DATA_{RAW} - 16384 + 52428,8 \cdot Offset_{level}}{65535 \times Gain} \times 5$$

- $DATA_{RAW}$ is an integer between 0 and 65535
- $Offset_{level}$ is an integer between 0 and 15

	Photometer in mVrms	Spectrometer in mVrms	TC in mVrms
$V_{in \max}$	11,6	18	31,5
$\Delta V_{in_{RMS} \max}$ within the same offset level	0,91	1,415	2,47

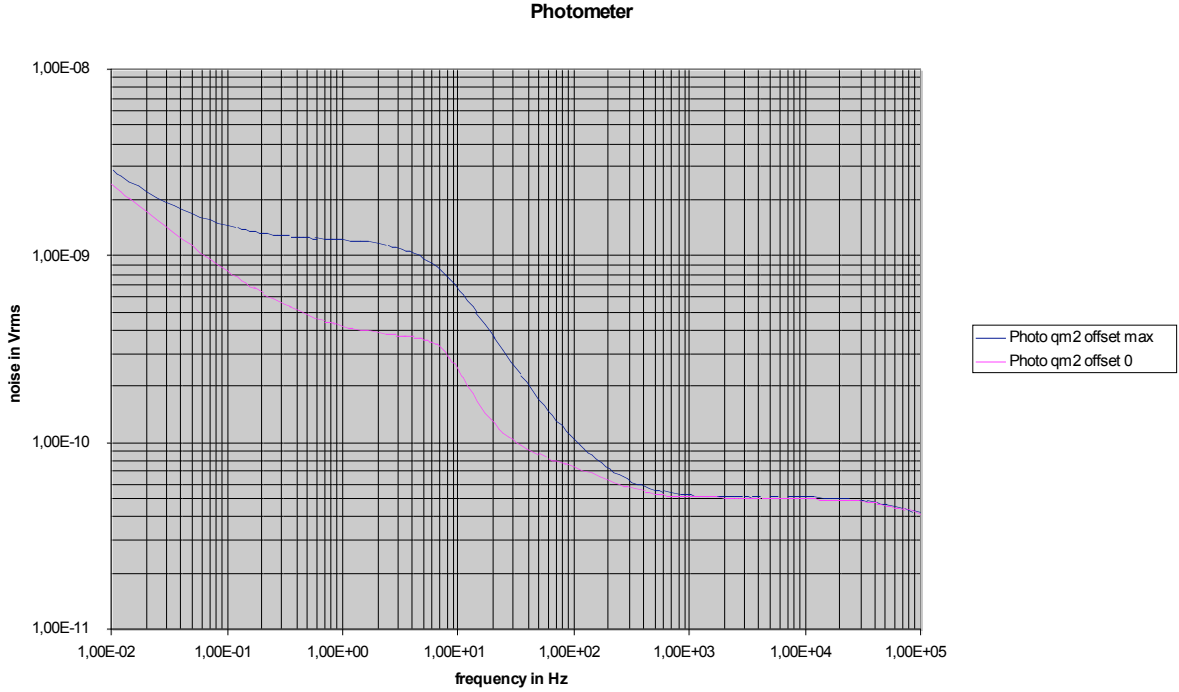
3.8.3.6 Noise Synthesis (from LIA input to DAQ+IF ADC output)

Spectrometer simulation result:



	Total noise in the BW 30mHz-100kHz	Noise density in the BW 0-25Hz
Spectrometer QM2 with offset at 0	23,25 nVrms	4.65 nVrms/rt(Hz)
Spectrometer QM2 with offset at is maximum	24,17 nVrms	4.83 nVrms/rt(Hz)

Photometer simulation result:

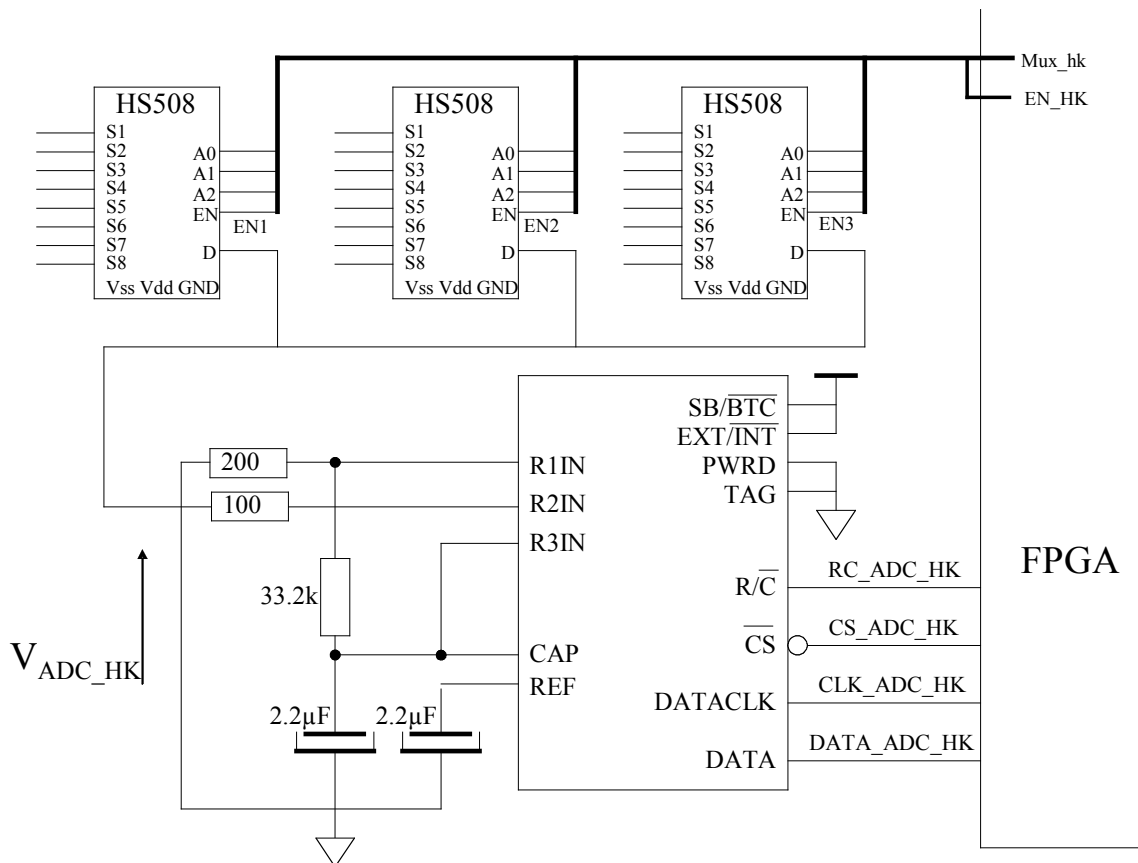


	Total noise in the BW 30mHz-100kHz	Noise density in the BW 0-5Hz
Photometer QM2 with offset at 0	14.87 nVrms	6.65 nVrms/rt(Hz)
Photometer QM2 with offset at is maximum	15.47 nVrms	6,92 nVrms/rt(Hz)

3.8.3.7 Boards Temperature and power supplies Acquisition FUNC-09-1, FUNC-09-2 and FUNC-09-3

- MUX_HK selects the board temperature and power supplies voltage, that will be digitized.
 - o Board temperature:
 - The temperature range is -40°C to 80°C .
 - The digitized signal voltage range is 2.33V to 3.53V.
 - The ADC is 16-bit with a -5V to 5V input range.
 - The ADC voltage resolution is $152\mu\text{V}$.
 - So the temperature resolution is 0.0152°C .
 - o Power supplies voltage
 - All the power supplies are divided by 10 before digitization
 - The ADC is 16-bit with a -5V to 5V input range.
 - The voltage resolution for each power supplies voltage is 0.456mV.
 - The power supplies voltage range is -15V to 15V

3.8.3.7.1 Circuit



EN_HK			MUX_HK			HK
2	1	0	2	1	0	
0	0	1	0	0	0	BIAS temperature
0	0	1	0	0	1	LIA_S1 temperature
0	0	1	0	1	0	LIA_S2 temperature
0	0	1	0	1	1	LIA_S3 temperature
0	0	1	1	0	0	LIA_P9 temperature
0	0	1	1	0	1	LIA_P8 temperature
0	0	1	1	1	0	LIA_P7 temperature
0	0	1	1	1	1	LIA_P6 temperature
0	1	0	0	0	0	LIA_P5 temperature
0	1	0	0	0	1	LIA_P4 temperature
0	1	0	0	1	0	LIA_P3 temperature
0	1	0	0	1	1	LIA_P2 temperature
0	1	0	1	0	0	LIA_P1 temperature
0	1	0	1	0	1	DAQ+IF temperature
0	1	0	1	1	0	BIAS/DAQ IF +5V
0	1	0	1	1	1	BIAS/DAQ IF +9V
1	0	0	0	0	0	BIAS/DAQ IF -9V
1	0	0	0	0	1	LIA_P +5V
1	0	0	0	1	0	LIA_P +11V
1	0	0	0	1	1	LIA_P -11V
1	0	0	1	0	0	LIA_S +5V
1	0	0	1	0	1	LIA_S +11V
1	0	0	1	1	0	LIA_S -11V
1	0	0	1	1	1	--

3.9 DAQ+IF FPGA

3.9.1 DAQ+IF FPGA Overview

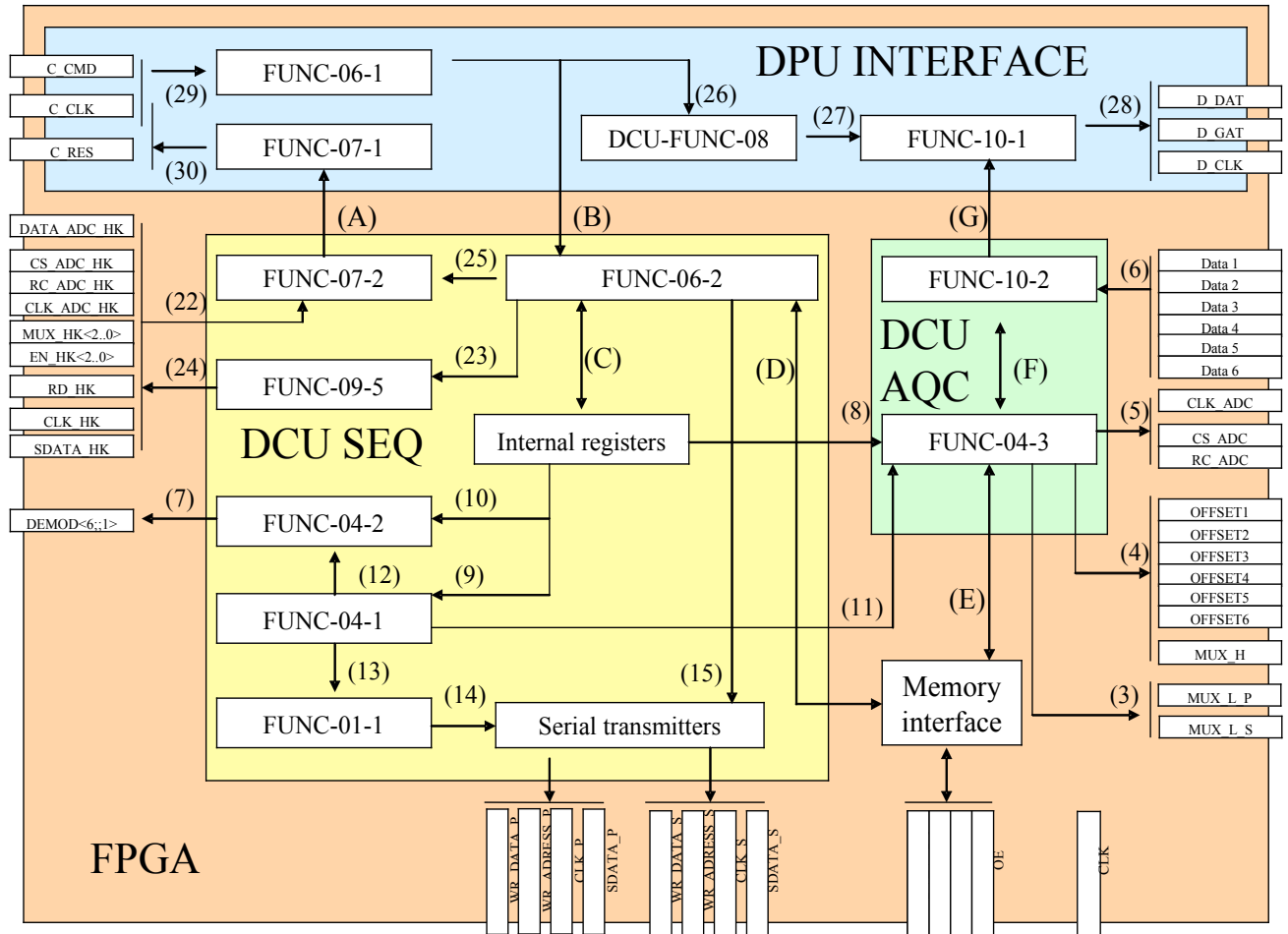


Figure 3-25 DAQ+IF FPGA Overview

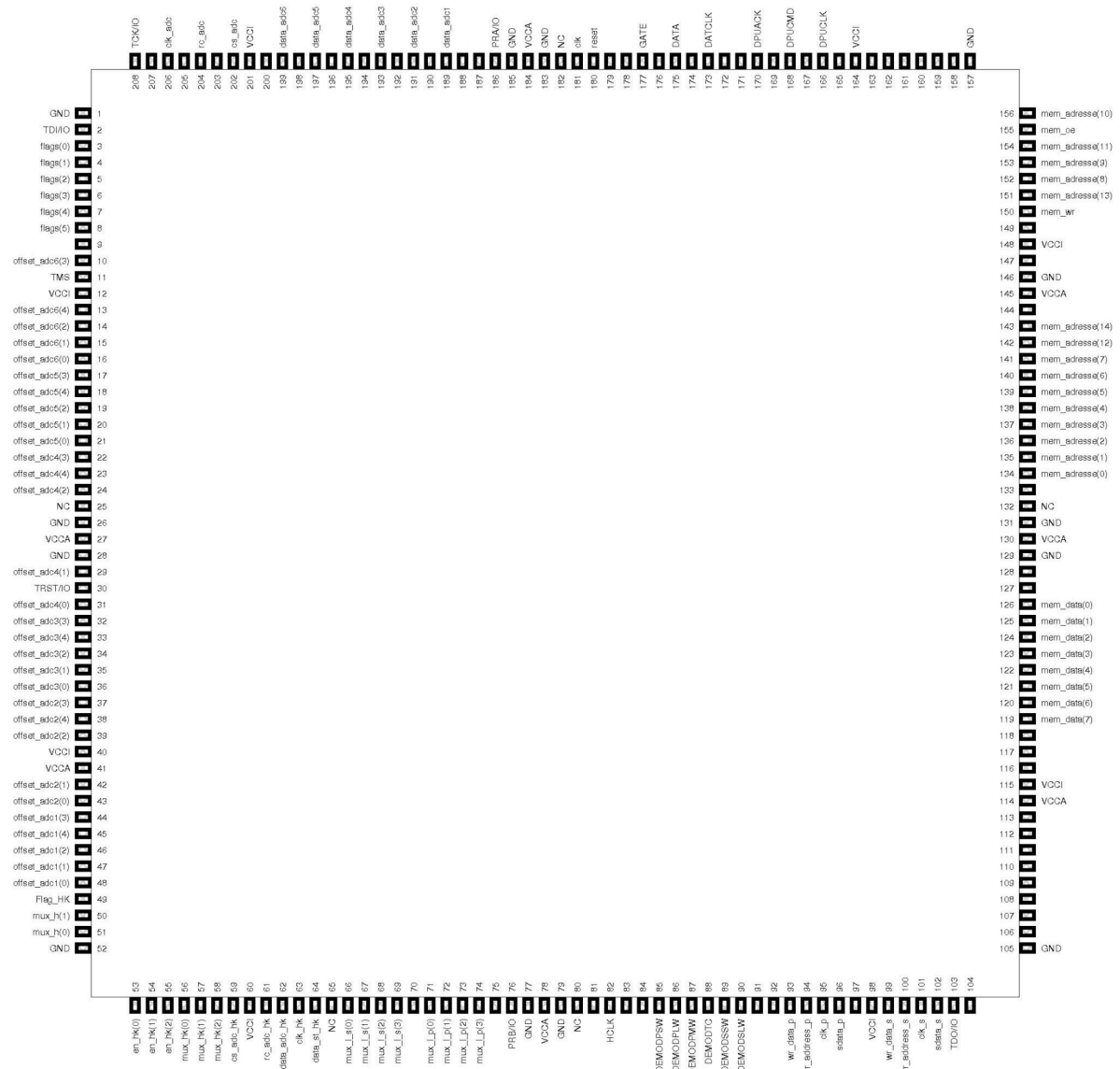
This FPGA is divided into 3 main parts:

- One handles the communication with the DPU (DPU interface)
- One handles the command executions and the “high-level sequencer” (DCU SEQ)
 - o Bias generator management (Frequency, amplitude, demodulation signals phase shift...)
 - o Mode management (picture acquisition Number and frequency, Spectrometer or photometer mode, offset set up...)
 - o Board Temperature acquisition.
- The last one handles the sequencing of picture acquisition and the offset set up (DCU AQC)

3.9.2 DAQ+IF FPGA Interfaces

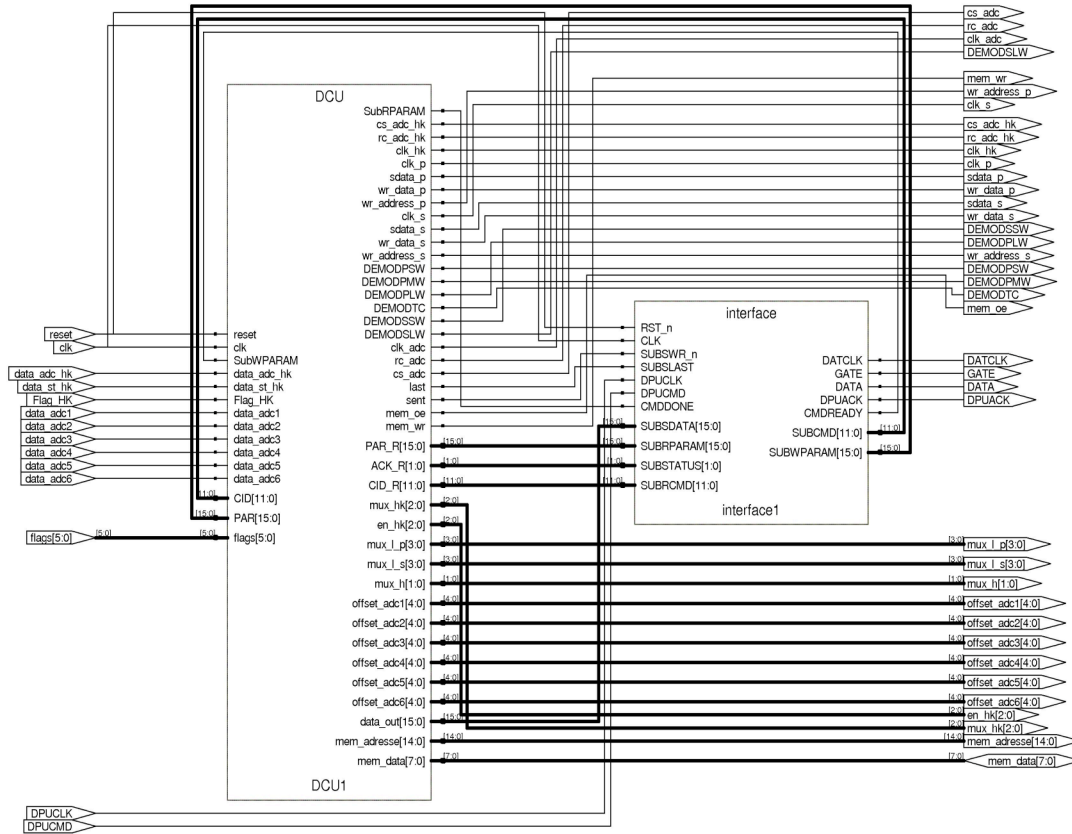
3.9.2.1 FPGA PINOUT

Name	Number	Name	Number	Name	Number
DATA	175	mem_adresse(2)	136	offset_adc1(3)	44
DATCLK	173	mem_adresse(3)	137	offset_adc1(4)	45
DEMODOPLW	86	mem_adresse(4)	138	offset_adc2(0)	43
DEMODPMW	87	mem_adresse(5)	139	offset_adc2(1)	42
DEMODPSW	85	mem_adresse(6)	140	offset_adc2(2)	39
DEMODSLW	90	mem_adresse(7)	141	offset_adc2(3)	37
DEMODSSW	89	mem_adresse(8)	152	offset_adc2(4)	38
DEMOTC	88	mem_adresse(9)	153	offset_adc3(0)	36
DPUACK	170	mem_adresse(10)	156	offset_adc3(1)	35
DPUCLK	166	mem_adresse(11)	154	offset_adc3(2)	34
DPUCMD	168	mem_adresse(12)	142	offset_adc3(3)	32
Flag_HK	49	mem_adresse(13)	151	offset_adc3(4)	33
GATE	177	mem_adresse(14)	143	offset_adc4(0)	31
clk	181	mem_data(0)	126	offset_adc4(1)	29
clk_adc	206	mem_data(1)	125	offset_adc4(2)	24
clk_hk	63	mem_data(2)	124	offset_adc4(3)	22
clk_p	95	mem_data(3)	123	offset_adc4(4)	23
clk_s	101	mem_data(4)	122	offset_adc5(0)	21
cs_adc	202	mem_data(5)	121	offset_adc5(1)	20
cs_adc_hk	59	mem_data(6)	120	offset_adc5(2)	19
data_adc1	189	mem_data(7)	119	offset_adc5(3)	17
data_adc2	191	mem_oe	155	offset_adc5(4)	18
data_adc3	193	mem_wr	150	offset_adc6(0)	16
data_adc4	195	mux_h(0)	51	offset_adc6(1)	15
data_adc5	197	mux_h(1)	50	offset_adc6(2)	14
data_adc6	199	mux_hk(0)	56	offset_adc6(3)	10
data_adc_hk	62	mux_hk(1)	57	offset_adc6(4)	13
data_st_hk	64	mux_hk(2)	58	rc_adc	204
en_hk(0)	53	mux_l_p(0)	71	rc_adc_hk	61
en_hk(1)	54	mux_l_p(1)	72	reset	180
en_hk(2)	55	mux_l_p(2)	73	sdata_p	96
flags(0)	3	mux_l_p(3)	74	sdata_s	102
flags(1)	4	mux_l_s(0)	66	wr_address_p	94
flags(2)	5	mux_l_s(1)	67	wr_address_s	100
flags(3)	6	mux_l_s(2)	68	wr_data_p	93
flags(4)	7	mux_l_s(3)	69	wr_data_s	99
flags(5)	8	offset_adc1(0)	48		
mem_adresse(0)	134	offset_adc1(1)	47		
mem_adresse(1)	135	offset_adc1(2)	46		

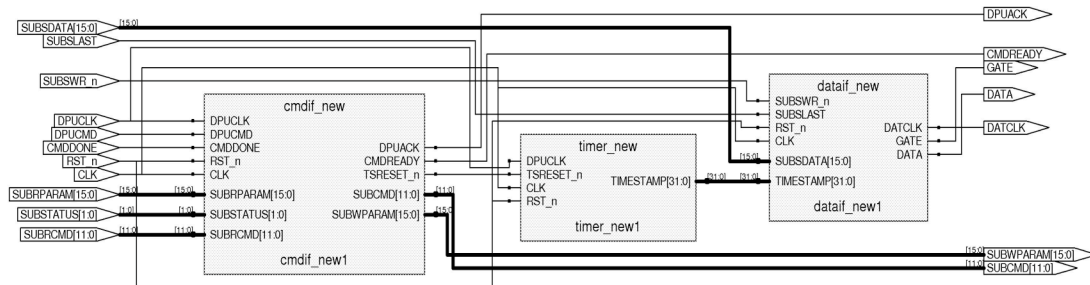


3.9.2.2 FPGA internal architecture

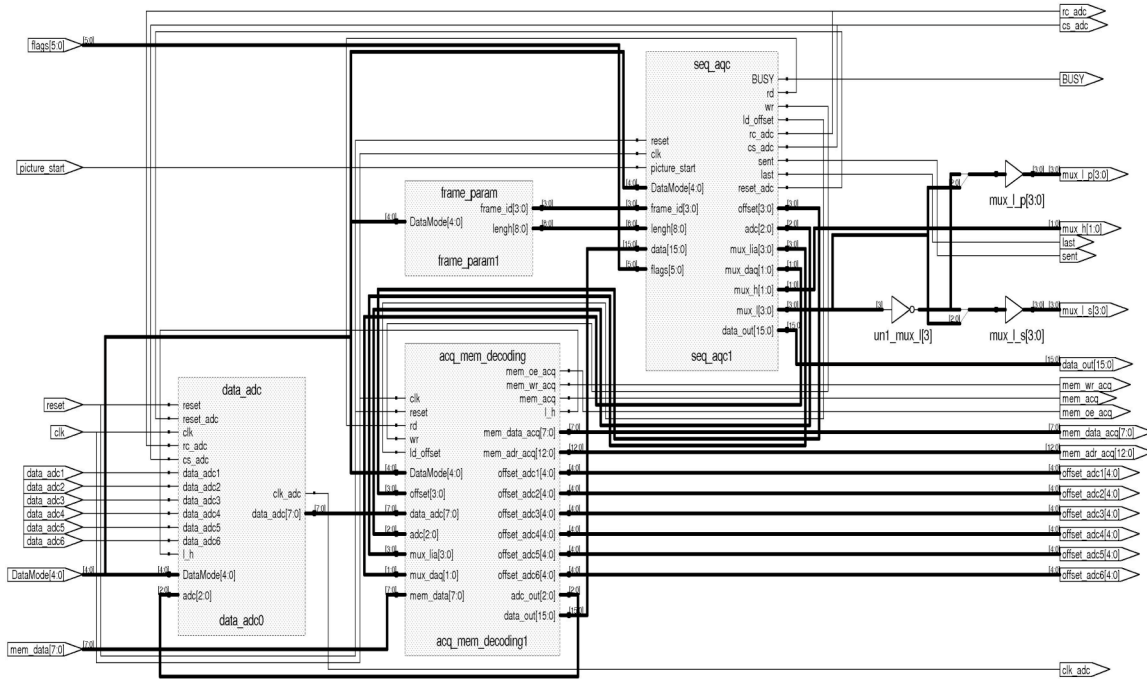
3.9.2.2.1 DCU+IF (Top) level



3.9.2.2.2 Interface (module)



3.9.2.2.5 DCU_ACQ (module)



3.9.3 DAQ+IF FPGA FUNCTIONS

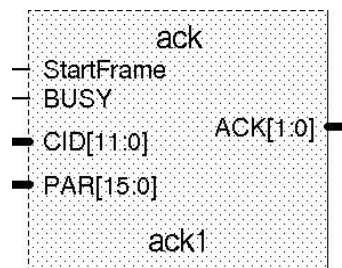
3.9.3.1 DCU SEQ: DECODING (FUNC-06-2)

This process is divided in three parts:

- Part one does the commands checking.
- Part two sequence the commands execution and the associated response sending.
- Part three decodes the commands from groups related to the load of the internal register.

3.9.3.1.1 Part one: Commands check

(VHLD module: ack.vhd)



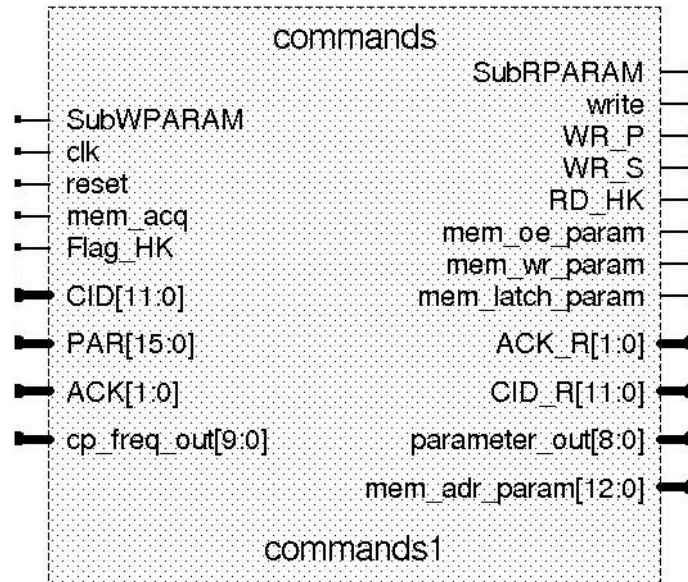
This module checks if a command is allowed in the DCU and return a command status (ACK):

Input				input		input	ouput		
CID(11)	CID(10)	CID(9..6)	CID(5..0)	PAR(15..9)	PAR(8..6)	StartFrame or busy*	ACK	Command status	
0	0	≠ 003x					01b	unknow	
1							01b	unknow	
1	1	≠ 00x					01b	unknow	
				≠ 00x			01b	unknow	
				15x	00x	00x		01b	unknow
				16x				01b	unknow
				17x				01b	unknow
				1Ex				01b	unknow
				1Fx				01b	unknow
				29x				01b	unknow
				2Ax				01b	unknow
				2Bx				01b	unknow
				2Fx				01b	unknow
				20x				01b	unknow
				21x				01b	unknow
				22x				01b	unknow
		23x		01b			unknow		
		24x		01b			unknow		
		25x		01b	unknow				
		26x		01b	unknow				
		27x		01b	unknow				
		28x		01b	unknow				
		2Cx		01b	unknow				
		2Dx		01b	unknow				
		2Ex		01b	unknow				
		2Fx		01b	unknow				
0	0				0x		01b	unknow	
							10b	forbidden	
							10b	forbidden	
Others						1	10b	forbidden	
							00b	OK	

* The DataMode (cmd: 43Cx) can't be changed when a mode is running (StartFrame=1) or the mode sequence isn't finished (busy=1).

3.9.3.1.2 Part two: Commands and response sequence diagram

(VHDL module: commands.vhd)



Commands decoding: (If ACK=00 and CID(10)=1)

CID							Action	Notes
11	5	4	3	2	1	0		
0 (set)	x	1	1	x	x	x	Write=1	Write parameter in internal register
	1	1	0	x	x	x	WR_S=1	Sent parameter to bias spectrometer
	1	0	x	x	x	x		Only writing in memory (offsets)
	others			x	x	x	WR_P=1	Sent parameter to bias photometer
1 (get)	1	1	1	1	1	1	RD_HK	Wait and get HK
	other							Get parameter from register or memory

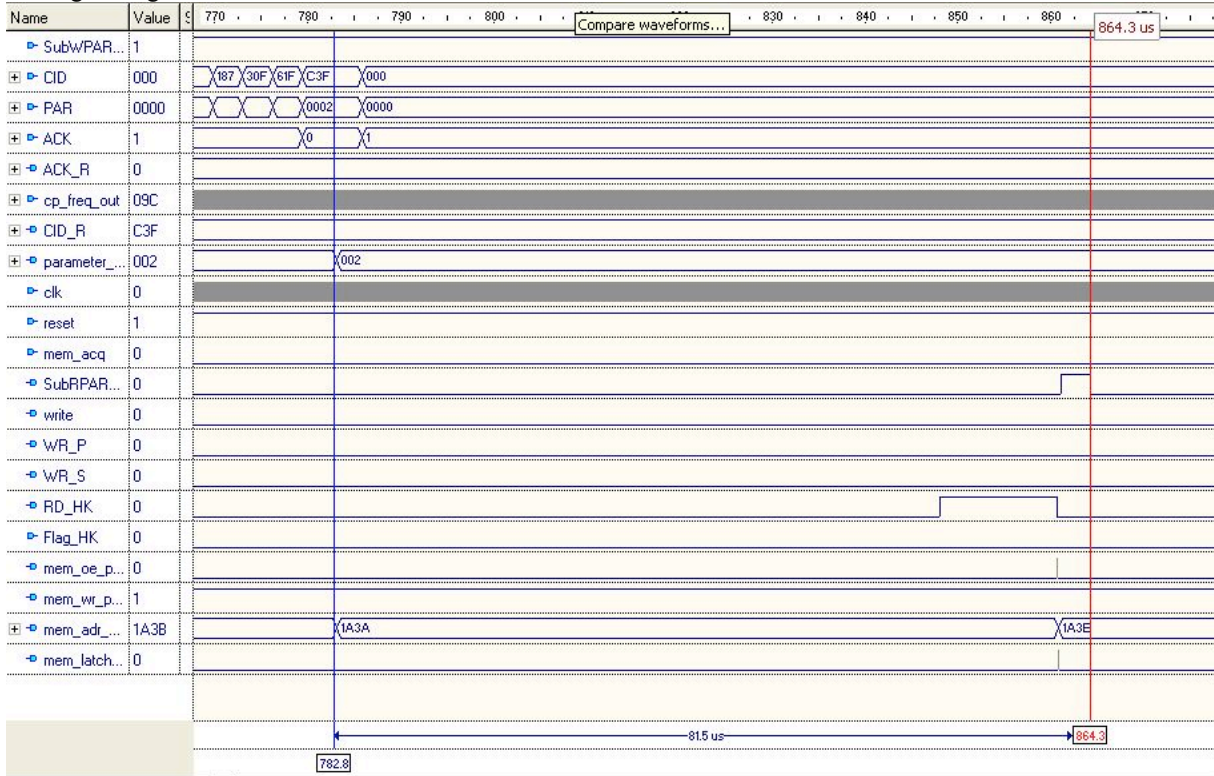
Final commands status: ACK R

ACK	CID(5..0)	Parameter(8..0)	ACK_R(1)	ACK_R(0)	notes
00	3Fx	From 00x to 16x	FLAG_HK	0	If FLAG_HK =1 there is a latch up on the ADC_HK So the response is return with a FORBIDDEN command status
		17x	0		
		1Ax			
		1Cx			
		1Ex			
others	1	command status : FORBIDDEN			
others			ACK(1)	ACK(0)	command status: see the table in the previous paragraph (Commands check)

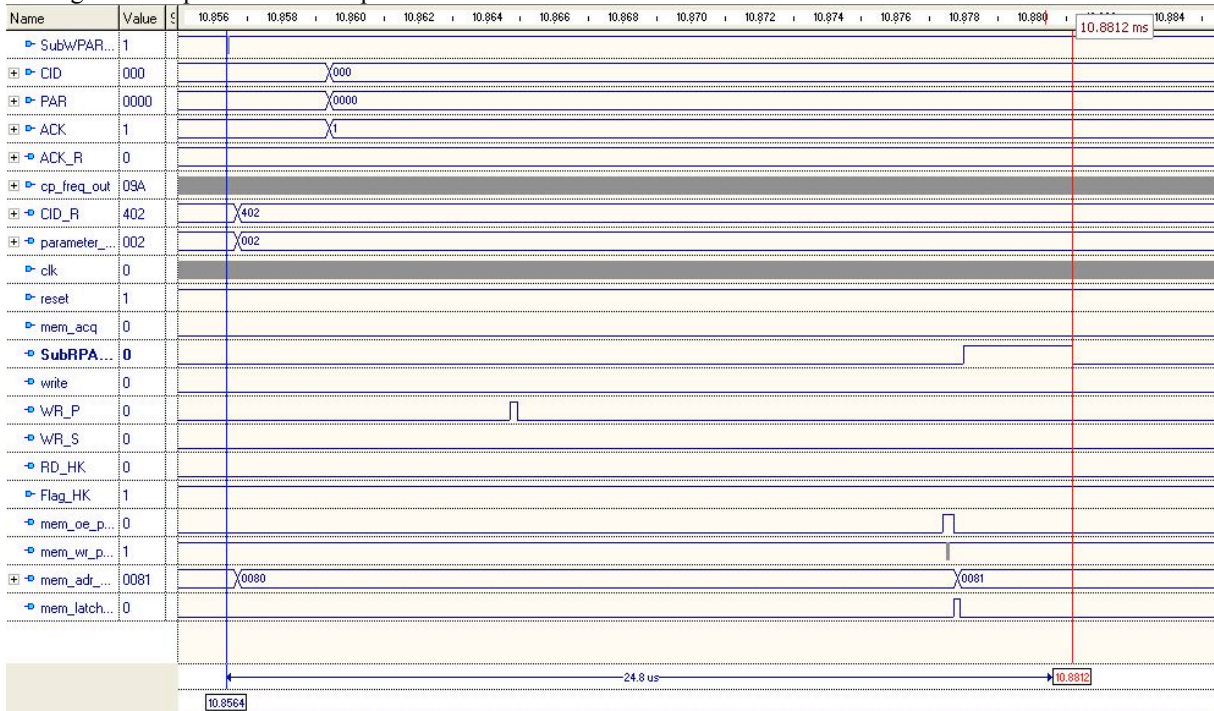
Memory structure :

CID		PAR	MEM ADR PAR				Notes
(5..4)	(3..2)	(8..4)	12	(11..6)	(5..3)	(2..1)	
3F		x	347x			PAR(2..1)	Get HK TC1, TC2, TC3
2x	3x	0x	0	CID(5..0)	0x	0	Offset spectro
		1x			1x		
		2x			2x		
		3x			3x		
		4x			4x		
		5x			5x		
		6x			6x		
		7x			7x		
		8x			8x		
		9x			9x		
		Ax			Ax		
		Bx			Bx		
		Cx			10x		
		Dx			11x		
		Ex			12x		
		Fx			13x		
		10x			14x		
		11x			15x		
		12x			16x		
		13x			17x		
14x	18x						
15x	19x						
16x	1Ax						
17x	1Bx						
others	1Fx						
	others	x			PAR(8..4)		Offset photo
Others	x	x			00x		Others parameters

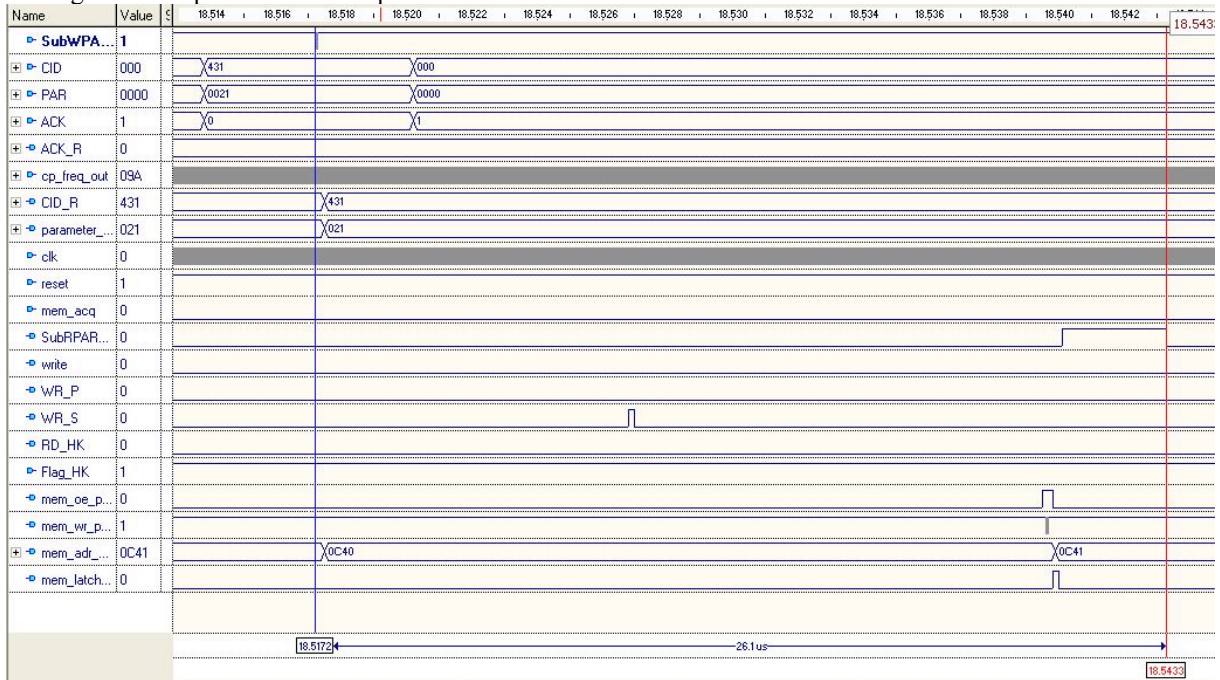
Timing for a get HK command:



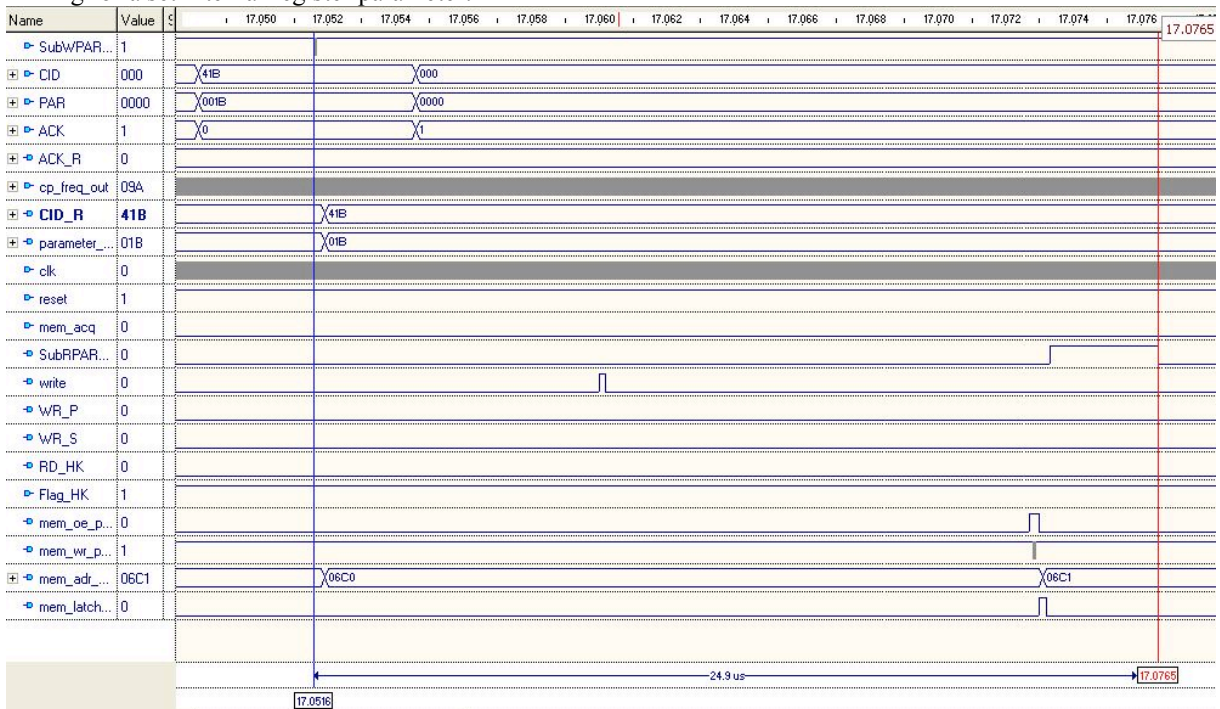
Timing for a set photometer bias parameter:



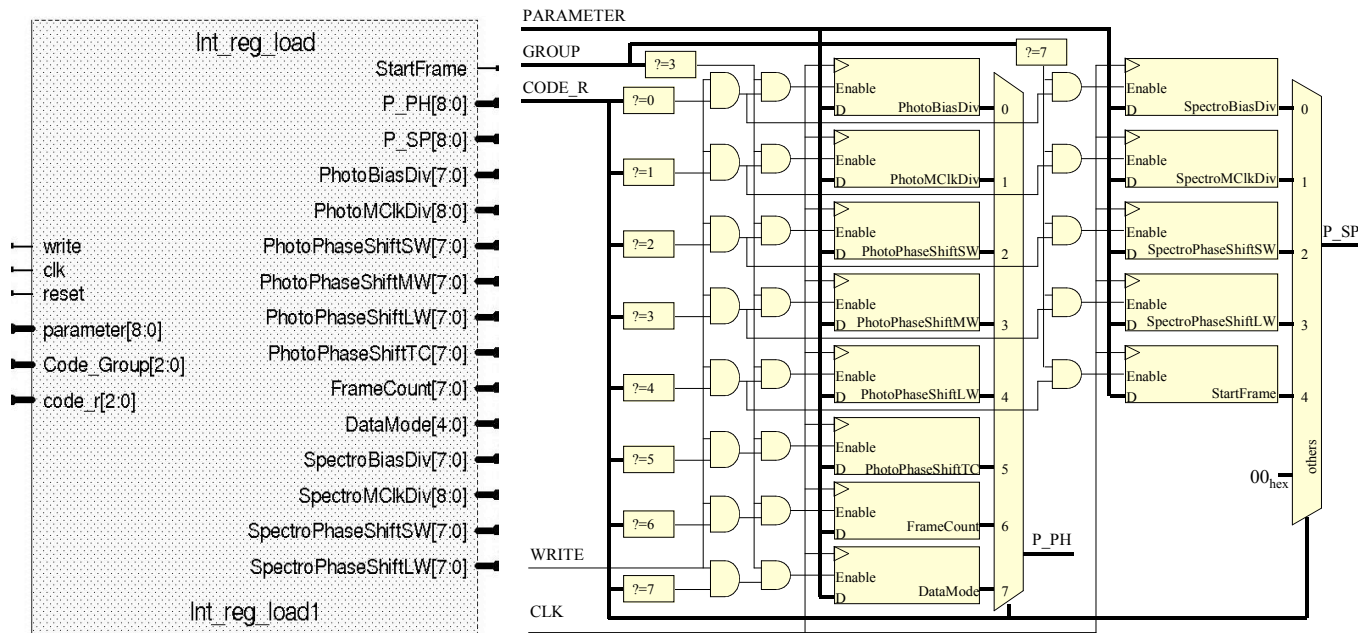
Timing for a set spectrometer bias parameter:



Timing for a set internal register parameter:



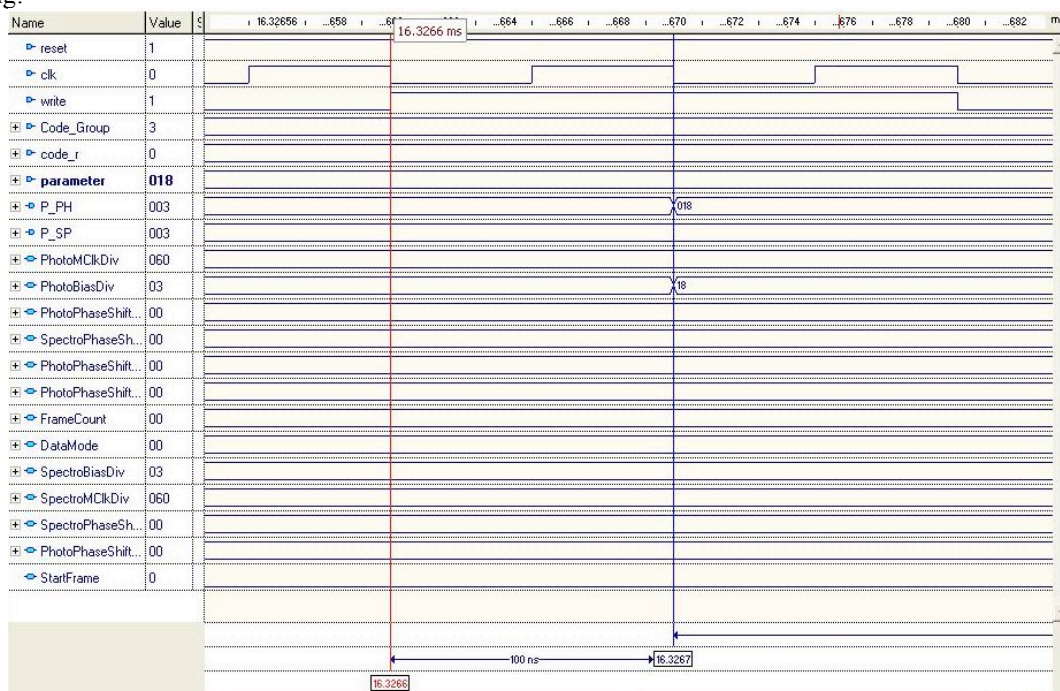
3.9.3.1.3 Part three: Internal registers load diagram (VHDL module: int_reg_load.vhd)



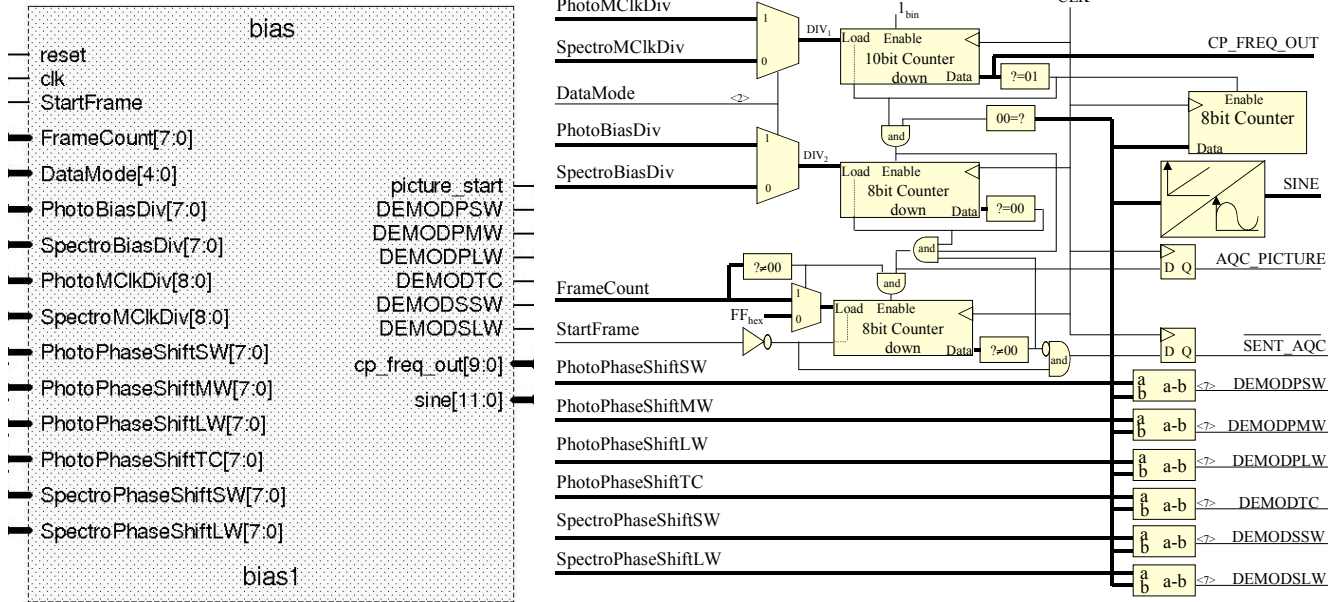
REGISTER RESET POSITION:

PhotoBiasDiv=03x; SpectroBiasDiv=03x; PhotoMClkDiv=060x; SpectroMClkDiv=060x
All the others register are set to 00x.

Timing:



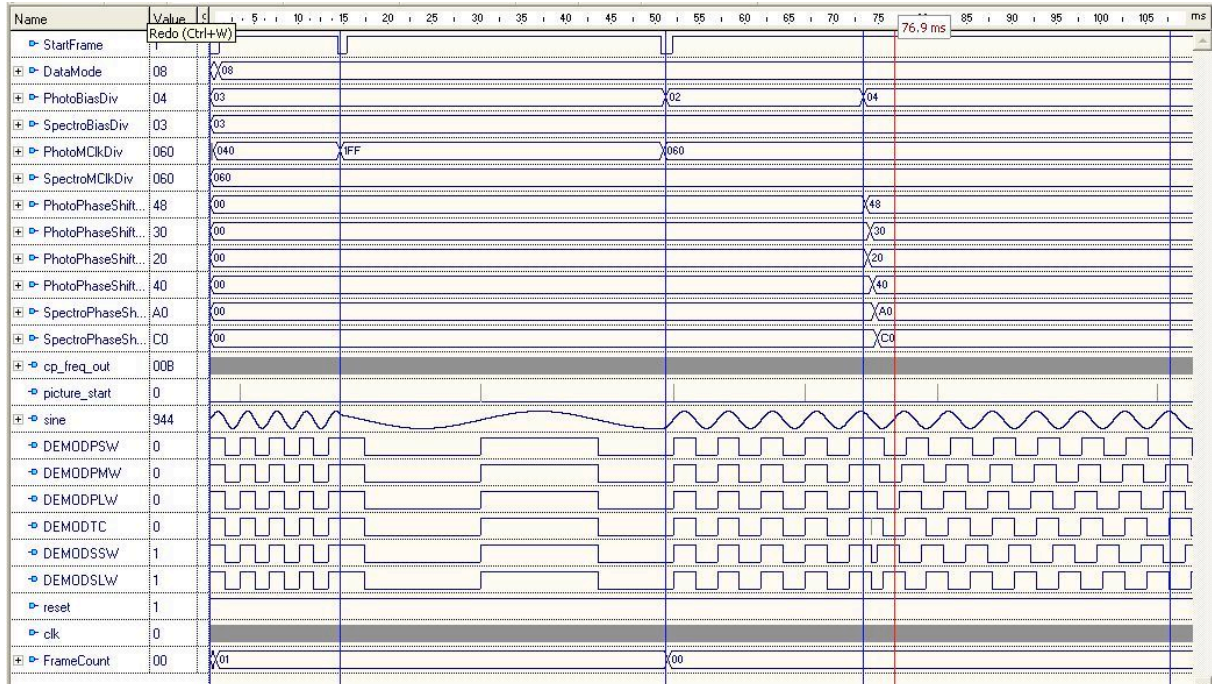
3.9.3.2 DCU SEQ: BIAS (FUNC-01-1, FUNC-04-1 and FUNC-04-2)
(VHDL module: bias.vhd)



REGISTER and COUNTER RESET POSITION:

CP_FREQ_OUT = 070x; MClkDiv = 040x; BiasDiv = 03x; All the others are set to 00x

TIMING:

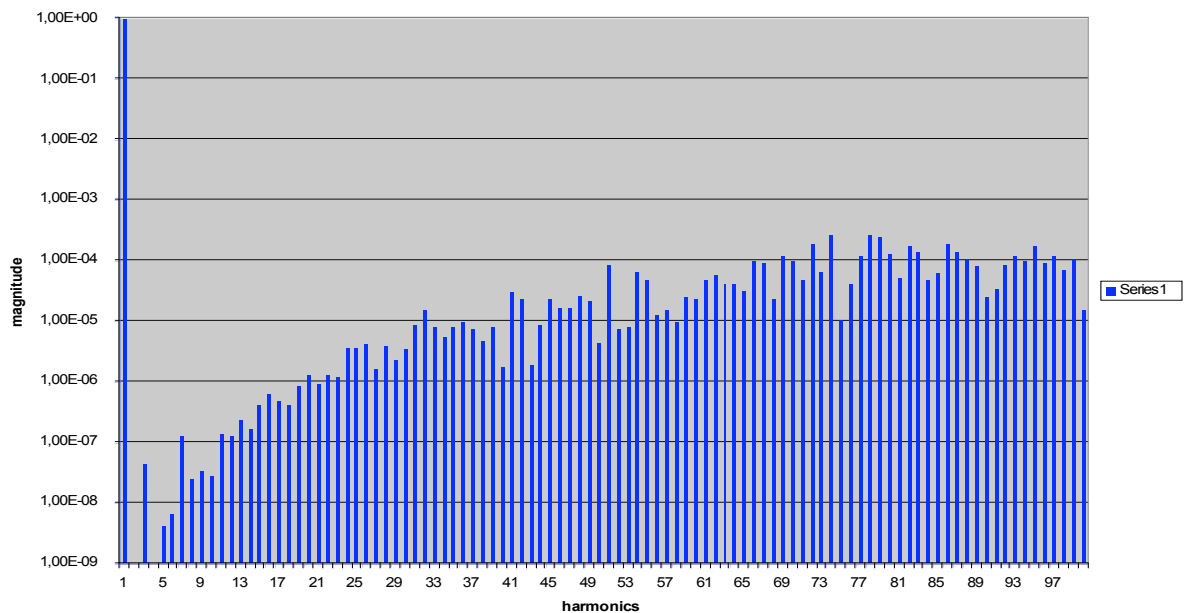


3.9.3.2.1 12bits Sine table:

nb	sine	nb	sine	nb	sine	nb	sine	nb	sine	nb	sine	nb	sine	nb	sine
1	2048	33	3386	65	3946	97	3391	129	2048	161	705	193	150	225	711
2	2094	34	3425	66	3945	98	3357	130	2003	162	674	194	150	226	735
3	2143	35	3453	67	3943	99	3320	131	1951	163	642	195	151	227	776
4	2185	36	3488	68	3943	100	3291	132	1913	164	609	196	159	228	808
5	2237	37	3511	69	3934	101	3251	133	1859	165	583	197	154	229	843
6	2277	38	3547	70	3933	102	3214	134	1816	166	550	198	170	230	881
7	2329	39	3572	71	3927	103	3181	135	1771	167	526	199	165	231	917
8	2372	40	3599	72	3916	104	3139	136	1721	168	493	200	182	232	956
9	2417	41	3628	73	3911	105	3105	137	1682	169	472	201	184	233	992
10	2465	42	3649	74	3898	106	3060	138	1626	170	444	202	198	234	1033
11	2510	43	3679	75	3890	107	3027	139	1593	171	420	203	206	235	1074
12	2553	44	3695	76	3879	108	2982	140	1538	172	397	204	217	236	1110
13	2598	45	3727	77	3861	109	2942	141	1497	173	373	205	236	237	1155
14	2645	46	3740	78	3854	110	2902	142	1455	174	353	206	242	238	1194
15	2688	47	3764	79	3831	111	2861	143	1407	175	333	207	261	239	1236
16	2729	48	3784	80	3822	112	2815	144	1365	176	312	208	280	240	1280
17	2776	49	3803	81	3800	113	2775	145	1321	177	296	209	293	241	1320
18	2816	50	3816	82	3784	114	2731	146	1281	178	274	210	312	242	1367
19	2860	51	3835	83	3763	115	2689	147	1235	179	265	211	332	243	1408
20	2902	52	3854	84	3743	116	2641	148	1194	180	242	212	356	244	1451
21	2941	53	3860	85	3723	117	2599	149	1154	181	235	213	369	245	1498
22	2986	54	3879	86	3699	118	2558	150	1114	182	217	214	401	246	1543
23	3022	55	3890	87	3676	119	2503	151	1069	183	206	215	417	247	1586
24	3063	56	3898	88	3652	120	2470	152	1036	184	198	216	447	248	1631
25	3104	57	3912	89	3624	121	2414	153	991	185	185	217	468	249	1679
26	3140	58	3914	90	3603	122	2375	154	957	186	180	218	497	250	1724
27	3179	59	3931	91	3570	123	2325	155	915	187	169	219	524	251	1767
28	3215	60	3926	92	3546	124	2280	156	882	188	163	220	549	252	1819
29	3253	61	3942	93	3513	125	2237	157	845	189	162	221	586	253	1860
30	3288	62	3937	94	3487	126	2183	158	805	190	153	222	604	254	1908
31	3320	63	3945	95	3454	127	2145	159	776	191	153	223	649	255	1956
32	3361	64	3946	96	3422	128	2093	160	739	192	151	224	667	256	2001

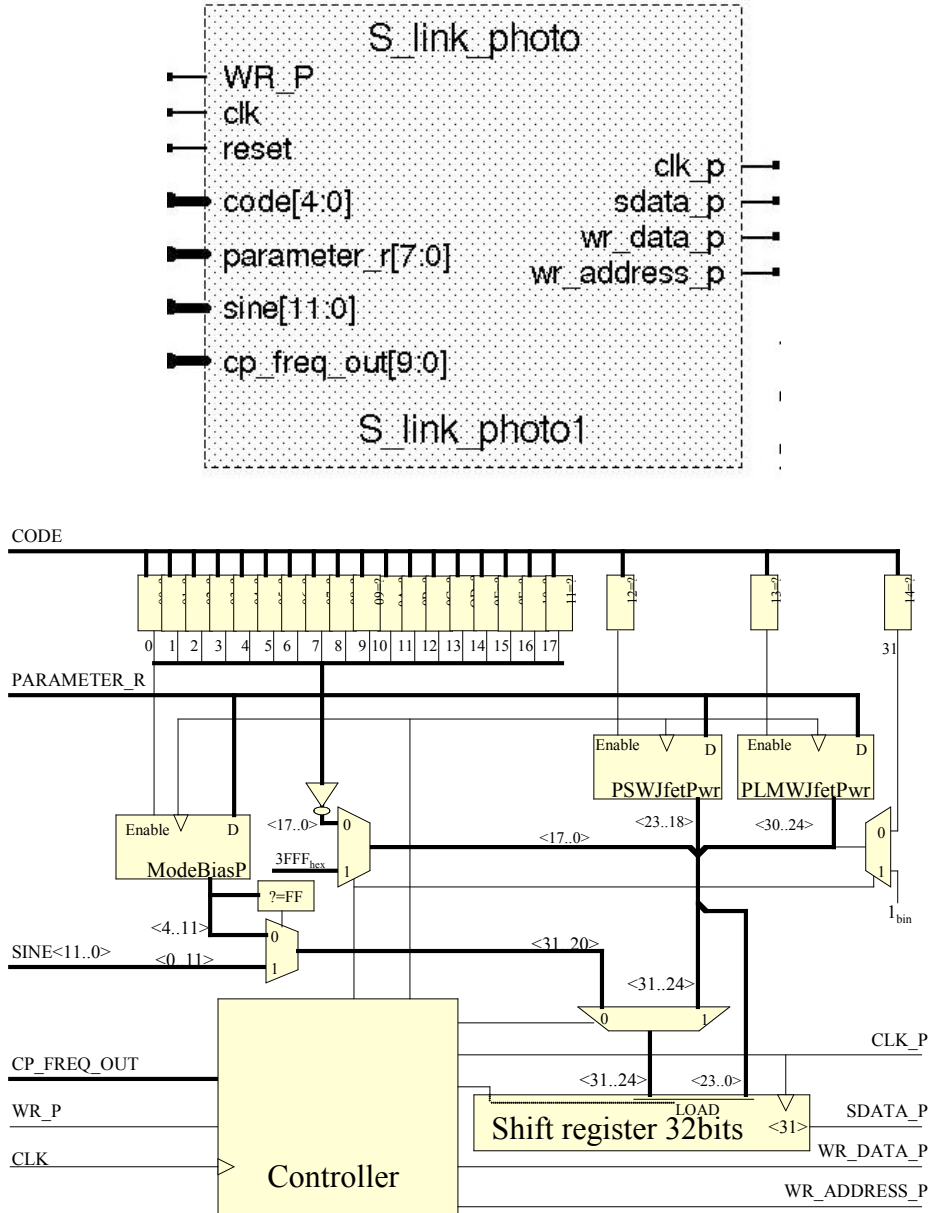
Total Harmonic Distortion = $76,160 \cdot 10^{-3} \%$

Harmonics graph:



3.9.3.3 DCU SEQ: SERIAL LINK PHOTOMETER

(VHDL module:S_link_photo.vhd)

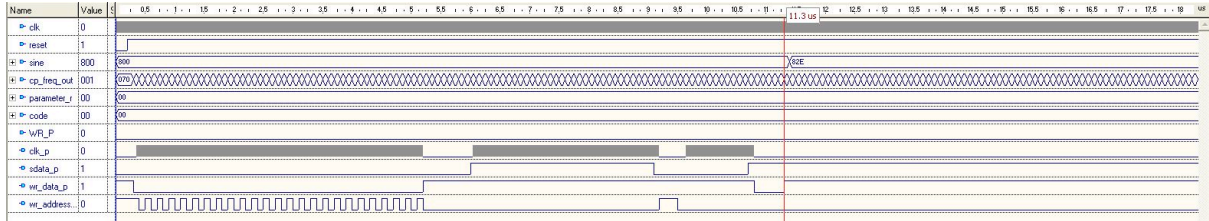


REGISTER RESET POSITION:

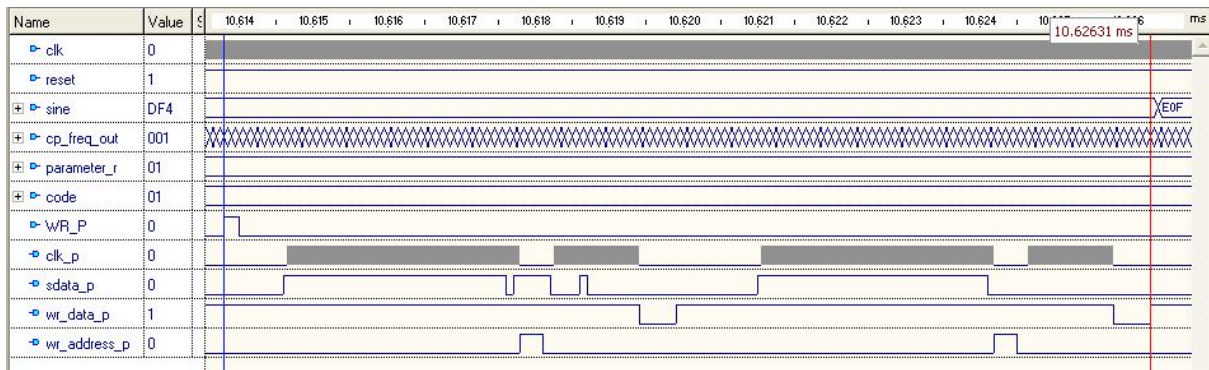
PSWjfetPwr = 3Fx; PLMWjfetPwr = 7Fx; ModeBiasP=FFx; ShiftReg=00000000x

TIMING:

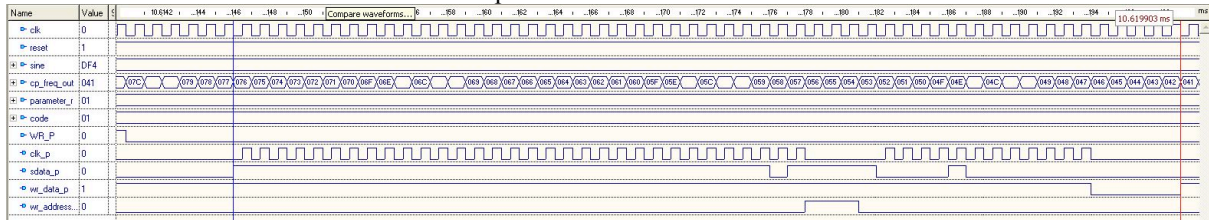
1) Bias initialization sequence:



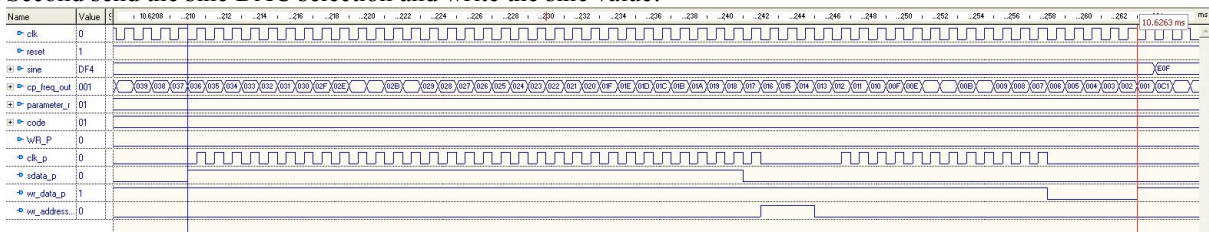
2) Bias parameter writing:



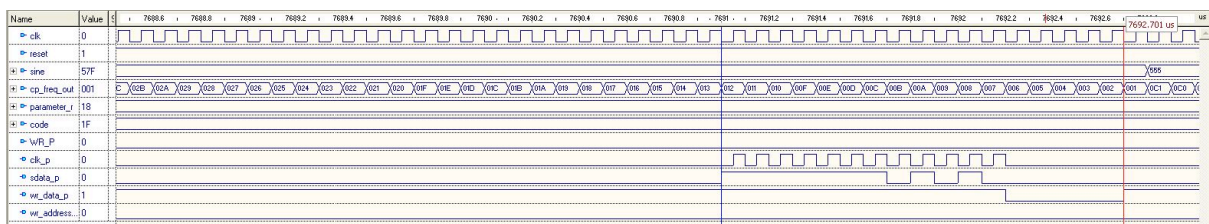
First send the DAC selection and write of the parameter:



Second send the sine DAC selection and write the sine value:

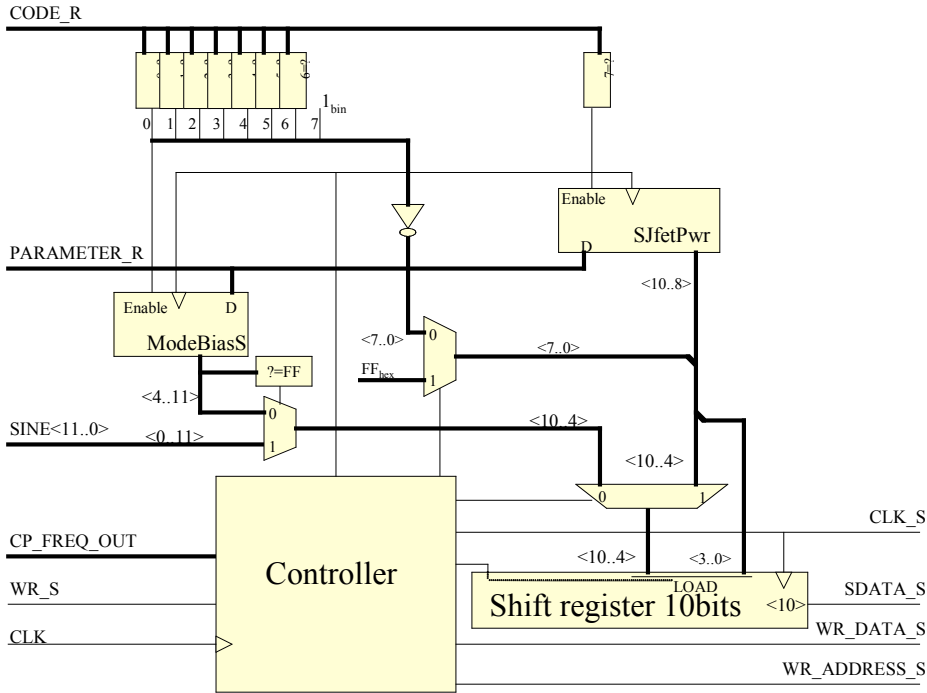
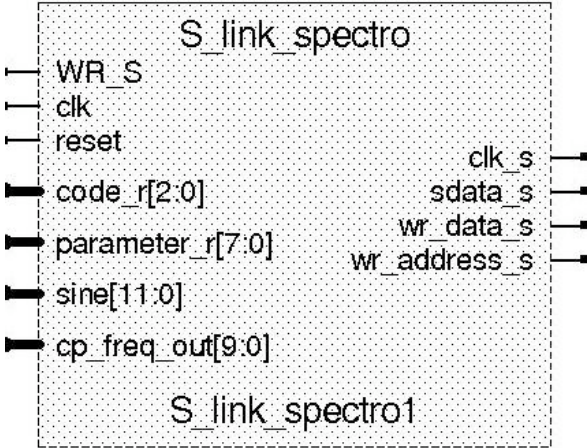


3) Writing of a sine level when the sine mode is running:



3.9.3.4 DCU SEQ: SERIAL LINK SPECTROMETER

(VHLD module:S_link_photo.vhd)

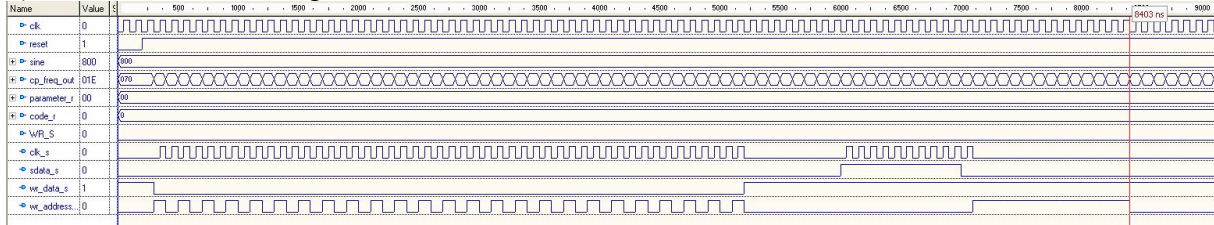


REGISTER RESET POSITION:

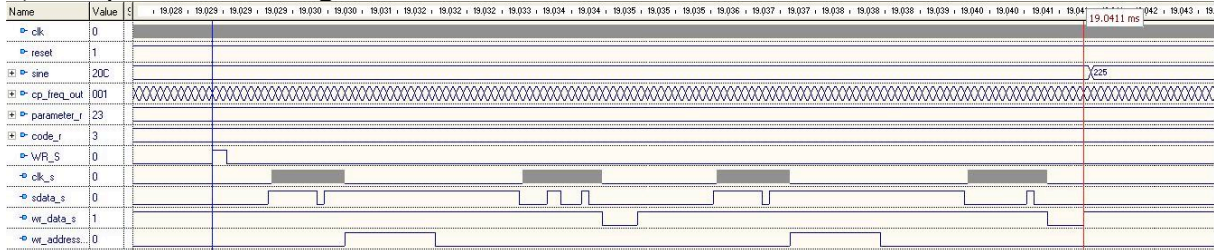
SJfetPwr = 3x; ModeBiasS=FFx; ShiftReg=000x

TIMING:

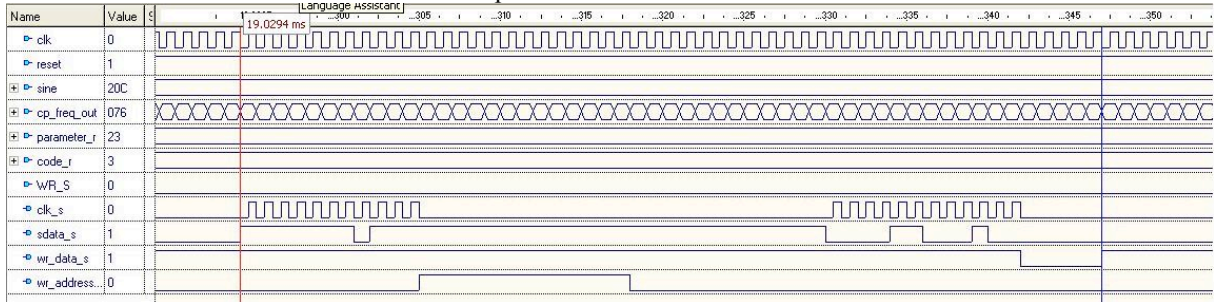
1) Bias initialization sequence:



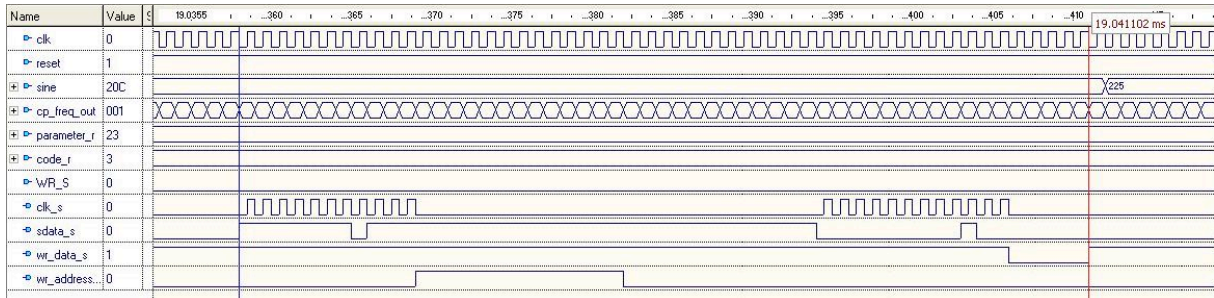
2) Bias parameter writing:



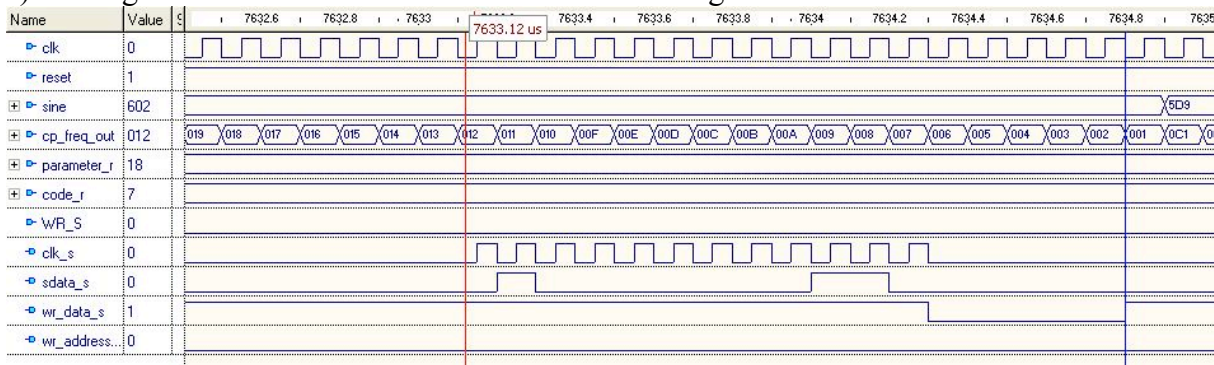
First send the DAC selection and write of the parameter:



Second send the sine DAC selection and write the sine value:

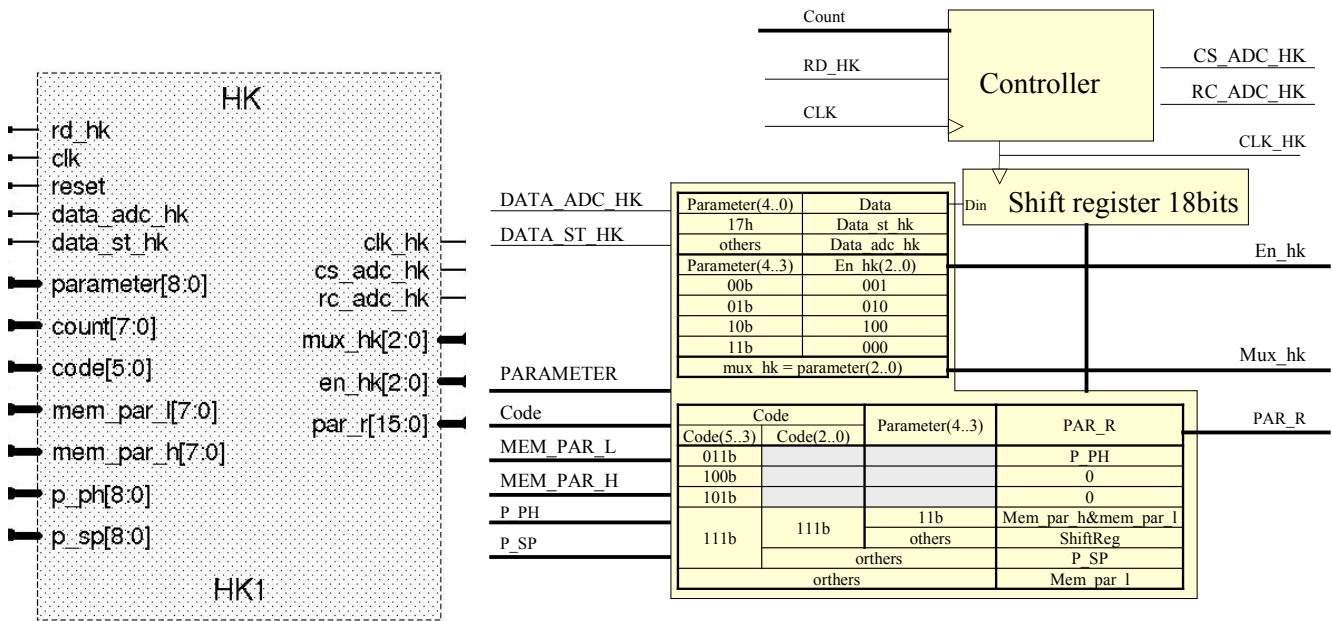


3) Writing of a sine level when the sine mode is running:

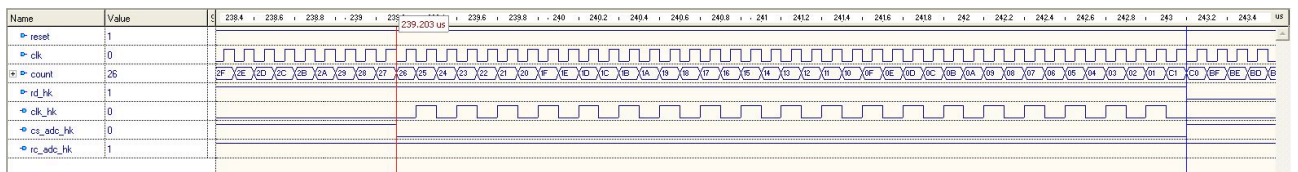
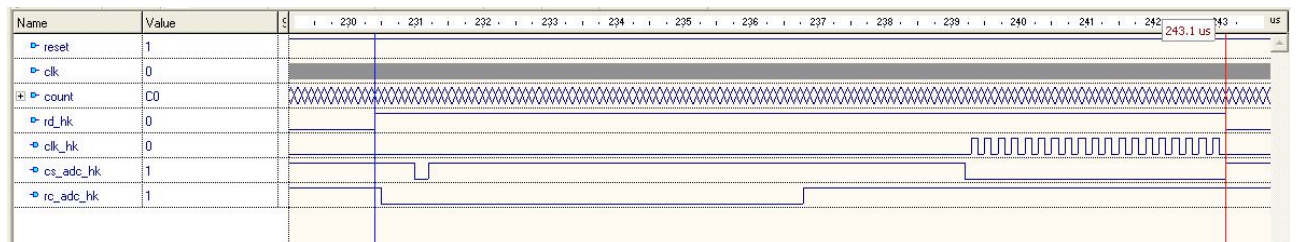
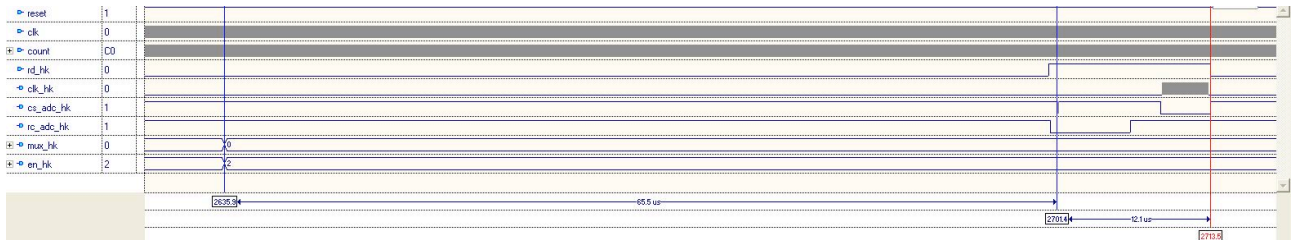


3.9.3.5 DCU SEQ: HK ACQUISITION and COMMANDS RESPONSE (FUNC-07-2 and FUNC-09-5)

(VHDL module: hk.vhd)

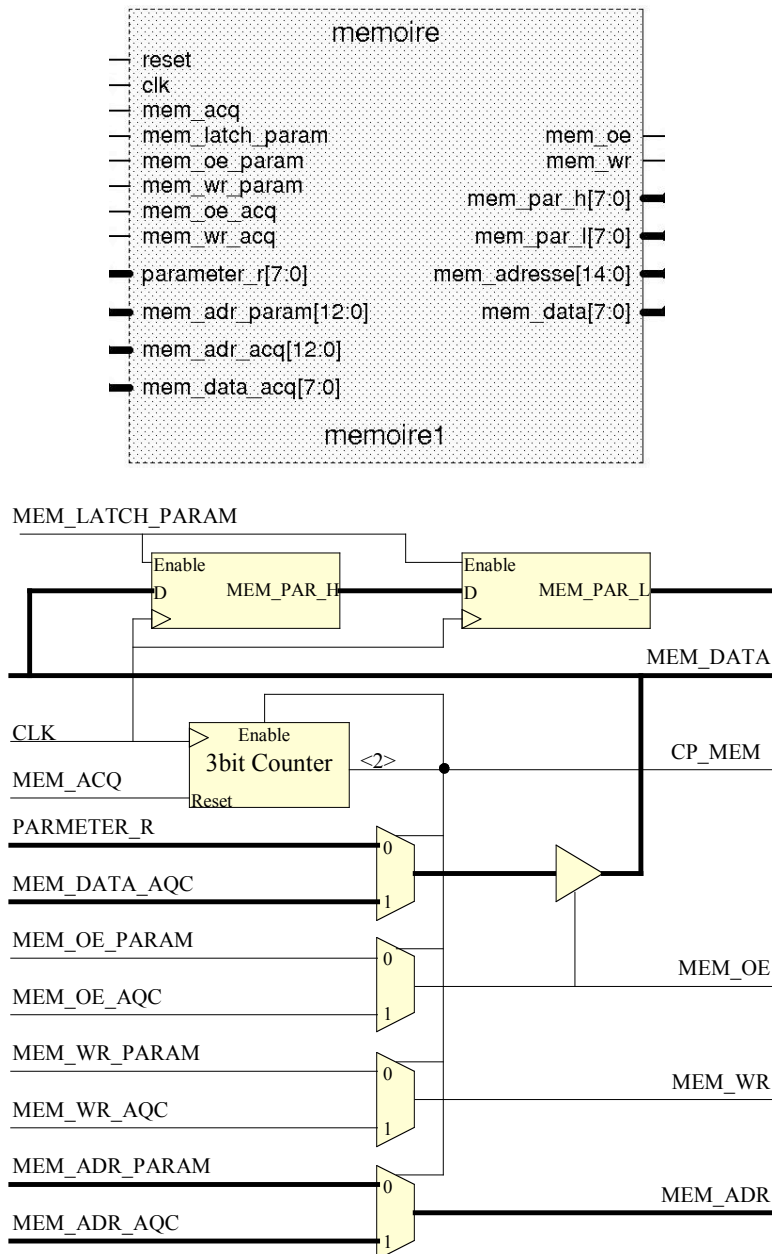


Timings:



3.9.3.6 MEMORY INTERFACE

(VHDL module: memoire.vhd)



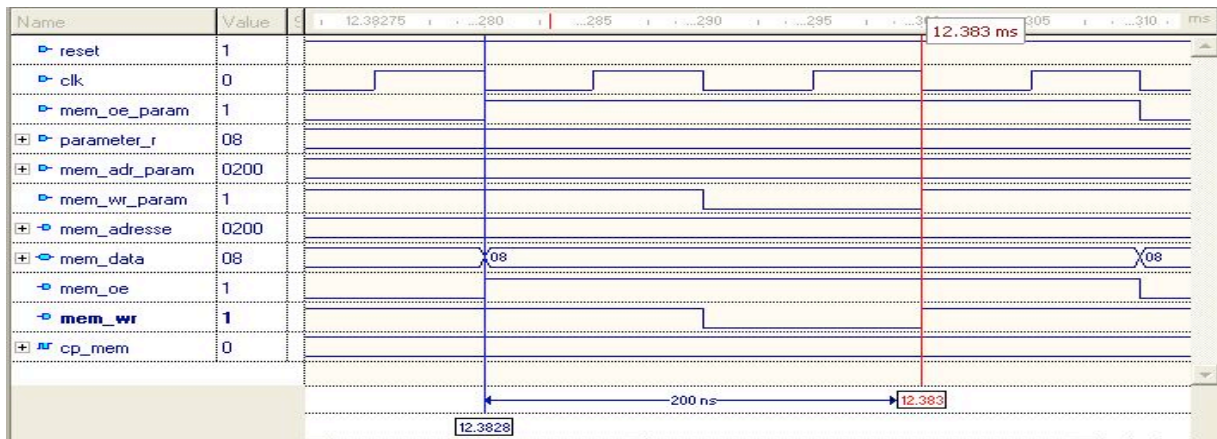
The memory access is chaired between the data acquisition processes and the commands processes. The priority is given to the acquisition processes.

Memory mapping:

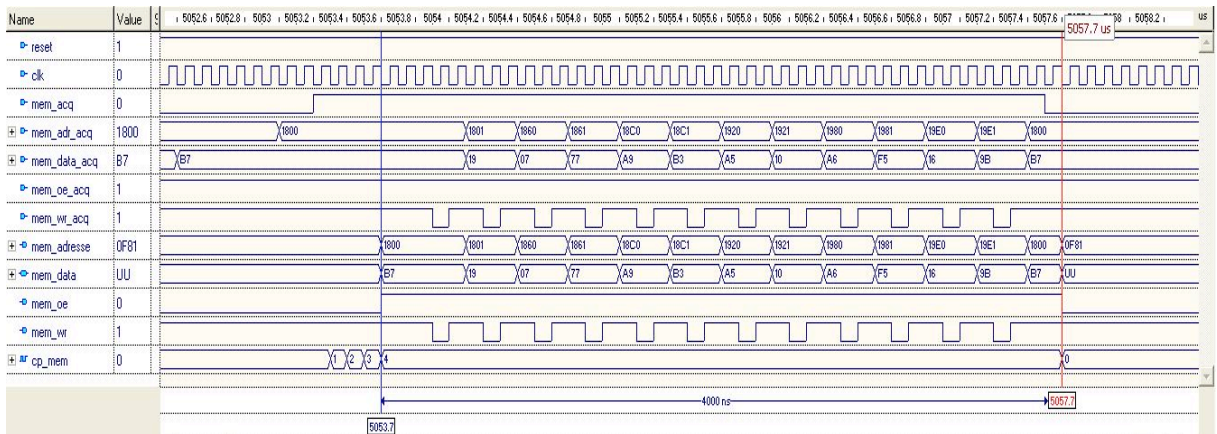
MEM_ADR		Type of data
From	To	
0000	07C0	Cmd parameter
0800	0A3E	Offset Photometer
0B00	0BB6	Offset Spectrometer
1800	1A3F	DATA Photometer
1B00	1BB7	DATA Spectrometer

Timing:

Write parameter cycle:



Write data cycle:



3.9.3.7 DCU ACQ (FUNC-10-2 and FUNC-04-3)

3.9.3.7.1 Mode/Frame conversion table

(VHDL module: frame_param.vhd)

frame_param

frame_id[3:0] —

DataMode[4:0] —

length[8:0] —

frame_param1

DataMode	Frame_id	length	Mode
00x	0x	294	Photo
01x	2x	150	Psw
02x	3x	102	Pmw
03x	4x	54	Plw
04x	1x	78	Spectro
05x	5x	54	Ssw
06x	6x	30	Slw
08x	9x	294	Photo test
09x	Ax	150	Psw test
0Ax	Bx	102	Pmw test
0Bx	Cx	54	Plw test
0Cx	Dx	78	Spectro test
0Dx	Ex	54	Ssw test
0Ex	Fx	30	Slw test
18x	7x	294	Offset photo
1Cx	8x	78	Offset spectro
others	Fx	0	Error

3.9.3.7.2 Acquisition memory structure

(VHDL module: acq_mem_decoding.vhd)

acq_mem_decoding

mem_oe_acq —

mem_wr_acq —

mem_acq —

l_h —

clk —

reset —

rd —

wr —

ld_offset —

mem_data_acq[7:0] —

mem_adr_acq[12:0] —

offset_adc1[4:0] —

offset_adc2[4:0] —

data_adc[7:0] —

offset_adc3[4:0] —

adc[2:0] —

offset_adc4[4:0] —

mux_lia[3:0] —

offset_adc5[4:0] —

mux_daq[1:0] —

offset_adc6[4:0] —

mem_data[7:0] —

adc_out[2:0] —

data_out[15:0] —

acq_mem_decoding1

Mux_daq	adc	Mem_adr_acq (9..5)	DataMode	Mem_adr_acq (12)	Mem_adr_acq (0)
00	x	11&adc	offset	0	0
01	000	00000	Data	1	L H
	001	00011			
	010	00110	Mem_adr_acq (11..10)		
	011	01001	10		
	100	01100			
	others	01111	Mem_adr_acq (4..1)		
	10	000	00001	Mux_lia	
001		00100			
010		00111	DataMode	Mem_data_adc	
011		01010	offset	"0000"&offset_adc(adc)	
100		01101	Data	Data_adc	
others		10000			
11	000	00010			
	001	00101			
	010	01000			
	011	01011			
	100	01110			
	others	10001			

MEMORY MAPPING:

Data Spectrometer mapping					
Adr_mem:1B00	L	LIA_S1_ch1	Adr_mem:1B40	L	LIA_S2_ch1
Adr_mem:1B01	H	LIA_S1_ch1	Adr_mem:1B41	H	LIA_S2_ch1
Adr_mem:1B02	L	LIA_S1_ch2	Adr_mem:1B42	L	LIA_S2_ch2
Adr_mem:1B03	H	LIA_S1_ch2	Adr_mem:1B43	H	LIA_S2_ch2
Adr_mem:1B04	L	LIA_S1_ch3	Adr_mem:1B44	L	LIA_S2_ch3
Adr_mem:1B05	H	LIA_S1_ch3	Adr_mem:1B45	H	LIA_S2_ch3
Adr_mem:1B06	L	LIA_S1_ch4	Adr_mem:1B46	L	LIA_S2_ch4
Adr_mem:1B07	H	LIA_S1_ch4	Adr_mem:1B47	H	LIA_S2_ch4
Adr_mem:1B08	L	LIA_S1_ch5	Adr_mem:1B48	L	LIA_S2_ch5
Adr_mem:1B09	H	LIA_S1_ch5	Adr_mem:1B49	H	LIA_S2_ch5
Adr_mem:1B0A	L	LIA_S1_ch6	Adr_mem:1B4A	L	LIA_S2_ch6
Adr_mem:1B0B	H	LIA_S1_ch6	Adr_mem:1B4B	H	LIA_S2_ch6
Adr_mem:1B0C	L	LIA_S1_ch7	Adr_mem:1B4C	L	LIA_S2_ch7
Adr_mem:1B0D	H	LIA_S1_ch7	Adr_mem:1B4D	H	LIA_S2_ch7
Adr_mem:1B0E	L	LIA_S1_ch8	Adr_mem:1B4E	L	LIA_S2_ch8
Adr_mem:1B0F	H	LIA_S1_ch8	Adr_mem:1B4F	H	LIA_S2_ch8
Adr_mem:1B10	L	LIA_S1_ch9	Adr_mem:1B50	L	LIA_S2_ch9
Adr_mem:1B11	H	LIA_S1_ch9	Adr_mem:1B51	H	LIA_S2_ch9
Adr_mem:1B12	L	LIA_S1_ch10	Adr_mem:1B52	L	LIA_S2_ch10
Adr_mem:1B13	H	LIA_S1_ch10	Adr_mem:1B53	H	LIA_S2_ch10
Adr_mem:1B14	L	LIA_S1_ch11	Adr_mem:1B54	L	LIA_S2_ch11
Adr_mem:1B15	H	LIA_S1_ch11	Adr_mem:1B55	H	LIA_S2_ch11
Adr_mem:1B16	L	LIA_S1_ch12	Adr_mem:1B56	L	LIA_S2_ch12
Adr_mem:1B17	H	LIA_S1_ch12	Adr_mem:1B57	H	LIA_S2_ch12
Adr_mem:1B20	L	LIA_S1_ch13	Adr_mem:1B60	L	LIA_S2_ch13
Adr_mem:1B21	H	LIA_S1_ch13	Adr_mem:1B61	H	LIA_S2_ch13
Adr_mem:1B22	L	LIA_S1_ch14	Adr_mem:1B62	L	LIA_S2_ch14
Adr_mem:1B23	H	LIA_S1_ch14	Adr_mem:1B63	H	LIA_S2_ch14
Adr_mem:1B24	L	LIA_S1_ch15	Adr_mem:1B64	L	LIA_S2_ch15
Adr_mem:1B25	H	LIA_S1_ch15	Adr_mem:1B65	H	LIA_S2_ch15
Adr_mem:1B26	L	LIA_S1_ch16	Adr_mem:1B66	L	LIA_S2_ch16
Adr_mem:1B27	H	LIA_S1_ch16	Adr_mem:1B67	H	LIA_S2_ch16
Adr_mem:1B28	L	LIA_S1_ch17	Adr_mem:1B68	L	LIA_S2_ch17
Adr_mem:1B29	H	LIA_S1_ch17	Adr_mem:1B69	H	LIA_S2_ch17
Adr_mem:1B2A	L	LIA_S1_ch18	Adr_mem:1B6A	L	LIA_S2_ch18
Adr_mem:1B2B	H	LIA_S1_ch18	Adr_mem:1B6B	H	LIA_S2_ch18
Adr_mem:1B2C	L	LIA_S1_ch19	Adr_mem:1B6C	L	LIA_S2_ch19
Adr_mem:1B2D	H	LIA_S1_ch19	Adr_mem:1B6D	H	LIA_S2_ch19
Adr_mem:1B2E	L	LIA_S1_ch20	Adr_mem:1B6E	L	LIA_S2_ch20
Adr_mem:1B2F	H	LIA_S1_ch20	Adr_mem:1B6F	H	LIA_S2_ch20
Adr_mem:1B30	L	LIA_S1_ch21	Adr_mem:1B70	L	LIA_S2_ch21
Adr_mem:1B31	H	LIA_S1_ch21	Adr_mem:1B71	H	LIA_S2_ch21
Adr_mem:1B32	L	LIA_S1_ch22	Adr_mem:1B72	L	LIA_S2_ch22
Adr_mem:1B33	H	LIA_S1_ch22	Adr_mem:1B73	H	LIA_S2_ch22
Adr_mem:1B34	L	LIA_S1_ch23	Adr_mem:1B74	L	LIA_S2_ch23
Adr_mem:1B35	H	LIA_S1_ch23	Adr_mem:1B75	H	LIA_S2_ch23
Adr_mem:1B36	L	LIA_S1_ch24	Adr_mem:1B76	L	LIA_S2_ch24
Adr_mem:1B37	H	LIA_S1_ch24	Adr_mem:1B77	H	LIA_S2_ch24
Adr_mem:1BA0	L	LIA_S3_ch13	Adr_mem:1B80	L	LIA_S3_ch1
Adr_mem:1BA1	H	LIA_S3_ch13	Adr_mem:1B81	H	LIA_S3_ch1
Adr_mem:1BA2	L	LIA_S3_ch14	Adr_mem:1B82	L	LIA_S3_ch2
Adr_mem:1BA3	H	LIA_S3_ch14	Adr_mem:1B83	H	LIA_S3_ch2
Adr_mem:1BA4	L	LIA_S3_ch15	Adr_mem:1B84	L	LIA_S3_ch3
Adr_mem:1BA5	H	LIA_S3_ch15	Adr_mem:1B85	H	LIA_S3_ch3
Adr_mem:1BA6	L	LIA_S3_ch16	Adr_mem:1B86	L	LIA_S3_ch4
Adr_mem:1BA7	H	LIA_S3_ch16	Adr_mem:1B87	H	LIA_S3_ch4
Adr_mem:1BA8	L	LIA_S3_ch17	Adr_mem:1B88	L	LIA_S3_ch5
Adr_mem:1BA9	H	LIA_S3_ch17	Adr_mem:1B89	H	LIA_S3_ch5
Adr_mem:1BAA	L	LIA_S3_ch18	Adr_mem:1B8A	L	LIA_S3_ch6
Adr_mem:1BAB	H	LIA_S3_ch18	Adr_mem:1B8B	H	LIA_S3_ch6
Adr_mem:1BAC	L	LIA_S3_ch19	Adr_mem:1B8C	L	LIA_S3_ch7
Adr_mem:1BAD	H	LIA_S3_ch19	Adr_mem:1B8D	H	LIA_S3_ch7
Adr_mem:1BAE	L	LIA_S3_ch20	Adr_mem:1B8E	L	LIA_S3_ch8
Adr_mem:1BAF	H	LIA_S3_ch20	Adr_mem:1B8F	H	LIA_S3_ch8
Adr_mem:1BB0	L	LIA_S3_ch21	Adr_mem:1B90	L	LIA_S3_ch9
Adr_mem:1BB1	H	LIA_S3_ch21	Adr_mem:1B91	H	LIA_S3_ch9
Adr_mem:1BB2	L	LIA_S3_ch22	Adr_mem:1B92	L	LIA_S3_ch10
Adr_mem:1BB3	H	LIA_S3_ch22	Adr_mem:1B93	H	LIA_S3_ch10
Adr_mem:1BB4	L	LIA_S3_ch23	Adr_mem:1B94	L	LIA_S3_ch11
Adr_mem:1BB5	H	LIA_S3_ch23	Adr_mem:1B95	H	LIA_S3_ch11
Adr_mem:1BB6	L	LIA_S3_ch24	Adr_mem:1B96	L	LIA_S3_ch12
Adr_mem:1BB7	H	LIA_S3_ch24	Adr_mem:1B97	H	LIA_S3_ch12

Data Photometer mapping 1/3					
Adr_mem:1800	L	LIA_P1_ch1	Adr_mem:1840	L	LIA_P2_ch1
Adr_mem:1801	H	LIA_P1_ch1	Adr_mem:1841	H	LIA_P2_ch1
Adr_mem:1802	L	LIA_P1_ch2	Adr_mem:1842	L	LIA_P2_ch2
Adr_mem:1803	H	LIA_P1_ch2	Adr_mem:1843	H	LIA_P2_ch2
Adr_mem:1804	L	LIA_P1_ch3	Adr_mem:1844	L	LIA_P2_ch3
Adr_mem:1805	H	LIA_P1_ch3	Adr_mem:1845	H	LIA_P2_ch3
Adr_mem:1806	L	LIA_P1_ch4	Adr_mem:1846	L	LIA_P2_ch4
Adr_mem:1807	H	LIA_P1_ch4	Adr_mem:1847	H	LIA_P2_ch4
Adr_mem:1808	L	LIA_P1_ch5	Adr_mem:1848	L	LIA_P2_ch5
Adr_mem:1809	H	LIA_P1_ch5	Adr_mem:1849	H	LIA_P2_ch5
Adr_mem:180A	L	LIA_P1_ch6	Adr_mem:184A	L	LIA_P2_ch6
Adr_mem:180B	H	LIA_P1_ch6	Adr_mem:184B	H	LIA_P2_ch6
Adr_mem:180C	L	LIA_P1_ch7	Adr_mem:184C	L	LIA_P2_ch7
Adr_mem:180D	H	LIA_P1_ch7	Adr_mem:184D	H	LIA_P2_ch7
Adr_mem:180E	L	LIA_P1_ch8	Adr_mem:184E	L	LIA_P2_ch8
Adr_mem:180F	H	LIA_P1_ch8	Adr_mem:184F	H	LIA_P2_ch8
Adr_mem:1810	L	LIA_P1_ch9	Adr_mem:1850	L	LIA_P2_ch9
Adr_mem:1811	H	LIA_P1_ch9	Adr_mem:1851	H	LIA_P2_ch9
Adr_mem:1812	L	LIA_P1_ch10	Adr_mem:1852	L	LIA_P2_ch10
Adr_mem:1813	H	LIA_P1_ch10	Adr_mem:1853	H	LIA_P2_ch10
Adr_mem:1814	L	LIA_P1_ch11	Adr_mem:1854	L	LIA_P2_ch11
Adr_mem:1815	H	LIA_P1_ch11	Adr_mem:1855	H	LIA_P2_ch11
Adr_mem:1816	L	LIA_P1_ch12	Adr_mem:1856	L	LIA_P2_ch12
Adr_mem:1817	H	LIA_P1_ch12	Adr_mem:1857	H	LIA_P2_ch12
Adr_mem:1818	L	LIA_P1_ch13	Adr_mem:1858	L	LIA_P2_ch13
Adr_mem:1819	H	LIA_P1_ch13	Adr_mem:1859	H	LIA_P2_ch13
Adr_mem:181A	L	LIA_P1_ch14	Adr_mem:185A	L	LIA_P2_ch14
Adr_mem:181B	H	LIA_P1_ch14	Adr_mem:185B	H	LIA_P2_ch14
Adr_mem:181C	L	LIA_P1_ch15	Adr_mem:185C	L	LIA_P2_ch15
Adr_mem:181D	H	LIA_P1_ch15	Adr_mem:185D	H	LIA_P2_ch15
Adr_mem:181E	L	LIA_P1_ch16	Adr_mem:185E	L	LIA_P2_ch16
Adr_mem:181F	H	LIA_P1_ch16	Adr_mem:185F	H	LIA_P2_ch16
Adr_mem:1820	L	LIA_P1_ch17	Adr_mem:1860	L	LIA_P2_ch17
Adr_mem:1821	H	LIA_P1_ch17	Adr_mem:1861	H	LIA_P2_ch17
Adr_mem:1822	L	LIA_P1_ch18	Adr_mem:1862	L	LIA_P2_ch18
Adr_mem:1823	H	LIA_P1_ch18	Adr_mem:1863	H	LIA_P2_ch18
Adr_mem:1824	L	LIA_P1_ch19	Adr_mem:1864	L	LIA_P2_ch19
Adr_mem:1825	H	LIA_P1_ch19	Adr_mem:1865	H	LIA_P2_ch19
Adr_mem:1826	L	LIA_P1_ch20	Adr_mem:1866	L	LIA_P2_ch20
Adr_mem:1827	H	LIA_P1_ch20	Adr_mem:1867	H	LIA_P2_ch20
Adr_mem:1828	L	LIA_P1_ch21	Adr_mem:1868	L	LIA_P2_ch21
Adr_mem:1829	H	LIA_P1_ch21	Adr_mem:1869	H	LIA_P2_ch21
Adr_mem:182A	L	LIA_P1_ch22	Adr_mem:186A	L	LIA_P2_ch22
Adr_mem:182B	H	LIA_P1_ch22	Adr_mem:186B	H	LIA_P2_ch22
Adr_mem:182C	L	LIA_P1_ch23	Adr_mem:186C	L	LIA_P2_ch23
Adr_mem:182D	H	LIA_P1_ch23	Adr_mem:186D	H	LIA_P2_ch23
Adr_mem:182E	L	LIA_P1_ch24	Adr_mem:186E	L	LIA_P2_ch24
Adr_mem:182F	H	LIA_P1_ch24	Adr_mem:186F	H	LIA_P2_ch24
Adr_mem:1830	L	LIA_P1_ch25	Adr_mem:1870	L	LIA_P2_ch25
Adr_mem:1831	H	LIA_P1_ch25	Adr_mem:1871	H	LIA_P2_ch25
Adr_mem:1832	L	LIA_P1_ch26	Adr_mem:1872	L	LIA_P2_ch26
Adr_mem:1833	H	LIA_P1_ch26	Adr_mem:1873	H	LIA_P2_ch26
Adr_mem:1834	L	LIA_P1_ch27	Adr_mem:1874	L	LIA_P2_ch27
Adr_mem:1835	H	LIA_P1_ch27	Adr_mem:1875	H	LIA_P2_ch27
Adr_mem:1836	L	LIA_P1_ch28	Adr_mem:1876	L	LIA_P2_ch28
Adr_mem:1837	H	LIA_P1_ch28	Adr_mem:1877	H	LIA_P2_ch28
Adr_mem:1838	L	LIA_P1_ch29	Adr_mem:1878	L	LIA_P2_ch29
Adr_mem:1839	H	LIA_P1_ch29	Adr_mem:1879	H	LIA_P2_ch29
Adr_mem:183A	L	LIA_P1_ch30	Adr_mem:187A	L	LIA_P2_ch30
Adr_mem:183B	H	LIA_P1_ch30	Adr_mem:187B	H	LIA_P2_ch30
Adr_mem:183C	L	LIA_P1_ch31	Adr_mem:187C	L	LIA_P2_ch31
Adr_mem:183D	H	LIA_P1_ch31	Adr_mem:187D	H	LIA_P2_ch31
Adr_mem:183E	L	LIA_P1_ch32	Adr_mem:187E	L	LIA_P2_ch32
Adr_mem:183F	H	LIA_P1_ch32	Adr_mem:187F	H	LIA_P2_ch32
Adr_mem:1880	L	LIA_P3_ch1	Adr_mem:1881	H	LIA_P3_ch1
Adr_mem:1882	L	LIA_P3_ch2	Adr_mem:1883	H	LIA_P3_ch2
Adr_mem:1884	L	LIA_P3_ch3	Adr_mem:1885	H	LIA_P3_ch3
Adr_mem:1886	L	LIA_P3_ch4	Adr_mem:1887	H	LIA_P3_ch4
Adr_mem:1888	L	LIA_P3_ch5	Adr_mem:1889	H	LIA_P3_ch5
Adr_mem:188A	L	LIA_P3_ch6	Adr_mem:188B	H	LIA_P3_ch6
Adr_mem:188C	L	LIA_P3_ch7	Adr_mem:188D	H	LIA_P3_ch7
Adr_mem:188E	L	LIA_P3_ch8	Adr_mem:188F	H	LIA_P3_ch8
Adr_mem:1890	L	LIA_P3_ch9	Adr_mem:1891	H	LIA_P3_ch9
Adr_mem:1892	L	LIA_P3_ch10	Adr_mem:1893	H	LIA_P3_ch10
Adr_mem:1894	L	LIA_P3_ch11	Adr_mem:1895	H	LIA_P3_ch11
Adr_mem:1896	L	LIA_P3_ch12	Adr_mem:1897	H	LIA_P3_ch12
Adr_mem:1898	L	LIA_P3_ch13	Adr_mem:1899	H	LIA_P3_ch13
Adr_mem:189A	L	LIA_P3_ch14	Adr_mem:189B	H	LIA_P3_ch14
Adr_mem:189C	L	LIA_P3_ch15	Adr_mem:189D	H	LIA_P3_ch15
Adr_mem:189E	L	LIA_P3_ch16	Adr_mem:189F	H	LIA_P3_ch16
Adr_mem:18A0	L	LIA_P3_ch17	Adr_mem:18A1	H	LIA_P3_ch17
Adr_mem:18A2	L	LIA_P3_ch18	Adr_mem:18A3	H	LIA_P3_ch18
Adr_mem:18A4	L	LIA_P3_ch19	Adr_mem:18A5	H	LIA_P3_ch19
Adr_mem:18A6	L	LIA_P3_ch20	Adr_mem:18A7	H	LIA_P3_ch20
Adr_mem:18A8	L	LIA_P3_ch21	Adr_mem:18A9	H	LIA_P3_ch21
Adr_mem:18AA	L	LIA_P3_ch22	Adr_mem:18AB	H	LIA_P3_ch22
Adr_mem:18AC	L	LIA_P3_ch23	Adr_mem:18AD	H	LIA_P3_ch23
Adr_mem:18AE	L	LIA_P3_ch24	Adr_mem:18AF	H	LIA_P3_ch24
Adr_mem:18B0	L	LIA_P3_ch25	Adr_mem:18B1	H	LIA_P3_ch25
Adr_mem:18B2	L	LIA_P3_ch26	Adr_mem:18B3	H	LIA_P3_ch26
Adr_mem:18B4	L	LIA_P3_ch27	Adr_mem:18B5	H	LIA_P3_ch27
Adr_mem:18B6	L	LIA_P3_ch28	Adr_mem:18B7	H	LIA_P3_ch28
Adr_mem:18B8	L	LIA_P3_ch29	Adr_mem:18B9	H	LIA_P3_ch29
Adr_mem:18BA	L	LIA_P3_ch30	Adr_mem:18BB	H	LIA_P3_ch30
Adr_mem:18BC	L	LIA_P3_ch31	Adr_mem:18BD	H	LIA_P3_ch31
Adr_mem:18BE	L	LIA_P3_ch32	Adr_mem:18BF	H	LIA_P3_ch32

Data Photometer mapping 2/3					
Adr_mem:18C0	L	LIA_P4_ch1	Adr_mem:1900	L	LIA_P5_ch1
Adr_mem:18C1	H	LIA_P4_ch1	Adr_mem:1901	H	LIA_P5_ch1
Adr_mem:18C2	L	LIA_P4_ch2	Adr_mem:1902	L	LIA_P5_ch2
Adr_mem:18C3	H	LIA_P4_ch2	Adr_mem:1903	H	LIA_P5_ch2
Adr_mem:18C4	L	LIA_P4_ch3	Adr_mem:1904	L	LIA_P5_ch3
Adr_mem:18C5	H	LIA_P4_ch3	Adr_mem:1905	H	LIA_P5_ch3
Adr_mem:18C6	L	LIA_P4_ch4	Adr_mem:1906	L	LIA_P5_ch4
Adr_mem:18C7	H	LIA_P4_ch4	Adr_mem:1907	H	LIA_P5_ch4
Adr_mem:18C8	L	LIA_P4_ch5	Adr_mem:1908	L	LIA_P5_ch5
Adr_mem:18C9	H	LIA_P4_ch5	Adr_mem:1909	H	LIA_P5_ch5
Adr_mem:18CA	L	LIA_P4_ch6	Adr_mem:190A	L	LIA_P5_ch6
Adr_mem:18CB	H	LIA_P4_ch6	Adr_mem:190B	H	LIA_P5_ch6
Adr_mem:18CC	L	LIA_P4_ch7	Adr_mem:190C	L	LIA_P5_ch7
Adr_mem:18CD	H	LIA_P4_ch7	Adr_mem:190D	H	LIA_P5_ch7
Adr_mem:18CE	L	LIA_P4_ch8	Adr_mem:190E	L	LIA_P5_ch8
Adr_mem:18CF	H	LIA_P4_ch8	Adr_mem:190F	H	LIA_P5_ch8
Adr_mem:18D0	L	LIA_P4_ch9	Adr_mem:1910	L	LIA_P5_ch9
Adr_mem:18D1	H	LIA_P4_ch9	Adr_mem:1911	H	LIA_P5_ch9
Adr_mem:18D2	L	LIA_P4_ch10	Adr_mem:1912	L	LIA_P5_ch10
Adr_mem:18D3	H	LIA_P4_ch10	Adr_mem:1913	H	LIA_P5_ch10
Adr_mem:18D4	L	LIA_P4_ch11	Adr_mem:1914	L	LIA_P5_ch11
Adr_mem:18D5	H	LIA_P4_ch11	Adr_mem:1915	H	LIA_P5_ch11
Adr_mem:18D6	L	LIA_P4_ch12	Adr_mem:1916	L	LIA_P5_ch12
Adr_mem:18D7	H	LIA_P4_ch12	Adr_mem:1917	H	LIA_P5_ch12
Adr_mem:18D8	L	LIA_P4_ch13	Adr_mem:1918	L	LIA_P5_ch13
Adr_mem:18D9	H	LIA_P4_ch13	Adr_mem:1919	H	LIA_P5_ch13
Adr_mem:18DA	L	LIA_P4_ch14	Adr_mem:191A	L	LIA_P5_ch14
Adr_mem:18DB	H	LIA_P4_ch14	Adr_mem:191B	H	LIA_P5_ch14
Adr_mem:18DC	L	LIA_P4_ch15	Adr_mem:191C	L	LIA_P5_ch15
Adr_mem:18DD	H	LIA_P4_ch15	Adr_mem:191D	H	LIA_P5_ch15
Adr_mem:18DE	L	LIA_P4_ch16	Adr_mem:191E	L	LIA_P5_ch16
Adr_mem:18DF	H	LIA_P4_ch16	Adr_mem:191F	H	LIA_P5_ch16
Adr_mem:18E0	L	LIA_P4_ch17	Adr_mem:1920	L	LIA_P5_ch17
Adr_mem:18E1	H	LIA_P4_ch17	Adr_mem:1921	H	LIA_P5_ch17
Adr_mem:18E2	L	LIA_P4_ch18	Adr_mem:1922	L	LIA_P5_ch18
Adr_mem:18E3	H	LIA_P4_ch18	Adr_mem:1923	H	LIA_P5_ch18
Adr_mem:18E4	L	LIA_P4_ch19	Adr_mem:1924	L	LIA_P5_ch19
Adr_mem:18E5	H	LIA_P4_ch19	Adr_mem:1925	H	LIA_P5_ch19
Adr_mem:18E6	L	LIA_P4_ch20	Adr_mem:1926	L	LIA_P5_ch20
Adr_mem:18E7	H	LIA_P4_ch20	Adr_mem:1927	H	LIA_P5_ch20
Adr_mem:18E8	L	LIA_P4_ch21	Adr_mem:1928	L	LIA_P5_ch21
Adr_mem:18E9	H	LIA_P4_ch21	Adr_mem:1929	H	LIA_P5_ch21
Adr_mem:18EA	L	LIA_P4_ch22	Adr_mem:192A	L	LIA_P5_ch22
Adr_mem:18EB	H	LIA_P4_ch22	Adr_mem:192B	H	LIA_P5_ch22
Adr_mem:18EC	L	LIA_P4_ch23	Adr_mem:192C	L	LIA_P5_ch23
Adr_mem:18ED	H	LIA_P4_ch23	Adr_mem:192D	H	LIA_P5_ch23
Adr_mem:18EE	L	LIA_P4_ch24	Adr_mem:192E	L	LIA_P5_ch24
Adr_mem:18EF	H	LIA_P4_ch24	Adr_mem:192F	H	LIA_P5_ch24
Adr_mem:18F0	L	LIA_P4_ch25	Adr_mem:1930	L	LIA_P5_ch25
Adr_mem:18F1	H	LIA_P4_ch25	Adr_mem:1931	H	LIA_P5_ch25
Adr_mem:18F2	L	LIA_P4_ch26	Adr_mem:1932	L	LIA_P5_ch26
Adr_mem:18F3	H	LIA_P4_ch26	Adr_mem:1933	H	LIA_P5_ch26
Adr_mem:18F4	L	LIA_P4_ch27	Adr_mem:1934	L	LIA_P5_ch27
Adr_mem:18F5	H	LIA_P4_ch27	Adr_mem:1935	H	LIA_P5_ch27
Adr_mem:18F6	L	LIA_P4_ch28	Adr_mem:1936	L	LIA_P5_ch28
Adr_mem:18F7	H	LIA_P4_ch28	Adr_mem:1937	H	LIA_P5_ch28
Adr_mem:18F8	L	LIA_P4_ch29	Adr_mem:1938	L	LIA_P5_ch29
Adr_mem:18F9	H	LIA_P4_ch29	Adr_mem:1939	H	LIA_P5_ch29
Adr_mem:18FA	L	LIA_P4_ch30	Adr_mem:193A	L	LIA_P5_ch30
Adr_mem:18FB	H	LIA_P4_ch30	Adr_mem:193B	H	LIA_P5_ch30
Adr_mem:18FC	L	LIA_P4_ch31	Adr_mem:193C	L	LIA_P5_ch31
Adr_mem:18FD	H	LIA_P4_ch31	Adr_mem:193D	H	LIA_P5_ch31
Adr_mem:18FE	L	LIA_P4_ch32	Adr_mem:193E	L	LIA_P5_ch32
Adr_mem:18FF	H	LIA_P4_ch32	Adr_mem:193F	H	LIA_P5_ch32

Data Photometer mapping 3/3					
Adr_mem:1980	L	LIA_P7_ch1	Adr_mem:19C0	L	LIA_P8_ch1
Adr_mem:1981	H	LIA_P7_ch1	Adr_mem:19C1	H	LIA_P8_ch1
Adr_mem:1982	L	LIA_P7_ch2	Adr_mem:19C2	L	LIA_P8_ch2
Adr_mem:1983	H	LIA_P7_ch2	Adr_mem:19C3	H	LIA_P8_ch2
Adr_mem:1984	L	LIA_P7_ch3	Adr_mem:19C4	L	LIA_P8_ch3
Adr_mem:1985	H	LIA_P7_ch3	Adr_mem:19C5	H	LIA_P8_ch3
Adr_mem:1986	L	LIA_P7_ch4	Adr_mem:19C6	L	LIA_P8_ch4
Adr_mem:1987	H	LIA_P7_ch4	Adr_mem:19C7	H	LIA_P8_ch4
Adr_mem:1988	L	LIA_P7_ch5	Adr_mem:19C8	L	LIA_P8_ch5
Adr_mem:1989	H	LIA_P7_ch5	Adr_mem:19C9	H	LIA_P8_ch5
Adr_mem:198A	L	LIA_P7_ch6	Adr_mem:19CA	L	LIA_P8_ch6
Adr_mem:198B	H	LIA_P7_ch6	Adr_mem:19CB	H	LIA_P8_ch6
Adr_mem:198C	L	LIA_P7_ch7	Adr_mem:19CC	L	LIA_P8_ch7
Adr_mem:198D	H	LIA_P7_ch7	Adr_mem:19CD	H	LIA_P8_ch7
Adr_mem:198E	L	LIA_P7_ch8	Adr_mem:19CE	L	LIA_P8_ch8
Adr_mem:198F	H	LIA_P7_ch8	Adr_mem:19CF	H	LIA_P8_ch8
Adr_mem:1990	L	LIA_P7_ch9	Adr_mem:19D0	L	LIA_P8_ch9
Adr_mem:1991	H	LIA_P7_ch9	Adr_mem:19D1	H	LIA_P8_ch9
Adr_mem:1992	L	LIA_P7_ch10	Adr_mem:19D2	L	LIA_P8_ch10
Adr_mem:1993	H	LIA_P7_ch10	Adr_mem:19D3	H	LIA_P8_ch10
Adr_mem:1994	L	LIA_P7_ch11	Adr_mem:19D4	L	LIA_P8_ch11
Adr_mem:1995	H	LIA_P7_ch11	Adr_mem:19D5	H	LIA_P8_ch11
Adr_mem:1996	L	LIA_P7_ch12	Adr_mem:19D6	L	LIA_P8_ch12
Adr_mem:1997	H	LIA_P7_ch12	Adr_mem:19D7	H	LIA_P8_ch12
Adr_mem:1998	L	LIA_P7_ch13	Adr_mem:19D8	L	LIA_P8_ch13
Adr_mem:1999	H	LIA_P7_ch13	Adr_mem:19D9	H	LIA_P8_ch13
Adr_mem:199A	L	LIA_P7_ch14	Adr_mem:19DA	L	LIA_P8_ch14
Adr_mem:199B	H	LIA_P7_ch14	Adr_mem:19DB	H	LIA_P8_ch14
Adr_mem:199C	L	LIA_P7_ch15	Adr_mem:19DC	L	LIA_P8_ch15
Adr_mem:199D	H	LIA_P7_ch15	Adr_mem:19DD	H	LIA_P8_ch15
Adr_mem:199E	L	LIA_P7_ch16	Adr_mem:19DE	L	LIA_P8_ch16
Adr_mem:199F	H	LIA_P7_ch16	Adr_mem:19DF	H	LIA_P8_ch16
Adr_mem:19A0	L	LIA_P7_ch17	Adr_mem:19E0	L	LIA_P8_ch17
Adr_mem:19A1	H	LIA_P7_ch17	Adr_mem:19E1	H	LIA_P8_ch17
Adr_mem:19A2	L	LIA_P7_ch18	Adr_mem:19E2	L	LIA_P8_ch18
Adr_mem:19A3	H	LIA_P7_ch18	Adr_mem:19E3	H	LIA_P8_ch18
Adr_mem:19A4	L	LIA_P7_ch19	Adr_mem:19E4	L	LIA_P8_ch19
Adr_mem:19A5	H	LIA_P7_ch19	Adr_mem:19E5	H	LIA_P8_ch19
Adr_mem:19A6	L	LIA_P7_ch20	Adr_mem:19E6	L	LIA_P8_ch20
Adr_mem:19A7	H	LIA_P7_ch20	Adr_mem:19E7	H	LIA_P8_ch20
Adr_mem:19A8	L	LIA_P7_ch21	Adr_mem:19E8	L	LIA_P8_ch21
Adr_mem:19A9	H	LIA_P7_ch21	Adr_mem:19E9	H	LIA_P8_ch21
Adr_mem:19AA	L	LIA_P7_ch22	Adr_mem:19EA	L	LIA_P8_ch22
Adr_mem:19AB	H	LIA_P7_ch22	Adr_mem:19EB	H	LIA_P8_ch22
Adr_mem:19AC	L	LIA_P7_ch23	Adr_mem:19EC	L	LIA_P8_ch23
Adr_mem:19AD	H	LIA_P7_ch23	Adr_mem:19ED	H	LIA_P8_ch23
Adr_mem:19AE	L	LIA_P7_ch24	Adr_mem:19EE	L	LIA_P8_ch24
Adr_mem:19AF	H	LIA_P7_ch24	Adr_mem:19EF	H	LIA_P8_ch24
Adr_mem:19B0	L	LIA_P7_ch25	Adr_mem:19F0	L	LIA_P8_ch25
Adr_mem:19B1	H	LIA_P7_ch25	Adr_mem:19F1	H	LIA_P8_ch25
Adr_mem:19B2	L	LIA_P7_ch26	Adr_mem:19F2	L	LIA_P8_ch26
Adr_mem:19B3	H	LIA_P7_ch26	Adr_mem:19F3	H	LIA_P8_ch26
Adr_mem:19B4	L	LIA_P7_ch27	Adr_mem:19F4	L	LIA_P8_ch27
Adr_mem:19B5	H	LIA_P7_ch27	Adr_mem:19F5	H	LIA_P8_ch27
Adr_mem:19B6	L	LIA_P7_ch28	Adr_mem:19F6	L	LIA_P8_ch28
Adr_mem:19B7	H	LIA_P7_ch28	Adr_mem:19F7	H	LIA_P8_ch28
Adr_mem:19B8	L	LIA_P7_ch29	Adr_mem:19F8	L	LIA_P8_ch29
Adr_mem:19B9	H	LIA_P7_ch29	Adr_mem:19F9	H	LIA_P8_ch29
Adr_mem:19BA	L	LIA_P7_ch30	Adr_mem:19FA	L	LIA_P8_ch30
Adr_mem:19BB	H	LIA_P7_ch30	Adr_mem:19FB	H	LIA_P8_ch30
Adr_mem:19BC	L	LIA_P7_ch31	Adr_mem:19FC	L	LIA_P8_ch31
Adr_mem:19BD	H	LIA_P7_ch31	Adr_mem:19FD	H	LIA_P8_ch31
Adr_mem:19BE	L	LIA_P7_ch32	Adr_mem:19FE	L	LIA_P8_ch32
Adr_mem:19BF	H	LIA_P7_ch32	Adr_mem:19FF	H	LIA_P8_ch32
Adr_mem:1A00	L	LIA_P9_ch1	Adr_mem:1A01	H	LIA_P9_ch1
Adr_mem:1A02	L	LIA_P9_ch2	Adr_mem:1A03	H	LIA_P9_ch2
Adr_mem:1A04	L	LIA_P9_ch3	Adr_mem:1A05	H	LIA_P9_ch3
Adr_mem:1A06	L	LIA_P9_ch4	Adr_mem:1A07	H	LIA_P9_ch4
Adr_mem:1A08	L	LIA_P9_ch5	Adr_mem:1A09	H	LIA_P9_ch5
Adr_mem:1A0A	L	LIA_P9_ch6	Adr_mem:1A0B	H	LIA_P9_ch6
Adr_mem:1A0C	L	LIA_P9_ch7	Adr_mem:1A0D	H	LIA_P9_ch7
Adr_mem:1A0E	L	LIA_P9_ch8	Adr_mem:1A0F	H	LIA_P9_ch8
Adr_mem:1A10	L	LIA_P9_ch9	Adr_mem:1A11	H	LIA_P9_ch9
Adr_mem:1A12	L	LIA_P9_ch10	Adr_mem:1A13	H	LIA_P9_ch10
Adr_mem:1A14	L	LIA_P9_ch11	Adr_mem:1A15	H	LIA_P9_ch11
Adr_mem:1A16	L	LIA_P9_ch12	Adr_mem:1A17	H	LIA_P9_ch12
Adr_mem:1A18	L	LIA_P9_ch13	Adr_mem:1A19	H	LIA_P9_ch13
Adr_mem:1A1A	L	LIA_P9_ch14	Adr_mem:1A1B	H	LIA_P9_ch14
Adr_mem:1A1C	L	LIA_P9_ch15	Adr_mem:1A1D	H	LIA_P9_ch15
Adr_mem:1A1E	L	LIA_P9_ch16	Adr_mem:1A1F	H	LIA_P9_ch16
Adr_mem:1A20	L	LIA_P9_ch17	Adr_mem:1A21	H	LIA_P9_ch17
Adr_mem:1A22	L	LIA_P9_ch18	Adr_mem:1A23	H	LIA_P9_ch18
Adr_mem:1A24	L	LIA_P9_ch19	Adr_mem:1A25	H	LIA_P9_ch19
Adr_mem:1A26	L	LIA_P9_ch20	Adr_mem:1A27	H	LIA_P9_ch20
Adr_mem:1A28	L	LIA_P9_ch21	Adr_mem:1A29	H	LIA_P9_ch21
Adr_mem:1A2A	L	LIA_P9_ch22	Adr_mem:1A2B	H	LIA_P9_ch22
Adr_mem:1A2C	L	LIA_P9_ch23	Adr_mem:1A2D	H	LIA_P9_ch23
Adr_mem:1A2E	L	LIA_P9_ch24	Adr_mem:1A2F	H	LIA_P9_ch24
Adr_mem:1A30	L	LIA_P9_ch25	Adr_mem:1A31	H	LIA_P9_ch25
Adr_mem:1A32	L	LIA_P9_ch26	Adr_mem:1A33	H	LIA_P9_ch26
Adr_mem:1A34	L	LIA_P9_ch27	Adr_mem:1A35	H	LIA_P9_ch27
Adr_mem:1A36	L	LIA_P9_ch28	Adr_mem:1A37	H	LIA_P9_ch28
Adr_mem:1A38	L	LIA_P9_ch29	Adr_mem:1A39	H	LIA_P9_ch29
Adr_mem:1A3A	L	LIA_P9_ch30	Adr_mem:1A3B	H	LIA_P9_ch30
Adr_mem:1A3C	L	LIA_P9_ch31	Adr_mem:1A3D	H	LIA_P9_ch31
Adr_mem:1A3E	L	LIA_P9_ch32	Adr_mem:1A3F	H	LIA_P9_ch32

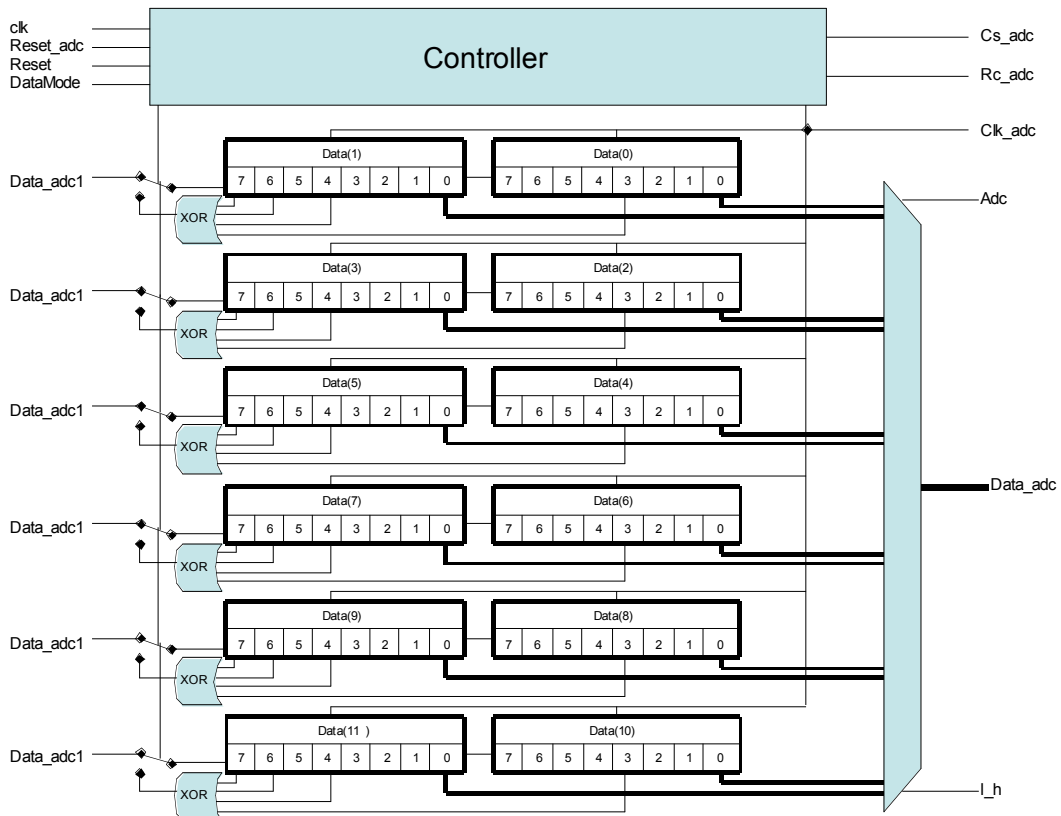
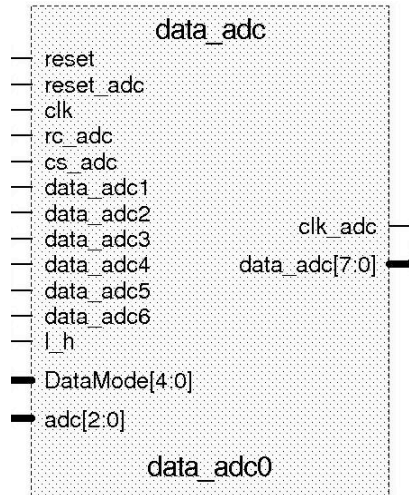
Offset Photometer mapping 1/2					
Adr_mem:0800	LIA_P1_ch1	Adr_mem:08C0	LIA_P4_ch1	Adr_mem:0980	LIA_P7_ch1
Adr_mem:0802	LIA_P1_ch2	Adr_mem:08C2	LIA_P4_ch2	Adr_mem:0982	LIA_P7_ch2
Adr_mem:0804	LIA_P1_ch3	Adr_mem:08C4	LIA_P4_ch3	Adr_mem:0984	LIA_P7_ch3
Adr_mem:0806	LIA_P1_ch4	Adr_mem:08C6	LIA_P4_ch4	Adr_mem:0986	LIA_P7_ch4
Adr_mem:0808	LIA_P1_ch5	Adr_mem:08C8	LIA_P4_ch5	Adr_mem:0988	LIA_P7_ch5
Adr_mem:080A	LIA_P1_ch6	Adr_mem:08CA	LIA_P4_ch6	Adr_mem:098A	LIA_P7_ch6
Adr_mem:080C	LIA_P1_ch7	Adr_mem:08CC	LIA_P4_ch7	Adr_mem:098C	LIA_P7_ch7
Adr_mem:080E	LIA_P1_ch8	Adr_mem:08CE	LIA_P4_ch8	Adr_mem:098E	LIA_P7_ch8
Adr_mem:0810	LIA_P1_ch9	Adr_mem:08D0	LIA_P4_ch9	Adr_mem:0990	LIA_P7_ch9
Adr_mem:0812	LIA_P1_ch10	Adr_mem:08D2	LIA_P4_ch10	Adr_mem:0992	LIA_P7_ch10
Adr_mem:0814	LIA_P1_ch11	Adr_mem:08D4	LIA_P4_ch11	Adr_mem:0994	LIA_P7_ch11
Adr_mem:0816	LIA_P1_ch12	Adr_mem:08D6	LIA_P4_ch12	Adr_mem:0996	LIA_P7_ch12
Adr_mem:0818	LIA_P1_ch13	Adr_mem:08D8	LIA_P4_ch13	Adr_mem:0998	LIA_P7_ch13
Adr_mem:081A	LIA_P1_ch14	Adr_mem:08DA	LIA_P4_ch14	Adr_mem:099A	LIA_P7_ch14
Adr_mem:081C	LIA_P1_ch15	Adr_mem:08DC	LIA_P4_ch15	Adr_mem:099C	LIA_P7_ch15
Adr_mem:081E	LIA_P1_ch16	Adr_mem:08DE	LIA_P4_ch16	Adr_mem:099E	LIA_P7_ch16
Adr_mem:0820	LIA_P1_ch17	Adr_mem:08E0	LIA_P4_ch17	Adr_mem:09A0	LIA_P7_ch17
Adr_mem:0822	LIA_P1_ch18	Adr_mem:08E2	LIA_P4_ch18	Adr_mem:09A2	LIA_P7_ch18
Adr_mem:0824	LIA_P1_ch19	Adr_mem:08E4	LIA_P4_ch19	Adr_mem:09A4	LIA_P7_ch19
Adr_mem:0826	LIA_P1_ch20	Adr_mem:08E6	LIA_P4_ch20	Adr_mem:09A6	LIA_P7_ch20
Adr_mem:0828	LIA_P1_ch21	Adr_mem:08E8	LIA_P4_ch21	Adr_mem:09A8	LIA_P7_ch21
Adr_mem:082A	LIA_P1_ch22	Adr_mem:08EA	LIA_P4_ch22	Adr_mem:09AA	LIA_P7_ch22
Adr_mem:082C	LIA_P1_ch23	Adr_mem:08EC	LIA_P4_ch23	Adr_mem:09AC	LIA_P7_ch23
Adr_mem:082E	LIA_P1_ch24	Adr_mem:08EE	LIA_P4_ch24	Adr_mem:09AE	LIA_P7_ch24
Adr_mem:0830	LIA_P1_ch25	Adr_mem:08F0	LIA_P4_ch25	Adr_mem:09B0	LIA_P7_ch25
Adr_mem:0832	LIA_P1_ch26	Adr_mem:08F2	LIA_P4_ch26	Adr_mem:09B2	LIA_P7_ch26
Adr_mem:0834	LIA_P1_ch27	Adr_mem:08F4	LIA_P4_ch27	Adr_mem:09B4	LIA_P7_ch27
Adr_mem:0836	LIA_P1_ch28	Adr_mem:08F6	LIA_P4_ch28	Adr_mem:09B6	LIA_P7_ch28
Adr_mem:0838	LIA_P1_ch29	Adr_mem:08F8	LIA_P4_ch29	Adr_mem:09B8	LIA_P7_ch29
Adr_mem:083A	LIA_P1_ch30	Adr_mem:08FA	LIA_P4_ch30	Adr_mem:09BA	LIA_P7_ch30
Adr_mem:083C	LIA_P1_ch31	Adr_mem:08FC	LIA_P4_ch31	Adr_mem:09BC	LIA_P7_ch31
Adr_mem:083E	LIA_P1_ch32	Adr_mem:08FE	LIA_P4_ch32	Adr_mem:09BE	LIA_P7_ch32
Adr_mem:0840	LIA_P2_ch1	Adr_mem:0900	LIA_P5_ch1	Adr_mem:09C0	LIA_P8_ch1
Adr_mem:0842	LIA_P2_ch2	Adr_mem:0902	LIA_P5_ch2	Adr_mem:09C2	LIA_P8_ch2
Adr_mem:0844	LIA_P2_ch3	Adr_mem:0904	LIA_P5_ch3	Adr_mem:09C4	LIA_P8_ch3
Adr_mem:0846	LIA_P2_ch4	Adr_mem:0906	LIA_P5_ch4	Adr_mem:09C6	LIA_P8_ch4
Adr_mem:0848	LIA_P2_ch5	Adr_mem:0908	LIA_P5_ch5	Adr_mem:09C8	LIA_P8_ch5
Adr_mem:084A	LIA_P2_ch6	Adr_mem:090A	LIA_P5_ch6	Adr_mem:09CA	LIA_P8_ch6
Adr_mem:084C	LIA_P2_ch7	Adr_mem:090C	LIA_P5_ch7	Adr_mem:09CC	LIA_P8_ch7
Adr_mem:084E	LIA_P2_ch8	Adr_mem:090E	LIA_P5_ch8	Adr_mem:09CE	LIA_P8_ch8
Adr_mem:0850	LIA_P2_ch9	Adr_mem:0910	LIA_P5_ch9	Adr_mem:09D0	LIA_P8_ch9
Adr_mem:0852	LIA_P2_ch10	Adr_mem:0912	LIA_P5_ch10	Adr_mem:09D2	LIA_P8_ch10
Adr_mem:0854	LIA_P2_ch11	Adr_mem:0914	LIA_P5_ch11	Adr_mem:09D4	LIA_P8_ch11
Adr_mem:0856	LIA_P2_ch12	Adr_mem:0916	LIA_P5_ch12	Adr_mem:09D6	LIA_P8_ch12
Adr_mem:0858	LIA_P2_ch13	Adr_mem:0918	LIA_P5_ch13	Adr_mem:09D8	LIA_P8_ch13
Adr_mem:085A	LIA_P2_ch14	Adr_mem:091A	LIA_P5_ch14	Adr_mem:09DA	LIA_P8_ch14
Adr_mem:085C	LIA_P2_ch15	Adr_mem:091C	LIA_P5_ch15	Adr_mem:09DC	LIA_P8_ch15
Adr_mem:085E	LIA_P2_ch16	Adr_mem:091E	LIA_P5_ch16	Adr_mem:09DE	LIA_P8_ch16
Adr_mem:0860	LIA_P2_ch17	Adr_mem:0920	LIA_P5_ch17	Adr_mem:09E0	LIA_P8_ch17
Adr_mem:0862	LIA_P2_ch18	Adr_mem:0922	LIA_P5_ch18	Adr_mem:09E2	LIA_P8_ch18
Adr_mem:0864	LIA_P2_ch19	Adr_mem:0924	LIA_P5_ch19	Adr_mem:09E4	LIA_P8_ch19
Adr_mem:0866	LIA_P2_ch20	Adr_mem:0926	LIA_P5_ch20	Adr_mem:09E6	LIA_P8_ch20
Adr_mem:0868	LIA_P2_ch21	Adr_mem:0928	LIA_P5_ch21	Adr_mem:09E8	LIA_P8_ch21
Adr_mem:086A	LIA_P2_ch22	Adr_mem:092A	LIA_P5_ch22	Adr_mem:09EA	LIA_P8_ch22
Adr_mem:086C	LIA_P2_ch23	Adr_mem:092C	LIA_P5_ch23	Adr_mem:09EC	LIA_P8_ch23
Adr_mem:086E	LIA_P2_ch24	Adr_mem:092E	LIA_P5_ch24	Adr_mem:09EE	LIA_P8_ch24
Adr_mem:0870	LIA_P2_ch25	Adr_mem:0930	LIA_P5_ch25	Adr_mem:09F0	LIA_P8_ch25
Adr_mem:0872	LIA_P2_ch26	Adr_mem:0932	LIA_P5_ch26	Adr_mem:09F2	LIA_P8_ch26
Adr_mem:0874	LIA_P2_ch27	Adr_mem:0934	LIA_P5_ch27	Adr_mem:09F4	LIA_P8_ch27
Adr_mem:0876	LIA_P2_ch28	Adr_mem:0936	LIA_P5_ch28	Adr_mem:09F6	LIA_P8_ch28
Adr_mem:0878	LIA_P2_ch29	Adr_mem:0938	LIA_P5_ch29	Adr_mem:09F8	LIA_P8_ch29
Adr_mem:087A	LIA_P2_ch30	Adr_mem:093A	LIA_P5_ch30	Adr_mem:09FA	LIA_P8_ch30
Adr_mem:087C	LIA_P2_ch31	Adr_mem:093C	LIA_P5_ch31	Adr_mem:09FC	LIA_P8_ch31
Adr_mem:087E	LIA_P2_ch32	Adr_mem:093E	LIA_P5_ch32	Adr_mem:09FE	LIA_P8_ch32

Offset Photometer mapping 2/2					
Adr_mem:0880	LIA_P3_ch1	Adr_mem:0940	LIA_P6_ch1	Adr_mem:0A00	LIA_P9_ch1
Adr_mem:0882	LIA_P3_ch2	Adr_mem:0942	LIA_P6_ch2	Adr_mem:0A02	LIA_P9_ch2
Adr_mem:0884	LIA_P3_ch3	Adr_mem:0944	LIA_P6_ch3	Adr_mem:0A04	LIA_P9_ch3
Adr_mem:0886	LIA_P3_ch4	Adr_mem:0946	LIA_P6_ch4	Adr_mem:0A06	LIA_P9_ch4
Adr_mem:0888	LIA_P3_ch5	Adr_mem:0948	LIA_P6_ch5	Adr_mem:0A08	LIA_P9_ch5
Adr_mem:088A	LIA_P3_ch6	Adr_mem:094A	LIA_P6_ch6	Adr_mem:0A0A	LIA_P9_ch6
Adr_mem:088C	LIA_P3_ch7	Adr_mem:094C	LIA_P6_ch7	Adr_mem:0A0C	LIA_P9_ch7
Adr_mem:088E	LIA_P3_ch8	Adr_mem:094E	LIA_P6_ch8	Adr_mem:0A0E	LIA_P9_ch8
Adr_mem:0890	LIA_P3_ch9	Adr_mem:0950	LIA_P6_ch9	Adr_mem:0A10	LIA_P9_ch9
Adr_mem:0892	LIA_P3_ch10	Adr_mem:0952	LIA_P6_ch10	Adr_mem:0A12	LIA_P9_ch10
Adr_mem:0894	LIA_P3_ch11	Adr_mem:0954	LIA_P6_ch11	Adr_mem:0A14	LIA_P9_ch11
Adr_mem:0896	LIA_P3_ch12	Adr_mem:0956	LIA_P6_ch12	Adr_mem:0A16	LIA_P9_ch12
Adr_mem:0898	LIA_P3_ch13	Adr_mem:0958	LIA_P6_ch13	Adr_mem:0A18	LIA_P9_ch13
Adr_mem:089A	LIA_P3_ch14	Adr_mem:095A	LIA_P6_ch14	Adr_mem:0A1A	LIA_P9_ch14
Adr_mem:089C	LIA_P3_ch15	Adr_mem:095C	LIA_P6_ch15	Adr_mem:0A1C	LIA_P9_ch15
Adr_mem:089E	LIA_P3_ch16	Adr_mem:095E	LIA_P6_ch16	Adr_mem:0A1E	LIA_P9_ch16
Adr_mem:08A0	LIA_P3_ch17	Adr_mem:0960	LIA_P6_ch17	Adr_mem:0A20	LIA_P9_ch17
Adr_mem:08A2	LIA_P3_ch18	Adr_mem:0962	LIA_P6_ch18	Adr_mem:0A22	LIA_P9_ch18
Adr_mem:08A4	LIA_P3_ch19	Adr_mem:0964	LIA_P6_ch19	Adr_mem:0A24	LIA_P9_ch19
Adr_mem:08A6	LIA_P3_ch20	Adr_mem:0966	LIA_P6_ch20	Adr_mem:0A26	LIA_P9_ch20
Adr_mem:08A8	LIA_P3_ch21	Adr_mem:0968	LIA_P6_ch21	Adr_mem:0A28	LIA_P9_ch21
Adr_mem:08AA	LIA_P3_ch22	Adr_mem:096A	LIA_P6_ch22	Adr_mem:0A2A	LIA_P9_ch22
Adr_mem:08AC	LIA_P3_ch23	Adr_mem:096C	LIA_P6_ch23	Adr_mem:0A2C	LIA_P9_ch23
Adr_mem:08AE	LIA_P3_ch24	Adr_mem:096E	LIA_P6_ch24	Adr_mem:0A2E	LIA_P9_ch24
Adr_mem:08B0	LIA_P3_ch25	Adr_mem:0970	LIA_P6_ch25	Adr_mem:0A30	LIA_P9_ch25
Adr_mem:08B2	LIA_P3_ch26	Adr_mem:0972	LIA_P6_ch26	Adr_mem:0A32	LIA_P9_ch26
Adr_mem:08B4	LIA_P3_ch27	Adr_mem:0974	LIA_P6_ch27	Adr_mem:0A34	LIA_P9_ch27
Adr_mem:08B6	LIA_P3_ch28	Adr_mem:0976	LIA_P6_ch28	Adr_mem:0A36	LIA_P9_ch28
Adr_mem:08B8	LIA_P3_ch29	Adr_mem:0978	LIA_P6_ch29	Adr_mem:0A38	LIA_P9_ch29
Adr_mem:08BA	LIA_P3_ch30	Adr_mem:097A	LIA_P6_ch30	Adr_mem:0A3A	LIA_P9_ch30
Adr_mem:08BC	LIA_P3_ch31	Adr_mem:097C	LIA_P6_ch31	Adr_mem:0A3C	LIA_P9_ch31
Adr_mem:08BE	LIA_P3_ch32	Adr_mem:097E	LIA_P6_ch32	Adr_mem:0A3E	LIA_P9_ch32

Offset Spectrometer mapping					
Adr_mem:0B00	LIA_S1_ch1	Adr_mem:0B40	LIA_S2_ch1	Adr_mem:0B80	LIA_S3_ch1
Adr_mem:0B02	LIA_S1_ch2	Adr_mem:0B42	LIA_S2_ch2	Adr_mem:0B82	LIA_S3_ch2
Adr_mem:0B04	LIA_S1_ch3	Adr_mem:0B44	LIA_S2_ch3	Adr_mem:0B84	LIA_S3_ch3
Adr_mem:0B06	LIA_S1_ch4	Adr_mem:0B46	LIA_S2_ch4	Adr_mem:0B86	LIA_S3_ch4
Adr_mem:0B08	LIA_S1_ch5	Adr_mem:0B48	LIA_S2_ch5	Adr_mem:0B88	LIA_S3_ch5
Adr_mem:0B0A	LIA_S1_ch6	Adr_mem:0B4A	LIA_S2_ch6	Adr_mem:0B8A	LIA_S3_ch6
Adr_mem:0B0C	LIA_S1_ch7	Adr_mem:0B4C	LIA_S2_ch7	Adr_mem:0B8C	LIA_S3_ch7
Adr_mem:0B0E	LIA_S1_ch8	Adr_mem:0B4E	LIA_S2_ch8	Adr_mem:0B8E	LIA_S3_ch8
Adr_mem:0B10	LIA_S1_ch9	Adr_mem:0B50	LIA_S2_ch9	Adr_mem:0B90	LIA_S3_ch9
Adr_mem:0B12	LIA_S1_ch10	Adr_mem:0B52	LIA_S2_ch10	Adr_mem:0B92	LIA_S3_ch10
Adr_mem:0B14	LIA_S1_ch11	Adr_mem:0B54	LIA_S2_ch11	Adr_mem:0B94	LIA_S3_ch11
Adr_mem:0B16	LIA_S1_ch12	Adr_mem:0B56	LIA_S2_ch12	Adr_mem:0B96	LIA_S3_ch12
Adr_mem:0B20	LIA_S1_ch13	Adr_mem:0B60	LIA_S2_ch13	Adr_mem:0BA0	LIA_S3_ch13
Adr_mem:0B22	LIA_S1_ch14	Adr_mem:0B62	LIA_S2_ch14	Adr_mem:0BA2	LIA_S3_ch14
Adr_mem:0B24	LIA_S1_ch15	Adr_mem:0B64	LIA_S2_ch15	Adr_mem:0BA4	LIA_S3_ch15
Adr_mem:0B26	LIA_S1_ch16	Adr_mem:0B66	LIA_S2_ch16	Adr_mem:0BA6	LIA_S3_ch16
Adr_mem:0B28	LIA_S1_ch17	Adr_mem:0B68	LIA_S2_ch17	Adr_mem:0BA8	LIA_S3_ch17
Adr_mem:0B2A	LIA_S1_ch18	Adr_mem:0B6A	LIA_S2_ch18	Adr_mem:0BAA	LIA_S3_ch18
Adr_mem:0B2C	LIA_S1_ch19	Adr_mem:0B6C	LIA_S2_ch19	Adr_mem:0BAC	LIA_S3_ch19
Adr_mem:0B2E	LIA_S1_ch20	Adr_mem:0B6E	LIA_S2_ch20	Adr_mem:0BAE	LIA_S3_ch20
Adr_mem:0B30	LIA_S1_ch21	Adr_mem:0B70	LIA_S2_ch21	Adr_mem:0BB0	LIA_S3_ch21
Adr_mem:0B32	LIA_S1_ch22	Adr_mem:0B72	LIA_S2_ch22	Adr_mem:0BB2	LIA_S3_ch22
Adr_mem:0B34	LIA_S1_ch23	Adr_mem:0B74	LIA_S2_ch23	Adr_mem:0BB4	LIA_S3_ch23
Adr_mem:0B36	LIA_S1_ch24	Adr_mem:0B76	LIA_S2_ch24	Adr_mem:0BB6	LIA_S3_ch24

3.9.3.7.3 Channel Acquisition

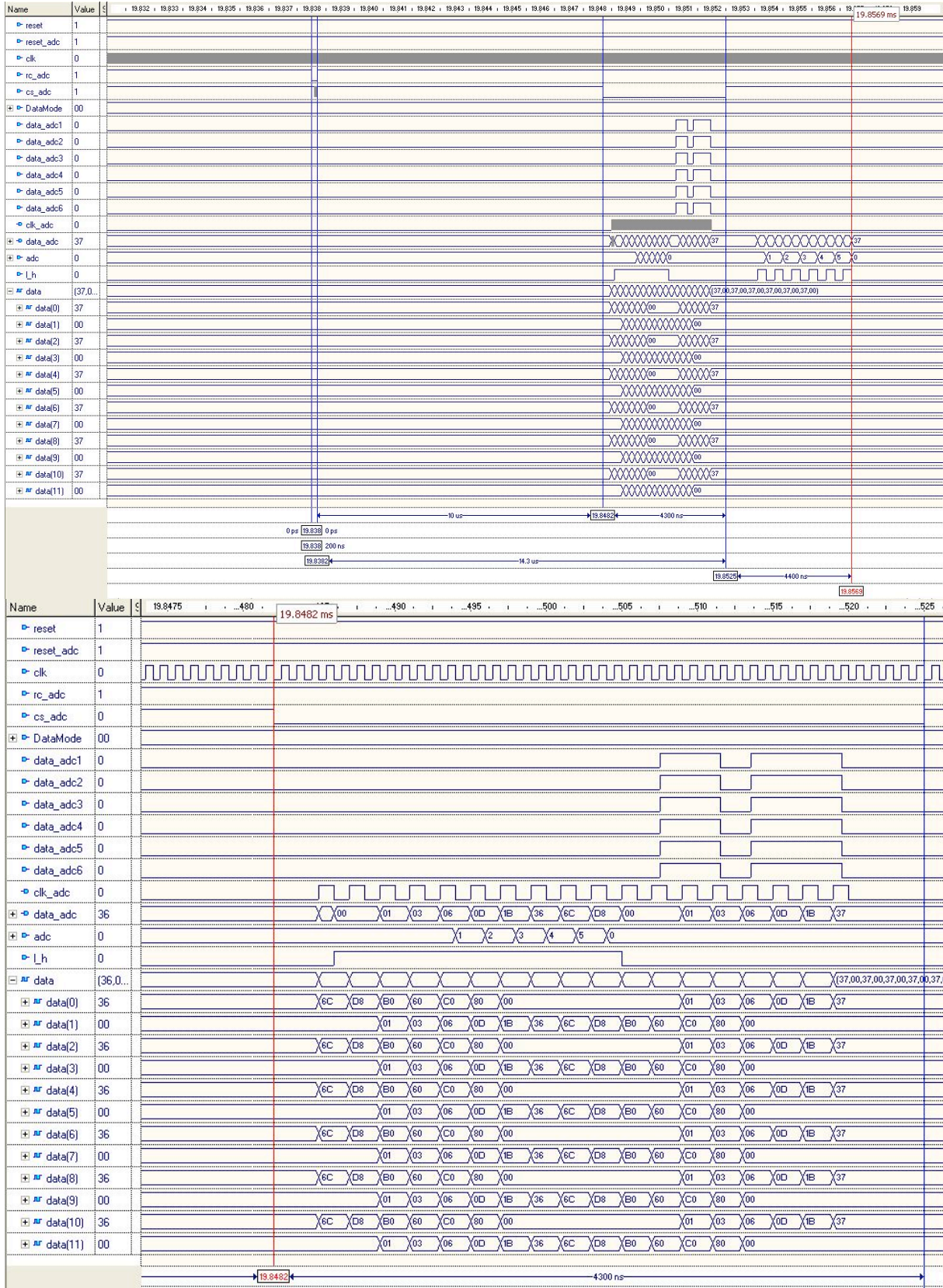
(VHDL module: Data_adc.vhd)



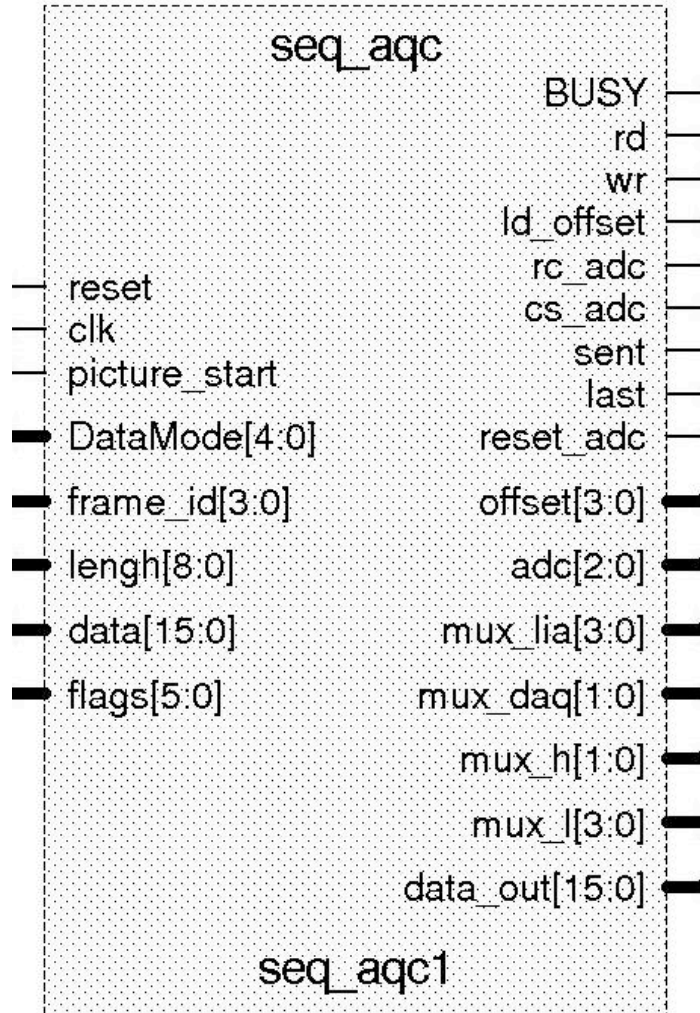
REGISTER RESET POSITION:

DATA(0)=01x; DATA(1)=02x; DATA(2)=03x; DATA(3)=04x; DATA(4)=05x; DATA(5)=06x
DATA(6)=0Fx; DATA(7)=10x; DATA(8)=11x; DATA(9)=12x; DATA(10)=13x; DATA(11)=14x

Timing of a data acquisition:



3.9.3.7.4 Mode sequence
(VHDL module: Data_adc.vhd)



The following tables shows the chronological sequence of the picture acquisition modes:

- The indicated times show when the digitization occurs. These times are given with reference to the frame timestamp of the picture acquisition.
- The six ADCs work in parallel.

Spectrometer modes:

Channels						Time:Relative to timestamps			Delta times	acquisition time
SSW			SLW			full spectromete r	SSW	SLW		
LIA S1 ch1	LIA S1 ch13	LIA S2 ch1	LIA S2 ch13	LIA S3 ch1	LIA S3 ch13	-1729,6 μs	-1547,2 μs	-1364,8 μs		
LIA S1 ch3	LIA S1 ch15	LIA S2 ch3	LIA S2 ch15	LIA S3 ch3	LIA S3 ch15	-1625,7 μs	-1443,3 μs	-1260,9 μs	103,9 μs	
LIA S1 ch5	LIA S1 ch17	LIA S2 ch5	LIA S2 ch17	LIA S3 ch5	LIA S3 ch17	-1521,8 μs	-1339,4 μs	-1157 μs	103,9 μs	
LIA S1 ch7	LIA S1 ch19	LIA S2 ch7	LIA S2 ch19	LIA S3 ch7	LIA S3 ch19	-1417,9 μs	-1235,5 μs	-1053,1 μs	103,9 μs	
LIA S1 ch9	LIA S1 ch21	LIA S2 ch9	LIA S2 ch21	LIA S3 ch9	LIA S3 ch21	-1314 μs	-1131,6 μs	-949,2 μs	103,9 μs	
LIA S1 ch11	LIA S1 ch23	LIA S2 ch11	LIA S2 ch23	LIA S3 ch11	LIA S3 ch23	-1210,1 μs	-1027,7 μs	-845,3 μs	103,9 μs	
LIA S1 ch2	LIA S1 ch14	LIA S2 ch2	LIA S2 ch14	LIA S3 ch2	LIA S3 ch14	-1106,2 μs	-923,8 μs	-741,4 μs	103,9 μs	
LIA S1 ch4	LIA S1 ch16	LIA S2 ch4	LIA S2 ch16	LIA S3 ch4	LIA S3 ch16	-1002,3 μs	-819,9 μs	-637,5 μs	103,9 μs	
LIA S1 ch6	LIA S1 ch18	LIA S2 ch6	LIA S2 ch18	LIA S3 ch6	LIA S3 ch18	-898,4 μs	-716 μs	-533,6 μs	103,9 μs	
LIA S1 ch8	LIA S1 ch20	LIA S2 ch8	LIA S2 ch20	LIA S3 ch8	LIA S3 ch20	-794,5 μs	-612,1 μs	-429,7 μs	103,9 μs	
LIA S1 ch10	LIA S1 ch22	LIA S2 ch10	LIA S2 ch22	LIA S3 ch10	LIA S3 ch22	-690,6 μs	-508,2 μs	-325,8 μs	103,9 μs	
LIA S1 ch12	LIA S1 ch24	LIA S2 ch12	LIA S2 ch24	LIA S3 ch12	LIA S3 ch24	-586,7 μs	-404,3 μs	-221,9 μs	103,9 μs	

1142,9μs

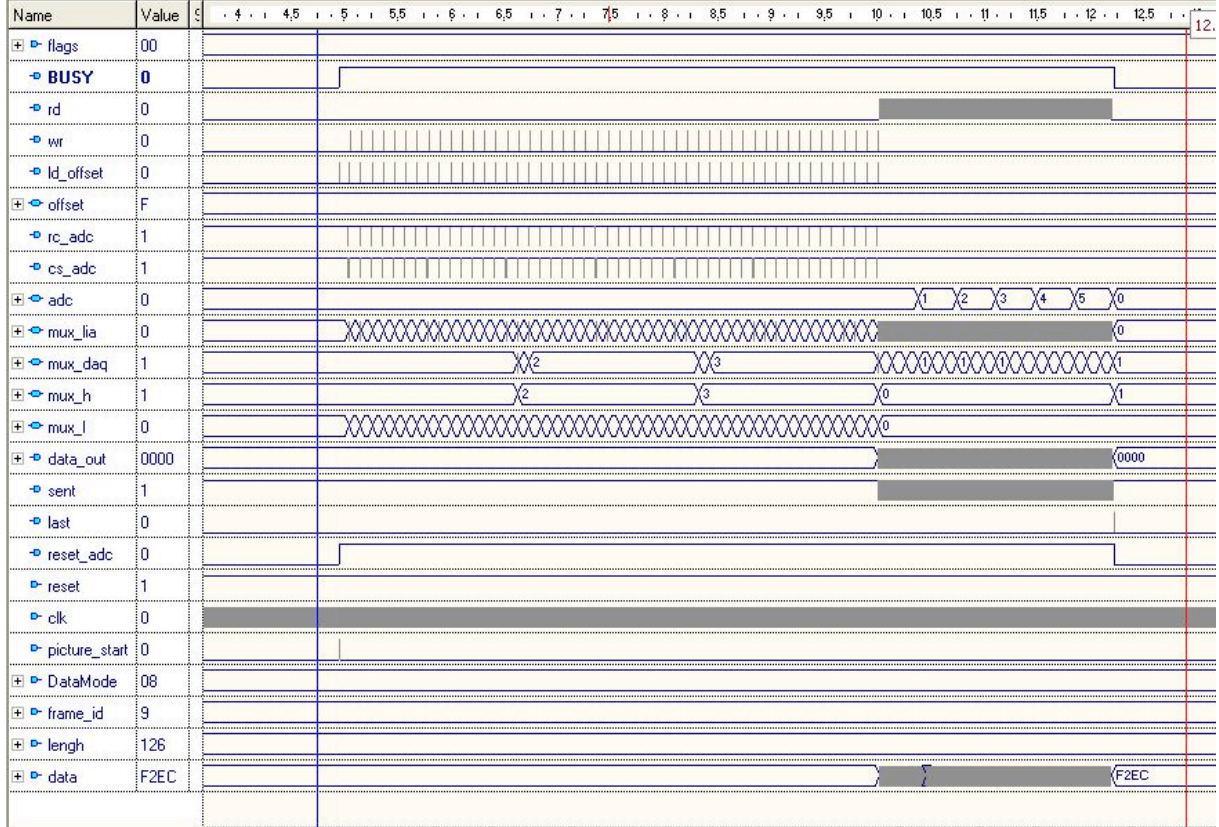
Photometer mode:

Channels						time:Relative to timestamps				Delta times	Acquisition time
PSW		PLW		PMW		full photometer	PSW	PMW	PLW		
LIA_P1_ch1	LIA_P2_ch17	LIA_P4_ch1	LIA_P5_ch17	LIA_P7_ch1	LIA_P8_ch17	-7111,6μs	-6017,2μs	-5652,4μs	-5287,6μs		
LIA_P1_ch3	LIA_P2_ch19	LIA_P4_ch3	LIA_P5_ch19	LIA_P7_ch3	LIA_P8_ch19	-7007,7μs	-5913,3μs	-5548,5μs	-5183,7μs	103,9μs	
LIA_P1_ch5	LIA_P2_ch21	LIA_P4_ch5	LIA_P5_ch21	LIA_P7_ch5	LIA_P8_ch21	-6903,8μs	-5809,4μs	-5444,6μs	-5079,8μs	103,9μs	
LIA_P1_ch7	LIA_P2_ch23	LIA_P4_ch7	LIA_P5_ch23	LIA_P7_ch7	LIA_P8_ch23	-6799,9μs	-5705,5μs	-5340,7μs	-4975,9μs	103,9μs	
LIA_P1_ch9	LIA_P2_ch25	LIA_P4_ch9	LIA_P5_ch25	LIA_P7_ch9	LIA_P8_ch25	-6696μs	-5601,6μs	-5236,8μs	-4872 μs	103,9μs	
LIA_P1_ch11	LIA_P2_ch27	LIA_P4_ch11	LIA_P5_ch27	LIA_P7_ch11	LIA_P8_ch27	-6592,1μs	-5497,7μs	-5132,9μs	-4768,1μs	103,9μs	
LIA_P1_ch13	LIA_P2_ch29	LIA_P4_ch13	LIA_P5_ch29	LIA_P7_ch13	LIA_P8_ch29	-6488,2μs	-5393,8μs	-5029μs	-4664,2μs	103,9μs	
LIA_P1_ch15	LIA_P2_ch31	LIA_P4_ch15	LIA_P5_ch31	LIA_P7_ch15	LIA_P8_ch31	-6384,3μs	-5289,9μs	-4925,1μs	-4560,3μs	103,9μs	
LIA_P1_ch2	LIA_P2_ch18	LIA_P4_ch2	LIA_P5_ch18	LIA_P7_ch2	LIA_P8_ch18	-6280,4μs	-5186μs	-4821,2μs	-4456,4μs	103,9μs	
LIA_P1_ch4	LIA_P2_ch20	LIA_P4_ch4	LIA_P5_ch20	LIA_P7_ch4	LIA_P8_ch20	-6176,5μs	-5082,1μs	-4717,3μs	-4352,5μs	103,9μs	
LIA_P1_ch6	LIA_P2_ch22	LIA_P4_ch6	LIA_P5_ch22	LIA_P7_ch6	LIA_P8_ch22	-6072,6μs	-4978,2μs	-4613,4μs	-4248,6μs	103,9μs	
LIA_P1_ch8	LIA_P2_ch24	LIA_P4_ch8	LIA_P5_ch24	LIA_P7_ch8	LIA_P8_ch24	-5968,7μs	-4874,3μs	-4509,5μs	-4144,7μs	103,9μs	
LIA_P1_ch10	LIA_P2_ch26	LIA_P4_ch10	LIA_P5_ch26	LIA_P7_ch10	LIA_P8_ch26	-5864,8μs	-4770,4μs	-4405,6μs	-4040,8μs	103,9μs	
LIA_P1_ch12	LIA_P2_ch28	LIA_P4_ch12	LIA_P5_ch28	LIA_P7_ch12	LIA_P8_ch28	-5760,9μs	-4666,5μs	-4301,7μs	-3936,9μs	103,9μs	
LIA_P1_ch14	LIA_P2_ch30	LIA_P4_ch14	LIA_P5_ch30	LIA_P7_ch14	LIA_P8_ch30	-5657μs	-4562,6μs	-4197,8μs	-3833μs	103,9μs	
LIA_P1_ch16	LIA_P2_ch32	LIA_P4_ch16	LIA_P5_ch32	LIA_P7_ch16	LIA_P8_ch32	-5553,1μs	-4458,7μs	-4093,9μs	-3729,1μs	103,9μs	
LIA_P1_ch17	LIA_P3_ch1	LIA_P4_ch17	LIA_P6_ch1	LIA_P7_ch17	LIA_P9_ch1	-5449,2μs	-4354,8μs	-3990μs	-3625,2μs	103,9μs	
LIA_P1_ch19	LIA_P3_ch3	LIA_P4_ch19	LIA_P6_ch3	LIA_P7_ch19	LIA_P9_ch3	-5345,3μs	-4250,9μs	-3886,1μs	-3521,3μs	103,9μs	
LIA_P1_ch21	LIA_P3_ch5	LIA_P4_ch21	LIA_P6_ch5	LIA_P7_ch21	LIA_P9_ch5	-5241,4μs	-4147μs	-3782,2μs	-3417,4μs	103,9μs	
LIA_P1_ch23	LIA_P3_ch7	LIA_P4_ch23	LIA_P6_ch7	LIA_P7_ch23	LIA_P9_ch7	-5137,5μs	-4043,1μs	-3678,3μs	-3313,5μs	103,9μs	
LIA_P1_ch25	LIA_P3_ch9	LIA_P4_ch25	LIA_P6_ch9	LIA_P7_ch25	LIA_P9_ch9	-5033,6μs	-3939,2μs	-3574,4μs	-3209,6μs	103,9μs	
LIA_P1_ch27	LIA_P3_ch11	LIA_P4_ch27	LIA_P6_ch11	LIA_P7_ch27	LIA_P9_ch11	-4929,7μs	-3835,3μs	-3470,5μs	-3105,7μs	103,9μs	
LIA_P1_ch29	LIA_P3_ch13	LIA_P4_ch29	LIA_P6_ch13	LIA_P7_ch29	LIA_P9_ch13	-4825,8μs	-3731,4μs	-3366,6μs	-3001,8μs	103,9μs	
LIA_P1_ch31	LIA_P3_ch15	LIA_P4_ch31	LIA_P6_ch15	LIA_P7_ch31	LIA_P9_ch15	-4721,9μs	-3627,5μs	-3262,7μs	-2897,9μs	103,9μs	
LIA_P1_ch18	LIA_P3_ch2	LIA_P4_ch18	LIA_P6_ch2	LIA_P7_ch18	LIA_P9_ch2	-4618μs	-3523,6μs	-3158,8μs	-2794μs	103,9μs	
LIA_P1_ch20	LIA_P3_ch4	LIA_P4_ch20	LIA_P6_ch4	LIA_P7_ch20	LIA_P9_ch4	-4514,1μs	-3419,7μs	-3054,9μs	-2690,1μs	103,9μs	
LIA_P1_ch22	LIA_P3_ch6	LIA_P4_ch22	LIA_P6_ch6	LIA_P7_ch22	LIA_P9_ch6	-4410,2μs	-3315,8μs	-2951μs	-2586,2μs	103,9μs	
LIA_P1_ch24	LIA_P3_ch8	LIA_P4_ch24	LIA_P6_ch8	LIA_P7_ch24	LIA_P9_ch8	-4306,3μs	-3211,9μs	-2847,1μs	-2482,3μs	103,9μs	
LIA_P1_ch26	LIA_P3_ch10	LIA_P4_ch26	LIA_P6_ch10	LIA_P7_ch26	LIA_P9_ch10	-4202,4μs	-3108μs	-2743,2μs	-2378,4μs	103,9μs	
LIA_P1_ch28	LIA_P3_ch12	LIA_P4_ch28	LIA_P6_ch12	LIA_P7_ch28	LIA_P9_ch12	-4098,5μs	-3004,1μs	-2639,3μs	-2274,5μs	103,9μs	
LIA_P1_ch30	LIA_P3_ch14	LIA_P4_ch30	LIA_P6_ch14	LIA_P7_ch30	LIA_P9_ch14	-3994,6μs	-2900,2μs	-2535,4μs	-2170,6μs	103,9μs	
LIA_P1_ch32	LIA_P3_ch16	LIA_P4_ch32	LIA_P6_ch16	LIA_P7_ch32	LIA_P9_ch16	-3890,7μs	-2796,3μs	-2431,5μs	-2066,7μs	103,9μs	
LIA_P2_ch1	LIA_P3_ch17	LIA_P5_ch1	LIA_P6_ch17	LIA_P8_ch1	LIA_P9_ch17	-3786,8μs	-2692,4μs	-2327,6μs	-1962,8μs	103,9μs	
LIA_P2_ch3	LIA_P3_ch19	LIA_P5_ch3	LIA_P6_ch19	LIA_P8_ch3	LIA_P9_ch19	-3682,9μs	-2588,5μs	-2223,7μs	-1858,9μs	103,9μs	
LIA_P2_ch5	LIA_P3_ch21	LIA_P5_ch5	LIA_P6_ch21	LIA_P8_ch5	LIA_P9_ch21	-3579μs	-2484,6μs	-2119,8μs	-1755μs	103,9μs	
LIA_P2_ch7	LIA_P3_ch23	LIA_P5_ch7	LIA_P6_ch23	LIA_P8_ch7	LIA_P9_ch23	-3475,1μs	-2380,7μs	-2015,9μs	-1651,1μs	103,9μs	
LIA_P2_ch9	LIA_P3_ch25	LIA_P5_ch9	LIA_P6_ch25	LIA_P8_ch9	LIA_P9_ch25	-3371,2μs	-2276,8μs	-1912μs	-1547,2μs	103,9μs	
LIA_P2_ch11	LIA_P3_ch27	LIA_P5_ch11	LIA_P6_ch27	LIA_P8_ch11	LIA_P9_ch27	-3267,3μs	-2172,9μs	-1808,1μs	-1443,3μs	103,9μs	
LIA_P2_ch13	LIA_P3_ch29	LIA_P5_ch13	LIA_P6_ch29	LIA_P8_ch13	LIA_P9_ch29	-3163,4μs	-2069μs	-1704,2μs	-1339,4μs	103,9μs	
LIA_P2_ch15	LIA_P3_ch31	LIA_P5_ch15	LIA_P6_ch31	LIA_P8_ch15	LIA_P9_ch31	-3059,5μs	-1965,1μs	-1600,3μs	-1235,5μs	103,9μs	
LIA_P2_ch2	LIA_P3_ch18	LIA_P5_ch2	LIA_P6_ch18	LIA_P8_ch2	LIA_P9_ch18	-2955,6μs	-1861,2μs	-1496,4μs	-1131,6μs	103,9μs	
LIA_P2_ch4	LIA_P3_ch20	LIA_P5_ch4	LIA_P6_ch20	LIA_P8_ch4	LIA_P9_ch20	-2851,7μs	-1757,3μs	-1392,5μs	-1027,7μs	103,9μs	
LIA_P2_ch6	LIA_P3_ch22	LIA_P5_ch6	LIA_P6_ch22	LIA_P8_ch6	LIA_P9_ch22	-2747,8μs	-1653,4μs	-1288,6μs	-923,8μs	103,9μs	
LIA_P2_ch8	LIA_P3_ch24	LIA_P5_ch8	LIA_P6_ch24	LIA_P8_ch8	LIA_P9_ch24	-2643,9μs	-1549,5μs	-1184,7μs	-819,9μs	103,9μs	
LIA_P2_ch10	LIA_P3_ch26	LIA_P5_ch10	LIA_P6_ch26	LIA_P8_ch10	LIA_P9_ch26	-2540μs	-1445,6μs	-1080,8μs	-716μs	103,9μs	
LIA_P2_ch12	LIA_P3_ch28	LIA_P5_ch12	LIA_P6_ch28	LIA_P8_ch12	LIA_P9_ch28	-2436,1μs	-1341,7μs	-976,9μs	-612,1μs	103,9μs	
LIA_P2_ch14	LIA_P3_ch30	LIA_P5_ch14	LIA_P6_ch30	LIA_P8_ch14	LIA_P9_ch30	-2332,2μs	-1237,8μs	-873μs	-508,2μs	103,9μs	
LIA_P2_ch16	LIA_P3_ch32	LIA_P5_ch16	LIA_P6_ch32	LIA_P8_ch16	LIA_P9_ch32	-2228,3μs	-1133,9μs	-769,1μs	-404,3μs	103,9μs	

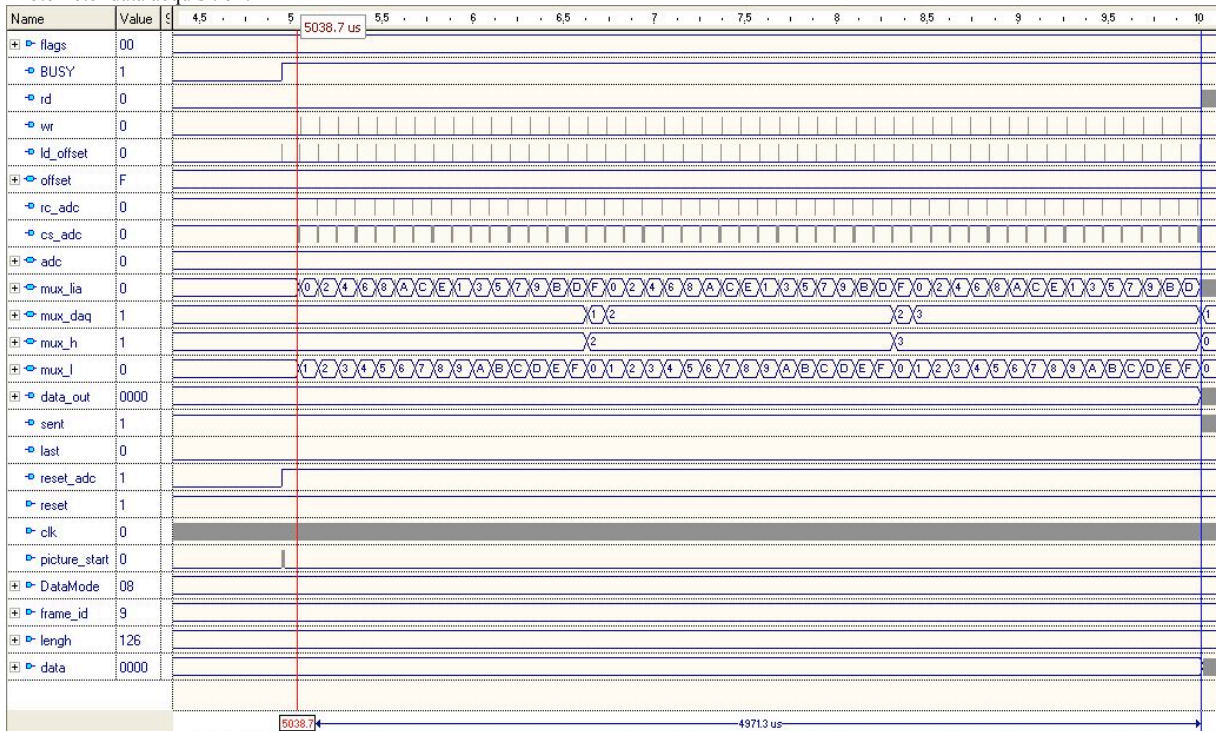
4883,3μs

Timing:

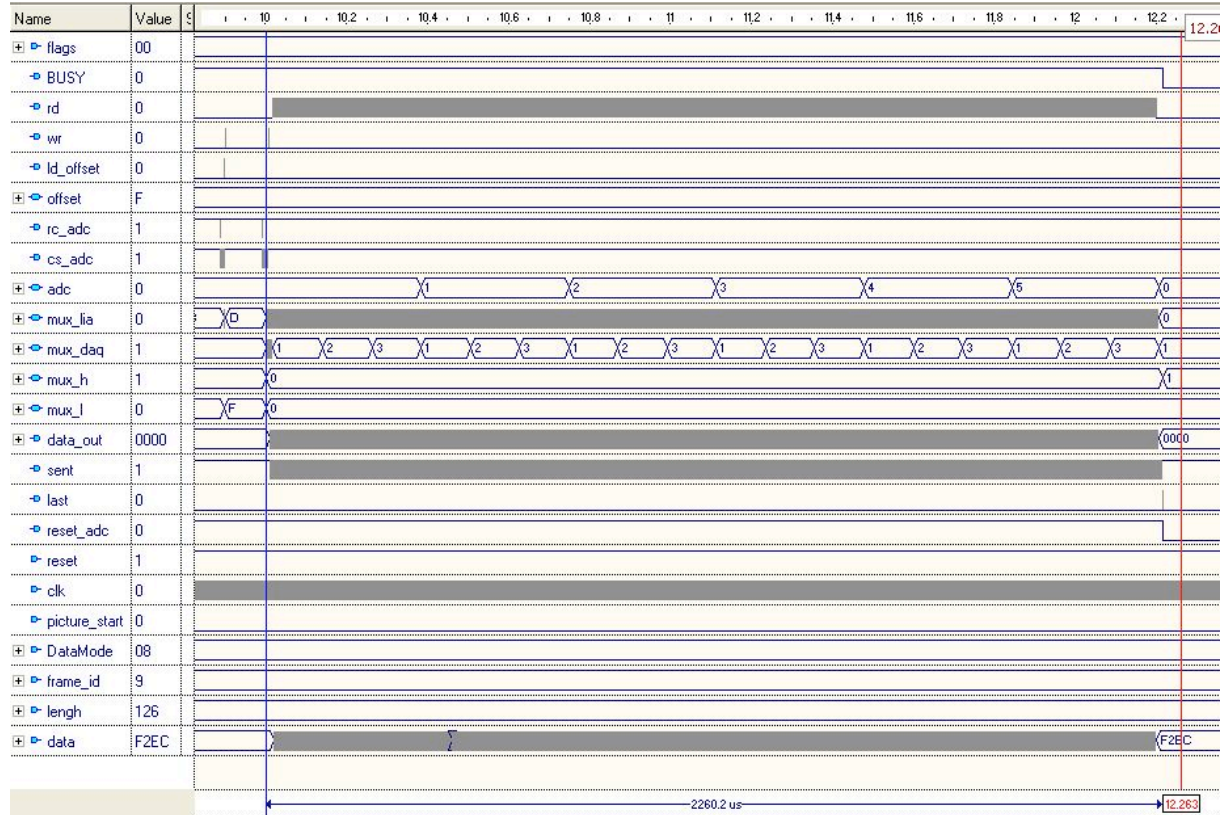
Photometer picture sequence:



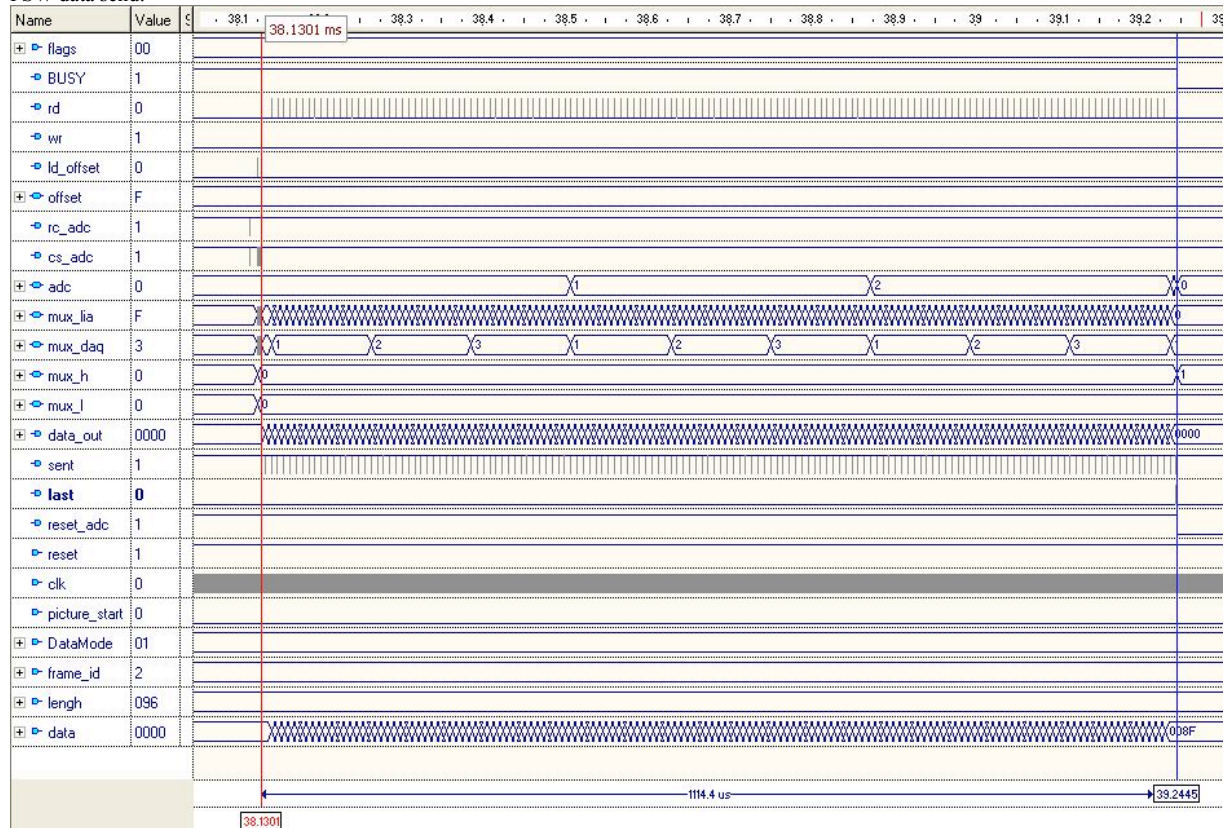
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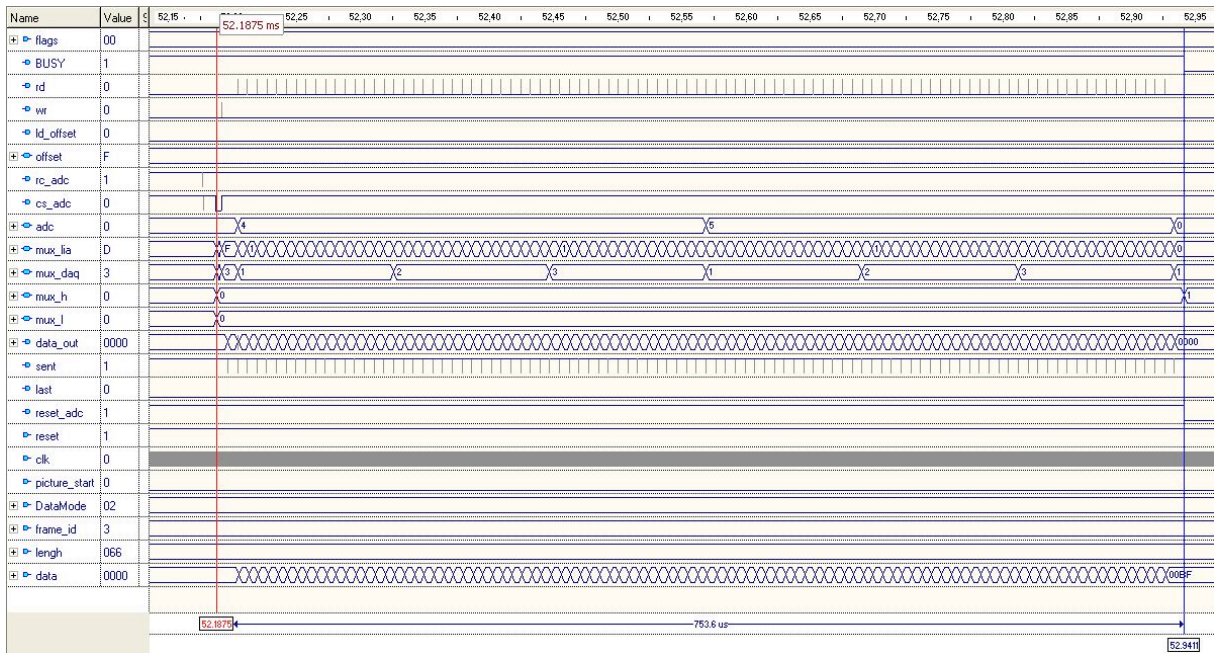
Full Photometer data send:



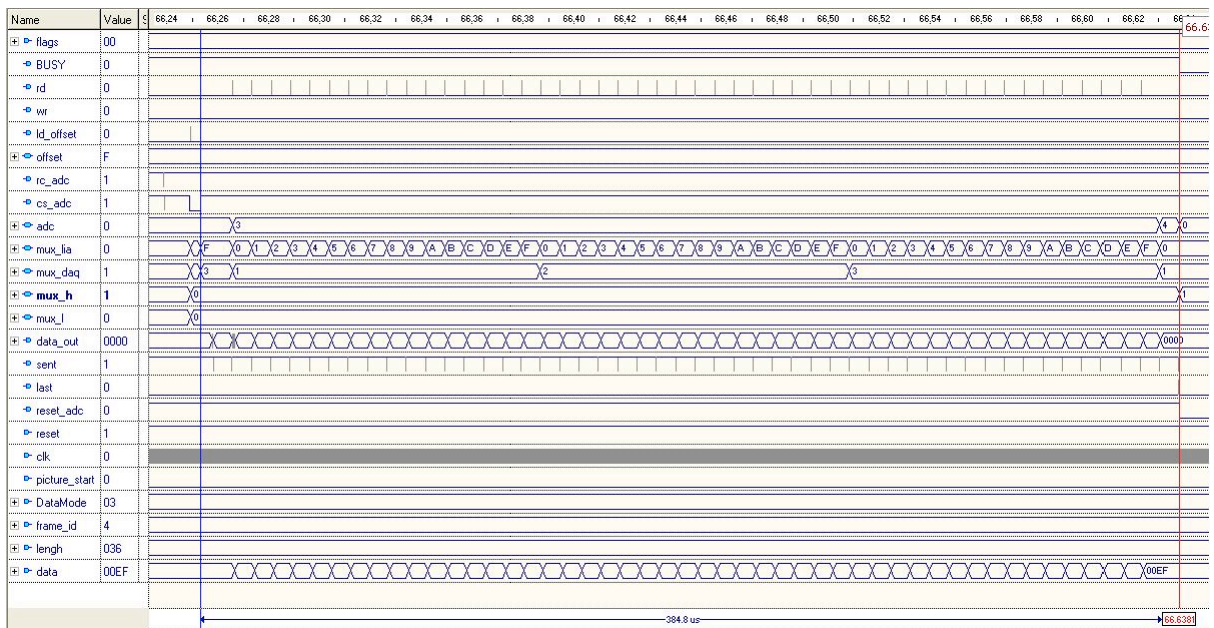
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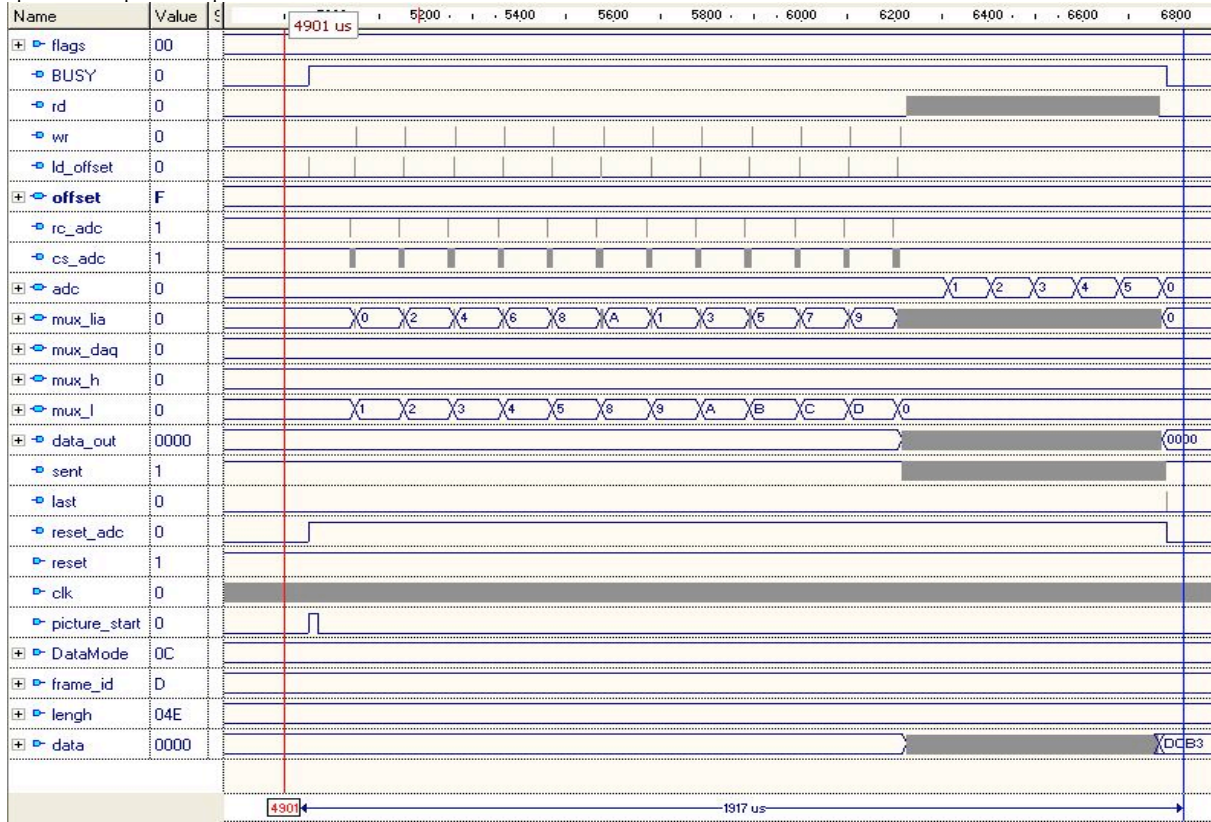
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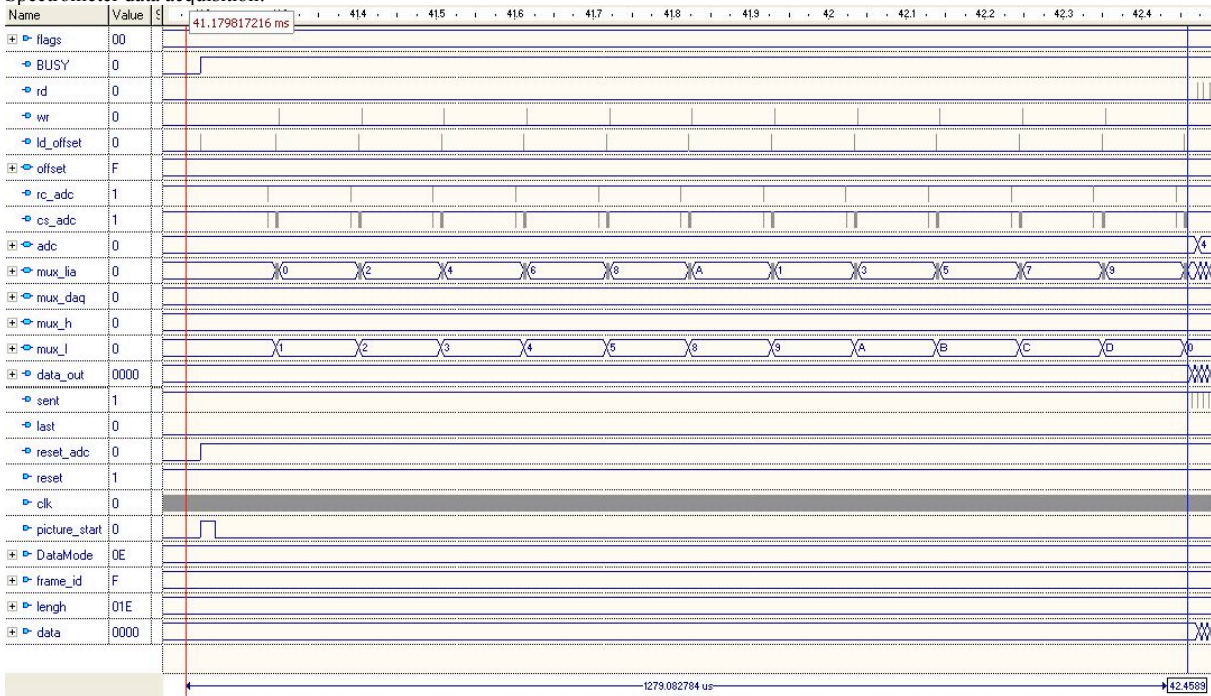
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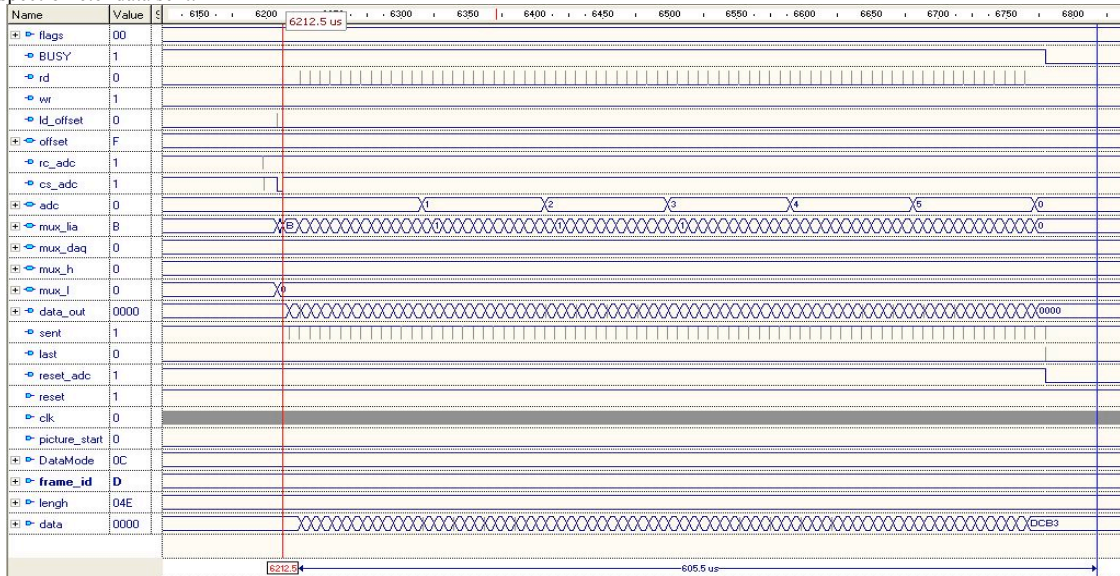
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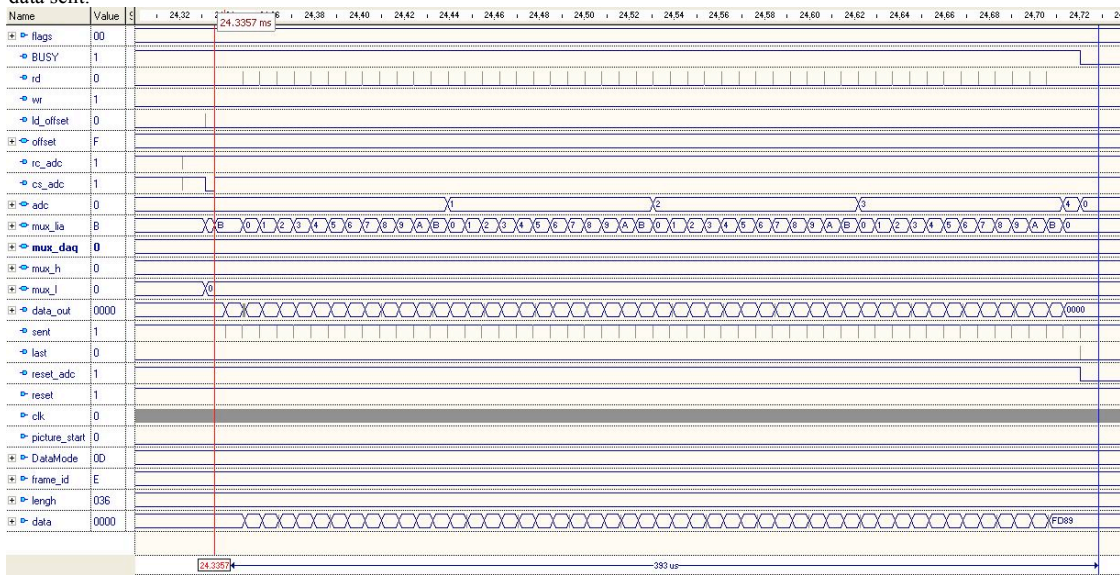
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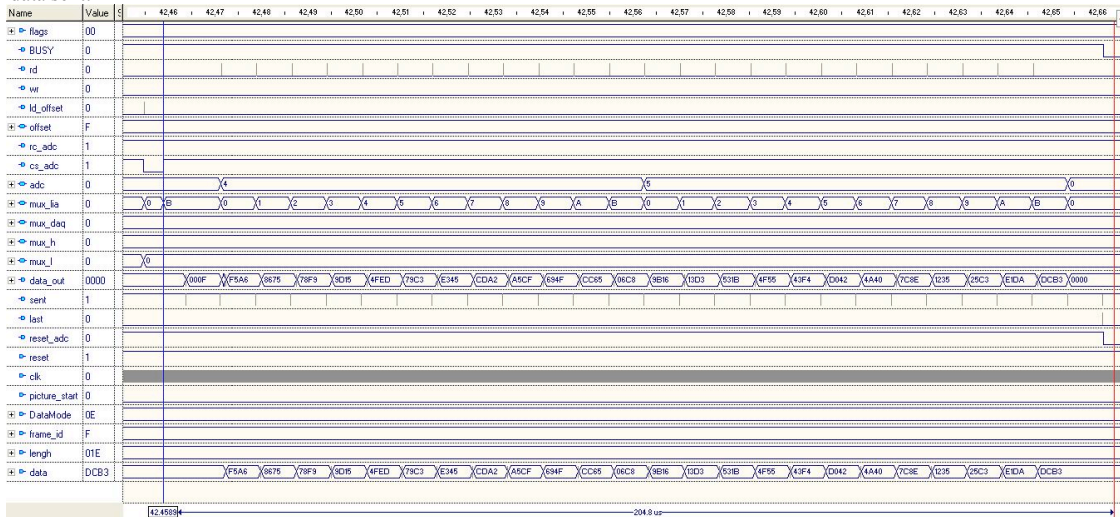
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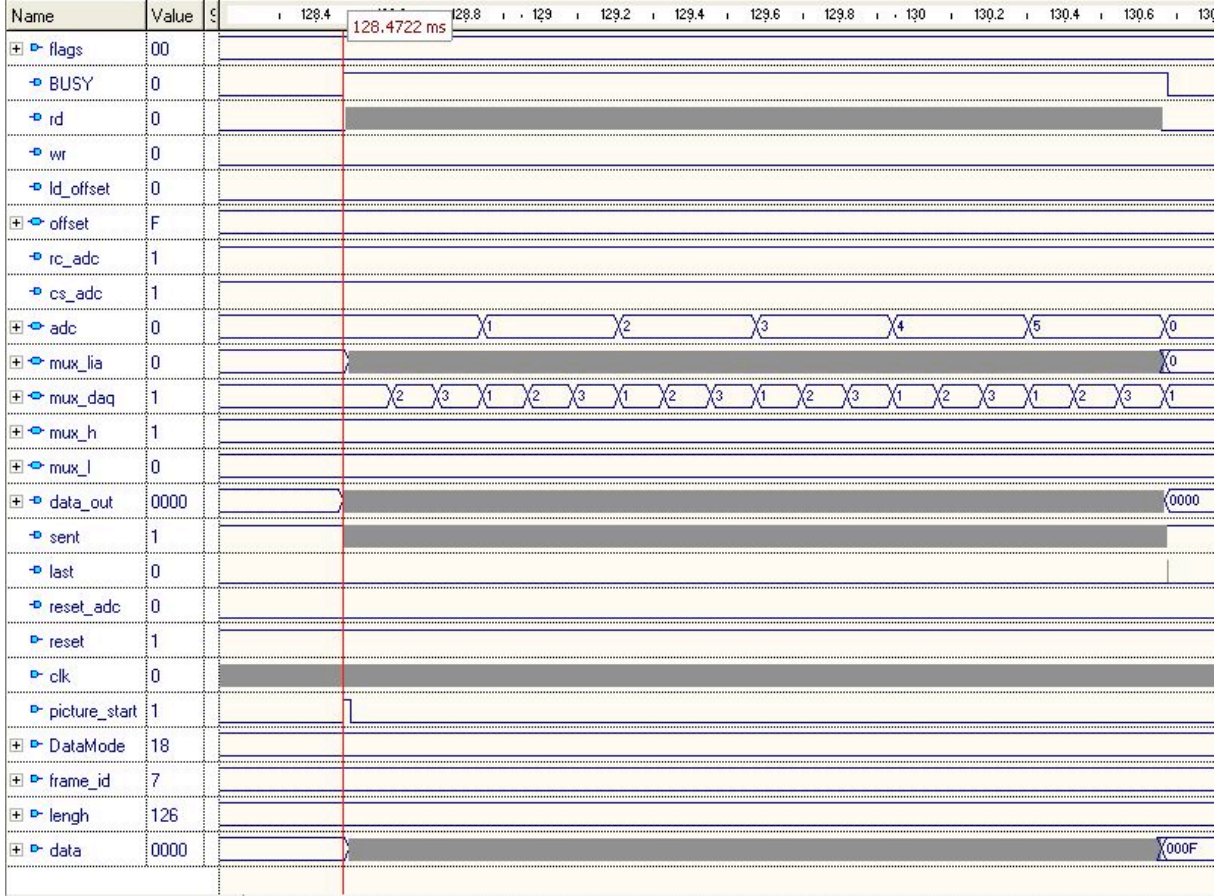
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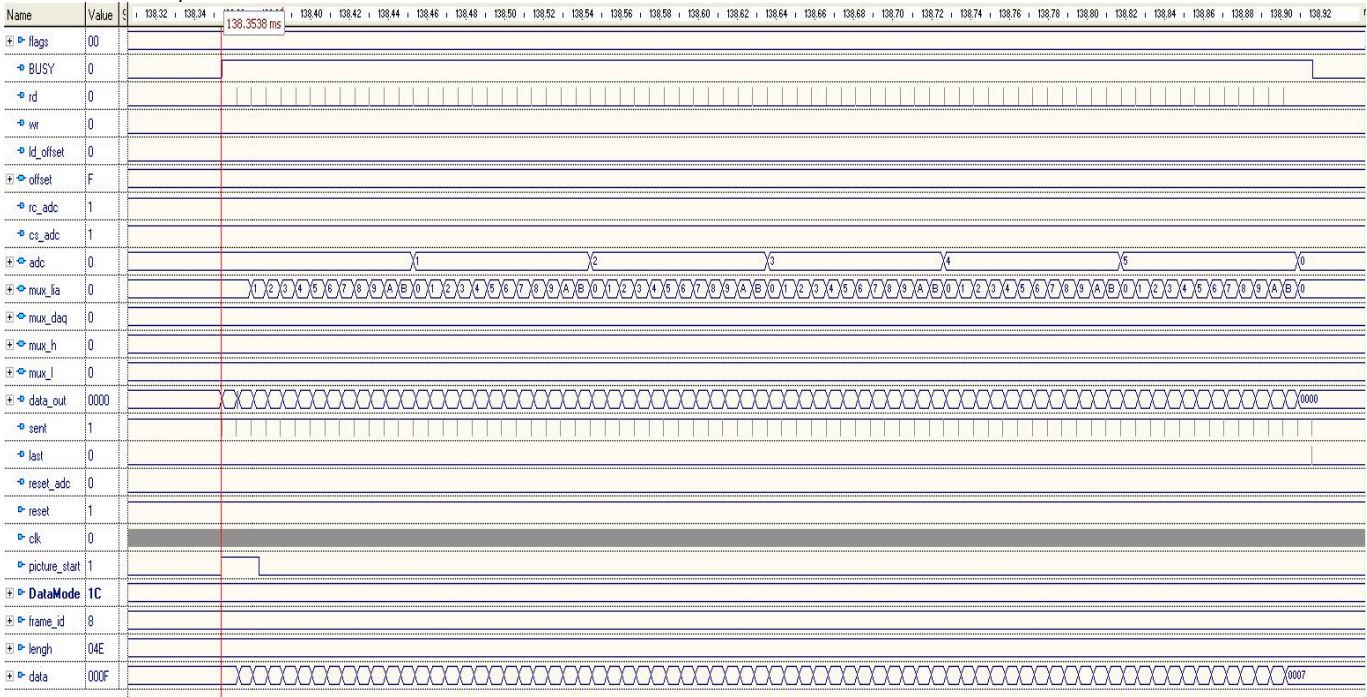
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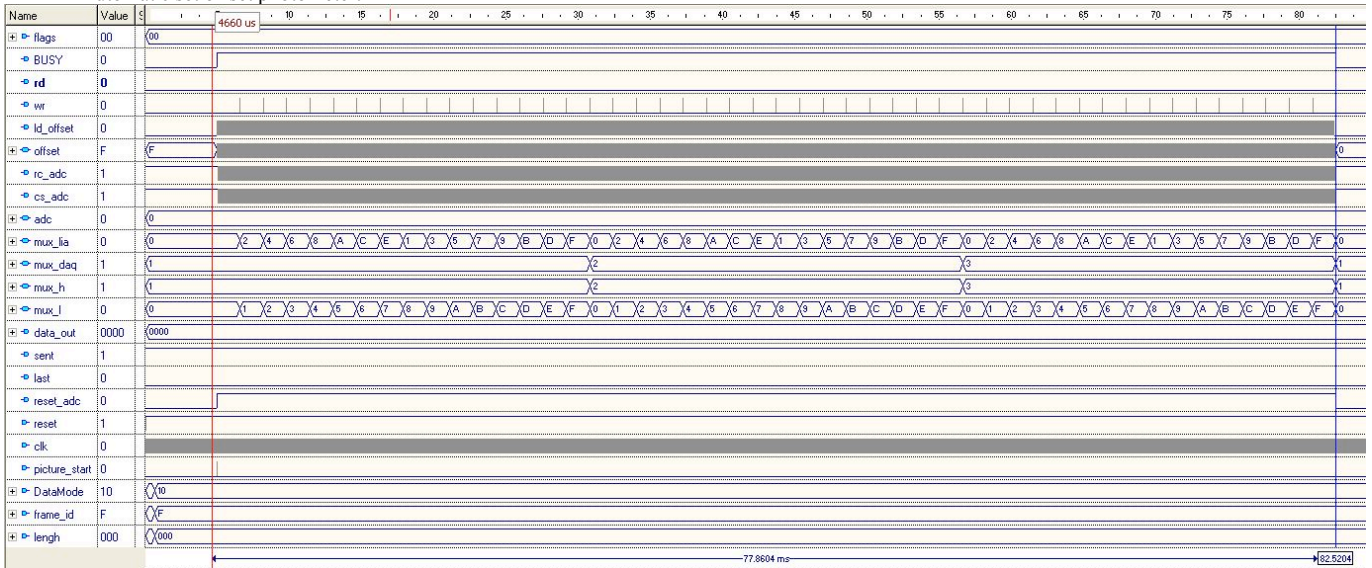
Get offset photometer:



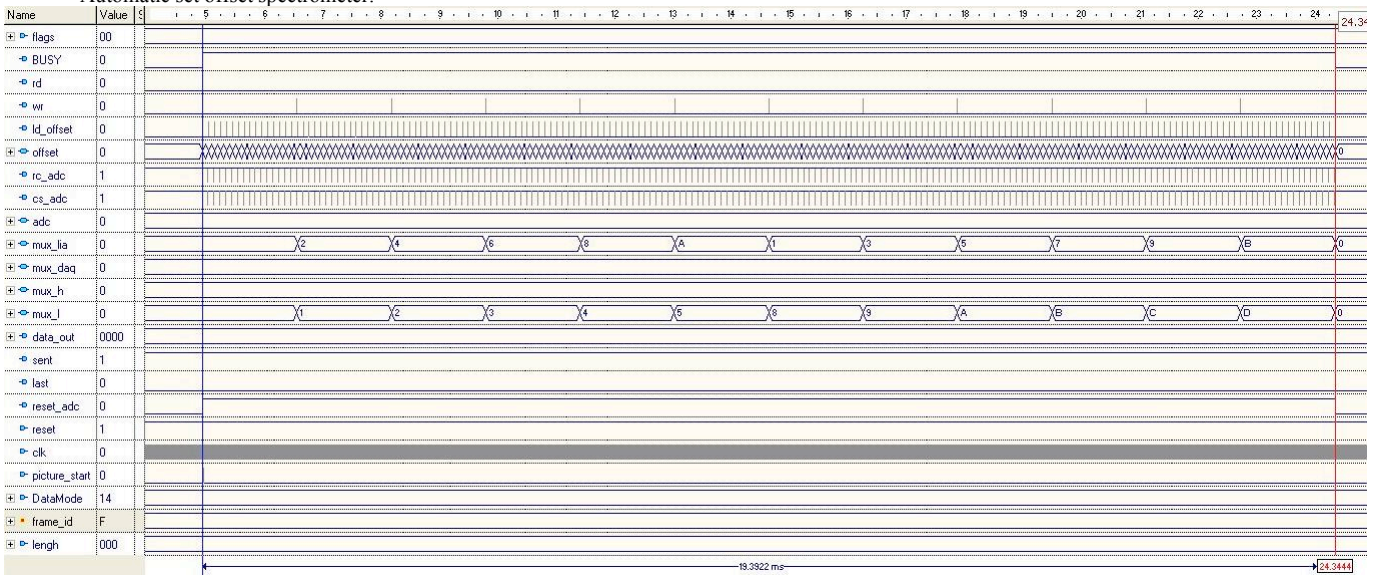
Get offset spectrometer



Automatic set offset photometer:



Automatic set offset spectrometer:



Photometer Frames:

mode	Acquisition				Acquisition test pattern				Get offset photo
	full photo	PSW	PMW	PLW	full photo	PSW	PMW	PLW	
command word	Cmd: 843C0000	Cmd: 843C0001	Cmd: 843C0002	Cmd: 843C0003	Cmd: 843C0008	Cmd: 843C0009	Cmd: 843C000A	Cmd: 843C000B	Cmd: 843C0018
1	Data:0126	Data:0096	Data:0066	Data:0036	Data:0126	Data:0096	Data:0066	Data:0036	Data:0126
2	Data:0000	Data:0002	Data:0003	Data:0004	Data:0009	Data:000A	Data:000B	Data:000C	Data:0007
3	Data:0030	Data:0060	Data:0090	Data:00C0	Data:19B7	Data:19B7	Data:F5A6	Data:10A5	Data:0000
4	Data:0038	Data:0068	Data:0098	Data:00C8	Data:AA8A	Data:AA8A	Data:79C3	Data:F60E	Data:0001
5	Data:0031	Data:0061	Data:0091	Data:00C1	Data:7A32	Data:7A32	Data:78F9	Data:A99C	Data:0002
6	Data:0039	Data:0069	Data:0099	Data:00C9	Data:2DE7	Data:2DE7	Data:CDA2	Data:3A20	Data:0003
7	Data:0032	Data:0062	Data:0092	Data:00C2	Data:E105	Data:E105	Data:4FED	Data:C548	Data:0004
8	Data:003A	Data:006A	Data:009A	Data:00CA	Data:BFB0	Data:BFB0	Data:694F	Data:5815	Data:0005
9	Data:0033	Data:0063	Data:0093	Data:00C3	Data:F3AB	Data:F3AB	Data:E345	Data:ACB2	Data:0006
10	Data:003B	Data:006B	Data:009B	Data:00CB	Data:FAE8	Data:FAE8	Data:06C8	Data:FD89	Data:0007
11	Data:0034	Data:0064	Data:0094	Data:00C4	Data:E813	Data:E813	Data:A5CF	Data:EFF7	Data:0008
12	Data:003C	Data:006C	Data:009C	Data:00CC	Data:7680	Data:7680	Data:D9EF	Data:F401	Data:0009
13	Data:0035	Data:0065	Data:0095	Data:00C5	Data:31A4	Data:31A4	Data:CC65	Data:F19B	Data:000A
14	Data:003D	Data:006D	Data:009D	Data:00CD	Data:B551	Data:B551	Data:413E	Data:99A5	Data:000B
15	Data:0036	Data:0066	Data:0096	Data:00C6	Data:5A8C	Data:5A8C	Data:8675	Data:B2FF	Data:000C
16	Data:003E	Data:006E	Data:009E	Data:00CE	Data:8D31	Data:8D31	Data:A0C0	Data:D238	Data:000D
17	Data:0037	Data:0067	Data:0097	Data:00C7	Data:D2E4	Data:D2E4	Data:9D15	Data:ED26	Data:000E
18	Data:003F	Data:006F	Data:009F	Data:00CF	Data:8340	Data:8340	Data:A76F	Data:864A	Data:000F
19	Data:0040	Data:0070	Data:00A0	Data:00D0	Data:5ABF	Data:5ABF	Data:8310	Data:647C	Data:0000
20	Data:0048	Data:0078	Data:00A8	Data:00D8	Data:7642	Data:7642	Data:6D47	Data:EDE1	Data:0001
21	Data:0041	Data:0071	Data:00A1	Data:00D1	Data:196F	Data:196F	Data:53EA	Data:2F6C	Data:0002
22	Data:0049	Data:0079	Data:00A9	Data:00D9	Data:214D	Data:214D	Data:9E34	Data:37DB	Data:0003
23	Data:0042	Data:0072	Data:00A2	Data:00D2	Data:4753	Data:4753	Data:1C63	Data:1AE3	Data:0004
24	Data:004A	Data:007A	Data:00AA	Data:00DA	Data:CA49	Data:CA49	Data:4B46	Data:4E3E	Data:0005
25	Data:0043	Data:0073	Data:00A3	Data:00D3	Data:3E4C	Data:3E4C	Data:E0E1	Data:11F6	Data:0006
26	Data:004B	Data:007B	Data:00AB	Data:00DB	Data:572A	Data:572A	Data:A5AB	Data:1F30	Data:0007
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40	Data:005A	Data:008A	Data:00BA	Data:00EA	Data:D2B6	Data:D2B6	Data:C224	Data:3755	Data:0005
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95	Data:0056	Data:0086	Data:00B6		Data:8053	Data:8053	Data:7DF3		Data:000C
96	Data:005E	Data:008E	Data:00BE		Data:004C	Data:004C	Data:78C7		Data:000D
97	Data:0057	Data:0087	Data:00B7		Data:E7D9	Data:E7D9	Data:712E		Data:000E
98	Data:005F	Data:008F	Data:00BF		Data:3959	Data:3959	Data:F2EC		Data:000F
99	Data:0030	Data:0060	Data:0000		Data:B3A9	Data:B3A9	Data:0000		Data:0000
100	Data:0038	Data:0068	Data:0000		Data:0BDF	Data:0BDF	Data:0000		Data:0001
101	Data:0031	Data:0061	Data:0D0D		Data:53ED	Data:53ED	Data:0D0D		Data:0002
102	Data:0039	Data:0069	Data:0D68		Data:E437	Data:E437	Data:E139		Data:0003
103	Data:0032	Data:0062			Data:C17A	Data:C17A			Data:0004
104	Data:003A	Data:006A			Data:E918	Data:E918			Data:0005
105	Data:0033	Data:0063			Data:98EE	Data:98EE			Data:0006
106	Data:003B	Data:006B			Data:F0B0	Data:F0B0			Data:0007
107	Data:0034	Data:0064			Data:1897	Data:1897			Data:0008
108	Data:003C	Data:006C			Data:7636	Data:7636			Data:0009
109	Data:0035	Data:0065			Data:5100	Data:5100			Data:000A
110	Data:003D	Data:006D			Data:3C64	Data:3C64			Data:000B
111	Data:0036	Data:0066			Data:F33E	Data:F33E			Data:000C
112	Data:003E	Data:006E			Data:A46F	Data:A46F			Data:000D
113	Data:0037	Data:0067			Data:A843	Data:A843			Data:000E
114	Data:003F	Data:006F			Data:F020	Data:F020			Data:000F
115	Data:0040	Data:0070			Data:63AF	Data:63AF			Data:0000
116	Data:0048	Data:0078			Data:01A7	Data:01A7			Data:0001
117	Data:0041	Data:0071			Data:3579	Data:3579			Data:0002
118	Data:0049	Data:0079			Data:E15C	Data:E15C			Data:0003
119	Data:0042	Data:0072			Data:899B	Data:899B			Data:0004
120	Data:004A	Data:007A			Data:9DD5	Data:9DD5			Data:0005
121	Data:0043	Data:0073			Data:81C6	Data:81C6			Data:0006
122	Data:004B	Data:007B			Data:650F	Data:650F			Data:0007
123	Data:0044	Data:0074			Data:8966	Data:8966			Data:0008
124	Data:004C	Data:007C			Data:C1B3	Data:C1B3			Data:0009
125	Data:0045	Data:0075			Data:ECB3	Data:ECB3			Data:000A
126	Data:004D	Data:007D			Data:E309	Data:E309			Data:000B
127	Data:0046	Data:0076			Data:98B1	Data:98B1			Data:000C
128	Data:004E	Data:007E			Data:9C96	Data:9C96			Data:000D
129	Data:0047	Data:0077			Data:EF98	Data:EF98			Data:000E
130	Data:004F	Data:007F			Data:8CE3	Data:8CE3			Data:000F
131	Data:0050	Data:0080			Data:3B5D	Data:3B5D			Data:0000
132	Data:0058	Data:0088			Data:D52C	Data:D52C			Data:0001
133	Data:0051	Data:0081			Data:0CF8	Data:0CF8			Data:0002
134	Data:0059	Data:0089			Data:5D8A	Data:5D8A			Data:0003
135	Data:0052	Data:0082			Data:F47C	Data:F47C			Data:0004
136	Data:005A	Data:008A			Data:831A	Data:831A			Data:0005
137	Data:0053	Data:0083			Data:E3A7	Data:E3A7			Data:0006
138	Data:005B	Data:008B			Data:F879	Data:F879			Data:0007
139	Data:0054	Data:0084			Data:340E	Data:340E			Data:0008
140	Data:005C	Data:008C			Data:7AAE	Data:7AAE			Data:0009
141	Data:0055	Data:0085			Data:76E5	Data:76E5			Data:000A
142	Data:005D	Data:008D			Data:C67E	Data:C67E			Data:000B
143	Data:0056	Data:0086			Data:EEFE	Data:EEFE			Data:000C
144	Data:005E	Data:008E			Data:41C0	Data:41C0			Data:000D
145	Data:0057	Data:0087			Data:B85F	Data:B85F			Data:000E
146	Data:005F	Data:008F			Data:010D	Data:010D			Data:000F
147	Data:0030	Data:0000			Data:10A5	Data:0000			Data:0000
148	Data:0038	Data:0000			Data:F60E	Data:0000			Data:0001
149	Data:0031	Data:0D7F			Data:A99C	Data:0D7F			Data:0002
150	Data:0039	Data:0DEB			Data:3A20	Data:FFA8			Data:0003
151	Data:0032				Data:C548				Data:0004
152	Data:003A				Data:5815				Data:0005
153	Data:0033				Data:ACB2				Data:0006
154	Data:003B				Data:FD89				Data:0007
155	Data:0034				Data:EFF7				Data:0008
156	Data:003C				Data:F401				Data:0009
157	Data:0035				Data:F19B				Data:000A

158	Data:003D				Data:99A5			Data:000B
159	Data:0036				Data:B2FF			Data:000C
160	Data:003E				Data:D238			Data:000D
161	Data:0037				Data:ED26			Data:000E
162	Data:003F				Data:864A			Data:000F
163	Data:0040				Data:647C			Data:0000
164	Data:0048				Data:EDE1			Data:0001
165	Data:0041				Data:2F6C			Data:0002
166	Data:0049				Data:37DB			Data:0003
167	Data:0042				Data:1AE3			Data:0004
168	Data:004A				Data:4E3E			Data:0005
169	Data:0043				Data:11F6			Data:0006
170	Data:004B				Data:1F30			Data:0007
171	Data:0044				Data:429E			Data:0008
172	Data:004C				Data:563C			Data:0009
173	Data:0045				Data:C15A			Data:000A
174	Data:004D				Data:0E60			Data:000B
175	Data:0046				Data:9D33			Data:000C
176	Data:004E				Data:9F79			Data:000D
177	Data:0047				Data:E56F			Data:000E
178	Data:004F				Data:1898			Data:000F
179	Data:0050				Data:AF5A			Data:0000
180	Data:0058				Data:2EC7			Data:0001
181	Data:0051				Data:A695			Data:0002
182	Data:0059				Data:C95D			Data:0003
183	Data:0052				Data:1D93			Data:0004
184	Data:005A				Data:3755			Data:0005
185	Data:0053				Data:D5F1			Data:0006
186	Data:005B				Data:E37B			Data:0007
187	Data:0054				Data:3522			Data:0008
188	Data:005C				Data:18CE			Data:0009
189	Data:0055				Data:6F35			Data:000A
190	Data:005D				Data:3F7E			Data:000B
191	Data:0056				Data:47B3			Data:000C
192	Data:005E				Data:7E22			Data:000D
193	Data:0057				Data:275D			Data:000E
194	Data:005F				Data:5854			Data:000F
195	Data:0030				Data:F5A6			Data:0000
196	Data:0038				Data:79C3			Data:0001
197	Data:0031				Data:78F9			Data:0002
198	Data:0039				Data:CDA2			Data:0003
199	Data:0032				Data:4FED			Data:0004
200	Data:003A				Data:694F			Data:0005
201	Data:0033				Data:E345			Data:0006
202	Data:003B				Data:06C8			Data:0007
203	Data:0034				Data:A5CF			Data:0008
204	Data:003C				Data:D9EF			Data:0009
205	Data:0035				Data:CC65			Data:000A
206	Data:003D				Data:413E			Data:000B
207	Data:0036				Data:8675			Data:000C
208	Data:003E				Data:A0C0			Data:000D
209	Data:0037				Data:9D15			Data:000E
210	Data:003F				Data:A76F			Data:000F
211	Data:0040				Data:8310			Data:0000
212	Data:0048				Data:6D47			Data:0001
213	Data:0041				Data:53EA			Data:0002
214	Data:0049				Data:9E34			Data:0003
215	Data:0042				Data:1C63			Data:0004
216	Data:004A				Data:4B46			Data:0005
217	Data:0043				Data:E0E1			Data:0006
218	Data:004B				Data:A5AB			Data:0007
219	Data:0044				Data:D5F4			Data:0008
220	Data:004C				Data:D3A2			Data:0009
221	Data:0045				Data:60EB			Data:000A
222	Data:004D				Data:16AF			Data:000B
223	Data:0046				Data:5C53			Data:000C
224	Data:004E				Data:E46F			Data:000D
225	Data:0047				Data:D4FC			Data:000E
226	Data:004F				Data:C30E			Data:000F
227	Data:0050				Data:D818			Data:0000
228	Data:0058				Data:D3E4			Data:0001
229	Data:0051				Data:A937			Data:0002
230	Data:0059				Data:8465			Data:0003
231	Data:0052				Data:3819			Data:0004
232	Data:005A				Data:C224			Data:0005
233	Data:0053				Data:65D2			Data:0006
234	Data:005B				Data:58B9			Data:0007
235	Data:0054				Data:A91B			Data:0008
236	Data:005C				Data:DDC1			Data:0009
237	Data:0055				Data:0F26			Data:000A
238	Data:005D				Data:456E			Data:000B
239	Data:0056				Data:235C			Data:000C

240	Data:005E				Data:122A			Data:000D
241	Data:0057				Data:D110			Data:000E
242	Data:005F				Data:1D6E			Data:000F
243	Data:0030				Data:9B16			Data:0000
244	Data:0038				Data:D042			Data:0001
245	Data:0031				Data:531B			Data:0002
246	Data:0039				Data:7C8E			Data:0003
247	Data:0032				Data:43F4			Data:0004
248	Data:003A				Data:25C3			Data:0005
249	Data:0033				Data:4A40			Data:0006
250	Data:003B				Data:DCB3			Data:0007
251	Data:0034				Data:1235			Data:0008
252	Data:003C				Data:efd9			Data:0009
253	Data:0035				Data:E1DA			Data:000A
254	Data:003D				Data:4E74			Data:000B
255	Data:0036				Data:13D3			Data:000C
256	Data:003E				Data:BF18			Data:000D
257	Data:0037				Data:4F55			Data:000E
258	Data:003F				Data:CB01			Data:000F
259	Data:0040				Data:513D			Data:0000
260	Data:0048				Data:3311			Data:0001
261	Data:0041				Data:8287			Data:0002
262	Data:0049				Data:42DE			Data:0003
263	Data:0042				Data:B585			Data:0004
264	Data:004A				Data:CAE1			Data:0005
265	Data:0043				Data:82B2			Data:0006
266	Data:004B				Data:66C3			Data:0007
267	Data:0044				Data:E77F			Data:0008
268	Data:004C				Data:9CAD			Data:0009
269	Data:0045				Data:B2D0			Data:000A
270	Data:004D				Data:642B			Data:000B
271	Data:0046				Data:16A1			Data:000C
272	Data:004E				Data:FB20			Data:000D
273	Data:0047				Data:5E5D			Data:000E
274	Data:004F				Data:67E0			Data:000F
275	Data:0050				Data:7B27			Data:0000
276	Data:0058				Data:D546			Data:0001
277	Data:0051				Data:98CD			Data:0002
278	Data:0059				Data:F87F			Data:0003
279	Data:0052				Data:D1F2			Data:0004
280	Data:005A				Data:E3DF			Data:0005
281	Data:0053				Data:4225			Data:0006
282	Data:005B				Data:1BC5			Data:0007
283	Data:0054				Data:3EE5			Data:0008
284	Data:005C				Data:A3B5			Data:0009
285	Data:0055				Data:AAF			Data:000A
286	Data:005D				Data:8D1E			Data:000B
287	Data:0056				Data:7DF3			Data:000C
288	Data:005E				Data:78C7			Data:000D
289	Data:0057				Data:712E			Data:000E
290	Data:005F				Data:F2EC			Data:000F
291	Data:0000				Data:0000			Data:0000
292	Data:0000				Data:0000			Data:0000
293	Data:0ED5				Data:0ED5			Data:9F86
294	Data:0FF3				Data:F6C8			Data:9EA7

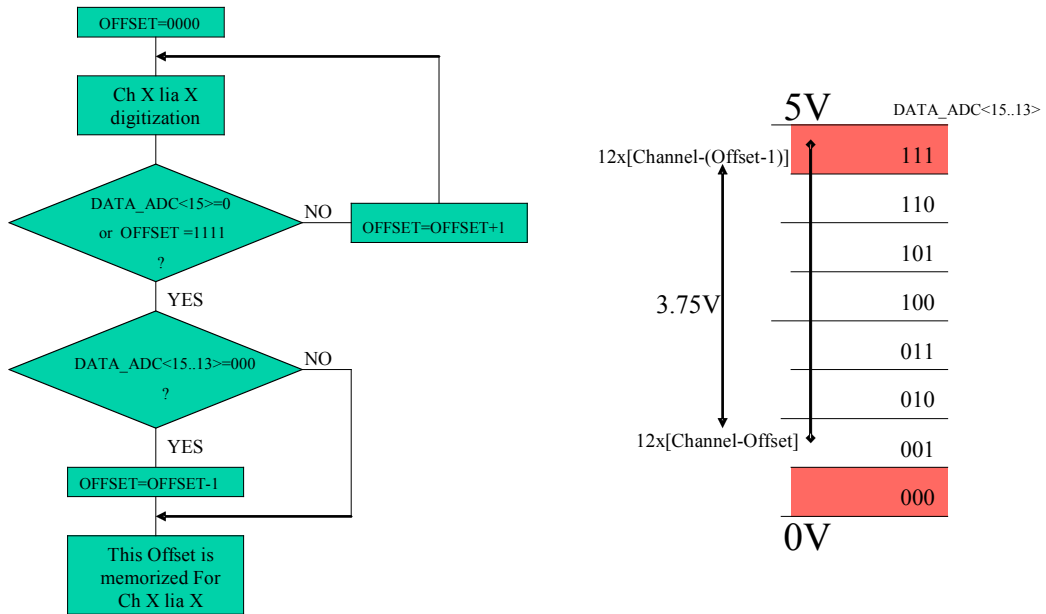
Spectrometer frames:

mode	Acquisition			Acquisition test pattern			Get offset
	full spectro	SSW	SLW	full spectro	SSW	SLW	Spectro
command word	Cmd: 843C0004	Cmd: 843C0005	Cmd: 843C0006	Cmd: 843C000C	Cmd: 843C000D	Cmd: 843C000E	Cmd: 843C001C
1	Data:004E	Data:0036	Data:001E	Data:004E	Data:0036	Data:001E	Data:004E
2	Data:0001	Data:0005	Data:0006	Data:000D	Data:000E	Data:000F	Data:0008
3	Data:000C	Data:0024	Data:003C	Data:19B7	Data:19B7	Data:F5A6	Data:0000
4	Data:0012	Data:002A	Data:0042	Data:5A8C	Data:5A8C	Data:8675	Data:0001
5	Data:000D	Data:0025	Data:003D	Data:7A32	Data:7A32	Data:78F9	Data:0002
6	Data:0013	Data:002B	Data:0043	Data:D2E4	Data:D2E4	Data:9D15	Data:0003
7	Data:000E	Data:0026	Data:003E	Data:E105	Data:E105	Data:4FED	Data:0004
8	Data:0014	Data:002C	Data:0044	Data:AA8A	Data:AA8A	Data:79C3	Data:0005
9	Data:000F	Data:0027	Data:003F	Data:F3AB	Data:F3AB	Data:E345	Data:0006
10	Data:0015	Data:002D	Data:0045	Data:2DE7	Data:2DE7	Data:CDA2	Data:0007
11	Data:0010	Data:0028	Data:0040	Data:E813	Data:E813	Data:A5CF	Data:0008
12	Data:0016	Data:002E	Data:0046	Data:BF80	Data:BF80	Data:694F	Data:0009
13	Data:0011	Data:0029	Data:0041	Data:31A4	Data:31A4	Data:CC65	Data:000A
14	Data:0017	Data:002F	Data:0047	Data:FAE8	Data:FAE8	Data:06C8	Data:000B
15	Data:000C	Data:0024	Data:003C	Data:7707	Data:7707	Data:9B16	Data:000C
16	Data:0012	Data:002A	Data:0042	Data:CF2A	Data:CF2A	Data:13D3	Data:000D
17	Data:000D	Data:0025	Data:003D	Data:51D0	Data:51D0	Data:531B	Data:000E
18	Data:0013	Data:002B	Data:0043	Data:00A4	Data:00A4	Data:4F55	Data:000F
19	Data:000E	Data:0026	Data:003E	Data:ED1C	Data:ED1C	Data:43F4	Data:0000
20	Data:0014	Data:002C	Data:0044	Data:030B	Data:030B	Data:D042	Data:0001
21	Data:000F	Data:0027	Data:003F	Data:5AAE	Data:5AAE	Data:4A40	Data:0002
22	Data:0015	Data:002D	Data:0045	Data:9CCB	Data:9CCB	Data:7C8E	Data:0003
23	Data:0010	Data:0028	Data:0040	Data:5FE9	Data:5FE9	Data:1235	Data:0004
24	Data:0016	Data:002E	Data:0046	Data:F33C	Data:F33C	Data:25C3	Data:0005
25	Data:0011	Data:0029	Data:0041	Data:1C1B	Data:1C1B	Data:E1DA	Data:0006
26	Data:0017	Data:002F	Data:0047	Data:2093	Data:2093	Data:DCB3	Data:0007
27	Data:000C	Data:0024	Data:003C	Data:B3A9	Data:B3A9	Data:0000	Data:0000
28	Data:0012	Data:002A	Data:0042	Data:F33E	Data:F33E	Data:0000	Data:0001
29	Data:000D	Data:0025	Data:003D	Data:53ED	Data:53ED	Data:07D1	Data:0002
30	Data:0013	Data:002B	Data:0043	Data:A843	Data:A843	Data:B477	Data:0003
31	Data:000E	Data:0026	Data:003E	Data:C17A	Data:C17A		Data:0004
32	Data:0014	Data:002C	Data:0044	Data:0BDF	Data:0BDF		Data:0005
33	Data:000F	Data:0027	Data:003F	Data:98EE	Data:98EE		Data:0006
34	Data:0015	Data:002D	Data:0045	Data:E437	Data:E437		Data:0007
35	Data:0010	Data:0028	Data:0040	Data:1897	Data:1897		Data:0008
36	Data:0016	Data:002E	Data:0046	Data:E918	Data:E918		Data:0009
37	Data:0011	Data:0029	Data:0041	Data:5100	Data:5100		Data:000A
38	Data:0017	Data:002F	Data:0047	Data:F0B0	Data:F0B0		Data:000B
39	Data:000C	Data:0024	Data:003C	Data:10A5	Data:10A5		Data:000C
40	Data:0012	Data:002A	Data:0042	Data:B2FF	Data:B2FF		Data:000D
41	Data:000D	Data:0025	Data:003D	Data:A99C	Data:A99C		Data:000E
42	Data:0013	Data:002B	Data:0043	Data:ED26	Data:ED26		Data:000F
43	Data:000E	Data:0026	Data:003E	Data:C548	Data:C548		Data:0000
44	Data:0014	Data:002C	Data:0044	Data:F60E	Data:F60E		Data:0001
45	Data:000F	Data:0027	Data:003F	Data:ACB2	Data:ACB2		Data:0002
46	Data:0015	Data:002D	Data:0045	Data:3A20	Data:3A20		Data:0003
47	Data:0010	Data:0028	Data:0040	Data:EFF7	Data:EFF7		Data:0004
48	Data:0016	Data:002E	Data:0046	Data:5815	Data:5815		Data:0005
49	Data:0011	Data:0029	Data:0041	Data:F19B	Data:F19B		Data:0006
50	Data:0017	Data:002F	Data:0047	Data:FD89	Data:FD89		Data:0007
51	Data:000C	Data:0024	Data:003C	Data:F5A6	Data:0000		Data:0000
52	Data:0012	Data:002A	Data:0042	Data:8675	Data:0000		Data:0001
53	Data:000D	Data:0025	Data:003D	Data:78F9	Data:080A		Data:0002
54	Data:0013	Data:002B	Data:0043	Data:9D15	Data:1E3B		Data:0003
55	Data:000E	Data:0026	Data:003E	Data:4FED			Data:0004
56	Data:0014	Data:002C	Data:0044	Data:79C3			Data:0005
57	Data:000F	Data:0027	Data:003F	Data:E345			Data:0006
58	Data:0015	Data:002D	Data:0045	Data:CDA2			Data:0007
59	Data:0010	Data:0028	Data:0040	Data:A5CF			Data:0008
60	Data:0016	Data:002E	Data:0046	Data:694F			Data:0009
61	Data:0011	Data:0029	Data:0041	Data:CC65			Data:000A
62	Data:0017	Data:002F	Data:0047	Data:06C8			Data:000B
63	Data:000C	Data:0024	Data:003C	Data:9B16			Data:000C
64	Data:0012	Data:002A	Data:0042	Data:13D3			Data:000D
65	Data:000D	Data:0025	Data:003D	Data:531B			Data:000E
66	Data:0013	Data:002B	Data:0043	Data:4F55			Data:000F
67	Data:000E	Data:0026	Data:003E	Data:43F4			Data:0000
68	Data:0014	Data:002C	Data:0044	Data:D042			Data:0001
69	Data:000F	Data:0027	Data:003F	Data:4A40			Data:0002
70	Data:0015	Data:002D	Data:0045	Data:7C8E			Data:0003
71	Data:0010	Data:0028	Data:0040	Data:1235			Data:0004
72	Data:0016	Data:002E	Data:0046	Data:25C3			Data:0005
73	Data:0011	Data:0029	Data:0041	Data:E1DA			Data:0006
74	Data:0017	Data:002F	Data:0047	Data:DCB3			Data:0007
75	Data:000C	Data:0024	Data:003C	Data:0000			Data:0000
76	Data:0012	Data:002A	Data:0042	Data:0000			Data:0000
77	Data:000D	Data:0025	Data:003D	Data:0843			Data:A995
78	Data:0013	Data:002B	Data:0043	Data:ADBE			Data:A9D3

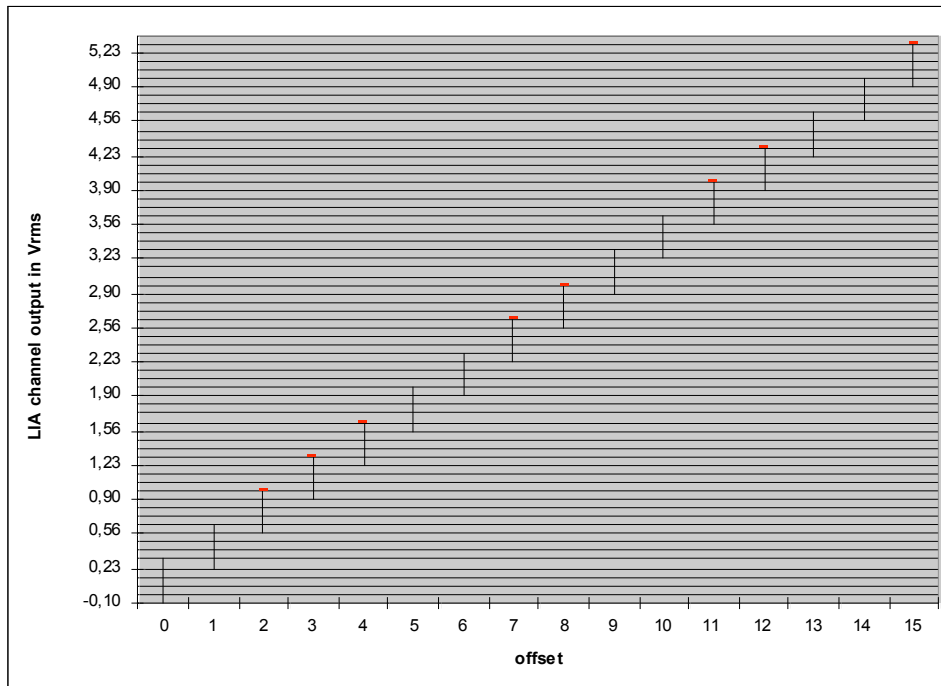
3.9.3.8 Offset

For each channel, the following algorithm determines its offset:

Offset Calculation for Ch X lia X



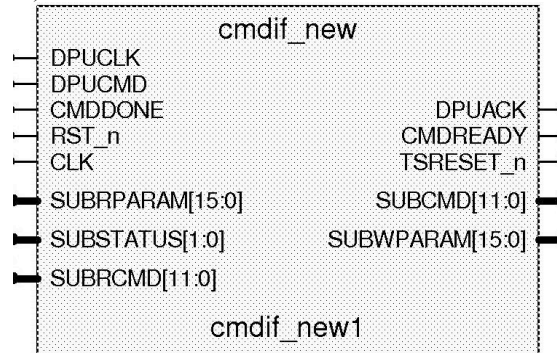
One offset step equal 52428.8 LSB (or 333 mV)



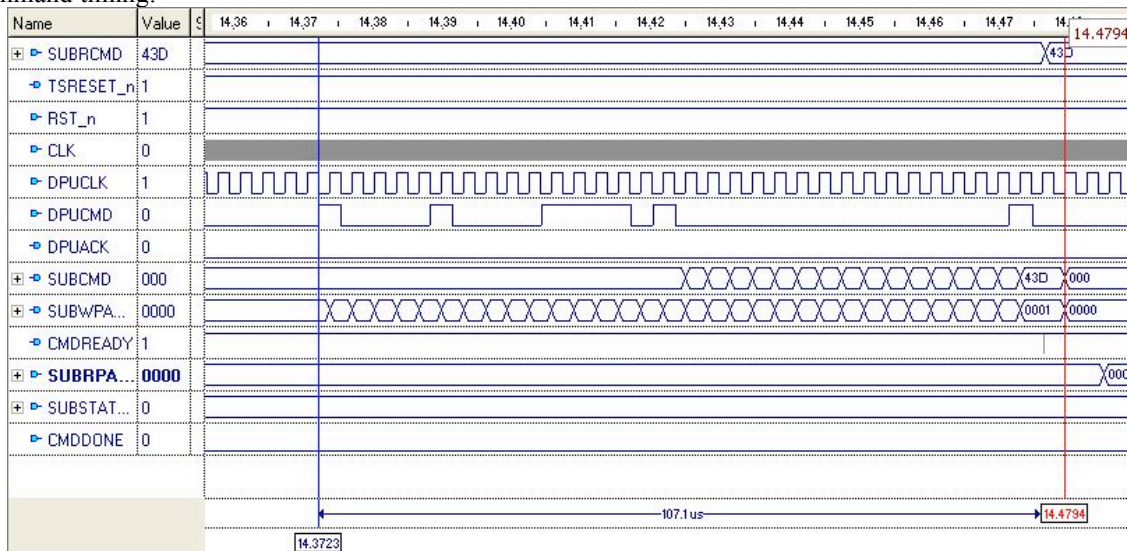
3.9.3.9 DPU INTERFACE (FUNC-06-1, FUNC-07-1, FUNC-10-1 and DCU-FUNC-08)

3.9.3.9.1 Command interface:

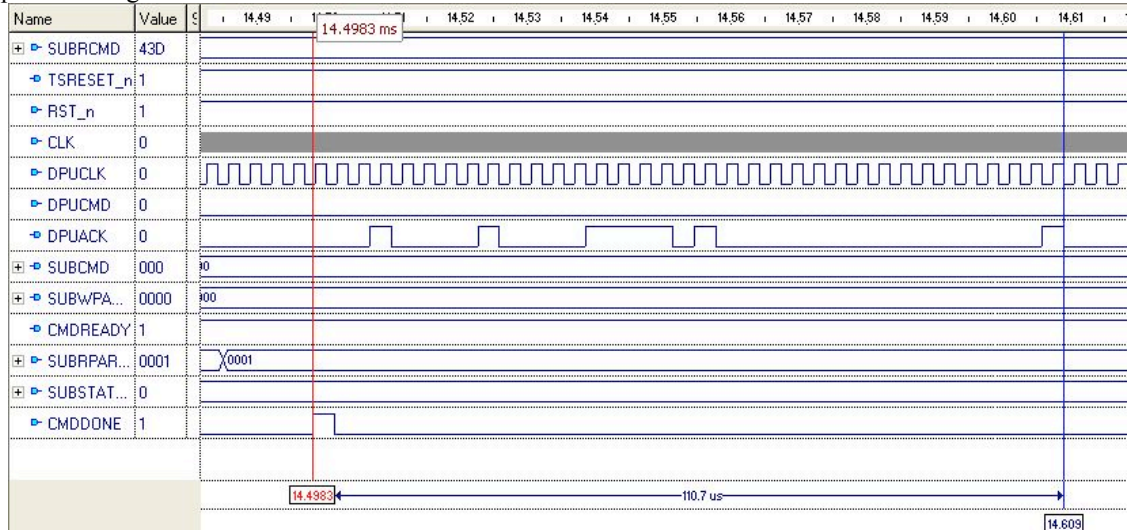
(VHDL module: cmdif_new.vhd)



Command timing:



Response timing:



The following file is the test log file of all the DCU commands
It shows the DCU responds to a command, give a typical delay between a command and its response:

```
begining of test get HK
Cmd:8C3F0000 Res:8C3F0000 Cmd to Res delay:99200 ns ACK= OK
Cmd:8C3F0001 Res:8C3F0001 Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F0002 Res:8C3F0002 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F0003 Res:8C3F0003 Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F0004 Res:8C3F0004 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F0005 Res:8C3F0005 Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F0006 Res:8C3F0006 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F0007 Res:8C3F0007 Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F0008 Res:8C3F0008 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F0009 Res:8C3F0009 Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F000A Res:8C3F000A Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F000B Res:8C3F000B Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F000C Res:8C3F000C Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F000D Res:8C3F000D Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F000E Res:8C3F000E Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F000F Res:8C3F000F Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F0010 Res:8C3F0010 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F0011 Res:8C3F0011 Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F0012 Res:8C3F0012 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F0013 Res:8C3F0013 Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F0014 Res:8C3F0014 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F0015 Res:8C3F0015 Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F0016 Res:8C3F0016 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F0017 Res:8C3F2224 Cmd to Res delay:92800 ns ACK= OK
Cmd:8C3F0018 Res:AC3F0000 Cmd to Res delay:89600 ns ACK= CID forbidden
Cmd:8C3F0019 Res:AC3F0000 Cmd to Res delay:92800 ns ACK= CID forbidden
Cmd:8C3F001A Res:8C3F0000 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F001B Res:AC3F0000 Cmd to Res delay:92800 ns ACK= CID forbidden
Cmd:8C3F001C Res:8C3F0000 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F001D Res:AC3F0000 Cmd to Res delay:92800 ns ACK= CID forbidden
Cmd:8C3F001E Res:8C3F0000 Cmd to Res delay:89600 ns ACK= OK
Cmd:8C3F001F Res:AC3F0000 Cmd to Res delay:92800 ns ACK= CID forbidden
Cmd:8C3F0020 Res:AC3F0020 Cmd to Res delay:89600 ns ACK= CID forbidden
begining of test set cmd
Cmd:84000000 Res:84000000 Cmd to Res delay:32000 ns ACK= OK
Cmd:84010001 Res:84010001 Cmd to Res delay:35200 ns ACK= OK
Cmd:84020002 Res:84020002 Cmd to Res delay:32000 ns ACK= OK
Cmd:84030003 Res:84030003 Cmd to Res delay:35200 ns ACK= OK
Cmd:84040004 Res:84040004 Cmd to Res delay:32000 ns ACK= OK
Cmd:84050005 Res:84050005 Cmd to Res delay:32000 ns ACK= OK
Cmd:84060006 Res:84060006 Cmd to Res delay:35200 ns ACK= OK
Cmd:84070007 Res:84070007 Cmd to Res delay:32000 ns ACK= OK
Cmd:84080008 Res:84080008 Cmd to Res delay:35200 ns ACK= OK
Cmd:84090009 Res:84090009 Cmd to Res delay:32000 ns ACK= OK
Cmd:840A000A Res:840A000A Cmd to Res delay:35200 ns ACK= OK
Cmd:840B000B Res:840B000B Cmd to Res delay:32000 ns ACK= OK
Cmd:840C000C Res:840C000C Cmd to Res delay:32000 ns ACK= OK
Cmd:840D000D Res:840D000D Cmd to Res delay:35200 ns ACK= OK
Cmd:840E000E Res:840E000E Cmd to Res delay:32000 ns ACK= OK
Cmd:840F000F Res:840F000F Cmd to Res delay:35200 ns ACK= OK
Cmd:84100010 Res:84100010 Cmd to Res delay:32000 ns ACK= OK
Cmd:84110011 Res:84110011 Cmd to Res delay:32000 ns ACK= OK
Cmd:84120012 Res:84120012 Cmd to Res delay:35200 ns ACK= OK
Cmd:84130013 Res:84130013 Cmd to Res delay:32000 ns ACK= OK
Cmd:84140014 Res:84140014 Cmd to Res delay:35200 ns ACK= OK
Cmd:84150015 Res:94150014 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:84160016 Res:94160014 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:84170017 Res:94170014 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:84180018 Res:84180018 Cmd to Res delay:35200 ns ACK= OK
Cmd:84190019 Res:A4190060 Cmd to Res delay:12800 ns ACK= CID forbidden
Cmd:841A001A Res:841A001A Cmd to Res delay:35200 ns ACK= OK
Cmd:841B001B Res:841B001B Cmd to Res delay:32000 ns ACK= OK
Cmd:841C001C Res:841C001C Cmd to Res delay:35200 ns ACK= OK
Cmd:841D001D Res:841D001D Cmd to Res delay:32000 ns ACK= OK
Cmd:841E001E Res:941E0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:841F001F Res:941F0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:84300020 Res:84300020 Cmd to Res delay:35200 ns ACK= OK
```

Cmd:84310021 Res:84310021 Cmd to Res delay:35200 ns ACK= OK
Cmd:84320022 Res:84320022 Cmd to Res delay:32000 ns ACK= OK
Cmd:84330023 Res:84330023 Cmd to Res delay:32000 ns ACK= OK
Cmd:84340024 Res:84340024 Cmd to Res delay:35200 ns ACK= OK
Cmd:84350025 Res:84350025 Cmd to Res delay:32000 ns ACK= OK
Cmd:84360026 Res:84360026 Cmd to Res delay:35200 ns ACK= OK
Cmd:84370027 Res:84370027 Cmd to Res delay:32000 ns ACK= OK
Cmd:84380028 Res:84380028 Cmd to Res delay:35200 ns ACK= OK
Cmd:84390029 Res:A4390060 Cmd to Res delay:12800 ns ACK= CID forbidden
Cmd:843A002A Res:843A002A Cmd to Res delay:32000 ns ACK= OK
Cmd:843B002B Res:843B002B Cmd to Res delay:35200 ns ACK= OK
Cmd:843C002C Res:843C000C Cmd to Res delay:32000 ns ACK= OK
Cmd:843D002D Res:843D002D Cmd to Res delay:35200 ns ACK= OK
Cmd:843E002E Res:843E0000 Cmd to Res delay:32000 ns ACK= OK
Cmd:843F002F Res:943F0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:84190062 Res:84190062 Cmd to Res delay:35200 ns ACK= OK
Cmd:843900E3 Res:843900E3 Cmd to Res delay:32000 ns ACK= OK
Cmd:80000000 Res:900000E3 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:80010000 Res:900100E3 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:80020000 Res:900200E3 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:80030000 Res:800300E3 Cmd to Res delay:12800 ns ACK= OK
Cmd:80040000 Res:900400E3 Cmd to Res delay:12800 ns ACK= CID unknown
beging of test get cmd
Cmd:8C000000 Res:8C000000 Cmd to Res delay:28800 ns ACK= OK
Cmd:8C010000 Res:8C010001 Cmd to Res delay:41600 ns ACK= OK
Cmd:8C020000 Res:8C020002 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C030000 Res:8C030003 Cmd to Res delay:32000 ns ACK= OK
Cmd:8C040000 Res:8C040004 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C050000 Res:8C050005 Cmd to Res delay:28800 ns ACK= OK
Cmd:8C060000 Res:8C060006 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C070000 Res:8C070007 Cmd to Res delay:28800 ns ACK= OK
Cmd:8C080000 Res:8C080008 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C090000 Res:8C090009 Cmd to Res delay:32000 ns ACK= OK
Cmd:8C0A0000 Res:8C0A000A Cmd to Res delay:35200 ns ACK= OK
Cmd:8C0B0000 Res:8C0B000B Cmd to Res delay:28800 ns ACK= OK
Cmd:8C0C0000 Res:8C0C000C Cmd to Res delay:35200 ns ACK= OK
Cmd:8C0D0000 Res:8C0D000D Cmd to Res delay:32000 ns ACK= OK
Cmd:8C0E0000 Res:8C0E000E Cmd to Res delay:35200 ns ACK= OK
Cmd:8C0F0000 Res:8C0F000F Cmd to Res delay:28800 ns ACK= OK
Cmd:8C100000 Res:8C100010 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C110000 Res:8C110011 Cmd to Res delay:28800 ns ACK= OK
Cmd:8C120000 Res:8C120012 Cmd to Res delay:38400 ns ACK= OK
Cmd:8C130000 Res:8C130013 Cmd to Res delay:28800 ns ACK= OK
Cmd:8C140000 Res:8C140014 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C150000 Res:9C150014 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C160000 Res:9C160014 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C170000 Res:9C170014 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C180000 Res:8C180018 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C190000 Res:8C190062 Cmd to Res delay:41600 ns ACK= OK
Cmd:8C1A0000 Res:8C1A001A Cmd to Res delay:35200 ns ACK= OK
Cmd:8C1B0000 Res:8C1B001B Cmd to Res delay:28800 ns ACK= OK
Cmd:8C1C0000 Res:8C1C001C Cmd to Res delay:35200 ns ACK= OK
Cmd:8C1D0000 Res:8C1D001D Cmd to Res delay:32000 ns ACK= OK
Cmd:8C1E0000 Res:9C1E0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C1F0000 Res:9C1F0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C200000 Res:9C200000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C210000 Res:9C210000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C220000 Res:9C220000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C230000 Res:9C230000 Cmd to Res delay:12800 ns ACK= CID unknown
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Cmd:8C250000 Res:9C250000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C260000 Res:9C260000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C270000 Res:9C270000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C280000 Res:9C280000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C290000 Res:9C290000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C2A0000 Res:9C2A0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C2B0000 Res:9C2B0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C2C0000 Res:9C2C0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C2D0000 Res:9C2D0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C2E0000 Res:9C2E0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C2F0000 Res:9C2F0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:8C300000 Res:8C300020 Cmd to Res delay:28800 ns ACK= OK

Cmd:8C310000 Res:8C310021 Cmd to Res delay:28800 ns ACK= OK
Cmd:8C320000 Res:8C320022 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C330000 Res:8C330023 Cmd to Res delay:28800 ns ACK= OK
Cmd:8C340000 Res:8C340024 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C350000 Res:8C350025 Cmd to Res delay:32000 ns ACK= OK
Cmd:8C360000 Res:8C360026 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C370000 Res:8C370027 Cmd to Res delay:28800 ns ACK= OK
Cmd:8C380000 Res:8C380028 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C390000 Res:8C3900E3 Cmd to Res delay:32000 ns ACK= OK
Cmd:8C3A0000 Res:8C3A002A Cmd to Res delay:35200 ns ACK= OK
Cmd:8C3B0000 Res:8C3B002B Cmd to Res delay:28800 ns ACK= OK
Cmd:8C3C0000 Res:8C3C000C Cmd to Res delay:35200 ns ACK= OK
Cmd:8C3D0000 Res:8C3D002D Cmd to Res delay:28800 ns ACK= OK
Cmd:8C3E0000 Res:8C3E0000 Cmd to Res delay:35200 ns ACK= OK
Cmd:8C3F0000 Res:AC3F0042 Cmd to Res delay:76800 ns ACK= CID forbidden
Cmd:8C400000 Res:9C400000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:88000000 Res:98000000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:88010000 Res:98010000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:88020000 Res:98020000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:88030000 Res:98030000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:88040000 Res:98040000 Cmd to Res delay:12800 ns ACK= CID unknown
begining of test set cmd BrC
Cmd:B4000020 Res:84000020 Cmd to Res delay:38400 ns ACK= OK
Cmd:B4010021 Res:84010021 Cmd to Res delay:35200 ns ACK= OK
Cmd:B4020022 Res:84020022 Cmd to Res delay:28800 ns ACK= OK
Cmd:B4030023 Res:84030023 Cmd to Res delay:35200 ns ACK= OK
Cmd:B4040024 Res:84040024 Cmd to Res delay:32000 ns ACK= OK
Cmd:B4050025 Res:84050025 Cmd to Res delay:35200 ns ACK= OK
Cmd:B4060026 Res:84060026 Cmd to Res delay:28800 ns ACK= OK
Cmd:B4070027 Res:84070027 Cmd to Res delay:35200 ns ACK= OK
Cmd:B4080028 Res:84080028 Cmd to Res delay:32000 ns ACK= OK
Cmd:B4090029 Res:84090029 Cmd to Res delay:35200 ns ACK= OK
Cmd:B40A002A Res:840A002A Cmd to Res delay:28800 ns ACK= OK
Cmd:B40B002B Res:840B002B Cmd to Res delay:35200 ns ACK= OK
Cmd:B40C002C Res:840C002C Cmd to Res delay:28800 ns ACK= OK
Cmd:B40D002D Res:840D002D Cmd to Res delay:35200 ns ACK= OK
Cmd:B40E002E Res:840E002E Cmd to Res delay:32000 ns ACK= OK
Cmd:B40F002F Res:840F002F Cmd to Res delay:35200 ns ACK= OK
Cmd:B4100030 Res:84100030 Cmd to Res delay:28800 ns ACK= OK
Cmd:B4110031 Res:84110031 Cmd to Res delay:35200 ns ACK= OK
Cmd:B4120032 Res:84120032 Cmd to Res delay:32000 ns ACK= OK
Cmd:B4130033 Res:84130033 Cmd to Res delay:35200 ns ACK= OK
Cmd:B4140034 Res:84140034 Cmd to Res delay:28800 ns ACK= OK
Cmd:B4150035 Res:94150034 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B4160036 Res:94160034 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B4170037 Res:94170034 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B4180038 Res:84180038 Cmd to Res delay:25600 ns ACK= OK
Cmd:B4190039 Res:A4190062 Cmd to Res delay:12800 ns ACK= CID forbidden
Cmd:B41A003A Res:841A003A Cmd to Res delay:28800 ns ACK= OK
Cmd:B41B003B Res:841B003B Cmd to Res delay:35200 ns ACK= OK
Cmd:B41C003C Res:841C003C Cmd to Res delay:28800 ns ACK= OK
Cmd:B41D003D Res:841D003D Cmd to Res delay:35200 ns ACK= OK
Cmd:B41E003E Res:941E0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B41F003F Res:941F0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B4300040 Res:84300040 Cmd to Res delay:25600 ns ACK= OK
Cmd:B4310041 Res:84310041 Cmd to Res delay:35200 ns ACK= OK
Cmd:B4320042 Res:84320042 Cmd to Res delay:28800 ns ACK= OK
Cmd:B4330043 Res:84330043 Cmd to Res delay:35200 ns ACK= OK
Cmd:B4340044 Res:84340044 Cmd to Res delay:32000 ns ACK= OK
Cmd:B4350045 Res:84350045 Cmd to Res delay:35200 ns ACK= OK
Cmd:B4360046 Res:84360046 Cmd to Res delay:28800 ns ACK= OK
Cmd:B4370047 Res:84370047 Cmd to Res delay:35200 ns ACK= OK
Cmd:B4380048 Res:84380048 Cmd to Res delay:28800 ns ACK= OK
Cmd:B4390049 Res:84390049 Cmd to Res delay:35200 ns ACK= OK
Cmd:B43A004A Res:843A004A Cmd to Res delay:35200 ns ACK= OK
Cmd:B43B004B Res:843B004B Cmd to Res delay:32000 ns ACK= OK
Cmd:B43C004C Res:843C000C Cmd to Res delay:32000 ns ACK= OK
Cmd:B43D004D Res:843D004D Cmd to Res delay:32000 ns ACK= OK
Cmd:B43E004E Res:843E0000 Cmd to Res delay:32000 ns ACK= OK
Cmd:B43F004F Res:943F0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B4190162 Res:84190162 Cmd to Res delay:38400 ns ACK= OK
Cmd:B43901E3 Res:843901E3 Cmd to Res delay:32000 ns ACK= OK

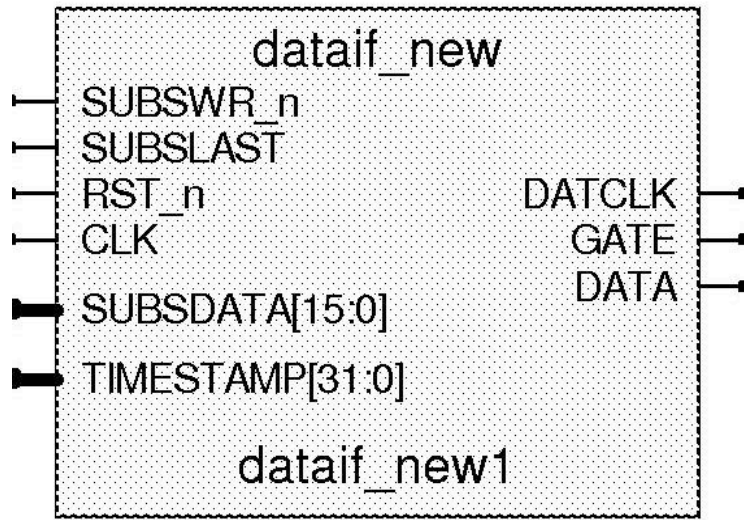
Cmd:B0000000 Res:900000E3 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B0010000 Res:900100E3 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B0020000 Res:900200E3 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B0030000 Res:800300E3 Cmd to Res delay:12800 ns ACK= OK
Cmd:B0040000 Res:900400E3 Cmd to Res delay:12800 ns ACK= CID unknown
begining of test get cmd BrC
Cmd:BC000000 Res:8C000020 Cmd to Res delay:28800 ns ACK= OK
Cmd:BC010000 Res:8C010021 Cmd to Res delay:25600 ns ACK= OK
Cmd:BC020000 Res:8C020022 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC030000 Res:8C030023 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC040000 Res:8C040024 Cmd to Res delay:25600 ns ACK= OK
Cmd:BC050000 Res:8C050025 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC060000 Res:8C060026 Cmd to Res delay:25600 ns ACK= OK
Cmd:BC070000 Res:8C070027 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC080000 Res:8C080028 Cmd to Res delay:25600 ns ACK= OK
Cmd:BC090000 Res:8C090029 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC0A0000 Res:8C0A002A Cmd to Res delay:35200 ns ACK= OK
Cmd:BC0B0000 Res:8C0B002B Cmd to Res delay:25600 ns ACK= OK
Cmd:BC0C0000 Res:8C0C002C Cmd to Res delay:35200 ns ACK= OK
Cmd:BC0D0000 Res:8C0D002D Cmd to Res delay:25600 ns ACK= OK
Cmd:BC0E0000 Res:8C0E002E Cmd to Res delay:35200 ns ACK= OK
Cmd:BC0F0000 Res:8C0F002F Cmd to Res delay:25600 ns ACK= OK
Cmd:BC100000 Res:8C100030 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC110000 Res:8C110031 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC120000 Res:8C120032 Cmd to Res delay:25600 ns ACK= OK
Cmd:BC130000 Res:8C130033 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC140000 Res:8C140034 Cmd to Res delay:25600 ns ACK= OK
Cmd:BC150000 Res:9C150034 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC160000 Res:9C160034 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC170000 Res:9C170034 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC180000 Res:8C180038 Cmd to Res delay:32000 ns ACK= OK
Cmd:BC190000 Res:8C190162 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC1A0000 Res:8C1A003A Cmd to Res delay:25600 ns ACK= OK
Cmd:BC1B0000 Res:8C1B003B Cmd to Res delay:35200 ns ACK= OK
Cmd:BC1C0000 Res:8C1C003C Cmd to Res delay:25600 ns ACK= OK
Cmd:BC1D0000 Res:8C1D003D Cmd to Res delay:35200 ns ACK= OK
Cmd:BC1E0000 Res:9C1E0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC1F0000 Res:9C1F0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC200000 Res:9C200000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC210000 Res:9C210000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC220000 Res:9C220000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC230000 Res:9C230000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC240000 Res:9C240000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC250000 Res:9C250000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC260000 Res:9C260000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC270000 Res:9C270000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC280000 Res:9C280000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC290000 Res:9C290000 Cmd to Res delay:12800 ns ACK= CID unknown
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Cmd:BC2B0000 Res:9C2B0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC2C0000 Res:9C2C0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC2D0000 Res:9C2D0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC2E0000 Res:9C2E0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC2F0000 Res:9C2F0000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:BC300000 Res:8C300040 Cmd to Res delay:25600 ns ACK= OK
Cmd:BC310000 Res:8C310041 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC320000 Res:8C320042 Cmd to Res delay:25600 ns ACK= OK
Cmd:BC330000 Res:8C330043 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC340000 Res:8C340044 Cmd to Res delay:32000 ns ACK= OK
Cmd:BC350000 Res:8C350045 Cmd to Res delay:28800 ns ACK= OK
Cmd:BC360000 Res:8C360046 Cmd to Res delay:32000 ns ACK= OK
Cmd:BC370000 Res:8C370047 Cmd to Res delay:28800 ns ACK= OK
Cmd:BC380000 Res:8C380048 Cmd to Res delay:35200 ns ACK= OK
Cmd:BC390000 Res:8C3901E3 Cmd to Res delay:25600 ns ACK= OK
Cmd:BC3A0000 Res:8C3A004A Cmd to Res delay:35200 ns ACK= OK
Cmd:BC3B0000 Res:8C3B004B Cmd to Res delay:32000 ns ACK= OK
Cmd:BC3C0000 Res:8C3C000C Cmd to Res delay:28800 ns ACK= OK
Cmd:BC3D0000 Res:8C3D004D Cmd to Res delay:32000 ns ACK= OK
Cmd:BC3E0000 Res:8C3E0000 Cmd to Res delay:28800 ns ACK= OK
Cmd:BC3F0000 Res:AC3F0000 Cmd to Res delay:70400 ns ACK= CID forbidden
Cmd:BC400000 Res:9C400000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B8000000 Res:98000000 Cmd to Res delay:12800 ns ACK= CID unknown

```

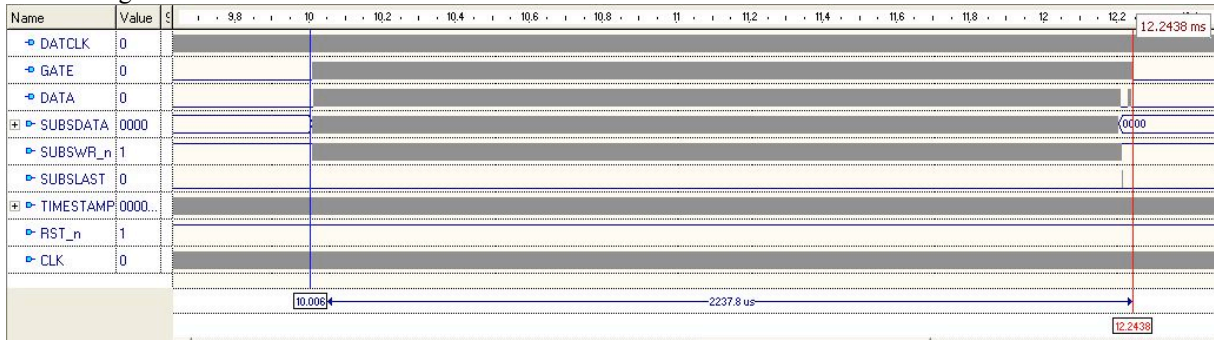
Cmd:B8010000 Res:98010000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B8020000 Res:98020000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B8030000 Res:98030000 Cmd to Res delay:12800 ns ACK= CID unknown
Cmd:B8040000 Res:98040000 Cmd to Res delay:12800 ns ACK= CID unknown
begining of test set cmd Resp_no
Cmd:C40000C0
Cmd:C40100C1
Cmd:C40200C2
Cmd:C40300C3
Cmd:C40400C4
Cmd:C40500C5
Cmd:C40600C6
Cmd:C40700C7
Cmd:C40800C8
Cmd:C40900C9
Cmd:C40A00CA
Cmd:C40B00CB
Cmd:C40C00CC
Cmd:C40D00CD
Cmd:C40E00CE
Cmd:C40F00CF
Cmd:C41000D0
Cmd:C41100D1
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Cmd:C41E00DE
Cmd:C41F00DF
Cmd:C43000E0
Cmd:C43100E1
Cmd:C43200E2
Cmd:C43300E3
Cmd:C43400E4
Cmd:C43500E5
Cmd:C43600E6
Cmd:C43700E7
Cmd:C43800E8
Cmd:C43900E9
Cmd:C43A00EA
Cmd:C43B00EB
Cmd:C43C00EC
Cmd:C43D00ED
Cmd:C43E00EE
Cmd:C43F00EF
Cmd:C419006A
Cmd:C43900EB
Cmd:C0000000
Cmd:C0010000
Cmd:C0020000
Cmd:C0030000
Cmd:C0040000
end of test cmd

```

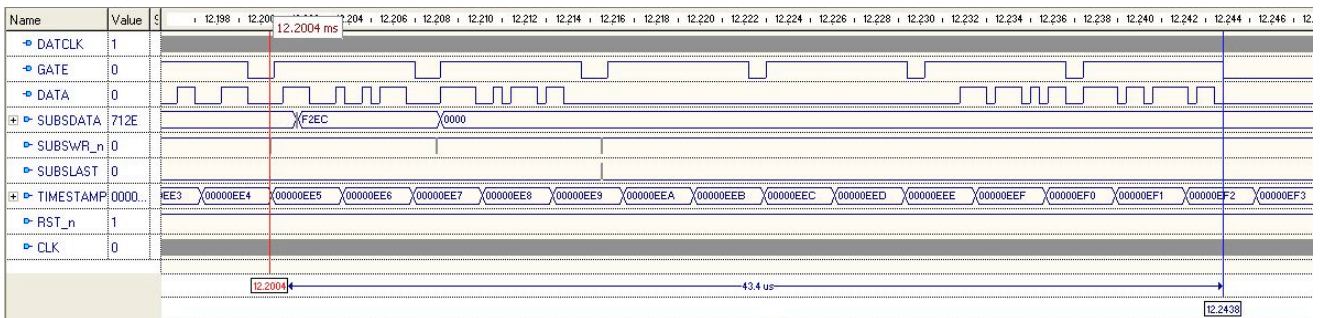
3.9.3.9.2 Data interface:
(VHDL module: dataif_new.vhd)



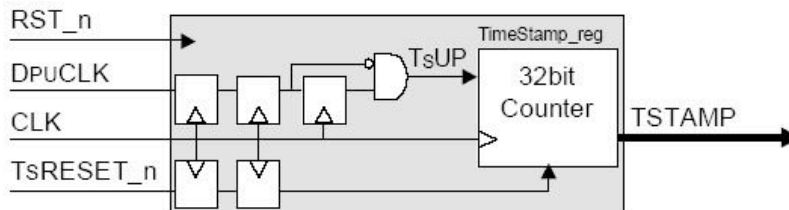
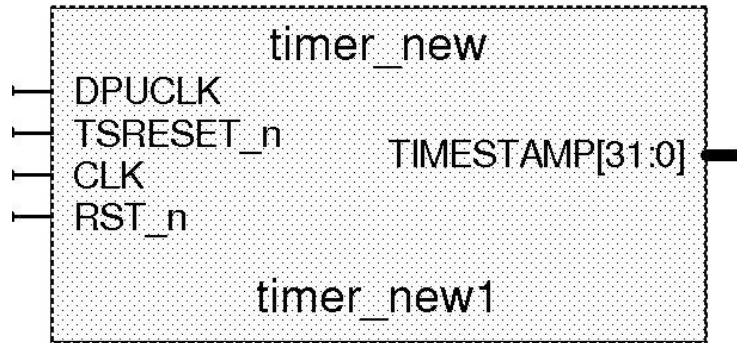
Data timing:



Zoon on the last datas of the frame:



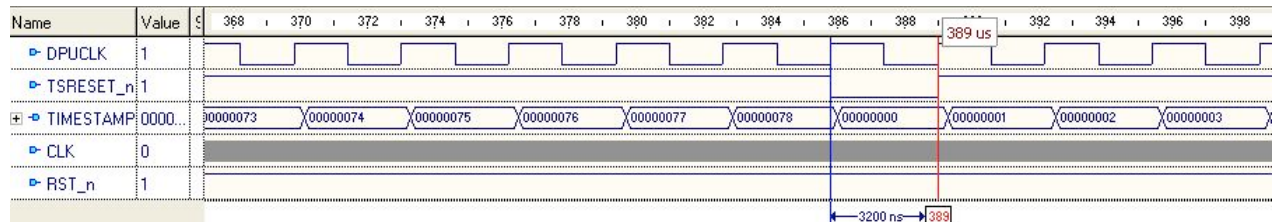
3.9.3.9.3 Timer



A 32-bit Time Stamp value is maintained in a free running counter incremented on the DPUCLK rising edge resynchronised with CLK.

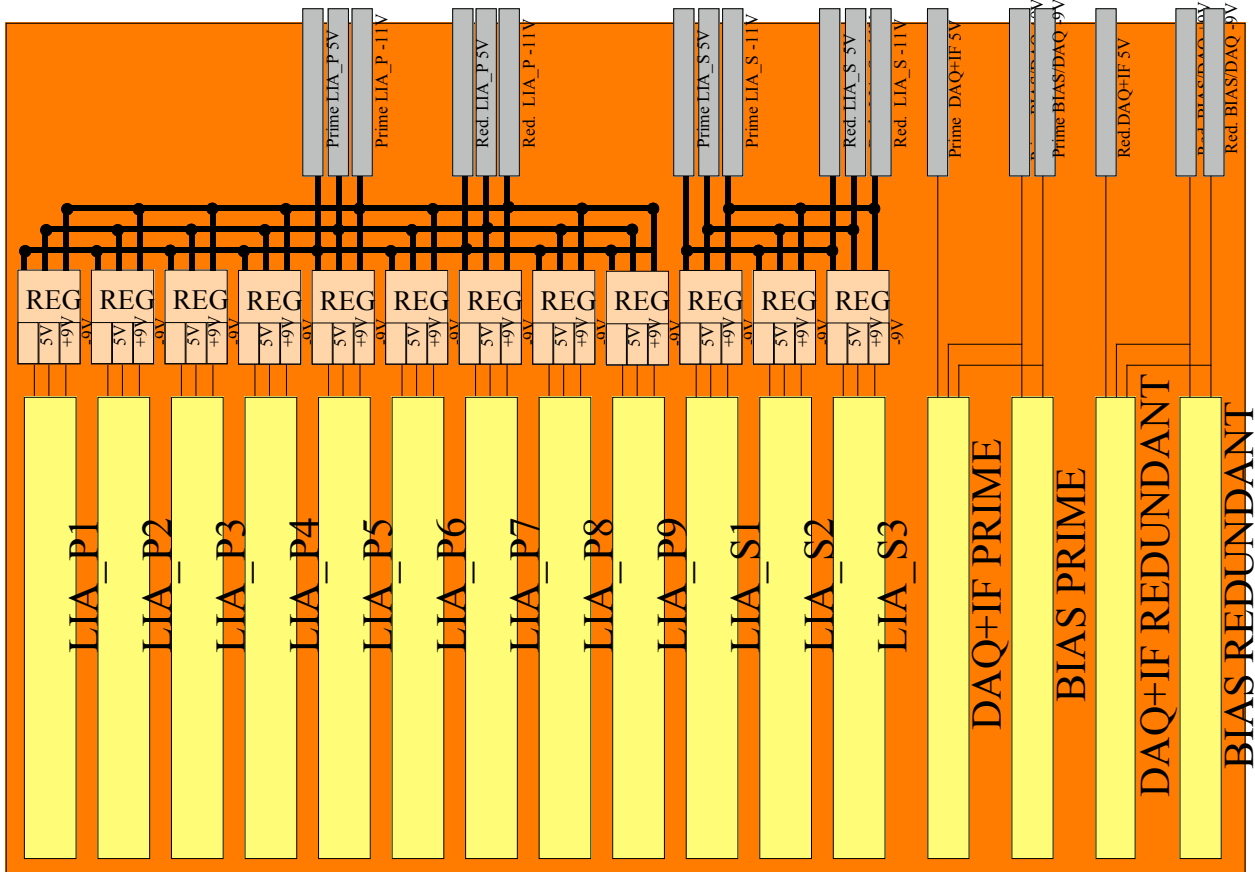
The reset of the Time Stamp is done with the TsRESET_n signal resynchronised with CLK. TsRESET_n is built by CmdIf from the TStampRst DPU command

Timing:



3.10 DCU Power Supply

3.10.1 DCU POWER SUPPLY OVERVIEW



4 PHYSICAL CHARACTERISTICS

4.1 PHYSICAL DESCRIPTION

4.1.1 DCU housing

4.1.1.1 QM2 and FM

All of the DCU electronics are housed in one box. A back plane printed circuit board insures the internal DCU connections.

The DCU is composed in its QM2 and FM versions of:

- 9 LIA_P boards
- 3 LIA_S boards
- 2 BIAS boards (PRIME and REDUNDANT)
- 2 DAQ+I/F boards (PRIME and REDUNDANT)

The layout of these boards is organized as shown in Figure 4-1 DCU Front Panel.

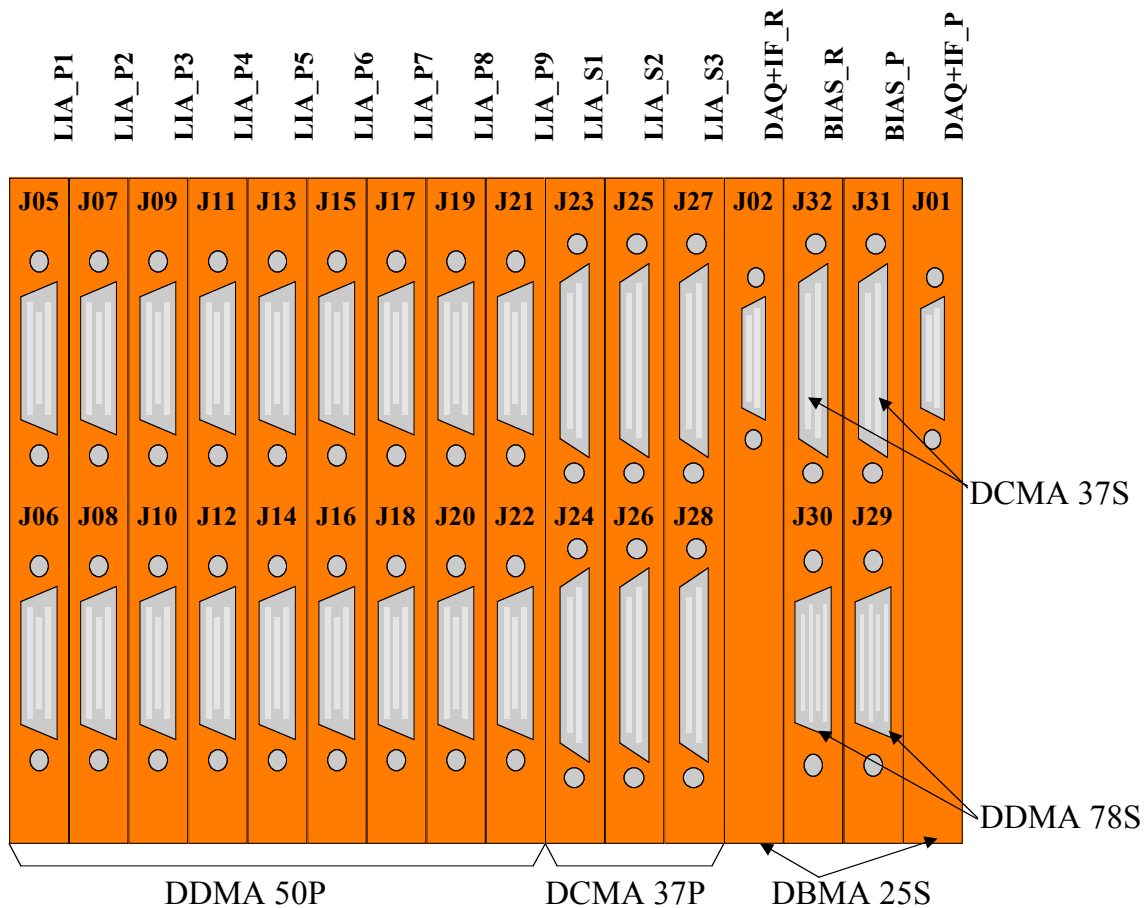


Figure 4-1 DCU Front Panel for QM2 and FM

4.1.2 Back plane

4.1.2.1 QM2 and FM

QM2, and FM all have the same kind of back plane.
The back plane is organized as shown in Figure 4-2 Back Plane.

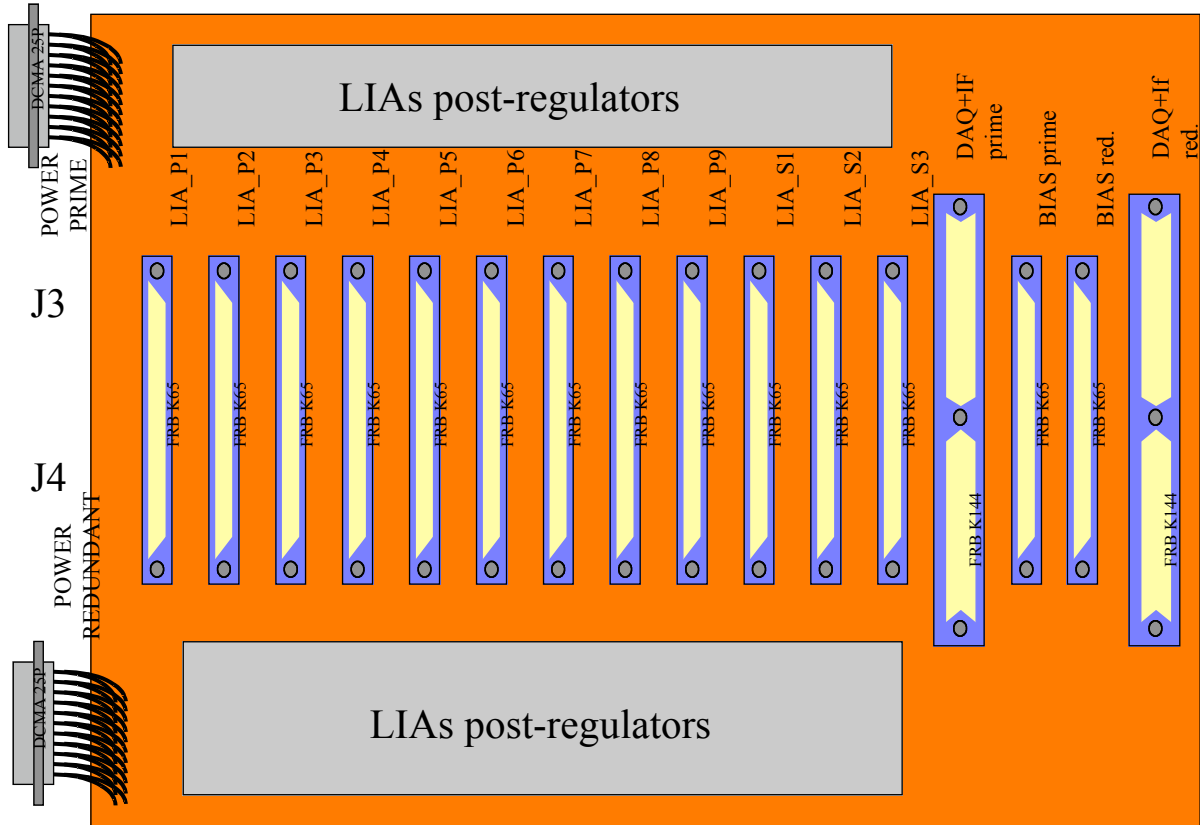


Figure 4-2 Back Plane

5 TRACEABILITY MATRIX

DRCU Subsystem Specification	FUNCTIONS	Description	Check by		
			Design	Simulation	Measurement
DRCU REQ-15	ALL	Number of channels	x		
DRCU REQ-16	DCU-FUNC-11	Short circuit protection	x		
DRCU REQ-17	DCU-FUNC-01	BIAS channels	x		
DRCU REQ-18	DCU-FUNC-01	BIAS individually adjustable	x		
DRCU REQ-19	FUNC-04-01	Bias frequency	x		
DRCU REQ-20	DCU-FUNC-05	DC JFET/heater bias channels	x		
DRCU REQ-21	FUNC-05-1 and FUNC-05-3	VDD/VSS ON/OFF	x		
DRCU REQ-22	FUNC-05-5	Heater ON/OFF	x		
DRCU REQ-23		BIAS redundancy	x		
DRCU REQ-24		DAQ+IF redundancy	x		
DRCU REQ-25	FUNC-04-1	Sampling frequency	x		
DRCU REQ-26	FUNC-04-1	Number of blocks to be transferred	x		
DRCU REQ-27	FUNC-09-3	Temperature measurement	x		
DRCU REQ-28	FUNC-09-3	AD590	x		
DRCU REQ-29	FUNC-09-2 and FUNC-09-1	Temperature range	x		
DRCU REQ-30	FUNC-09-1, FUNC-09-5 and FUNC-09-4	HK	x		
DRCU REQ-31		Conducted RF			
DRCU REQ-32-1	DCU-FUNC-02	Input Signal AC	x		
DRCU REQ-32-2	FUNC-02-2, FUNC-02-3	Input Signal DC	x		
DRCU REQ-32-3	FUNC-02-2, FUNC-02-3, FUNC-02-5	Output Signal AC	x		
DRCU REQ-32-4	FUNC-02-2, FUNC-02-3	Common mode offset			x
DRCU REQ-32-5	DCU-FUNC-02	Cross talk			x
DRCU REQ-32-6	DCU-FUNC-02	Noise $7nV/rt(Hz)$			x
DRCU REQ-32-7	FUNC-02-1	Input capa <math>< 100pF</math>	x		
DRCU REQ-32-8	FUNC-02-1	Input impedance >math>1M\Omega</math>	x		
DRCU REQ-32-9	FUNC-02-5	Bandwidth 0.03 to 5Hz 0.03 to 25Hz	x		
DRCU REQ-32-10	FUNC-02-1, FUNC-02-2, FUNC-02-3	BPF	x		
DRCU REQ-32-11	FUNC-02-5	LPF	x		
DRCU REQ-32-12	FUNC-02-1, FUNC-02-2, FUNC-02-3	Common mode rejection -60dB			x
DRCU REQ-32-14	FUNC-02-1	Interface	x		
DRCU REQ-33		NOISE with thermal drift			x

DRCU Subsystem Specification	FUNCTIONS	Description	Check by		
			Design	Simulation	Measurement
DRCU REQ-34	FUNC-01-4	Spec: 0-100mVrms Photo : 0-140mVrms	x		x
	FUNC-01-4	TC : 0-500mVrms	x		
	FUNC-04-1	50 to 300Hz	x		
	FUNC-01-3	Amplitude resolution	x		
		Load impedance			
		Interface type			
	FUNC-04-1	Sine wave	x		
	FUNC-01-4	Noise 20nVrms/rtHz			x
	FUNC-04-2	Phase	x		
DRCU REQ-35	FUNC-05-1	VSS amplitude	x		
	FUNC-05-1	VSS resolution	x		
	FUNC-05-2	VSS noise			x
	FUNC-05-4	VDDamplitude	x		
	FUNC-05-4	VDD noise			x
	FUNC-05-4	Current range			x
	FUNC-05-4	Voltage stability			x
		Load			
DRCU REQ-36	FUNC-05-2, FUNC-05-4	Overshoot<10%		x	x
DRCU REQ-37		Voltage	x		
		Current	x		
DRCU REQ-38	DCU-FUNC-03	ADC16bit	x		
	FUNC-04-3	<6.2ms	x		
	FUNC-04-3	<1.2ms	x		
	FUNC-02-6	Offset	x		
DRCU REQ-39	FUNC-04-3	frames	x		