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HERSCHEL/SPIRE

DETECTOR CONTROL UNIT
DESIGN DOCUMENT

	Function	Name	Date	Visa
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DOCUMENT STATUS and CHANGE RECORD

Date	Issue	Change(s) made
08/11/2001	0.1	Creation
05/07/2002	0.2	Removed pin out description of connectors
13/01/2003	0.3	Major changes

TABLE OF CONTENTS

PICTURES

List of Acronyms

ADC	Analog to Digital Converter
AMUX	Analog Multiplexer
DPU	Data Processing Unit
DCU	Detector Control Unit
DMUX	Digital Multiplexer
DRCU	Detector Readout & Control Unit
FPU	Focal Plane Unit
JFET	Junction Field Effect Transistor
LIA	Lock-in amplifier
BPF	Band Pass Filter
LPF	Low Pass Filter
NA	Not Applicable
SCU	Sub-system Control Unit
PSU	Power Supply Unit
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
WIH	Warm Interconnect Harnesses
PSW	Photometer Short Wavelength
PMW	Photometer Medium Wavelength
PLW	Photometer Long Wavelength
SSW	Spectrometer Short Wavelength
PSW	Spectrometer Long Wavelength
TC	Temperature Control
BDA	Bolometric Detector Assembly

1 INTRODUCTION

1.1 PURPOSE

The purpose of this document is to show how the DCU electronics is designed and implemented to comply with the DCU subsystem requirements.

1.2 SCOPE

This document deals only with the electronics of the Detector Control Unit.
It covers neither the mechanical nor the thermal aspects of the DCU box.

1.3 OVERALL DOCUMENT DESCRIPTION

First, functions and their interfaces are described: functions are split into sub-functions as necessary and are related to the corresponding functional requirements.

Next, function overall implementations are described.

Then, function implementations are detailed and demonstrations of the capabilities to cover the performance requirements are provided.

Finally, a verification cross table summarizes the compliance to the electronics requirements.

1.4 APPLICABLES DOCUMENTS

AD1	DRCU Interface Control DOCUMENT	Sap-SPIRE-CCA- 075-02	1.0
AD2	DRCU Subsystem Specification	Sap-SPIRE-CCA-25-00	1.0
AD3			
AD4	Spire harness definition	SPIRE-RAL-PRJ-000608	1.0
AD5	Spire instrument block diagram	SPIRE-RAL-DWG-000646	5.1
AD6	DRCU/DPU Interface Control DOCUMENT	Sap-SPIRE-CCA- 076-02	0.7

1.5 REFERENCES DOCUMENTS

RD1	MAT02 data sheet		REV.C
RD2	OP-400 data sheet		
RD3			
RD4			
AD5			

2   GENERAL DESCRIPTION

2.1   DCU FUNCTIONAL DESCRIPTION

The DCU functional diagram is shown here after:

This DCU diagram represents functions as well as communication between them.
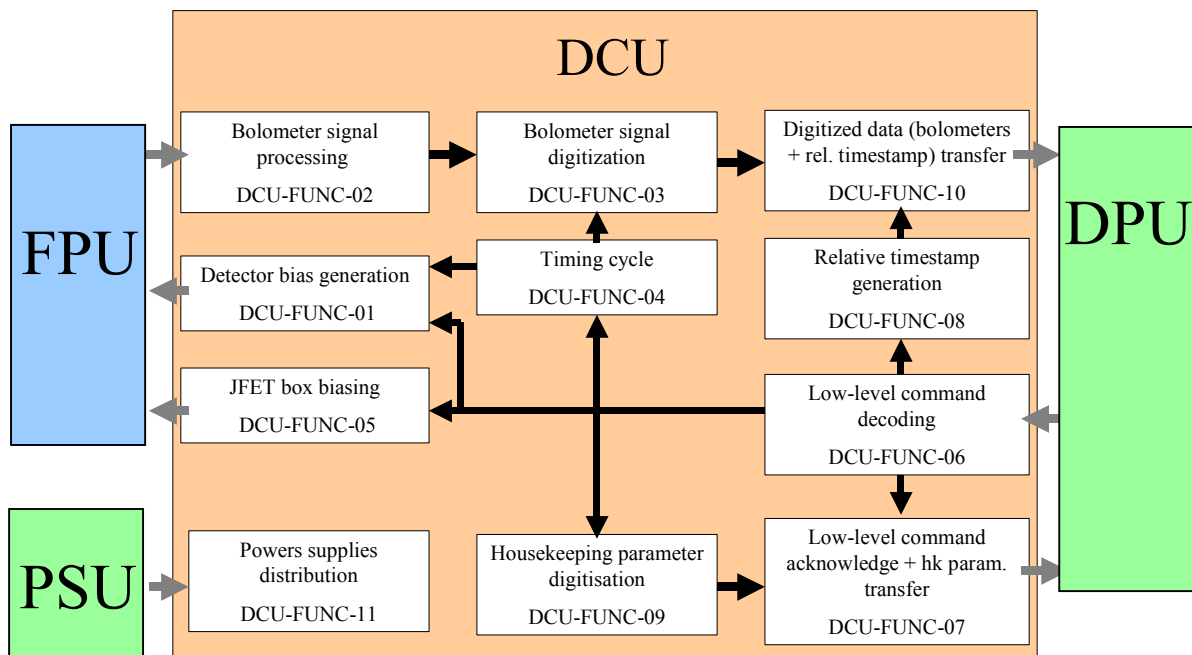
Figure 2-1: DCU Functional diagram

In the following paragraphs each function is detailed into elementary functions.

NOTE: DCU-FUN-xx and DRCU REQ-yy come from AD2

2.1.1 DCU-FUNC-01 (Detector bias generation)

2.1.1.1 Diagram
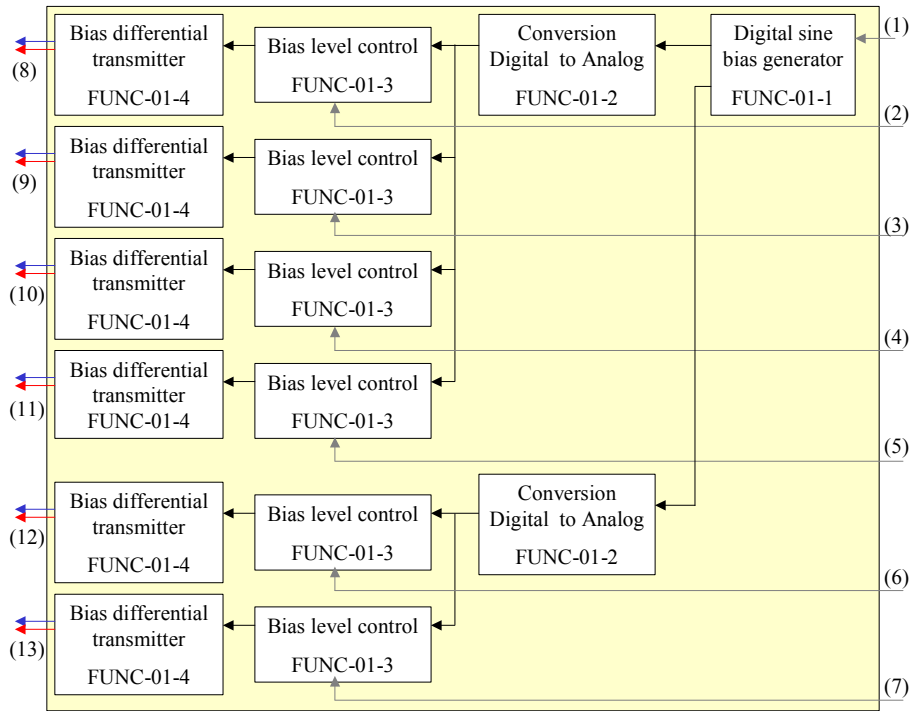
Figure 2-2: DCU-FUNC-01 diagram

2.1.1.2 Interface list

(1) Interface **SINE_GENERATOR**: carries the sine wave clock and the generator mode for the spectrometer and the photometer
(2) Interface **AMPL_BIAS_PSW**: commands the first bias level.
(3) Interface **AMPL_BIAS_PMW**: commands the second bias level.
(4) Interface **AMPL_BIAS_PLW**: commands the third bias level.
(5) Interface **AMPL_BIAS_TC**: commands the fourth bias level.
(6) Interface **AMPL_BIAS_SSW**: commands the fifth bias level.
(7) Interface **AMPL_BIAS_SLW**: commands the sixth bias level.
(8) Interface **BIAS_PSW**: biases the BDA PSW.
(9) Interface **BIAS_PMW**: biases the BDA PMW.
(10) Interface **BIAS_PLW**: biases the BDA PLW.
(11) Interface **BIAS_TC**: biases the BDA TC.
(12) Interface **BIAS_SSW**: biases the BDA SSW.
(13) Interface **BIAS_SLW**: biases the BDA SLW.

2.1.1.3   Functional requirement list

DRCU REQ-17: The DCU-FUNC-01 has 6 bias channels.

DRCU REQ-18: Each channel level is individually adjustable by a low-level command:

SetPhotoBiasAmplSW* set the PSW bias level.
SetPhotoBiasAmplMW* set the PMW bias level.
SetPhotoBiasAmplLW* set the PLW bias level.
SetPhotoBiasAmplTC* set the TC bias level.
SetSpectroBiasAmplSW* set the SSW bias level.
SetSpectroBiasAmplLW* set the SLW bias level.

DRCU REQ-19: The two following commands set the frequency of the photometer and the spectrometer:

SetPhotoBiasFreq* and SetSpectroBiasFreq*

Two commands switch the bias generators between a sine waveform and an adjustable DC level, independently for both photometer and spectrometer:

SetPhotoBiasMode* and SetSpectroBiasMode*

Note: The temperature channels are considered as part of the photometer

*see AD6

2.1.1.4   Physical implementation

The two FUNC-01-2 functions, the six FUNC-01-3 functions and the six FUNC-01-4 functions are implemented on the BIAS BOARD.
The function FUNC-01-1 is implemented in the FPGA of the DAQ+IF BOARD.

The interfaces AMPL_BIAS_PSW, AMPL_BIAS_PMW, AMPL_BIAS_PLW, AMPL_BIAS_TC, AMPL_BIAS_SSW, AMPL_BIAS_SLW and the data transmission between FUNC-01-1 and the two functions FUNC-01-2 is made by two serials links (one for the photometer and one for the spectrometer).

The performance and the implementation of the functions FUNC-01-2, FUNC-01-3, FUNC-01-4 and the serial link bias board side are described in the BIAS BOARD section.

The FUNC-01-1 and the other end of the serial link are described in the DAQ+IF board section.

2.1.2 DCU-FUNC-02 (Bolometer signal processing)

2.1.2.1 Diagram
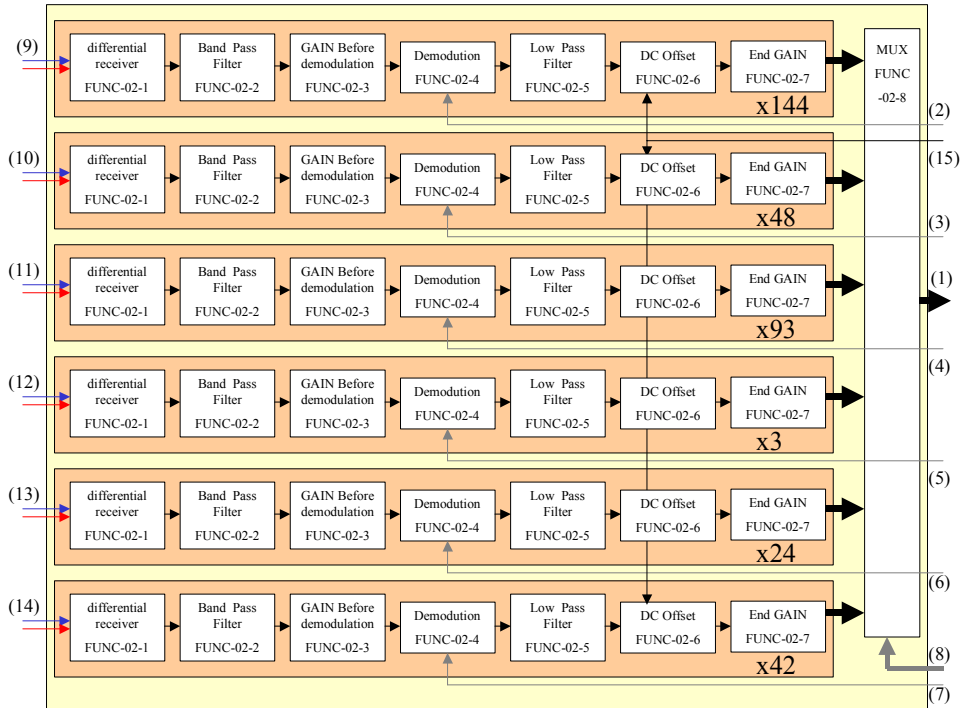
Figure 2-3: DCU-FUNC-02 diagram

2.1.2.2 Interface list

(1)   Interface **INPUT_ADC**: multiplexed channels to be digitized.
(2)   Interface **DEMOD_PSW**: demodulation signal for PSW BDA.
(3)   Interface **DEMOD_PLW**: demodulation signal for PLW BDA.
(4)   Interface **DEMOD_PMW**: demodulation signal for PMW BDA.
(5)   Interface **DEMOD_TC**: demodulation signal for TC BDA.
(6)   Interface **DEMOD_SLW**: demodulation signal for SLW BDA.
(7)   Interface **DEMOD_SSW**: demodulation signal for SSW BDA.
(8)   Interface **CMD_MUX**: commands mux positions.
(9)   Interface **IN_PSW**: modulated signals from BDA PSW.
(10)   Interface **IN_PLW**: modulated signals from BDA PLW.
(11)   Interface **IN_PMW**: modulated signals from BDA PMW.
(12)   Interface **IN_TC**: modulated signals from BDA TC.
(13)   Interface **IN_SLW**: modulated signals from BDA SLW.
(14)   Interface **IN_SSW**: modulated signals from BDA SSW.
(15)   Interface **CMD_OFFSET**: commands offsets.

2.1.2.3   Functional requirement list

DRCU REQ-15:

The DCU-FUNC-02 has 48 PLW channels, 93 PMW channels, 3 TC channels, 144 PSW channels, 24 SLW channels and 48 SSW channels.

DRCU REQ-32-6

To achieve a noise level of 7nVrms/rtHz as seen in the post demodulation after digitization:

The noise level for ADC with 5V full scale is about 58 µVrms (*adc_noise* value found by test). In order to have this noise equivalent to less than 5nVrms/√Hz *(in_noise)*at the input of the bolometer signal processing function, the gain should be:

- for the photometer greater than $\dfrac{adc\_noise}{in\_noise.\sqrt{photo\_BW}}=5187$ (0)

- for the photometer greater than $\dfrac{adc\_noise}{in\_noise.\sqrt{spectro\_BW}}=2320$

As such the noise level allocated to the bolometer signal processing is 5nVrms/rtHz.

DRCU REQ-32-1

In order to not saturate at an input voltage of 11mVmrs (at photometer inputs) and 17mVrms (at spectrometer inputs) the gains limits are going to be set as following:

The absolute maximum gain for a photometer signal before demodulation (FUNC-02-3) is:

$$\frac{5}{0,011.\sqrt{2}}=321 \qquad (1)$$

The absolute maximum gain for a spectrometer signal before demodulation (FUNC-02-3) is:

$$\frac{5}{0,017.\sqrt{2}}=207 \qquad (2)$$

The absolute maximum gain for a complete photometer channel before offset subtraction (FUNC-02-6) is:

$$\frac{5}{0,011}=454 \qquad (3)$$

The absolute maximum gain for a complete spectrometer channel before offset subtraction (FUNC-02-6) is:

$$\frac{5}{0,017}=294 \qquad (4)$$

Photometer LPF functions (FUNC-02-5) are 4 poles Bessel filters. Their structural gain is:

$$1.93 \qquad (5)$$

Spectrometer LPF functions (FUNC-02-5) are 6 poles Bessel filters. Their structural gain is:

$$3.03 \qquad (6)$$

So, in order to have the maximum gain (4), the photometer gain before demodulation (FUNC-02-3) shall be:

$$\frac{454.\pi}{1.93 \times 2\sqrt{2}} = 261$$

This value is compliant with (1)

So, in order to have the maximum gain (5), the spectrometer gain before demodulation (FUNC-02-3) shall be:

$$\frac{294.\pi}{3.03 \times 2\sqrt{2}} = 107$$

This value is compliant with (2)

From previous calculation (0), the end gain (FUNC-02-7) shall not be less than:

- 11.4 for the photometer.
- 8 for the spectrometer.

2.1.2.4   Physical implementation

The functions FUNC-02-1, FUNC-02-2, FUNC-02-3, FUNC-02-4, FUNC-02-5 and a part of FUNC-02-8 are implemented on the 9 LIA_P boards and 3 LIA_S boards.

The functions FUNC-02-6, FUNC-02-7 and the second part of FUNC-02-8 are implemented on the DAQ+IF BOARD.

The performance and the implementation of the functions FUNC-02-1, FUNC-02-2, FUNC-02-3, FUNC-02-4, FUNC-02-5 and the first part of FUNC-02-8 are described in the LIAs sections.

The functions FUNC-02-6, FUNC-02-7 and the second part of FUNC-02-8 are described in the DAQ+IF board section.

2.1.3   DCU-FUNC-03 (Bolometer signal digitization)

This function is made by six 16 bit ADC. Their acquisition timing is drive by the function DCU-FUNC-04 (timing cycle). They digitize the six analog signals provided by the function DCU-FUNC-02 (bolometer signal processing).

The function DCU-FUNC-03 is described in the DAQ+IF board section.

2.1.4 DCU-FUNC-04 (Timing cycle)

2.1.4.1 Diagram
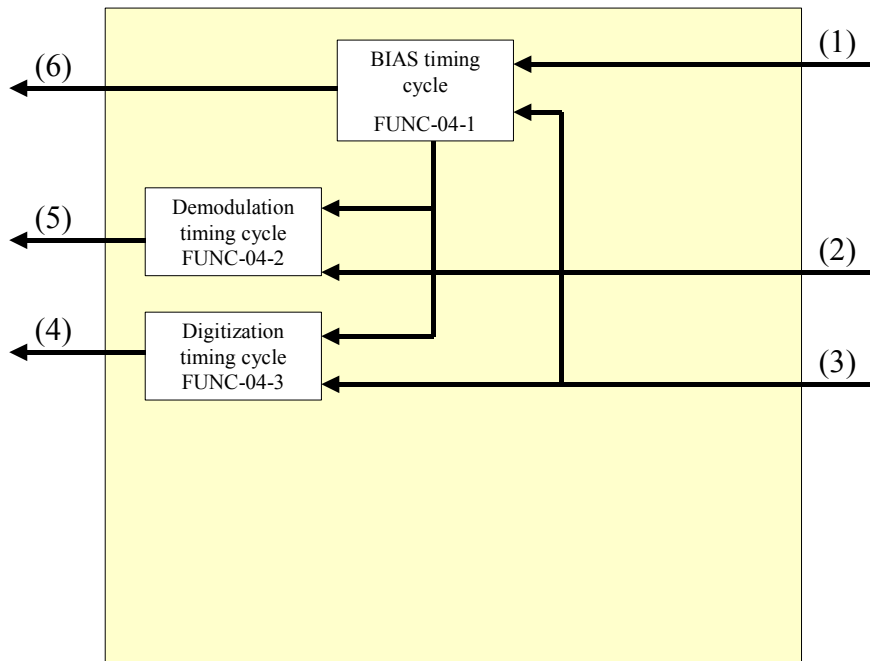
Figure 2-4: DCU-FUNC-04 diagram

2.1.4.2 Interface list

(1) Interface **CMD_FREQUENCY**: commands the bias frequency and the sample frequency.
(2) Interface **CMD_DEMOD**: commands the phase shift for each demodulation signals.
(3) Interface **CMD_MODE**: selects the different modes.
(4) Interface **CONTROL**: operates the MUXs, the offsets, the ADCs.
(5) Interface **DEMOD_SIGNALS**: gives 6 demodulation signals.
(6) Interface **BIAS_CLK**: is the bias clock for the bias generator.

2.1.4.3 Functional requirement list

DRCU REQ-25:

In FUNC-04-1, the 10MHz main clock is divided by the parameter PhotoMClkDiv when DataMode is in Photometer, and by the parameter SpectroMClkDiv when DataMode is in Spectrometer to give a clock 256 times the bias frequency.
The bias frequency is divided by 1+PhotoBiasDiv when DataMode is in Photometer, or by 1+SpectroBiasDiv when DataMode is in Spectrometer to give a clock at the sampling frequency.

DRCU REQ-26:

The number of blocks to be transferred is selected by the command SetFrameCounter

DRCU REQ-38:

In FUNC-04-3, a cycle takes less than 6.2ms for a complete picture of the photometer and less than 1.2ms for the spectrometer one.

The FUNC-04-2 generates the demodulation signals at the bias frequency:

Each BDA group signal has its own demodulation signal adjustable in phase by a low-level command:

SetPhotoDemodSW* set the PSW demodulation signal phase shift.
SetPhotoDemodMW* set the PMW demodulation signal phase shift.
SetPhotoDemodLW* set the PLW demodulation signal phase shift.
SetPhotoDemodTC* set the TC demodulation signal phase shift.
SetSpectroDemodSW* set the SSW demodulation signal phase shift.
SetSpectroDemodLW* set the SLW demodulation signal phase shift.

see AD1

2.1.4.4 Physical implementation

All the functions are implemented in the FPGA. See the FPGA section.

2.1.5   DCU-FUNC-05 (JFET box biasing)
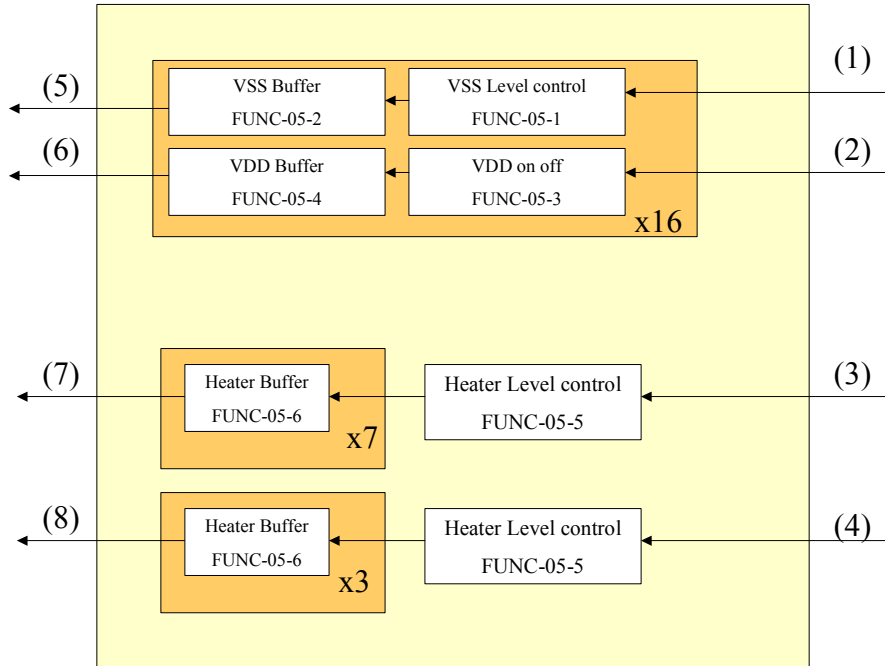
Figure 2-5: DCU-FUNC-05 diagram

2.1.5.1   Interface list

- (1)   Interface **CMD_VSS**: commands VSS levels.
- (2)   Interface **CMD_VDD**: commands VDD ON/OFF.
- (3)   Interface **CMD_HEATER_PH**: commands heater photometer level.
- (4)   Interface **CMD_ HEATER_SP**: commands heater spectrometer level.
- (5)   Interface **VSS**: is the group of VSS signals.
- (6)   Interface **VDD**: is the group of VDD signals.
- (7)   Interface **HEATER_PH**: is the group of heater photometer signals.
- (8)   Interface **HEATER_SP**: is the group of heater spectrometer signals.

2.1.5.2 Functional requirement list

DRCU REQ-20: The DCU-FUNC-05 has 16 JFET bias channels and 2 JFET heater bias channels

DRCU REQ-21:

Each VSS channel level is individually adjustable by a low-level command from 0V (OFF) to –5V:

SetPhSWJfetVSS1* set the PSW VSS1 level.
SetPhSWJfetVSS2* set the PSW VSS2 level.
SetPhSWJfetVSS3* set the PSW VSS3 level.
SetPhSWJfetVSS4* set the PSW VSS4 level.
SetPhSWJfetVSS5* set the PSW VSS5 level.
SetPhSWJfetVSS6* set the PSW VSS6 level.

SetPhMWJfetVSS1* set the PMW VSS1 level.
SetPhMWJfetVSS2* set the PMW VSS2 level.
SetPhMWJfetVSS3* set the PMW VSS3 level.
SetPhMWJfetVSS4* set the PMW VSS4 level.

SetPhLWJfetVSS1* set the PLW VSS1 level.
SetPhLWJfetVSS2* set the PLW VSS2 level.

SetTCJfetVSS1* set the TC VSS1 level.

SetSpSWJfetVSS1* set the SSW VSS1 level.
SetSpSWJfetVSS2* set the SSW VSS2 level.

SetSpLWJfetVSS1* set the SLW VSS1 level.

Each VDD channel level is individually switched ON or OFF by a low-level command:

SetPhSWJfetPwr* with the parameter PSW_JFET_1* switch On/Off the PSW VDD1 level.
SetPhSWJfetPwr* with the parameter PSW_JFET_2* switch On/Off the PSW VDD2 level.
SetPhSWJfetPwr* with the parameter PSW_JFET_3* switch On/Off the PSW VDD3 level.
SetPhSWJfetPwr* with the parameter PSW_JFET_4* switch On/Off the PSW VDD4 level.
SetPhSWJfetPwr* with the parameter PSW_JFET_5* switch On/Off the PSW VDD5 level.
SetPhSWJfetPwr* with the parameter PSW_JFET_6* switch On/Off the PSW VDD6 level.

SetPhMLTCWJfetPwr* with the parameter PMW_JFET_1* switch On/Off the PMW VDD1 level.
SetPhMLTCWJfetPwr* with the parameter PMW_JFET_2* switch On/Off the PMW VDD2 level.
SetPhMLWTCJfetPwr* with the parameter PMW_JFET_3* switch On/Off the PMW VDD3 level.
SetPhMLWTCJfetPwr* with the parameter PMW_JFET_4* switch On/Off the PMW VDD4 level.

SetPhMLWTCJfetPwr* with the parameter PLW_JFET_1* switch On/Off the PLW VDD1 level.

SetPhMLWTCJfetPwr* with the parameter PLW_JFET_2* switch On/Off the PLW VDD2 level.

SetPhMLWTCJfetPwr* with the parameter TC_JFET* switch On/Off the TC VDD1 level.

SetSpSLWJfetPwr* with the parameter SLW_JFET_1* switch On/Off the SLW VDD1 level.

SetSpSLWJfetPwr* with the parameter SSW_JFET_1* switch On/Off the SSW VDD1 level.

SetSpSLWJfetPwr* with the parameter SSW_JFET_2* switch On/Off the SSW VDD2 level.

DRCU REQ-22:

Each heater channel level is individually adjustable by a low-level command from 0V (OFF) to –5V:

SetPhotoHeaterBias* set the photometer heater level.
SetSpectroHeaterBias* set the spectrometer heater level.

2.1.5.3   Physical implementation

The complete FUNC-05 is implemented on the BIAS BOARD.

The same two serials links described with the FUNC-02 realize the interfaces CMD_VSS, CMD_VDD, CMD_HEATER_PH and CMD_HEATER_SP.

The performance and the implementation of the function FUNC-05 are described in the BIAS BOARD section.

2.1.6   DCU-FUNC-06 (Low-level command decoding)

See FPGA section.

2.1.7   DCU-FUNC-07 (Low-level command acknowledge + hk parameter transfer)

See FPGA section.

2.1.8   DCU-FUNC-08 (Relative timestamp generation)

See FPGA section.

2.1.9   DCU-FUNC-09 (Housekeeping parameter digitization)
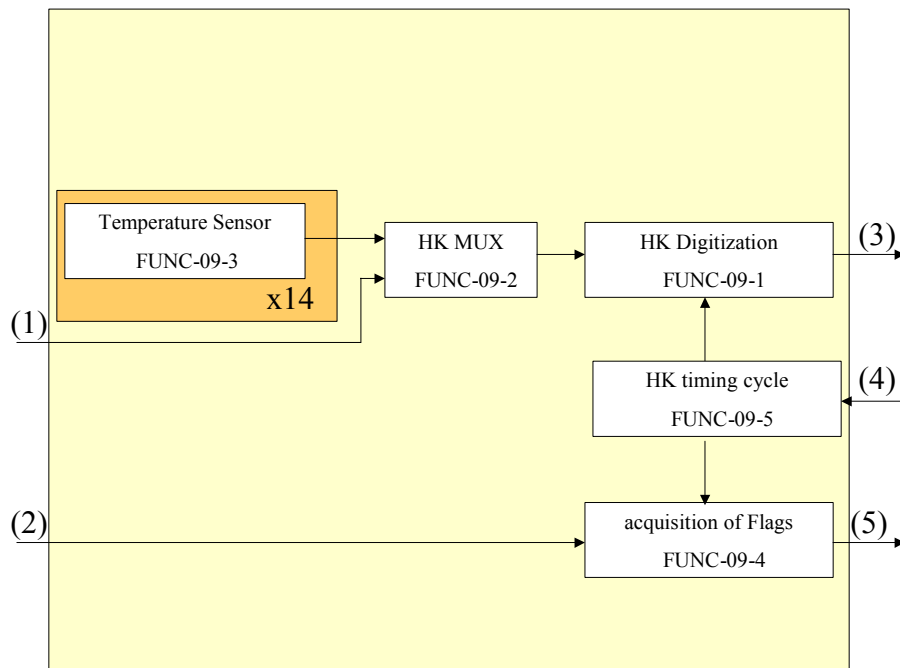
Figure 2-6: DCU-FUNC-09 diagram

2.1.9.1   Interface list

(1)   Interface **SUPPLIES**: power supplies signals.
(2)   Interface **FLAGS**: flags signals.
(3)   Interface **D_HK**: hk values.
(4)   Interface **CMD_HK**: commands the HK digitization.
(5)   Interface **D_FLAG**: flags values.

2.1.9.2   Functional requirement list

DRCU REQ-28: Each board has an AD590 temperature sensor.

2.1.9.3   Physical implementation

The functions FUNC-09-1, FUNC-09-2 and FUNC-09-4 are implemented on the DAQ+IF BOARD.

The performances and the implementations of these functions are described in the DAQ+IF BOARD section.

Function FUNC-09-3, each board has its temperature sensor.

2.1.10   DCU-FUNC-10 (Digitized data transfer)

See FPGA section.

2.1.11   DCU-FUNC-11 (Powers supplies distribution)

See DCU Power Supply section.

3   PERFOMANCE
3.1   PHYSICAL REPARTITION OF THE DCU FUNCTIONS

DCU functions repartition
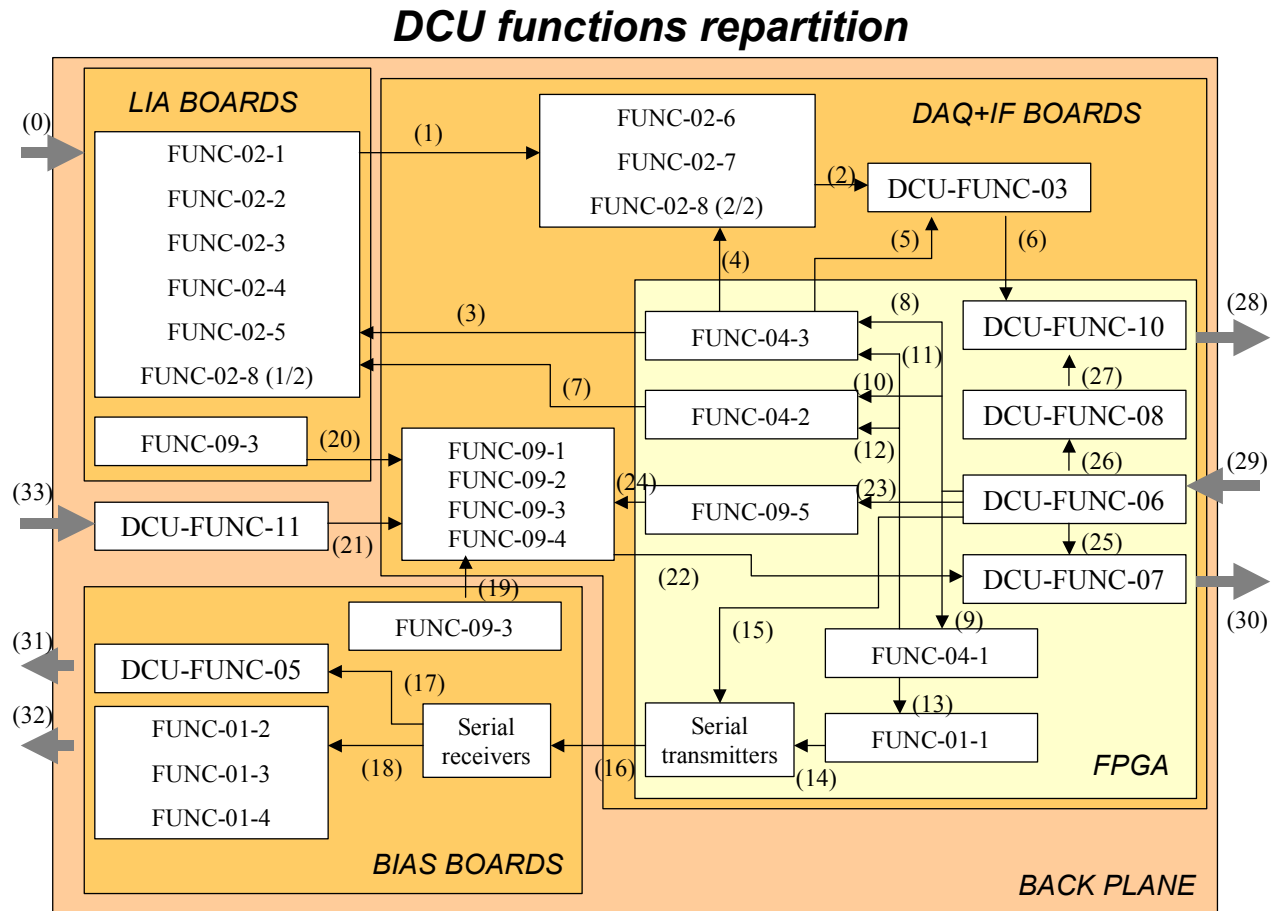
Figure 3-1: DCU functions repartition

Number	Link	Description
(0)	IN_PSW	Modulated signals from BDA PSW.
	IN_PLW	Modulated signals from BDA PLW.
	IN_PMW	Modulated signals from BDA PMW.
	IN_TC	Modulated signals from BDA TC.
	IN_SLW	Modulated signals from BDA SLW.
	IN_SSW	Modulated signals from BDA SSW.
(1)	MUX_CHANNELS	Multiplexed channels after the first mux stage.
(2)	INPUT_ADC	Multiplexed channels after the second mux stage.
(3)	CMD_MUX_L	Mux LIA commands
(4)	CMD_MUX_H	Mux DAQ+IF commands
	CMD_OFFSET	Offset commands
(5)	CMD_ADC	ADC commands
(6)	DATA_ADC	ADC data
(7)	DEMOD_PLW	Demodulation signal for PLW BDA.
	DEMOD_PMW	Demodulation signal for PMW BDA.
	DEMOD_TC	Demodulation signal for TC BDA.
	DEMOD_SLW	Demodulation signal for SLW BDA.
	DEMOD_SSW	Demodulation signal for SSW BDA.
	DEMOD_PLW	Demodulation signal for PLW BDA.
(8) (9)	CMD_MODE	Modes commands
(9)	CMD_FREQUENCY	Bias frequency and Sample frequency commands
(10)	CMD_DEMOD	Phases shift demodulation commands
(11)	SAMPLE_CLK	Sample clock
(12)(13)	BIAS_CLK	BIAS clock
(14)(17)(16)	SINE_WAVE_D	Data of the sine wave
(15)(17)(16)	AMPL_BIAS_PSW	First bias level command
	AMPL_BIAS_PMW	Second bias level command
	AMPL_BIAS_PLW	Third bias level command
	AMPL_BIAS_TC	Fourth bias level command
	AMPL_BIAS_SSW	Fifth bias level command
	AMPL_BIAS_SLW	Sixth bias level command
(15)(18)(16)	CMD_VSS	VSS levels commands
	CMD_VDD	VDD ON/OFF commands.
	CMD_HEATER_PH	Heater photometer level commands.
	CMD_HEATER_SP	Heater spectrometer level commands.
(19)	BIAS_TEMPERATURE	BIAS board temperature
(20)	LIA_TEMPERATURE	LIA boards temperature
(21)	SUPLIES	Powers supplies signals
	FLAGS	Flags signals
(22)	D_HK	HK values
	D_FLAG	Flags values
(23)	CMD_HK	HK commands
(24)	HK_CYCLE_SIG	HK cycle signals
(25)	CMD_ACK&STATUS	Commands acknowledge and DCU status
(26)	TIME_RST	Timestamp reset
(27)	TIME_DATA	Timestamp data
(28)	DATA	Instrument data
(29)	CMD	DPU commands
(30)	HK_ACK	HK and acknowledge
(31)	VSS/VDD/HEATER	JFET DC bias
(32)	BIAS	Bolometer bias
(33)	POWER	Powers supplies

Function	Detail	Description	Note	Pictogram
DCU-FUNC-01 Detector bias generation	FUNC-01-1	Digital sine generator	1 prime / 1 redundant	
	FUNC-01-2	Conversion digital to analog	2 prime / 2 redundant	
	FUNC-01-3	Bias Level control	6 prime / 6 redundant	
	FUNC-01-4	Bias differential transmitter	6 prime / 6 redundant	
DCU-FUNC-02 Bolometer signal processing	FUNC-02-1	Differential receiver	288 photo / 72 spectro	
	FUNC-02-2	Band pass filter	288 photo / 72 spectro	
	FUNC-02-3	Gain before demodulation	288 photo / 72 spectro	
	FUNC-02-4	Demodulation	288 photo / 72 spectro	
	FUNC-02-5	Low pass filter	288 photo / 72 spectro	
	FUNC-02-6	DC offset	288 photo / 72 spectro for prime and redundant	
	FUNC-02-7	End gain	6 prime / 6 redundant	
	FUNC-02-8	Mux N to M	(1/2) 18 mux 16 to 1 photo 6 mux 16 to 1 spectro (2/2) 6 mux 3 to 1 photo 6 mux 1 to 1 spectro For prime and redundant	
DCU-FUNC-03	x	Bolometer signal digitization	1 prime / 1 redundant	
DCU-FUNC-04 Timing cycle	FUNC-04-1	Bias timing cycle	1 prime / 1 redundant	
	FUNC-04-2	Demodulation timing cycle	1 prime / 1 redundant	
	FUNC-04-3	Digitization timing cycle	1 prime / 1 redundant	
DCU-FUNC-05 JFET box biasing	FUNC-05-1	Vss control level	16 prime / 16 redundant	
	FUNC-05-2	VSS buffer	16 prime / 16 redundant	
	FUNC-05-3	VDD on / off	16 prime / 16 redundant	
	FUNC-05-4	VDD buffer	16 prime / 16 redundant	
	FUNC-05-5	Heater control level	2 prime / 2 redundant	
	FUNC-05-6	Heater buffer	10 prime / 10 redundant	
DCU-FUNC-06	x	Low-level command decoding	1 prime / 1 redundant	
DCU-FUNC-07	x	Low-level command acknowledge + HK parameter transfer	1 prime / 1 redundant	
DCU-FUNC-08	x	The relative timestamp generation	1 prime / 1 redundant	
DCU-FUNC-09 JFET box biasing	FUNC-09-1	HK digitization	1 prime / 1 redundant	
	FUNC-09-2	HK mux	1 prime / 1 redundant	
	FUNC-09-3	Temperature sensor	14 prime / 14 redundant	
	FUNC-09-4	Flags acquisition	1 prime / 1 redundant	
	FUNC-09-5	HK timing cycle	1 prime / 1 redundant	
DCU-FUNC-10	x	Digitized data transfer	1 prime / 1 redundant	
DCU-FUNC-11	x	Powers supplies distribution		

3.2 PHYSICAL OVERVIEW

The following drawing shows:
- How the DCU is connected to the FPU.
- The different harness types and their location.
- That the DCU power supply is provided by the PSU.
- The data exchange link with the DPU PRIME and REDUNDANT.
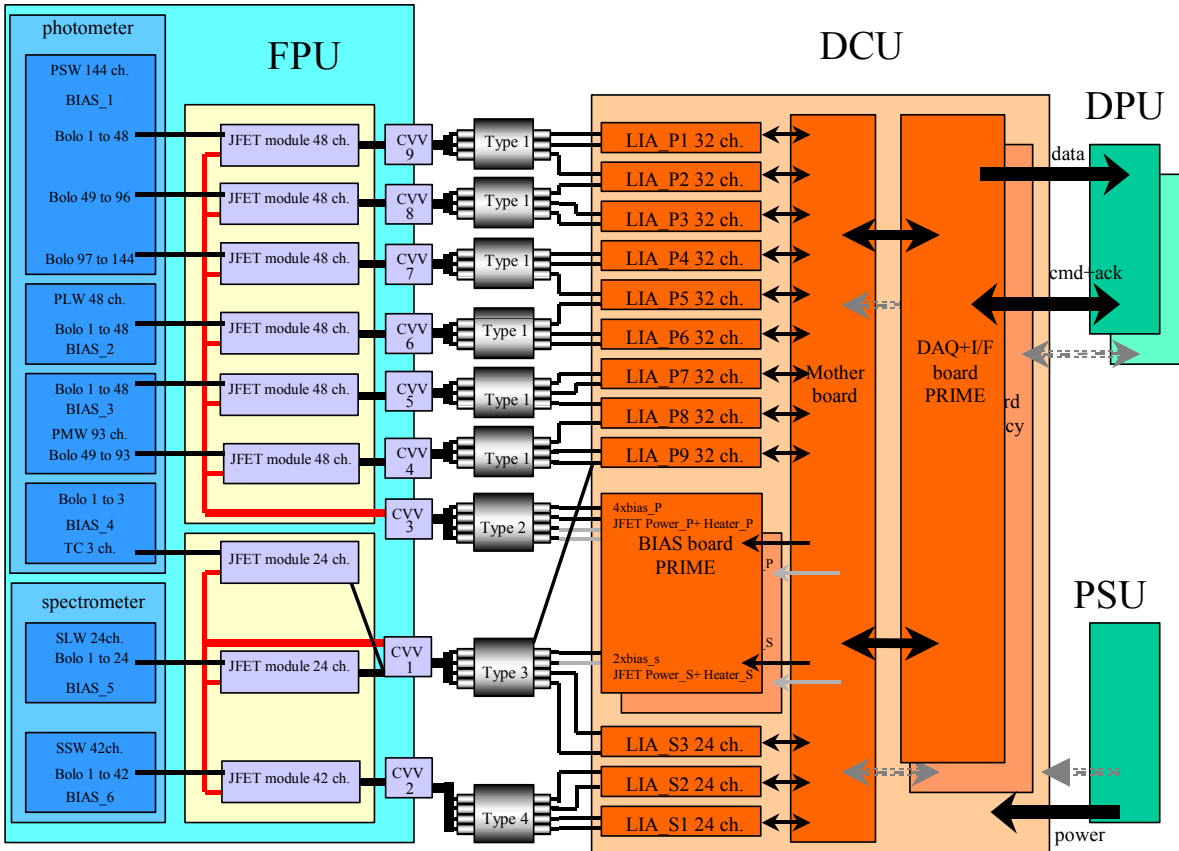
Figure 3-2: DCU Overview

3.3   PHOTOMETER

Nine LIA_P boards make up the LIA photometer section.

1.   LIA_P1 to LIA_P4 and the first 16 channels of LIA_P5 will receive and process the signals from 144 "PSW bolometers."
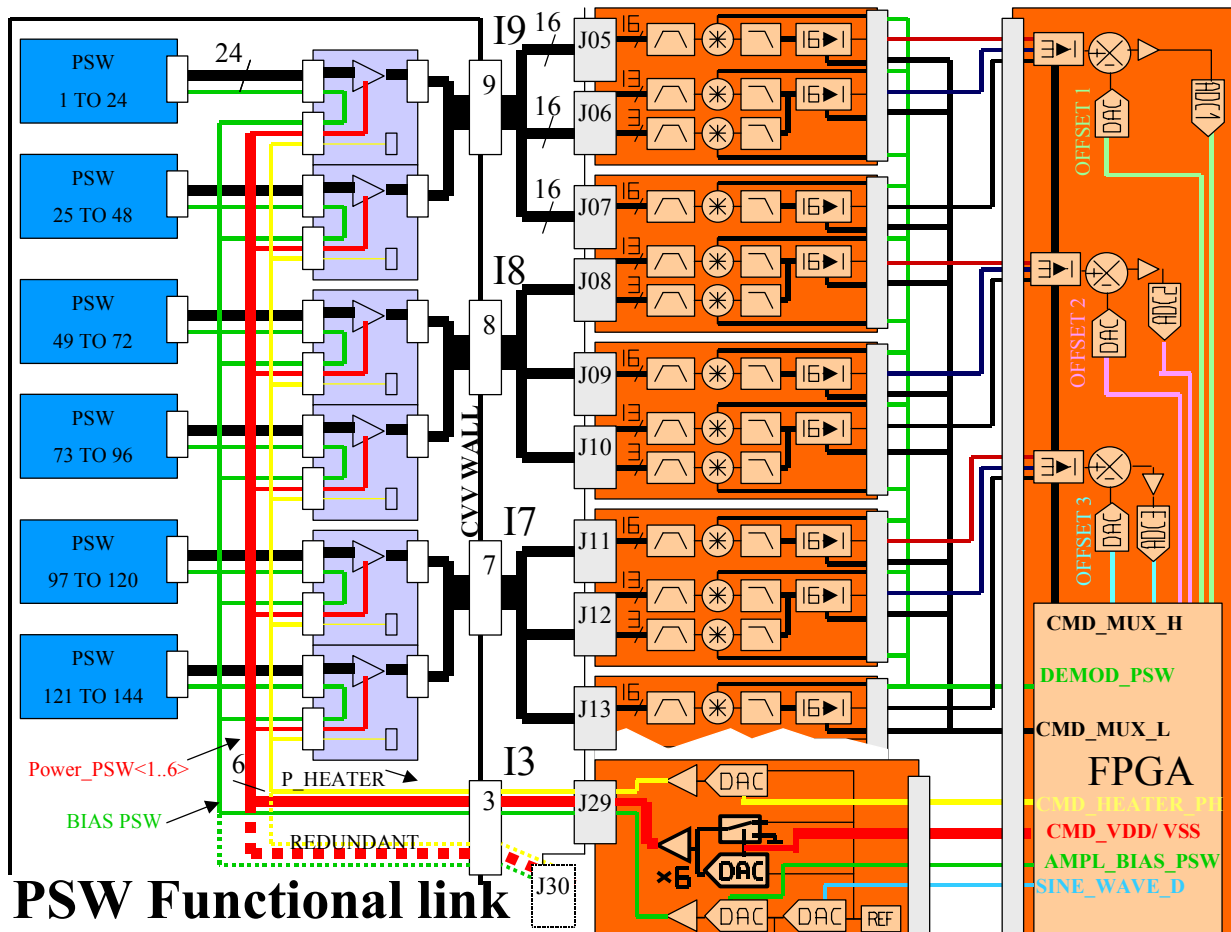
Figure 3-3 PSW Photometer Functional Links

- The 144 PSW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_PSW.)
- All of the 144 channels are sent to the DAQ+IF board through 9 differential links that are digitized by 3 ADCs.

2. The other 16 channels from LIA_P5 and LIA_P6 receive and process signals from 48 "PLW bolometers."

PLW Functional link
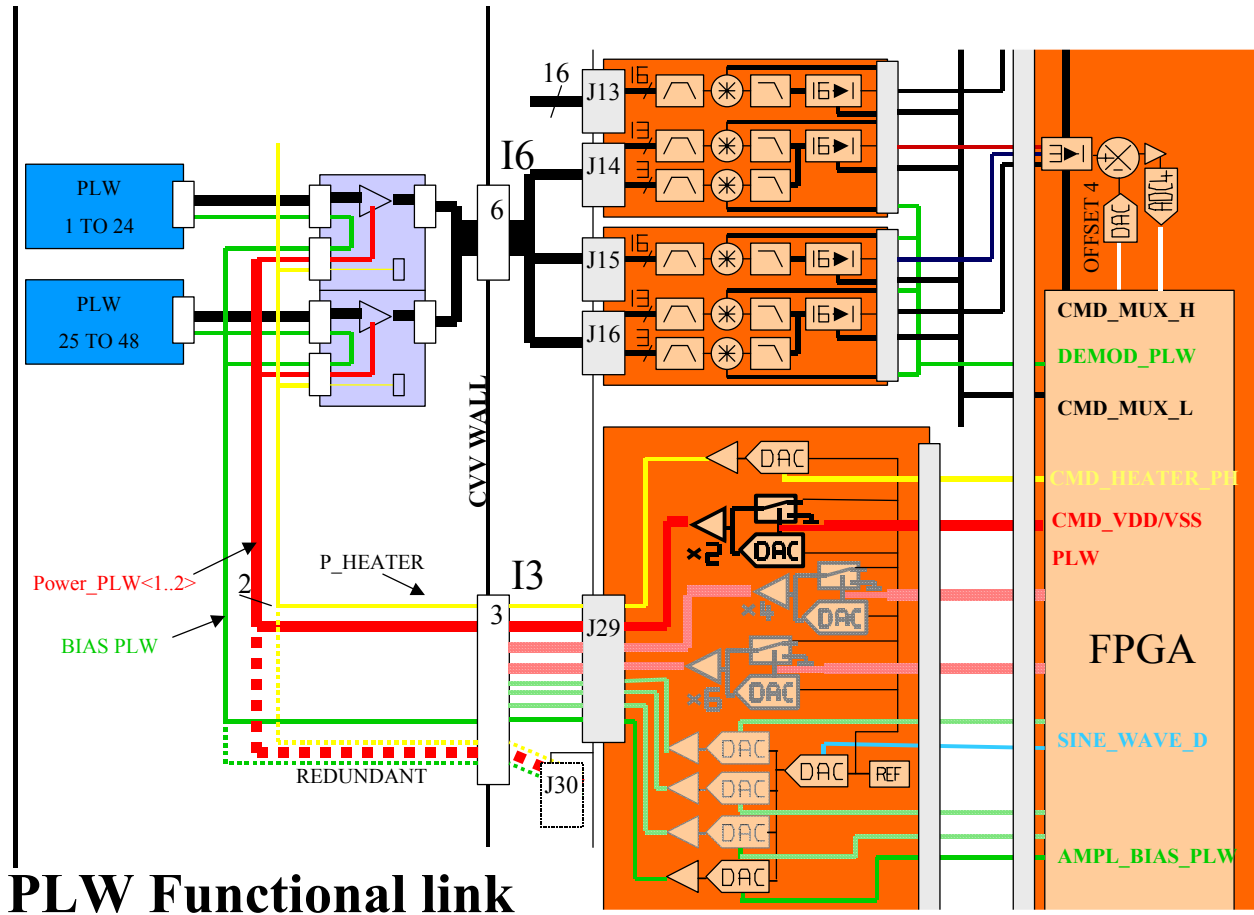
Figure 3-4 PLW Photometer Functional Links

- The 48 PLW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_PLW.)

- All of the 48 channels are sent to the DAQ+IF board through 3 differential links that are digitized by one ADC.

3. LIA_P7 to LIA_P8 and the first 29 channels of the LIA_P9 receive and process the signals from 93 "PMW bolometers."
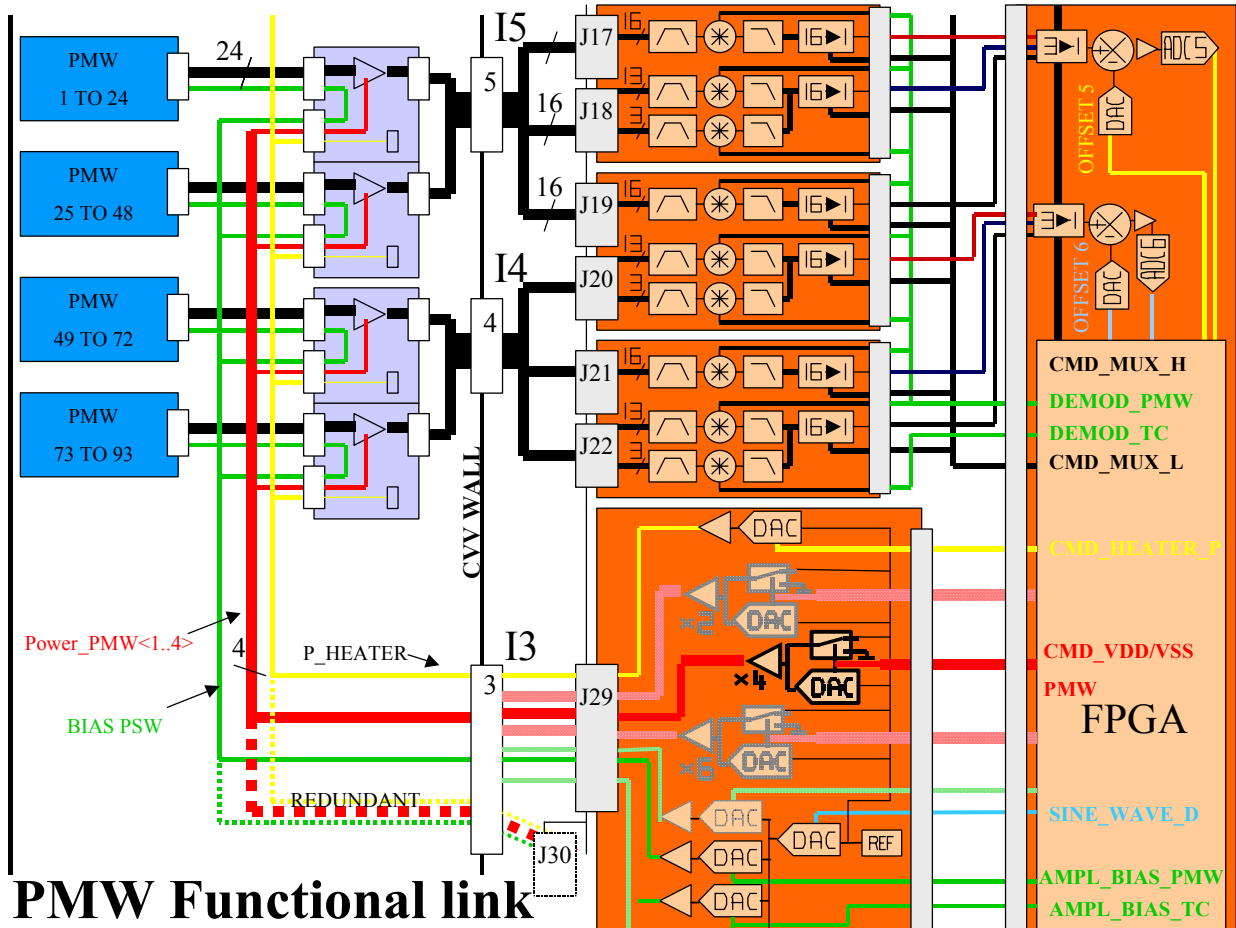
Figure 3-5 PMW Photometer Functional Links

- The 93 PMW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_PMW.)

- All of the 93 channels are sent to the DAQ+IF board through 6 differential links that are digitized by 2 ADCs.

4. The last 3 channels of the LIA_P9 receive and process signals from 3 "T/C bolometers.'
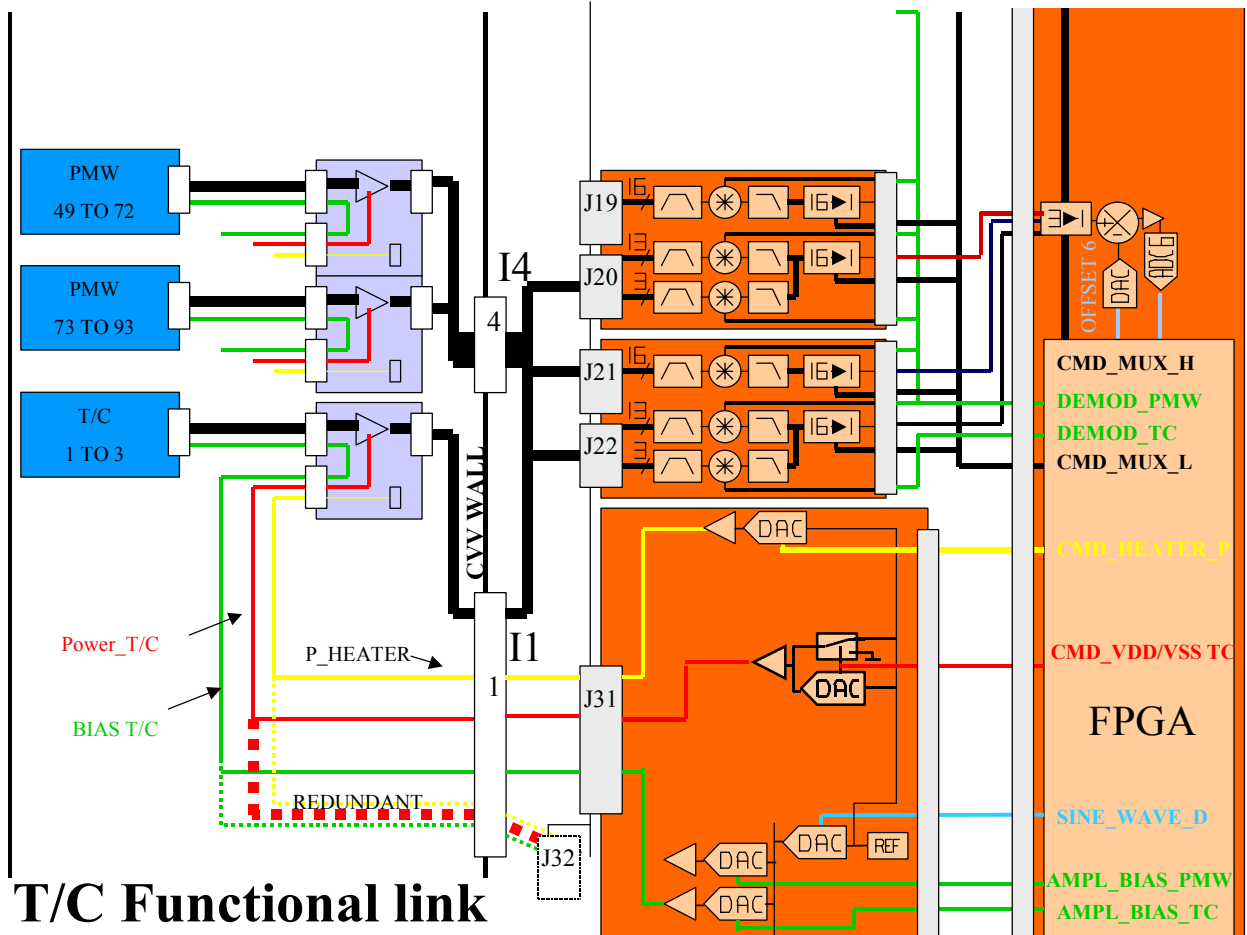
Figure 3-6 T/C Photometer Functional Links

- The 3 T/C channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_T/C)

- All 3 channels are sent to the DAQ+IF board through one differential link that is digitized by one ADC.

- Note: The T/C bias signals go through connectors J31and J32 as well as harness I1 that are mainly used to carry the spectrometer signals. However, these T/C signals always refer to the photometer's ground.
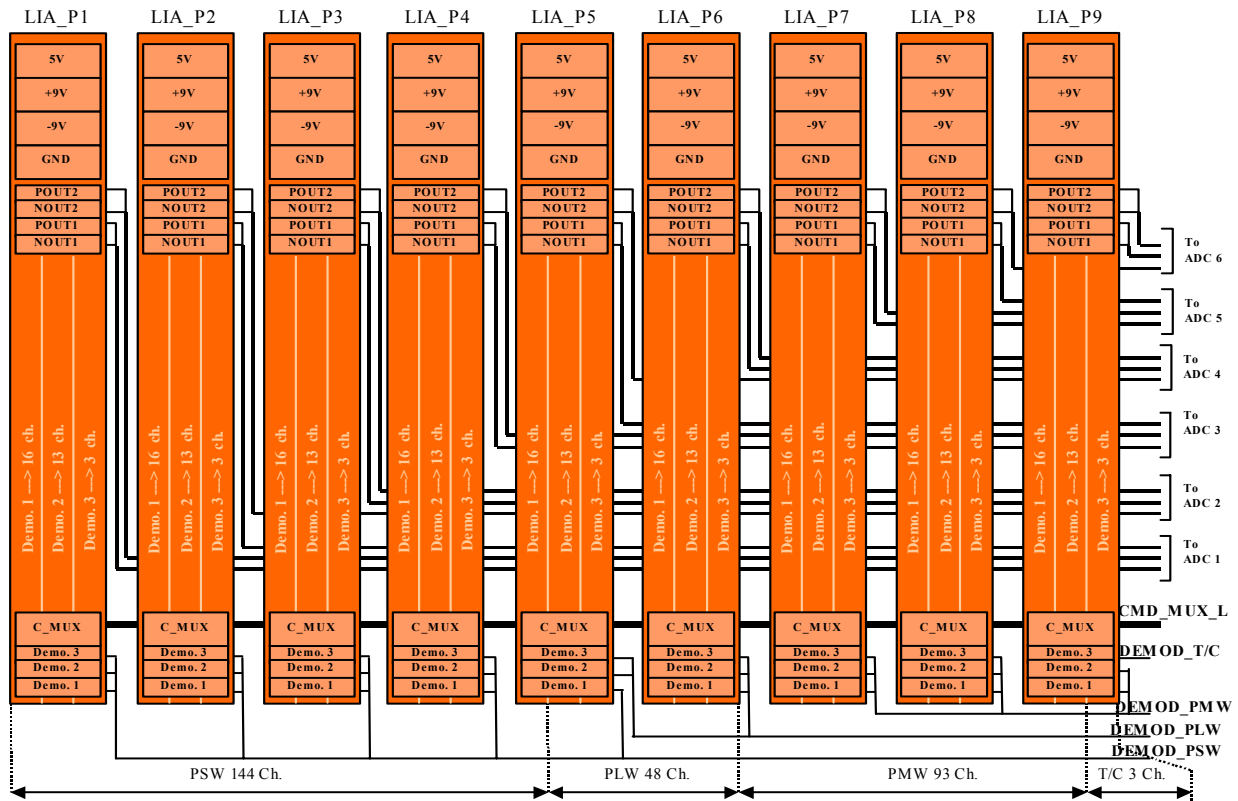
Figure 3-7 LIA Photometer Section

Each group receive its own respective demodulation signal: DEMOD_PSW, DEMOD_PMW, DEMOD_PLW and DEMOD_T/C. Each of these signals can have a different phase shift.

The LIA photometer is supplied only when the SPIRE instrument is running in the photometer mode.

Each LIA photometer board receives its own group of 3 supply lines (-9V, +9V and 5V), which will be automatically shutdown if an error occurs on one of these three lines.

3.4 SPECTROMETER

Three LIA_S boards make up the LIA spectrometer section.
- LIA_S1 and LIA_S2 receive and process signals from forty-two "S-SW bolometers."
- LIA_S3 receive and process signals from twenty-four "S-LW bolometers."
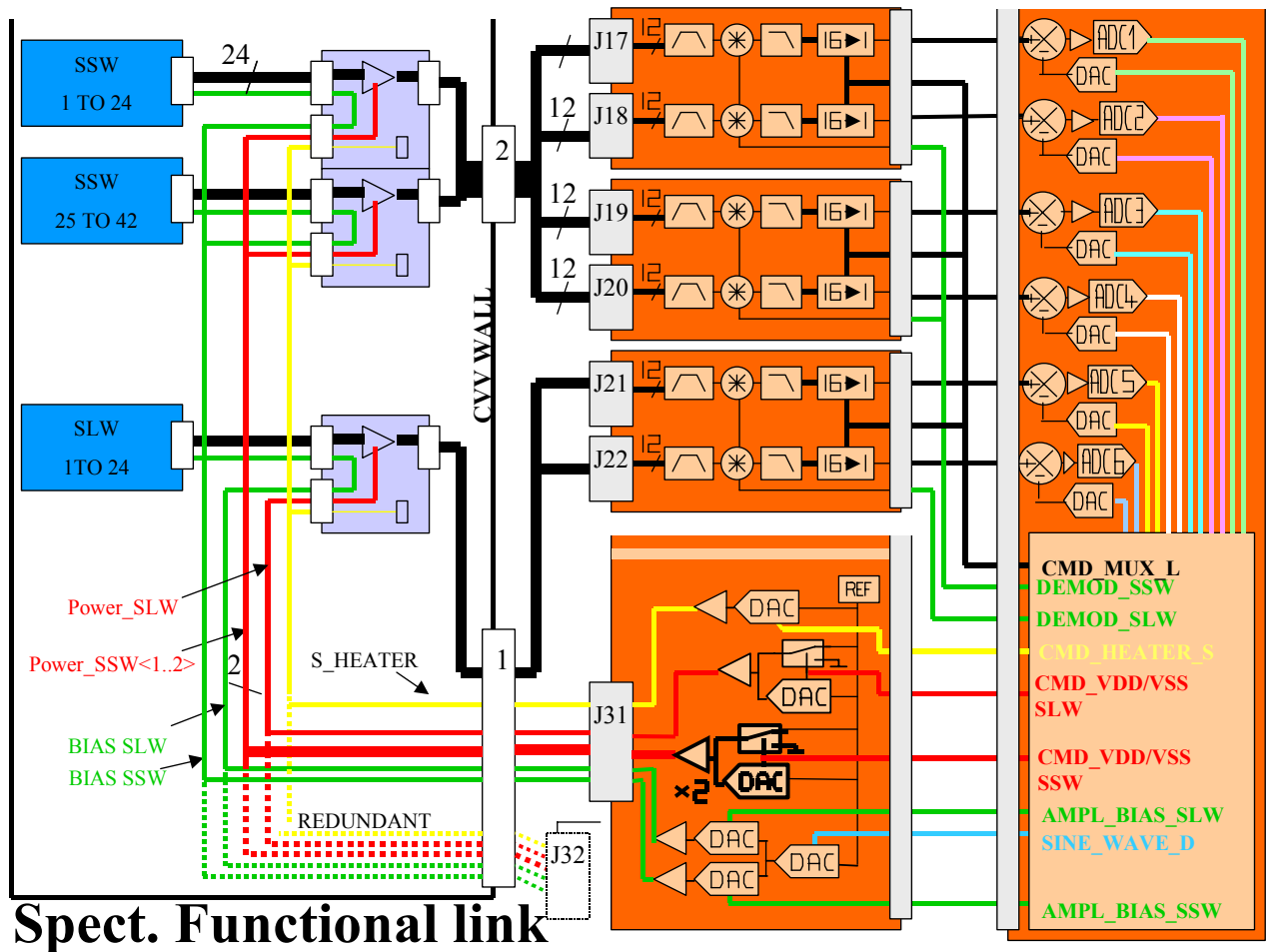
Figure 3-8 Spectrometer Functional Links

The 24 SLW channels receive the same sinus bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_SLW.)
All of the 24 channels are sent to the DAQ+IF board through two differential links that are digitized by two ADCs.

The 42 SSW channels + six spare channels receive the same sinus bias signal (the same frequency and the same amplitude) and the same square demodulation signal (DEMOD_SSW.)
All of the 42 channels are sent to the DAQ+IF board through four differential links that are digitized by four ADCs.
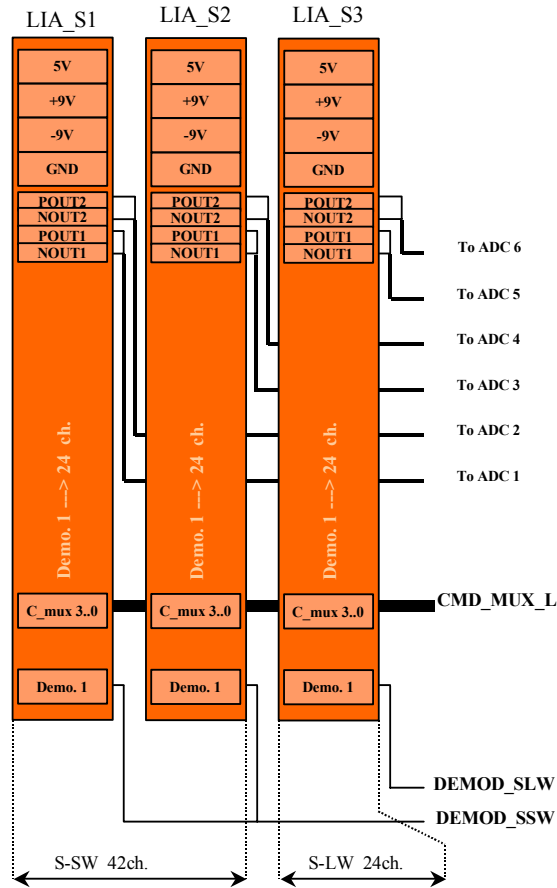
Figure 3-9 LIA Spectrometer Section

Each group receive its own respective demodulation signal: DEMOD_SSW and DEMOD_SLW. These signals can each have a different phase shift.

The LIA spectrometer is supplied only when the SPIRE instrument is running in spectrometer mode.

Each LIA spectrometer board receives its own group of 3 supply lines (-9V, +9V and 5V), which are automatically shutdown if an error occurs in on one of these three lines.

3.5 LIA PHOTOMETER BOARD

3.5.1 LIA Photometer Board Overview
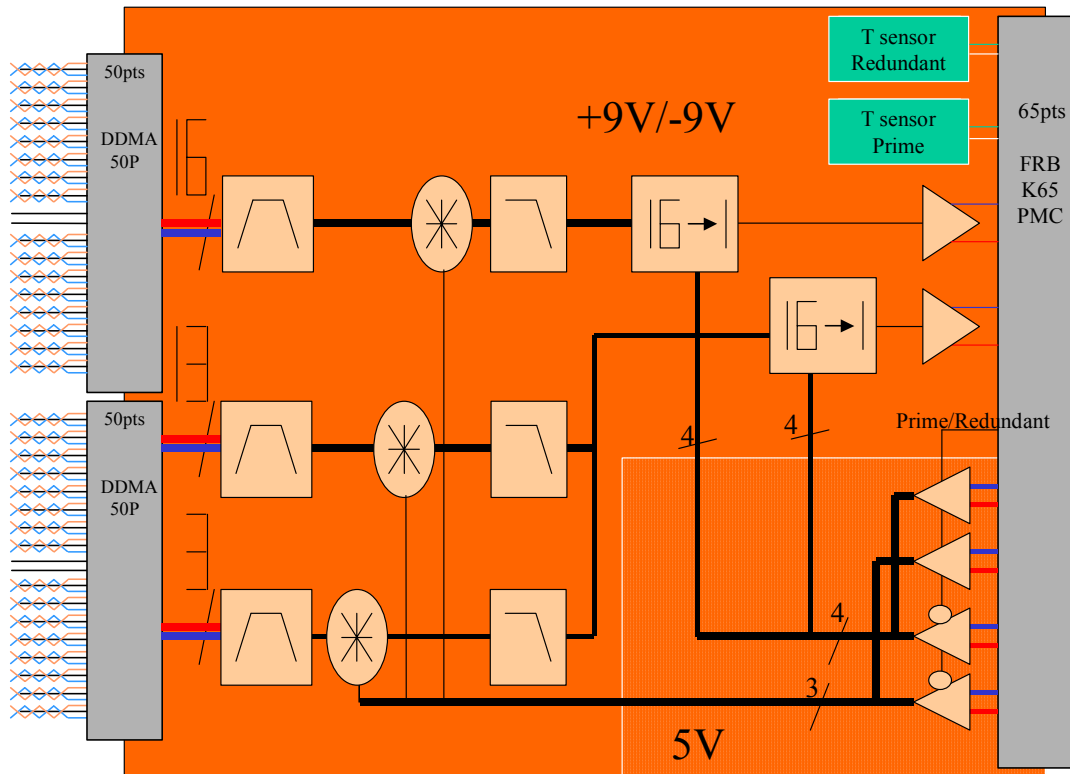
Figure 3-10 LIA Photometer Board Overview

• **The LIA_P board has thirty-two channels that are divided into three groups:**
- A group of sixteen channels which go to the first multiplexer.
- A group of thirteen channels, which go to the second multiplexer.
- A group of three channels, which also go to the second multiplexer.

•**Each of the three groups can receive its own demodulation signals.**

•**The receivers that relay the multiplexer command signals as well as the demodulation signals are redundant:**
- A PRIME/REDUNDANT signal from the PSU activates the PRIME receivers when the PRIME power supply turns on and the REDUNDANT receivers when the REDUNDANT power supply turns on.
- The LIA PRIME receivers are connected to the PRIME DAQ+IF board.
- The LIA REDUNDANT receivers are connected to the REDUNDANT DAQ+IF board.

•**The two multiplexers receive the same command signals.**

3.5.2 LIA Photometer Board Interface

Interface	Signal Name	Description	Type	Level	In/Out	Frequency
IN_PSW IN_PLW IN_PMW IN_TC	IN+ xx IN- xx	Bolometer Differential Signal JEFT output	Analogic	11mVrms (AC) + 15mV (DC) 1V Common mode offset	IN	50-300Hz
MUX_CHANNEL	POUT x NOUT x	sixteen LIA_P channels multiplexed in one differential signal	Analogic	0 to 5V	OUT	0-5Hz at mux freq. ~10kHz
CMD_MUX_H	PAx- PAx+	BIT Command Mux (PRIME) Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	~10kHz
	RAx- RAx+	BIT Command Mux (REDUNDANT) Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	~10kHz
DEMOD_PLW/PMW PSW	PDEMOD1- PDEMOD1+	Demodulation Differential Signal (PRIME) for Channels One to Sixteen	Numeric (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	PDEMOD2- PDEMOD2+	Demodulation Differential Signal (PRIME) for Channels Seventeen to Twenty-nine	Numeric (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
DEMOD_PLW/PMW PSW/TC	PDEMOD3- PDEMOD3+	Demodulation Differential Signal for Channels Thirty to Thirty two	Numeric (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
DEMOD_PLW/PMW PSW	RDEMOD1- RDEMOD1+	Demodulation Differential signal (REDUNDANT) for Channels One to Sixteen	Numeric (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	RDEMOD2- RDEMOD2+	Demodulation Differential Signal (REDUNDANT) for Channels Seventeen to Twenty-nine	Numeric (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
DEMOD_PLW/PMW PSW/TC	RDEMOD3- RDEMOD3+	Demodulation Differential Signal for (REDUNDANT) Channels Thirty to Thirty two	Numeric (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
LIA_TEMPERATURE	PT_P9V	Sensor PRIME Bias	Analogic	9V	IN	DC
	PT	Output Sensor PRIME	Analogic	2 to 4V	OUT	-
	RT_P9V	Sensor REDUNDANT Bias	Analogic	9V	IN	DC
	RT	Output Sensor REDUNDANT	Analogic	2 to 4V	OUT	-
POWER	P9V	9V Power Supply	Power	9V	IN	DC
	N9V	-9V Power Supply	Power	-9V	IN	DC
	P9V_P	PRIME/REDUNDANT Signal	Analogic	0 to 9V	IN	DC
	P5V	5V Power Supply	Power	5V	IN	DC
	GND	Grounding	Power	0V	-	DC

3.5.3   LIA PHOTOMETER FUNCTIONS

3.5.3.1   LIA Photometer Channel Overview
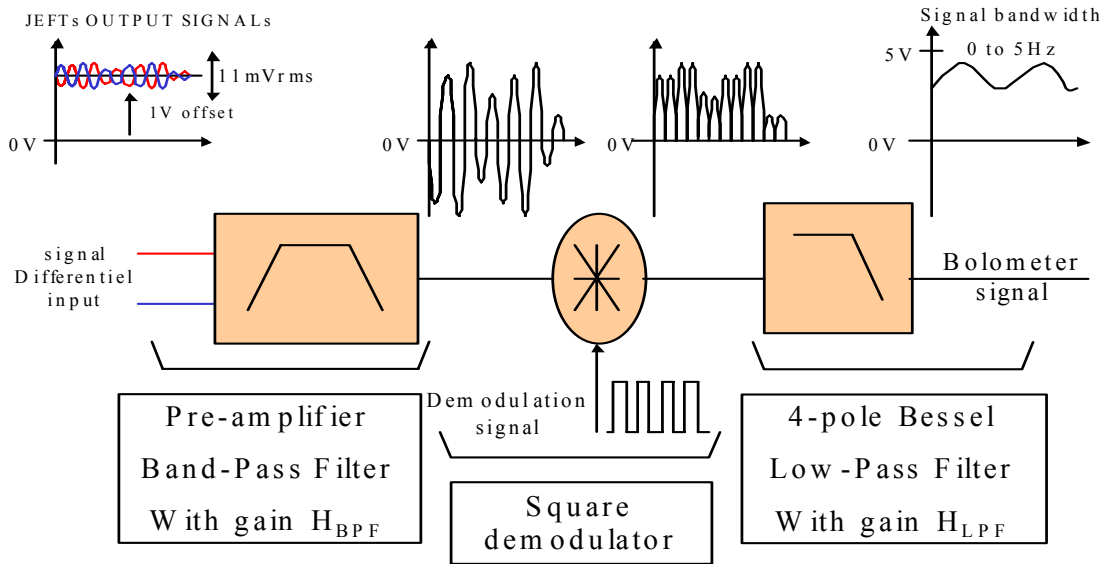
Figure 3-11 LIA Photometer Board Channel

The input differential signal that comes from a bolometer is amplified and its DC component is eliminated by the pre-amplifier BPF. Then, it is demodulated by a squared signal. Afterwards, a four-pole Bessel LPF filters it.

3.5.3.2   LIA Photometer Pre-amplifier BPF (FUNC-02 –1, FUNC-02 –2 and FUNC-02 –3)

The pre-amplifier BFP does the three following functions:

- FUNC-02-1 Differential receiver.
- FUNC-02-2 Band pass filter.
- FUNC-02-3 Gain before demodulation.
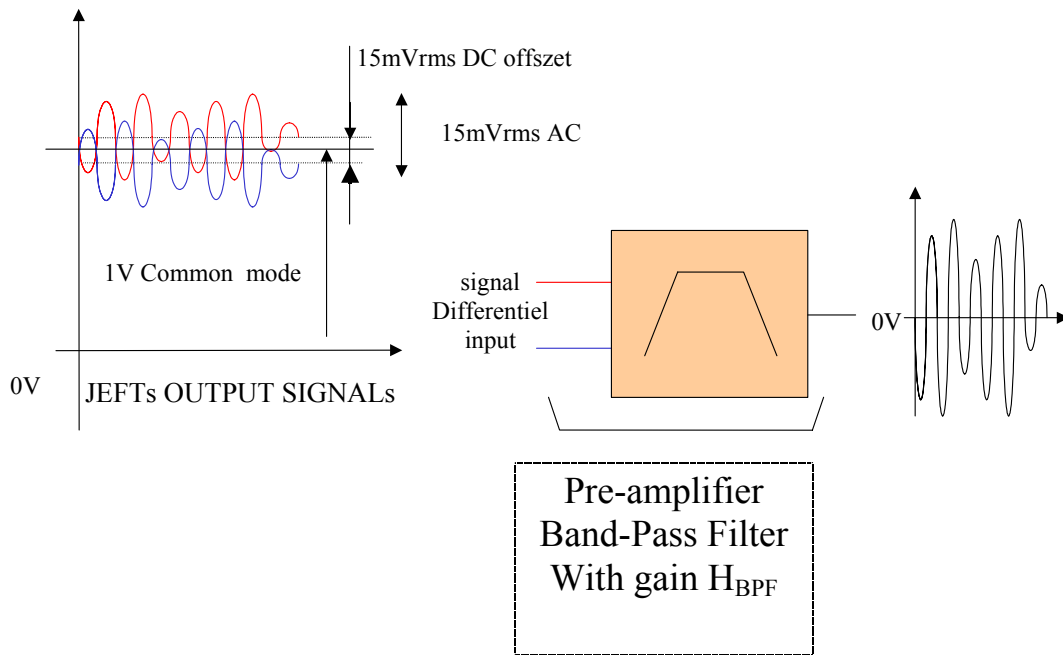
3.5.3.2.1 Preamplifier circuit
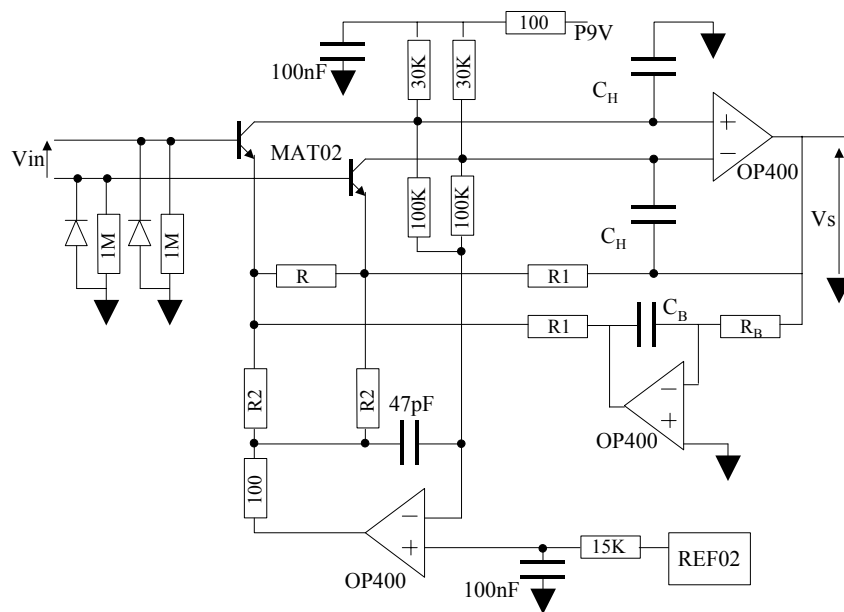
The differential input of the pre-amplifier use MAT02 and OP400 to provide a good common mode rejection
The MAT02 are chosen in order to make an every low noise differential input.
The integrator in the feedback loop removes the differential offset. The maximum differential DC offset removed is 19mV.

3.5.3.2.2 Preamplifier transfer function

$$\frac{Vs}{Vin} = H_{BPF} = G \cdot \left(\frac{R_B \cdot C_B \cdot p}{1 + (R_B \cdot C_B)p + \left(\frac{G}{S} + R1\right)C_H \cdot R_B \cdot C_B \cdot p^2} \right) \text{ with } G = \left(1 + \frac{R1}{R2} + \frac{2R1}{R}\right)$$

R1=R2=15K; R=115; R_B=100K; C_B=47nF; C_H=1.5nF;
Mat02 Tran conductance: S=3.868x10^{-3} for T=300K

$$\text{So } H_{BPF} = 262.8 \cdot \left(\frac{4.7 \cdot 10^{-3} \cdot p}{1 + 4.7 \cdot 10^{-3} p + 5.85 \cdot 10^{-7} \cdot p^2} \right)$$
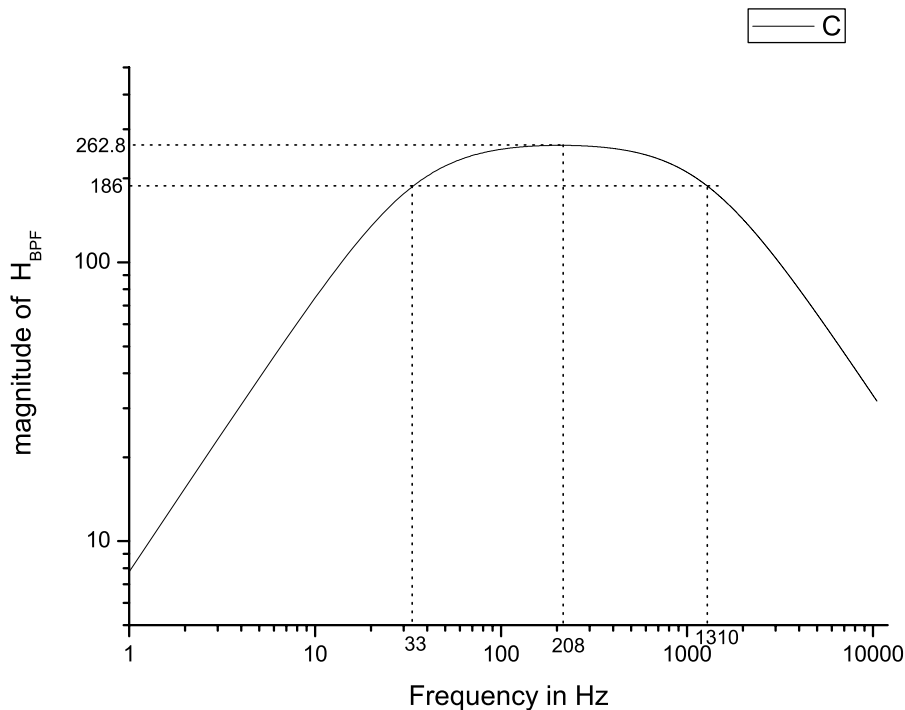
3.5.3.2.3 Preamplifier transfer function simulation result

The two following simulation results show respectively the magnitude and the phase transfer function of LIA Photometer Pre-amplifier BPF:
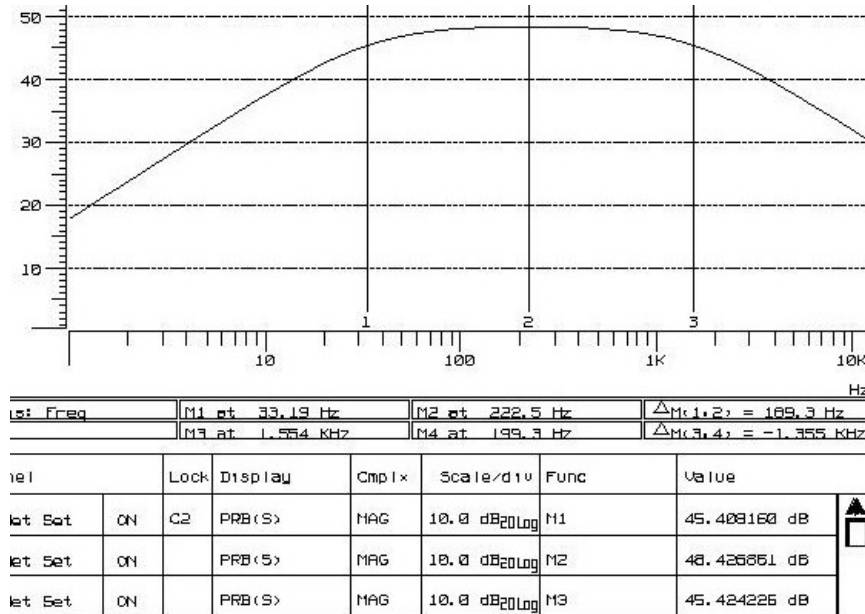
Figure 3-12 LIA Photometer Pre-amplifier BPF Magnitude Transfer Function

Simulation results:

-At 33,19Hz the gain of the BPF is 45.4 dB (186) and it's the −3dB low cutoff frequency.
-At 222.5 Hz the gain of the BPF is 48.4 dB (263) and it's the maximum gain.
-At 1554 Hz the gain of the BPF is 45.4 dB (186) and it's the −3dB high cutoff frequency.
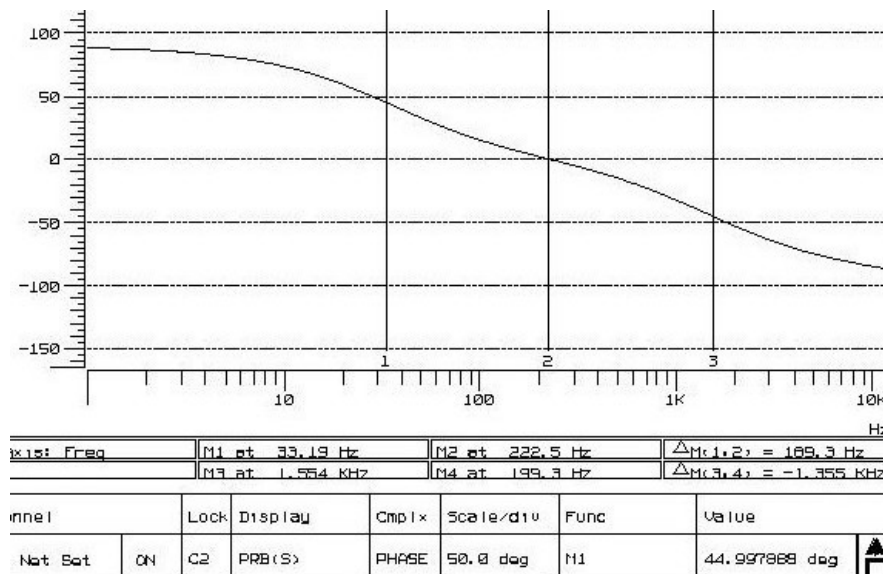
Figure 3-13 LIA Photometer Pre-amplifier BPF Phase Transfer Function

The following simulation result shows the common mode transfer function. It shows that we have at least –80dB common mode rejection between 50Hz and 300Hz.
In other words, there is some leeway with the –60dB requirement.

Axis: Freq	M1 at 33.19 Hz	M2 at 222.5 Hz	△M(1,2) = 189.3 Hz
	M3 at 1.554 KHz	M4 at 199.3 Hz	△M(3,4) = -1.355 KHz

annel	Lock	Display	Cmplx	Scale/div	Func	Value	
. Not Set	ON	C2 PRB(S)	MAG	20.0 dB20Log	M1	-105.12399 dB	
! Net Set	ON	PRB(S)	MAG	20.0 dB20Log	M2	-85.765663 dB	
	Net Set	ON	PRB(S)	MAG	20.0 dB20Log	M3	-71.480624 dB	
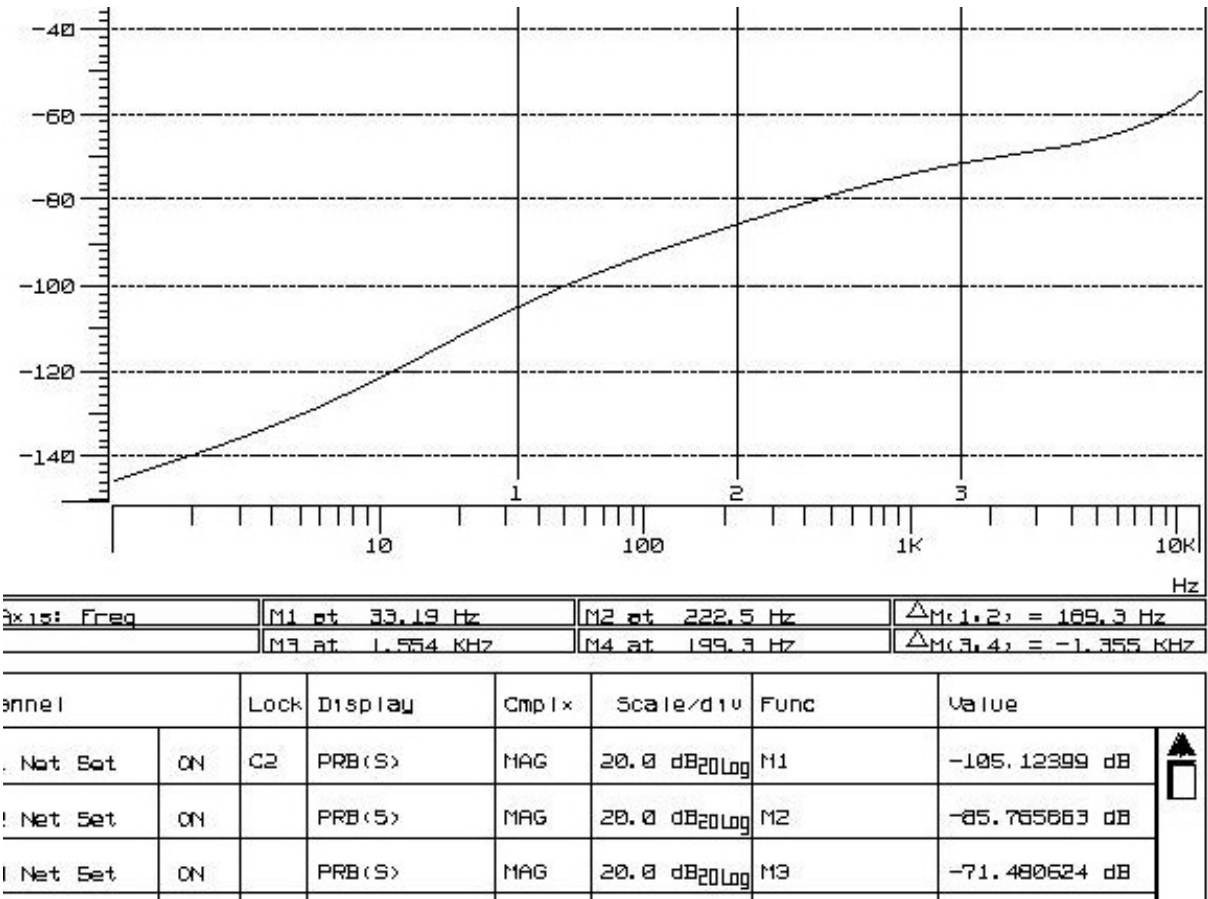
Figure 3-14 LIA Photometer Pre-amplifier BPF Common Mode Rejection

3.5.3.3 LIA Photometer demodulation (FUNC-02 –4)
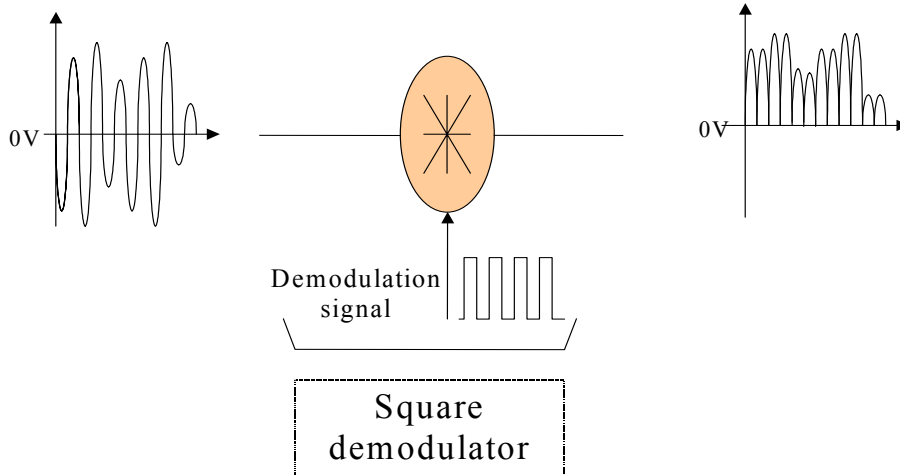
Switching between the signal and his opposite does the demodulation of the signal coming for the pre-amplifier. This switching is command by the signal DEMOD_PSW for PSW channels, DEMOD_PMW for PMW ones, DEMOD_PLW for PLW ones, and DEMOD_TC for TC ones.

The analog switch HI303 does the switch.
The opposite signal is done by an OP400 in inverter circuit.

3.5.3.3.1 Demodulation circuit
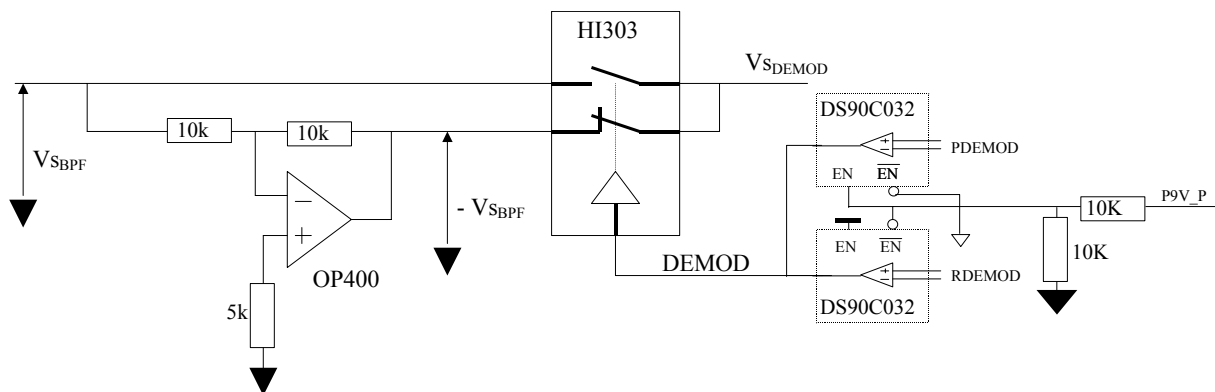
3.5.3.3.2 Output expression

$V_{SBPF} = Vin \cdot H_{BPF}$

$V_{SDEMOD}(\omega t) = V_{SBPF} \sum_{n=0}^{\infty} \frac{4}{(1+2n)\pi} \sin[(1+2n)\omega t]$

3.5.3.4 LIA Photometer LPF (FUNC-02 –5)

The photometer low pass filters are 4 pole Bessel low pass filters.
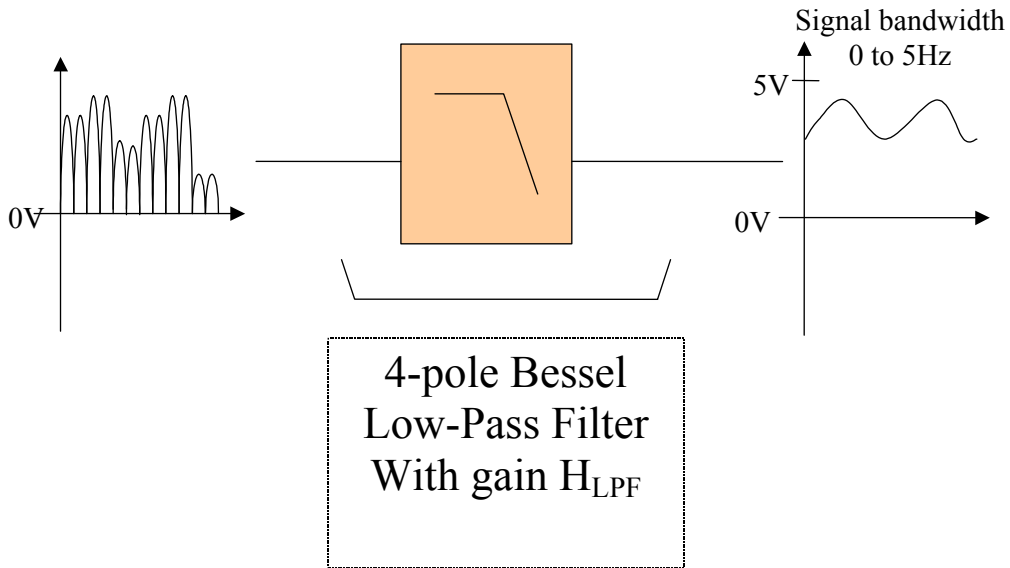
3.5.3.4.1 LPF circuit
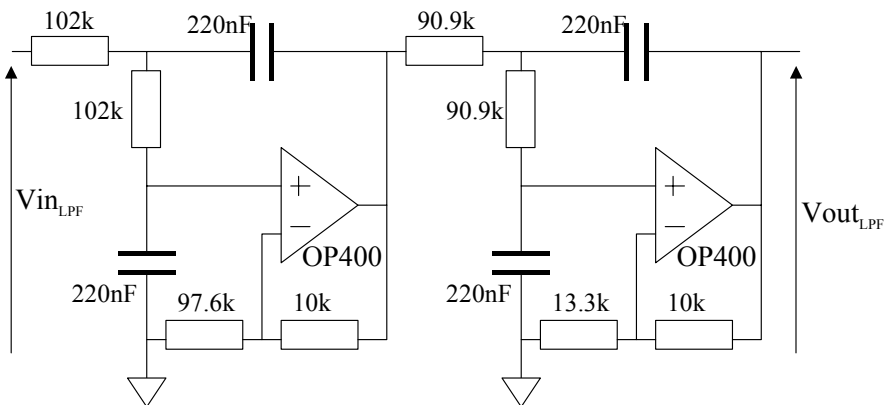
3.5.3.4.2 LPF transfer function

Transfer function: $\dfrac{V_{out\,LPF}}{V_{in\,LPF}}=1.93\times\dfrac{1}{1+42.58p+503p^2}\times\dfrac{1}{1+24.96p+400p^2}$ 　　　　($p=j2\pi f$)

3.5.3.4.3 LPF transfer function simulation result

The two following simulation results show respectively the magnitude and the phase transfer function of LIA Photometer four-pole Bessel LPF:

		Axis: Freg	M1 at 5.057 Hz	M2 at 1.02 Hz	△M(1.2) = -4.037 Hz
			M3 at 1 Hz	M4 at 10 KHz	△M(3.4) = 9.999 KHz

nannel		Lock	Display	Cmplx	Scale/div	Func	Value	
1 Net Set		ON		PRB(C)	MAG	50.0 dB20Log	M1	2.6120401 dB
2 Net Set		ON		PRB(C)	MAG	50.0 dB20Log	M2	5.6044131 dB
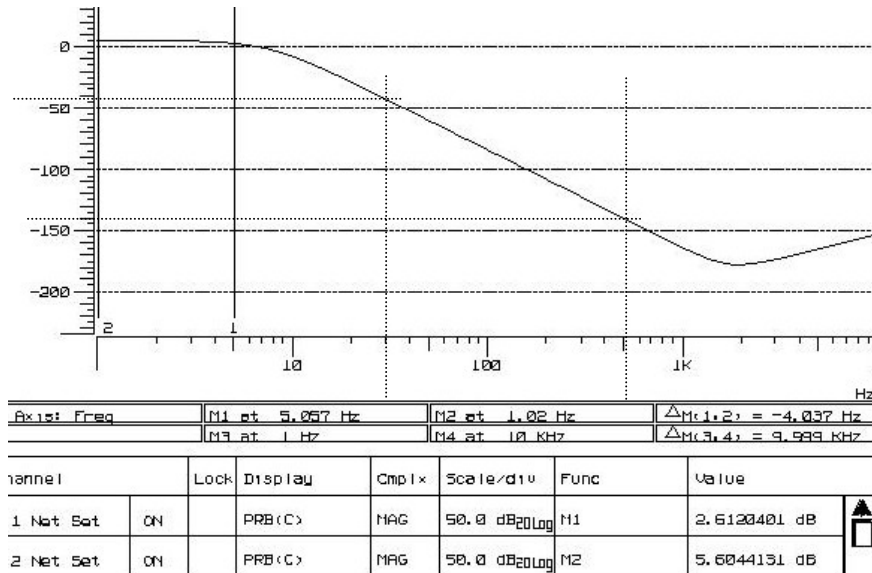
Figure 3-15 LIA Photometer LPF Magnitude Transfer Function

Simulation results:

- At a frequency of 1.02Hz the gain is 5.6 dB (1.9)
- The –3dB cut off frequency is at 5Hz.
- The slope is –80dB/decade.

		Axis: Freg	M1 at 5.057 Hz	M2 at 1.02 Hz	△M(1.2) = -4.037 Hz
			M3 at 1 Hz	M4 at 10 KHz	△M(3.4) = 9.999 KHz

nannel		Lock	Display	Cmplx	Scale/div	Func	Value	
1 Net Set		ON		PRB(C)	PHASE	100 deg	M1	-123.07263 deg
2 Net Set		ON		PRB(C)	PHASE	100 deg	M2	-24.607799 deg
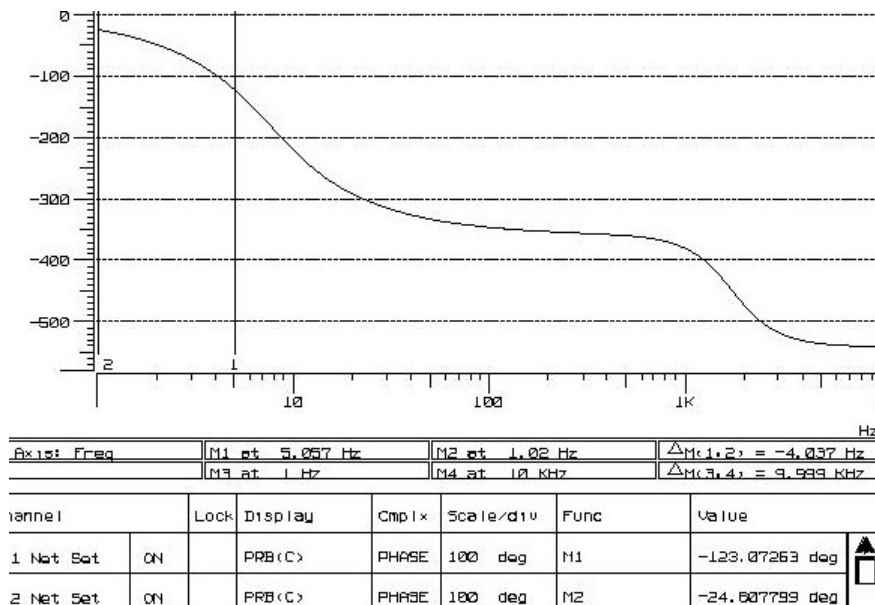
Figure 3-16 LIA Photometer LPF Phase Transfer Function

3.5.3.5 LIA Photometer Channel Input Noise

MAT02 : BW 50 –300Hz : Vn=1nV/√Hz

Resistors noise : $In = \sqrt{\dfrac{4kT}{R}}$; T=295K ; $4kT = 1.63 \times 10^{-20}$

Input preamplifier noise: $Vn_{preampl} = \sqrt{2 \times (Vn_{MAT02})^2 + 115^2 \left(In_{115}^2 + 4In_{15k}^2\right)} = 2nV/\sqrt{Hz}$

OP400 at 0.1Hz: Vn=66nV/√Hz; In=1.6pV/√Hz

LPF Stage 1: $Vn_{LPF1} = \sqrt{(Vn_{OP400})^2 + (213 \times 10^3 \times In_{OP400})^2 + 2Vn_{102k}^2} = 352nV/\sqrt{Hz}$

LPF Stage 2: $Vn_{LPF1} = \sqrt{(Vn_{OP400})^2 + (188 \times 10^3 \times In_{OP400})^2 + Vn_{188k}^2} = 313nV/\sqrt{Hz}$

Input noise LPF: $Vn_{LPF} = \sqrt{(Vn_{LPF1})^2 + \left(\dfrac{Vn_{LPF2}}{1.1}\right)^2} = 452nV/\sqrt{Hz}$

Noise total at the photometer LPF output:

$$Vn_{LPFout} = \sqrt{\left[(Vn_{preampl} \times H_{BPF})^2 \times \left(\frac{4}{\pi}\right)^2 \times \left[1 + \left(\frac{1}{3}\right)^2 + \left(\frac{1}{5}\right)^2 + \left(\frac{1}{7}\right)^2 + \left(\frac{1}{9}\right)^2\right] + (Vn_{LPF})^2\right] \times H_{LPF}^2} = 1646nV/\sqrt{Hz}$$

Band pass filter gain H_{BPF}=261; Low pass filter gain H_{LPF}=1.93 and Total channel gain H_{TOT}=454

So the input noise equivalent for a photometer channel is:

$$Vn_{in} = \frac{Vn_{LPFout}}{H_{TOT}} = 3.62nV/\sqrt{Hz}$$

3.5.3.6   LIA Photometer MUX FUNC-02-8 (1/2) and LIA outputs
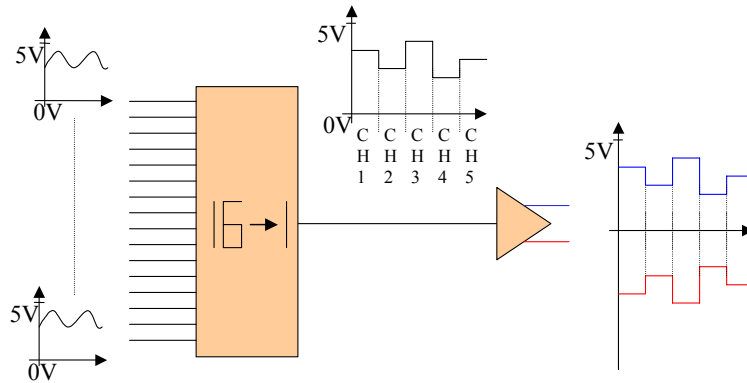
The first multiplexing stage FUNC-02-8 (1/2) is done by analog mux HS508. The differential output is done by two OP484.

See circuit.

3.5.3.6.1 Circuit
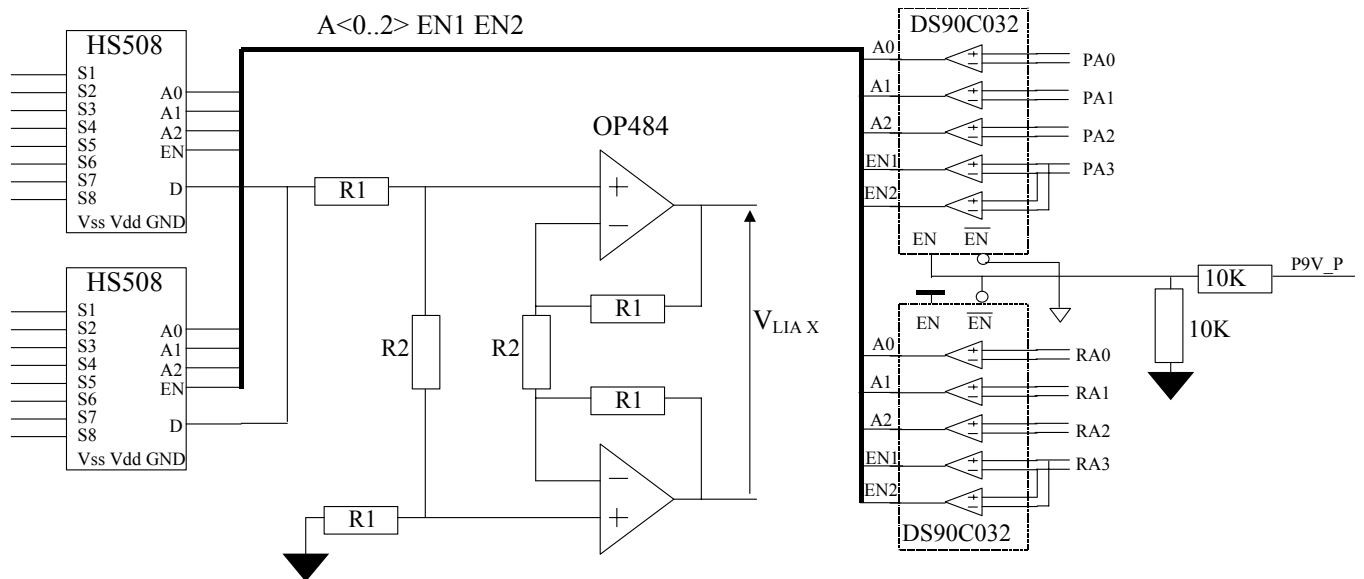
3.5.3.6.2 Noise

See noise synthesis section (on DAQ+IF).

3.5.3.6.3 Timing

See FPGA section.

3.6   LIA SPECTROMETER BOARD

3.6.1   LIA Spectrometer Board Overview
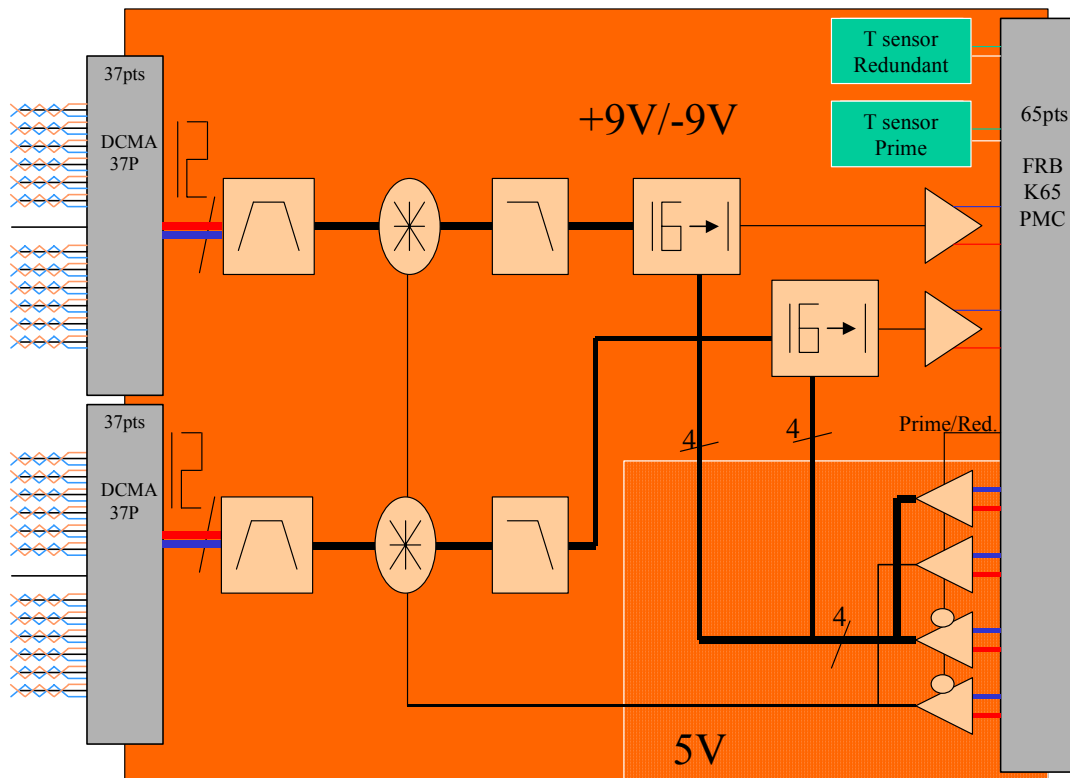
Figure 3-17 LIA Spectrometer Board Overview

•**Each LIA_S board has twenty-four channels, which are divided into two groups.**
        Each group of 12 channels goes to a multiplexer.

•**The two groups receive the same demodulation signal.**

•**The receivers that relay the multiplexers command signal and demodulation signal are redundant as they are on the LIA photometer boards.**

•**The two multiplexers receive the same command signals.**

3.6.2 LIA Spectrometer Board Interface

Interface	Name	Description	Type	Level	In/Out	Frequency
IN_SSW IN_SLW	IN+ xx IN- xx	Bolometer Differential Signal	Analogic	11mVrms (AC) + 1.5V (DC)	IN	50-300Hz
MUX_CHANNEL	POUT x NOUT x	The twelve LIA_S channels Multiplexed in a Differential Signal	Analogic	0 to 5V	OUT	0-25Hz at mux freq.
CMD_MUX_H	PAx- PAx+	BIT Command Mux (PRIME) Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	~10kHz
	RAx- RAx+	BIT Command Mux (REDUNDANT) Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	~10kHz
DEMOD_SSW DEMOD_SLW	PDEMOD1- PDEMOD1+	Demodulation Differential Signal (PRIME) for Channels One to Twenty-four	Numeric (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
	RDEMOD1- RDEMOD1+	Demodulation Differential Signal (REDUNDANT) for Channels One to Twenty-four	Numeric (LVDS)	-0,3Vto 0,3V	IN	50-300Hz
LIA_TEMPERATURE	PT_P9V	Sensor PRIME Bias	Analogic	9V	IN	DC
	PT	Output Sensor PRIME	Analogic	2 to 4V	OUT	-
	RT_P9V	Sensor REDUNDANT Bias	Analogic	9V	IN	DC
	RT	Output Sensor REDUNDANT	Analogic	2 to 4V	OUT	-
POWER	P9V	9V Power Supply	Power	9V	IN	DC
	N9V	-9V Power Supply	Power	-9V	IN	DC
	P9V_P	PRIME/REDUNDANT Signal	Analogic	0 to 9V	IN	DC
	P5V	5V Power Supply	Power	5V	IN	DC
	GND	Grounding	Power	0V	-	DC

3.6.3   LIA SPECTROMETER FUNCTIONS

3.6.3.1   LIA Spectrometer Channel Overview
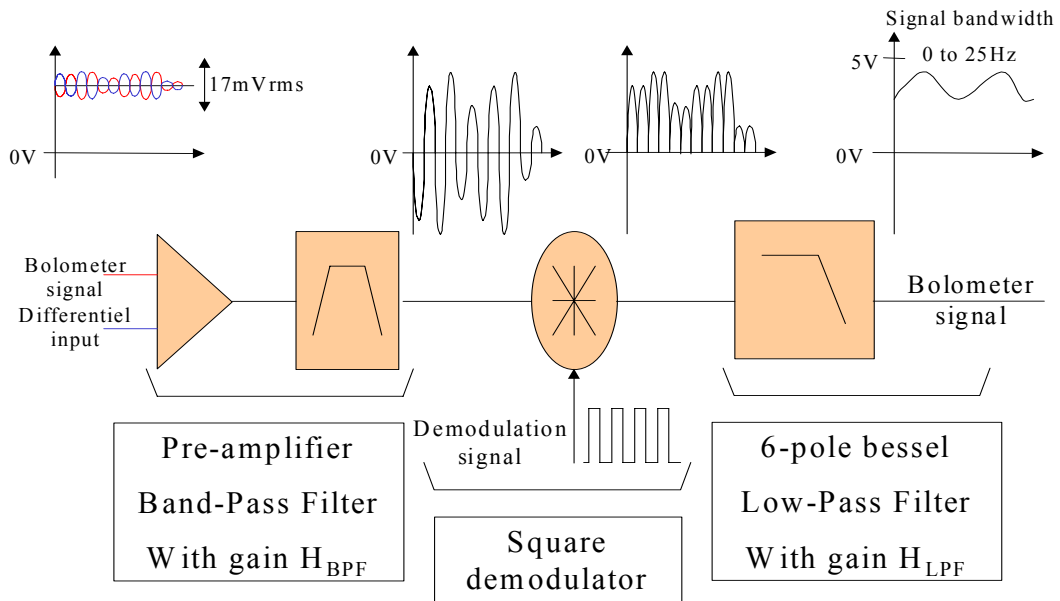
The input differential signal that comes from a bolometer is amplified and its DC component is eliminated by the pre-amplifier BPF. Then, it is demodulated by a squared signal. Afterwards a six-pole Bessel LPF filters it.

3.6.3.2   LIA Spectrometer Pre-amplifier BPF (FUNC-02 –1, FUNC-02 –2 and FUNC-02 –3)

The pre-amplifier BFP does the three following functions:

- - FUNC-02-1 Differential receiver.
- - FUNC-02-2 Band pass filter.
- - FUNC-02-3 Gain before demodulation.
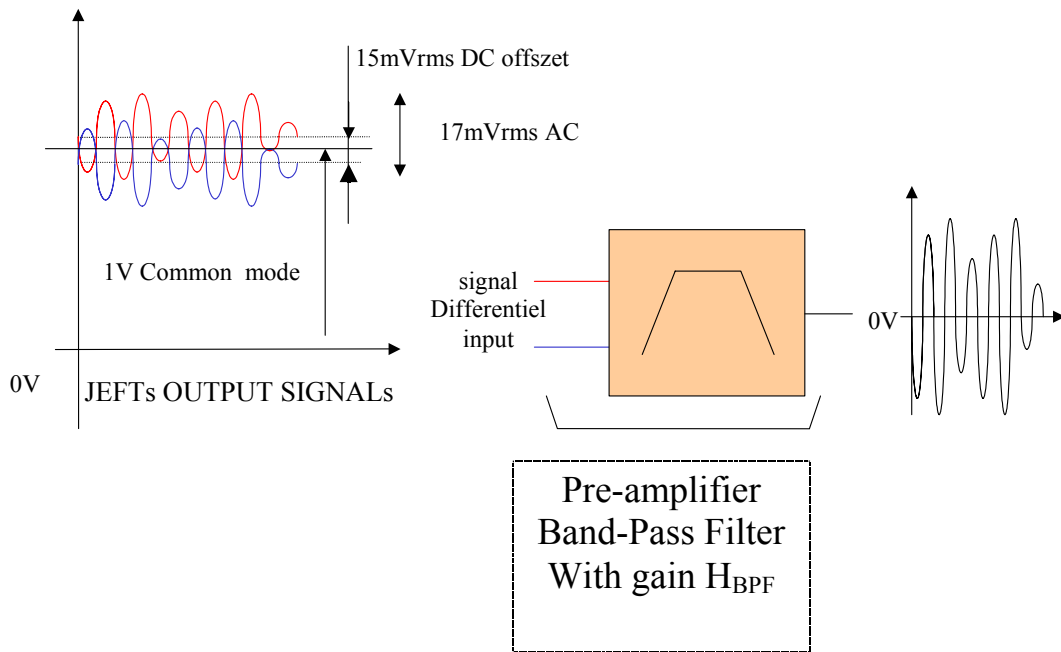
3.6.3.2.1 Circuit
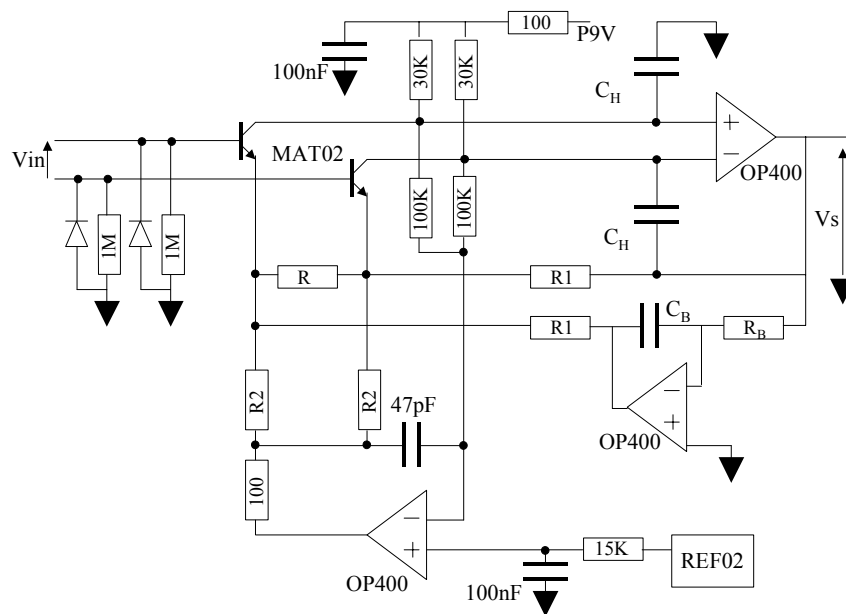
The differential input of the pre-amplifier use MAT02 and OP400 to provide a good common mode rejection

The MAT02 are chosen in order to make an every low noise differential input.

The integrator in the feedback loop removes the differential offset. The maximum differential DC offset removed is 19mV.

3.6.3.2.2 Preamplifier transfer function

Transfer function:

$$\frac{Vs}{Vin} = H_{BPF} = G \cdot \left(\frac{R_B \cdot C_B \cdot p}{1 + (R_B \cdot C_B) p + \left(\frac{G}{S} + R1\right) C_H \cdot R_B \cdot C_B \cdot p^2} \right) \text{ with } G = \left(1 + \frac{R1}{R2} + \frac{2R1}{R}\right)$$

R1=R2=15K; R=267; R_B=100K; C_B=47nF; C_H=1.5nF;
Mat02 Tran conductance: S=3.868x10^{-3} for T=300k

So $H_{BPF} = 114.4 \cdot \left(\dfrac{4.7 \cdot 10^{-3} \cdot p}{1 + 4.7 \cdot 10^{-3} p + 3.14 \cdot 10^{-7} \cdot p^2} \right)$
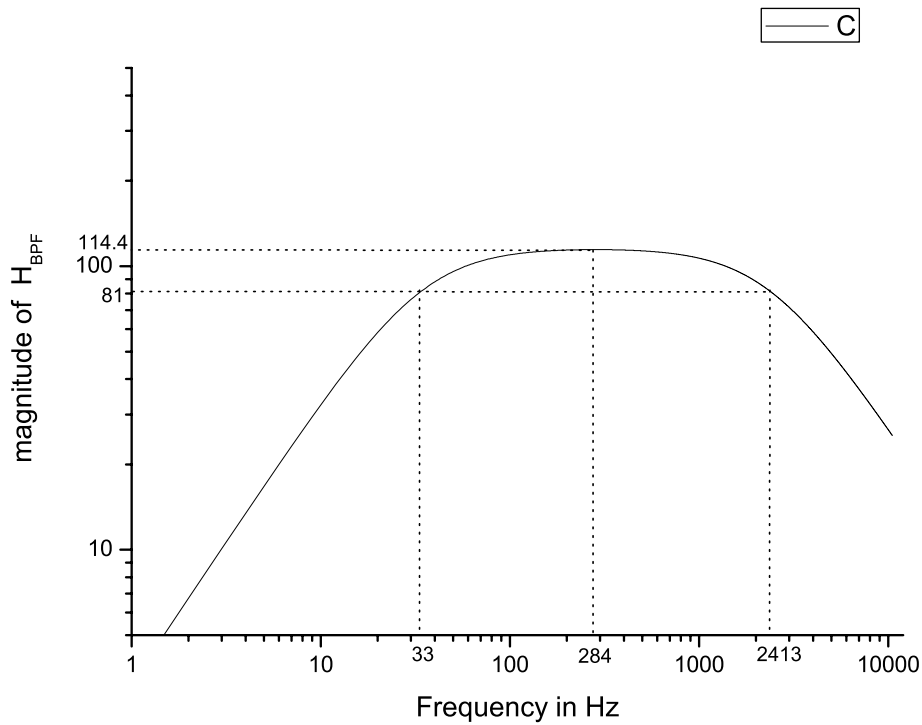
Preamplifier transfer function simulation result

The two following simulation results show respectively the magnitude and the phase transfer function of LIA Spectrometer Pre-amplifier BPF:
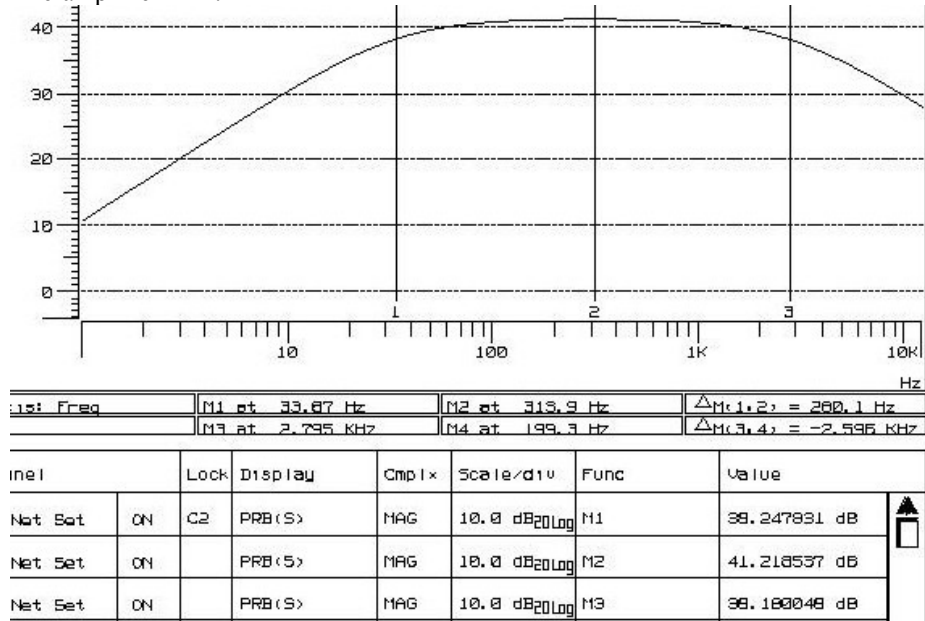
Figure 3-18 LIA Spectrometer Pre-amplifier BPF Magnitude Transfer Function

Simulation results:

-At 33.8 Hz the gain of the BPF is 38.2dB (81) and it's the –3dB low cutoff frequency.
-At 319 Hz the gain of the BPF is 41.2dB (114.8) and it's the maximum gain.
-At 2795 Hz the gain of the BPF is 38.2dB (81) and it's the –3dB high cutoff frequency.
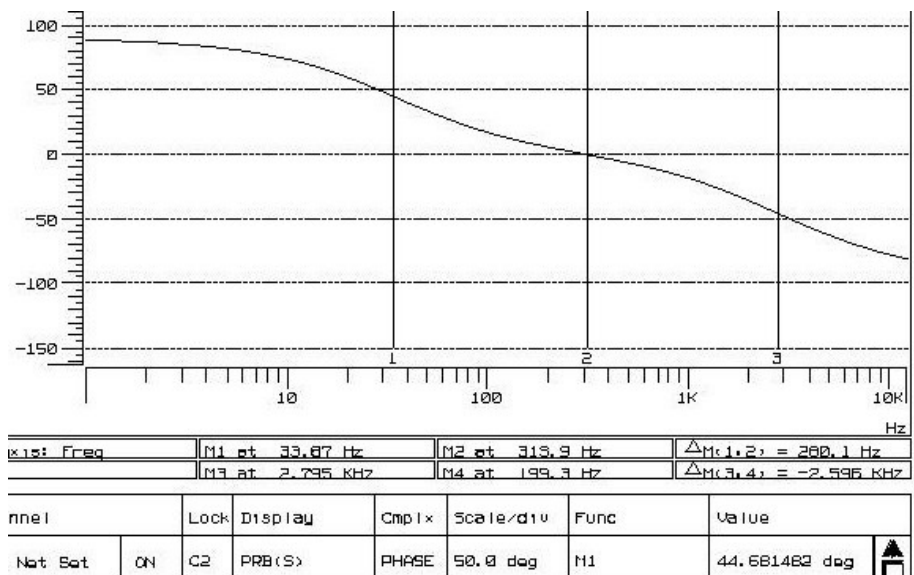
Figure 3-19 LIA Spectrometer Pre-amplifier BPF Phase Transfer Function

The following simulation result shows the common mode transfer function. It shows that we have at least –80dB common mode rejection between 50Hz and 300Hz.
In other words, there is some leeway with the –60dB requirement.

xis: Freq	M1 at 33.19 Hz	M2 at 222.5 Hz	△M(1,2) = 189.3 Hz
	M3 at 1.554 KHz	M4 at 199.3 Hz	△M(3,4) = -1.355 KHz

nnel		Lock	Display	Cmplx	Scale/div	Func	Value	
Not Set	ON	C2	PRB(S)	MAG	20.0 dB20Log	M1	-108.43893 dB	
Net Set	ON		PRB(S)	MAG	20.0 dB20Log	M2	-89.450751 dB	
Net Set	ON		PRB(S)	MAG	20.0 dB20Log	M3	-73.406450 dB	
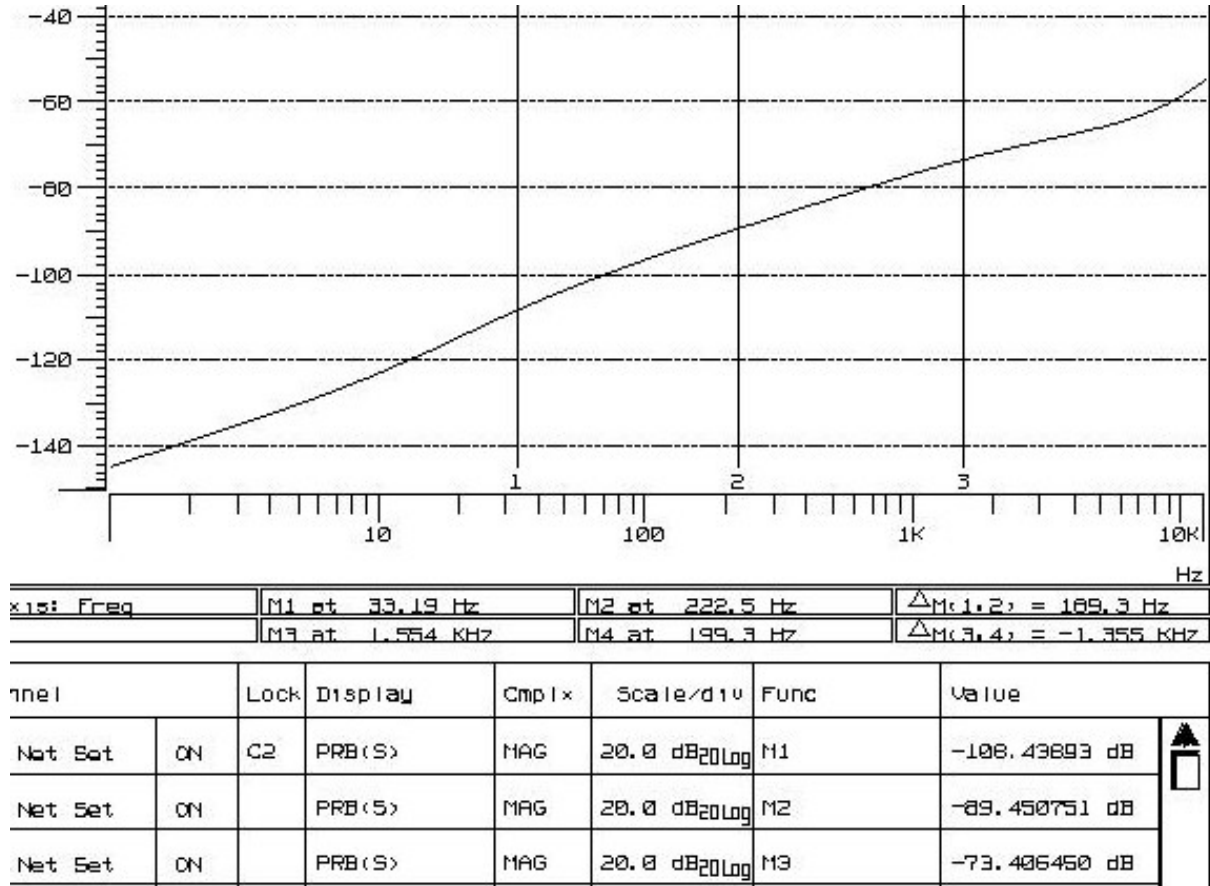
Figure 3-20 LIA Spectrometer Pre-amplifier BPF Common Mode Rejection

3.6.3.3 **LIA Spectrometer demodulation (FUNC-02 –4)**
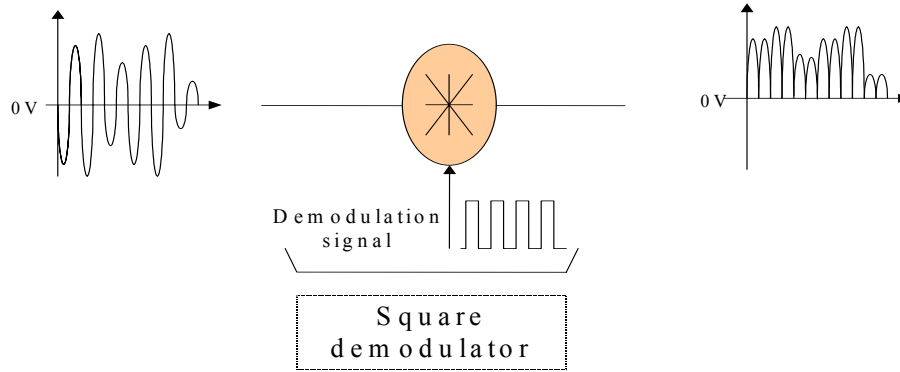
Switching between the signal and his opposite does the demodulation of the signal coming for the pre-amplifier. This switching is command by the signal DEMOD_SSW for SSW channels, and DEMOD_SLW for SLW ones.

The analog switch HI303 does the switch.
The opposite signal is done by an OP400 in inverter circuit.

3.6.3.3.1 Demodulation circuit
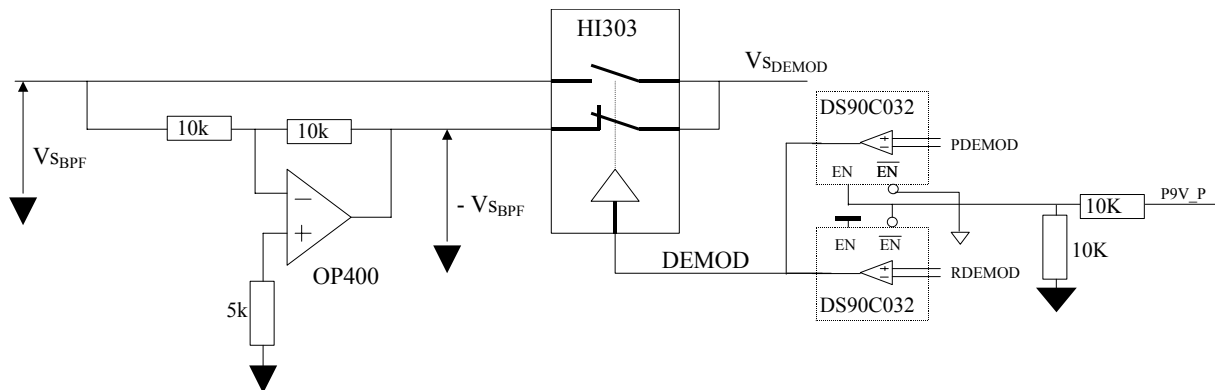
3.6.3.3.2 Output expression

$$V_{SBPF} = Vin \cdot H_{BPF}$$

$$V_{SDEMOD}(\omega t) = V_{SBPF} \sum_{n=0}^{\infty} \frac{4}{(1+2n)\pi} \sin[(1+2n)\omega t]$$

3.6.3.4 LIA Spectrometer LPF (FUNC-02 –5)

The photometer low pass filters are 6 pole Bessel low pass filters.
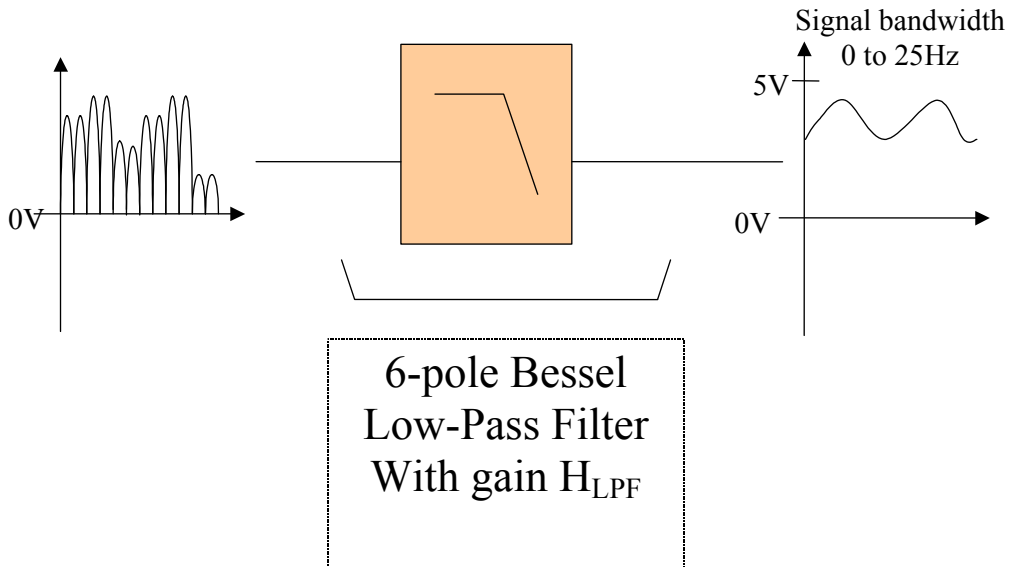
3.6.3.4.1 LPF circuit
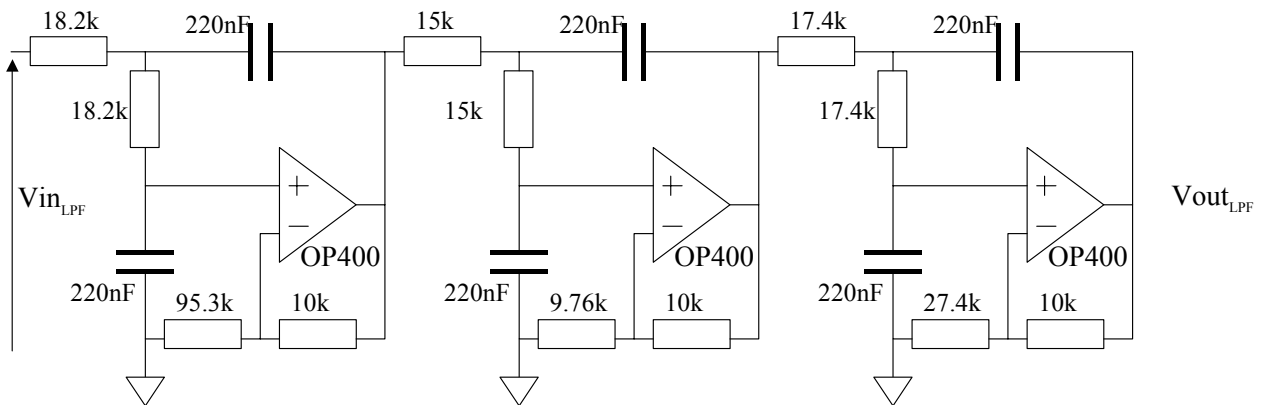
3.6.3.4.2 LPF transfer function

Transfer function: $\dfrac{V_{out}}{V_{in}} = 3{,}05 \times \dfrac{1}{1+7.58p+4p^2} \times \dfrac{1}{1+3.21p+3{,}3p^2} \times \dfrac{1}{1+6.26p+3.828p^2}$ (p=j2πf)

3.6.3.4.3 LPF transfer function simulation result

The two following simulation results show respectively the magnitude and the phase transfer function of LIA Spectrometer six-pole Bessel LPF:
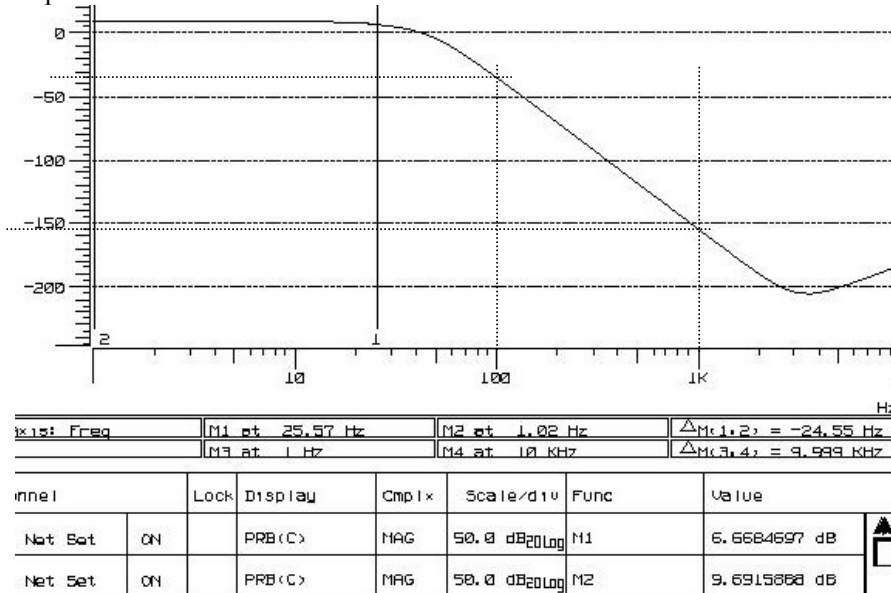
Figure 3-21 LIA Spectrometer LPF Magnitude Transfer Function

Simulation results:

- At a frequency of 1.02Hz the gain is 9.69 dB (3.05)
- The –3dB cut off frequency is at 25.5Hz.
- The slope is –120dB/decade.
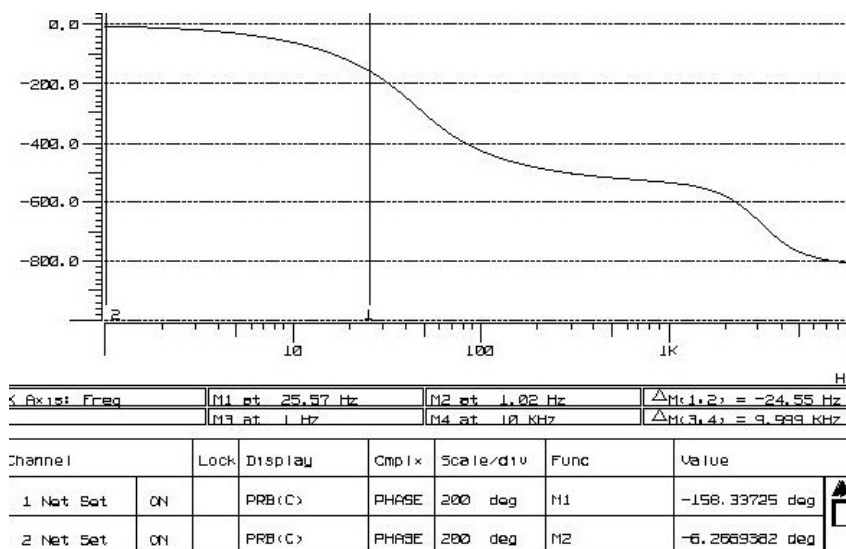
Figure 3-22 LIA Spectrometer LPF Phase Transfer Function

3.6.3.5 LIA Spectrometer Channel Noise

MAT02 : BW 50 –300Hz : Vn=1nV/√Hz

Resistors noise : $In=\sqrt{\dfrac{4kT}{R}}$; T=295K ; $4kT=1.63\times10^{-20}$

Input preamplifier noise: $Vn_{preampl}=\sqrt{2\times(Vn_{MAT02})^2+264^2(In_{264}{}^2+4In_{15k}{}^2)}=2.57nV/\sqrt{Hz}$

OP400 at 0.1Hz: Vn=66nV/√Hz; In=1.6pV/√Hz

LPF Stage 1: $Vn_{LPF1}=\sqrt{(Vn_{OP400})^2+(45\times10^3\times In_{OP400})^2+Vn_{45k}{}^2}=101nV/\sqrt{Hz}$

LPF Stage 2: $Vn_{LPF2}=\sqrt{(Vn_{OP400})^2+(35\times10^3\times In_{OP400})^2+Vn_{35k}{}^2}=90nV/\sqrt{Hz}$

LPF Stage 3: $Vn_{LPF3}=\sqrt{(Vn_{OP400})^2+(42\times10^3\times In_{OP400})^2+Vn_{42k}{}^2}=98nV/\sqrt{Hz}$

Input noise LPF: $Vn_{LPF}=\sqrt{(Vn_{LPF1})^2+\left(\dfrac{Vn_{LPF2}}{1.1}\right)^2+\left(\dfrac{Vn_{LPF3}}{2.2}\right)^2}=137nV/\sqrt{Hz}$

Noise total at the photometer LPF output:

$$Vn_{LPFout}=\sqrt{\left[(Vn_{preampl}\times H_{BPF})^2\times\left(\dfrac{4}{\pi}\right)^2\times\left[1+\left(\dfrac{1}{3}\right)^2+\left(\dfrac{1}{5}\right)^2+\left(\dfrac{1}{7}\right)^2+\left(\dfrac{1}{9}\right)^2\right]+(Vn_{LPF})^2\right]\times H_{LPF}{}^2}=1226nV/\sqrt{Hz}$$

Band pass filter gain H_{BPF}=107; Low pass filter gain H_{LPF}=3.03 and Total channel gain H_{TOT}=294

So the input noise equivalent for a photometer channel is:

$$Vn_{in}=\frac{Vn_{LPFout}}{H_{TOT}}=4.13nV/\sqrt{Hz}$$

LIA Spectrometer MUX FUNC-02-8 (1/2) and LIA outputs
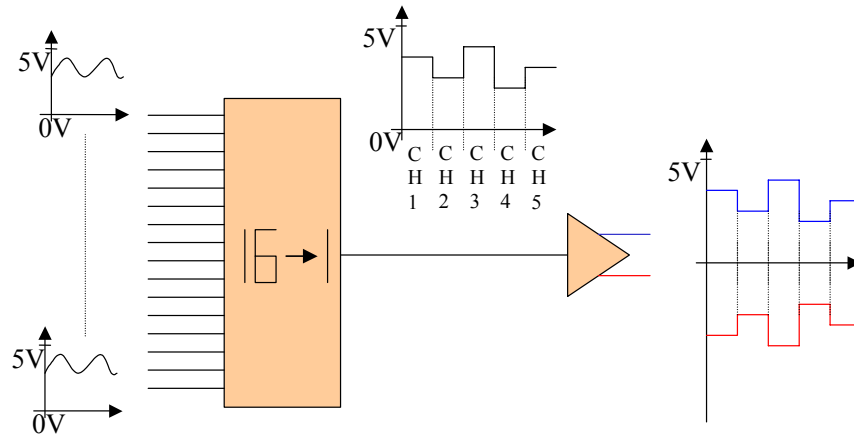
The first multiplexing stage FUNC-02-8 (1/2) is done by analog mux HS508. The differential output is done by two OP484.

See circuit.

3.6.3.5.1 Circuit
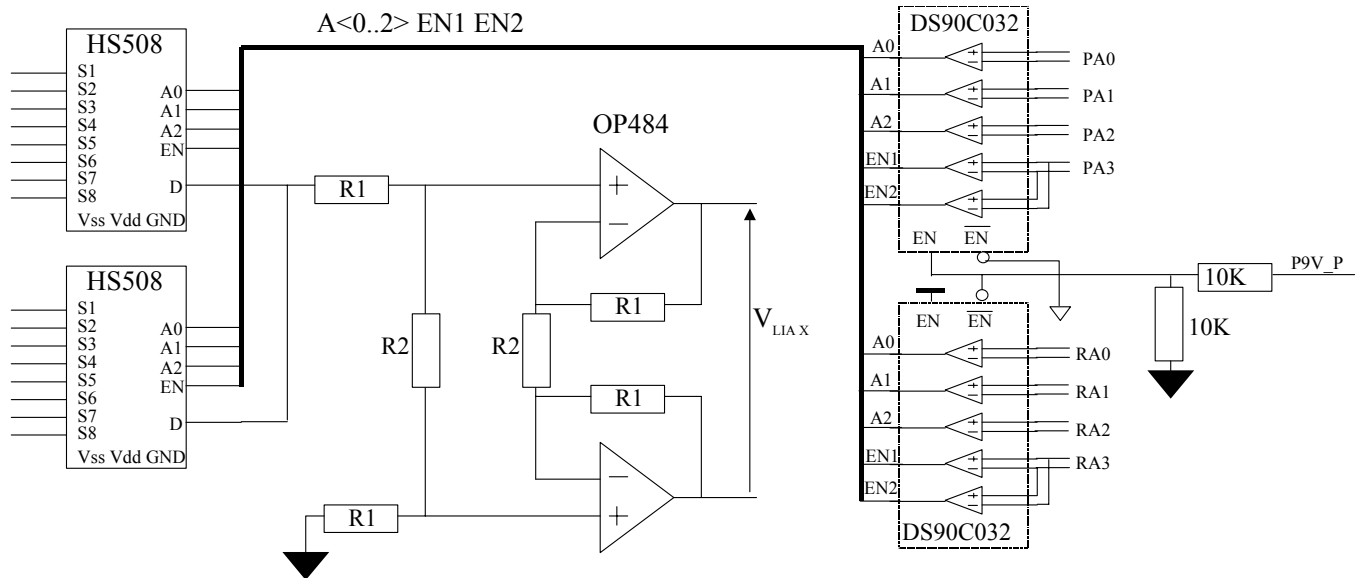
3.6.3.5.2 Noise

See noise synthesis section (on DAQ+IF).

3.6.3.5.3 Timing

See FPGA section.

3.7 BIAS BOARDS

3.7.1 BIAS Board Overview
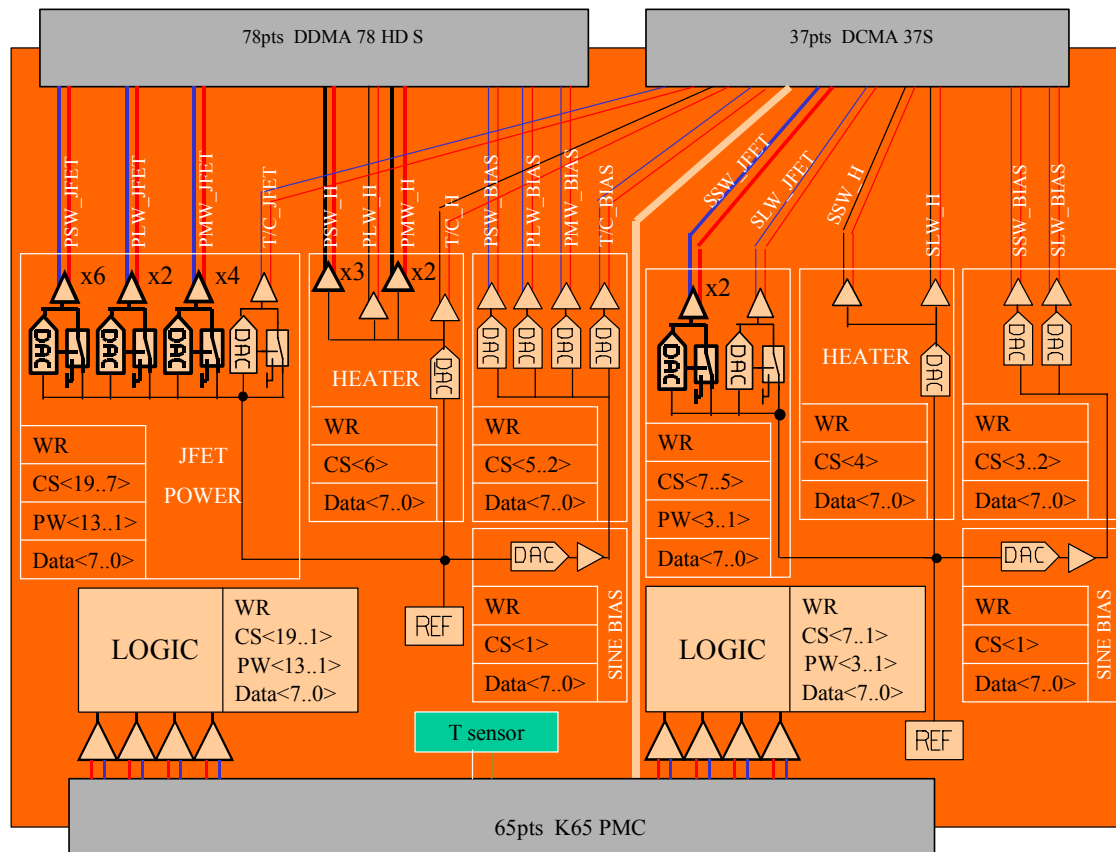
Figure 3-23 BIAS Board Overview

The BIAS boards generate sine biases for the bolometers and DC biases for JFETs and heaters.
- Adjustable sine biases:
  - Photometer: 1sine generator/ 4 channels with independent amplitudes
  - Spectrometer: 1sine generator/ 2 channels with independent amplitudes
  - Voltage range: 0 to 200 mVrms for the bolometers 0 to 500 mVrms for the thermometers
  - Accuracy: 256 levels
  - Frequency range: 50 to 300Hz
- Adjustable DC JFET biases:
  - Photometer: 13 generators for JFET
  - Spectrometer: 3 generators for JFET
  - Voltage range: 0 to –5V for VSS with 256 levels and VDD is set between 0 and 4V by two resistors
  - Output currents: 5mA max
- Adjustable DC heater biases:
  - Photometer: 1heater generator and 7 buffers
  - Spectrometer: 1 heater generator and 3 buffers
  - Voltage range: 0 to –5V with 256 levels
  - Output currents: 5mA max for each buffer

Note: Each buffer biases at most 2 JFET module* heaters.   (*JFETmodule = 24 channels)

3.7.2   BIAS Board Interface

Interface	Name	Description	Type	Level	In/Out	Frequency
BIAS	PBAIS_ xx	Bolometer BIAS Differential Signal	Analogic	200mVrms to 0v	OUT	50-300Hz
	NBAIS_ xx					
	PBAIS_TC	Bolometer TC BIAS Differential Signal	Analogic	500mVrms to 0v	OUT	50-300Hz
	NBAIS_TC					
VSS/VDD/HEATER	VSS xx	JFET source voltage	Analogic	0 to-5V	OUT	DC
	VDD xx	JFET Drain voltage	Analogic	2.5V	OUT	DC
	NHEATER xx	Heaters bias	Analogic	0 to-5V	OUT	DC
	PHEATER xx		Analogic	0V	OUT	DC
SERIAL LINK PHOTOMETER	CLK_P+	Serial link clock Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	0-10MHz
	CLK_P-					
	SDATA_P+	Serial link data Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	0-10MHz
	SDATA_P-					
	WR_DATA_P+	Serial link data write Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	0-768kHz
	WR_DATA_P-					
	WR_ADRESS_P+	Serial link address write Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	0-48kHz
	WR_ADRESS_P-					
SERIAL LINK SPECTROMETER	CLK_S+	Serial link clock Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	0-10MHz
	CLK_S-					
	SDATA_S+	Serial link data Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	0-10MHz
	SDATA_S-					
	WR_DATA_S+	Serial link data write Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	0-768kHz
	WR_DATA_S-					
	WR_ADRESS_S+	Serial link address write Differential Signal	Numeric (LVDS)	-0,3Vto 0,3V	IN	0-48kHz
	WR_ADRESS_S-					
BIAS_ TEMPERATURE	PT_P9V	Sensor PRIME Bias	Analogic	9V	IN	DC
	PT	Output Sensor PRIME	Analogic	2 to 4V	OUT	-
	RT_P9V	Sensor REDUNDANT Bias	Analogic	9V	IN	DC
	RT	Output Sensor REDUNDANT	Analogic	2 to 4V	OUT	-
POWER	P9V_P	9V Power Supply photometer	Power	9V	IN	DC
	N9V_P	-9V Power Supply photometer	Power	-9V	IN	DC
	P9V_S	9V Power Supply spectrometer	Power	9V	IN	DC
	N9V_S	-9V Power Supply spectrometer	Power	-9V	IN	DC

3.7.3 BIAS BOARD FUNCTIONS

3.7.3.1 BIAS sine conversion digital to analog (FUNC-01-2)

The function DCU-FUNC-01-2 generates a sinusoidal signal with amplitude of 5V and a 0Vcenter from a digital sine wave.
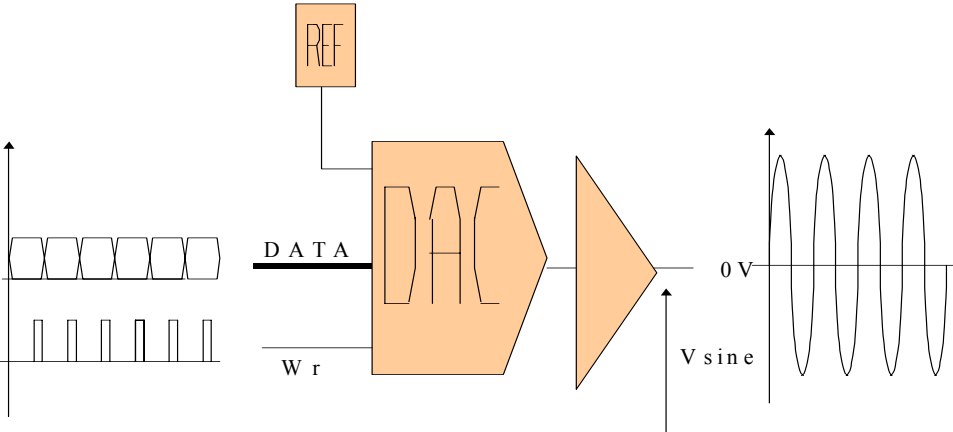
This function is implemented twice on the BIAS board (1for the photometer and 1 for the spectrometer.)

3.7.3.1.1 circuit
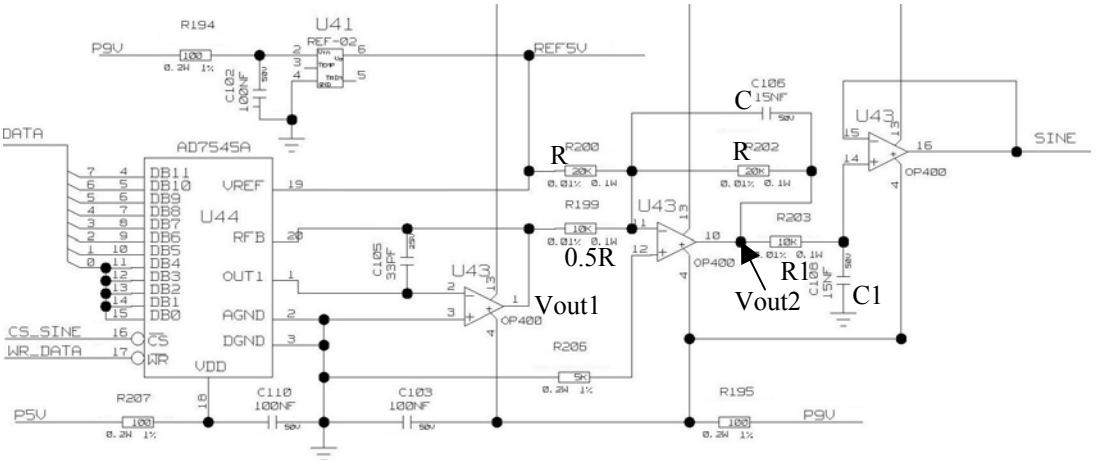
Figure 3-24 Sine Generator

3.7.3.1.2 Sine expression

$$V\sin e = REF \cdot \frac{\left(1 - \frac{DATA}{128}\right)}{(1 + RC \cdot p)(1 + R_1 C_1 \cdot p)} = \frac{5(128 - DATA)}{\left(1 + \frac{p}{2\pi.530}\right) \cdot \left(1 + \frac{p}{2\pi.1061}\right) \cdot 128} \quad (p = j2\pi f)$$

Note: DATA is an integer between 0 and 255

To generate sinusoidal signal with frequency **Fsine** the 256 integers, which describe a sine, should be wrote in the digital to analog converter with a frequency for **256.Fsine**.

The 256 values can be calculated by taken the nearest integer of $[\mathit{127.SIN(2\pi(n+1/2)/256)+128}]$ with **n** between **0** and **255**.

See FPGA section.

3.7.3.2   BIAS sine attenuator (FUNC-01-3 and FUNC-01-4)

The functions FUNC-01-3 and FUNC-01-4 determinate the sinusoidal signal amplitude for each BDA group.
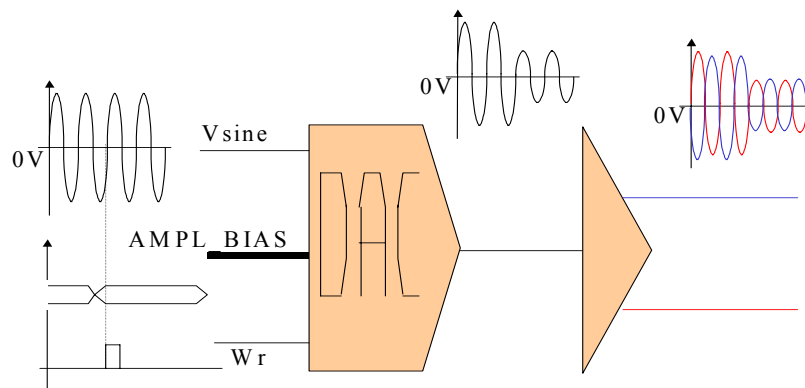
Each bolometer group has its own bias attenuator.

- The 4 bias attenuators of the photometer receive at their input the signal coming from the photometer BIAS sine conversion digital to analog.
- As well as The 2 bias attenuators of the spectrometer receive at their input the signal coming from the spectrometer BIAS sine conversion digital to analog.

3.7.3.2.1 Circuit

The bias attenuator circuit is as follow:
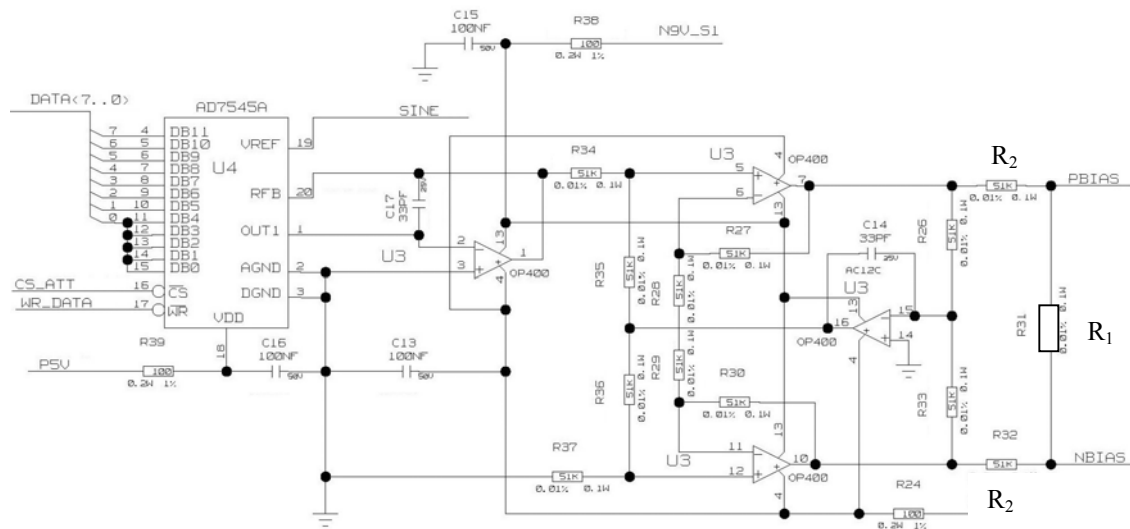
Figure 3-25 Bias Attenuator

3.7.3.2.2 BIAS expression

- FOR PSW, PMW, PLW, SSW and SLW: R1=8K and R2=51,1K

If the redundant and prime bias boards are connected together:

$$BIAS = \frac{AMPL\_BIAS}{256} \cdot \frac{R_1/2}{2.R_2 + R_1/2} \cdot V \sin e = \frac{AMPL\_BIAS}{256 \cdot 128} \cdot \frac{0.2 \cdot (128 - DATA)}{\left(1 + \frac{p}{2\pi.530}\right)\left(1 + \frac{p}{2\pi.1061}\right)}$$

If not:

$$BIAS = \frac{AMPL\_BIAS}{256} \cdot \frac{R_1}{2 \cdot R_2 + R_1} \cdot V \sin e = \frac{AMPL\_BIAS}{256 \cdot 128} \cdot \frac{0.4 \cdot (128 - DATA)}{\left(1 + \frac{p}{2\pi.530}\right)\left(1 + \frac{p}{2\pi.1061}\right)}$$

- FOR TC: R1=23K and R2=51,1K

If the redundant and prime bias boards are connected together:

$$BIAS = \frac{AMPL\_BIAS}{256} \cdot \frac{R_1/2}{2.R_2 + R_1/2} \cdot V \sin e = \frac{AMPL\_BIAS}{256 \cdot 128} \cdot \frac{0.5 \cdot (128 - DATA)}{\left(1 + \frac{p}{2\pi.530}\right)\left(1 + \frac{p}{2\pi.1061}\right)}$$

If not:

$$BIAS = \frac{AMPL\_BIAS}{256} \cdot \frac{R_1}{2 \cdot R_2 + R_1} \cdot V \sin e = \frac{AMPL\_BIAS}{256 \cdot 128} \cdot \frac{0.92 \cdot (128 - DATA)}{\left(1 + \frac{p}{2\pi.530}\right)\left(1 + \frac{p}{2\pi.1061}\right)}$$

3.7.3.3   JFET VSS and VDD (FUNC-05-1, FUNC-05-2, FUNC-05-3 and FUNC-05-4)

Each JFET module has its own JFET bias generator. A JFET bias generator provide a negative DC tension VSS (DCU-FUNC-05-1 and DCU-FUNC -05-2) and a positive DC tension VDD (DCU-FUNC-05-3 and DCU-FUNC -05-4)

3.7.3.3.1 Circuit

Figure 3-26 JFET Bias Generator

3.7.3.3.2 Characteristic

- VSS generator:

Function DCU-FUNC-05-1:
- From a +5V precision voltage reference, the DAC and the first OP generate a tension proportional to the digital 8 bits DATA: **$VSS = -REF5V(DATA/256)$.**

Function DCU-FUNC-05-2:
- The second OP and his following components are there to:
  o Avoid overshoot when VSS is set ON from OFF or the other way
  o Make the connection with the empowered redundant bias board safe and use full
  o Provide the 5mA required.

- VDD generator:

Function DCU-FUNC-05-3:
- When the switch is **ON** a +5V precision voltage reference is applied on two resistors R1 and R2 so **$VDD = REF5V.R2/(R1+R2)$.**
- When the switch is **OFF** the ground is applied on two resistors R1 and R2 so **$VDD= 0V$.**

Function DCU-FUNC-05-4:
- The second OP and his following components are there to:
  o Avoid overshoot when VDD is set ON from OFF or the other way
  o Make the connection with the empowered redundant bias board safe and use full
  o Provide the 5mA required.

3.7.3.3.3 Simulation

The following simulation shows the switching ON and OFF of VSS, VDD.
- VSS switched ON 0V to –5V. (A=5V)
- VSS switched OFF -5V to 0V. (A=0V)
- VDD switched ON 0V to 2.5V. (A=5V)
- VDD switched OFF 2.5V to 0V. (A=0V)

The prime generators are powered, the redundant ones are not.
The load resistor is set for a nominal generator output current of 5mA.

Channel		Lock	Display	Scale/Div	Func	Value	
1 Scope Set		OFF	PRB(D)	2.00 V	M1	2.4999798 V	
2 Scope Set		ON	C1	PRB(C) (VDD)	2.00 V	M1	2.4502415 V
3 Scope Set		ON	C1	PRB(B) (VSS)	2.00 V	M1	-4.9495840 V
4 Scope Set		ON		PRB(I)	2.00 mA	M1	4.9332169 mA
5 Scope Set		ON	C1	PRB(F)	2.00 V	M1	2.5000662 V
6 Scope Set		ON	C1	PRB(E)	2.00 V	M1	-4.9999111 V
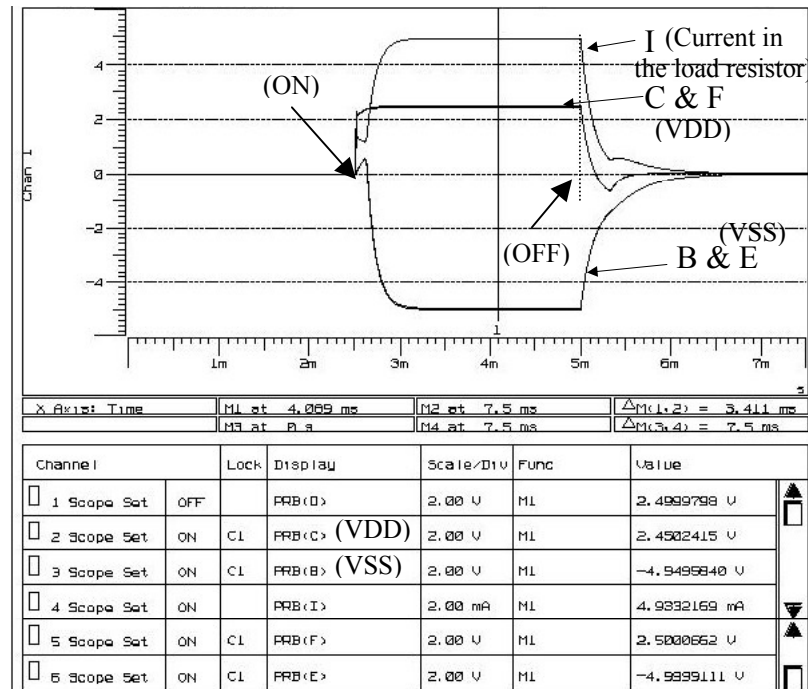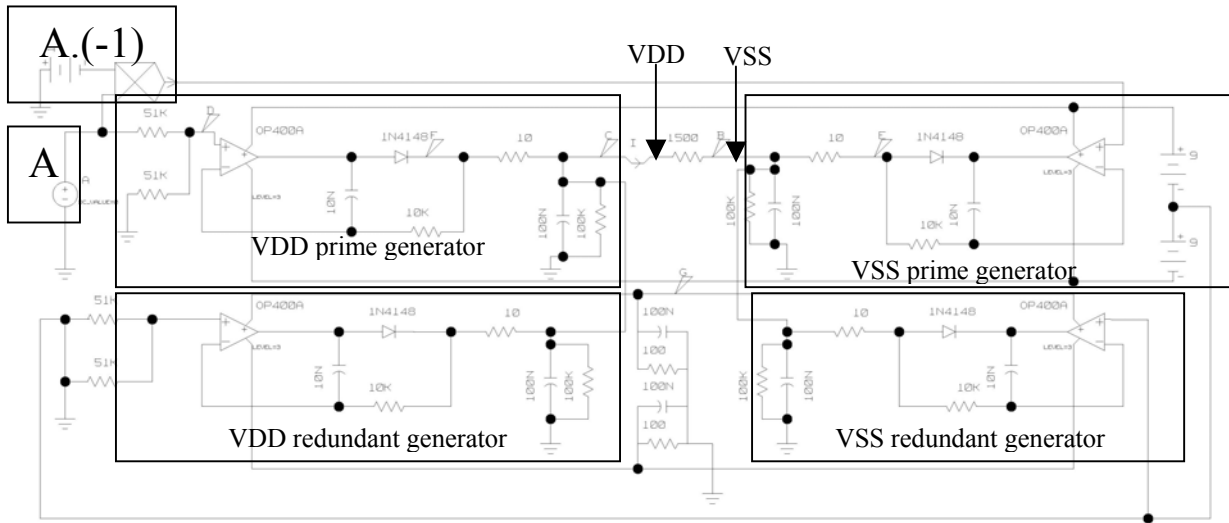
Figure 3-27 JFET Bias Generator Simulation

3.7.3.4   Heater (FUNC-05-5 and FUNC-05-6)

To bias the photometer heaters there are:

- A bias generator FUNC-05-5 and 7 buffers FUNC-05-6 (the buffer heater is similar to a VSS buffer) of which:
  o each 6 buffers bias each 2 JFET module heaters
  o 1 buffer biases only the T/C JFET module

To bias the spectrometer heaters there are:

- A bias generator FUNC-05-5 and 2 buffers FUNC-05-6 (the buffer heater is similar to a VSS buffer) of which:
  o 1 buffer biases 2 JFET module heaters
  o 1 buffer biases only 1 JFET module heater

3.7.3.4.1 Circuit
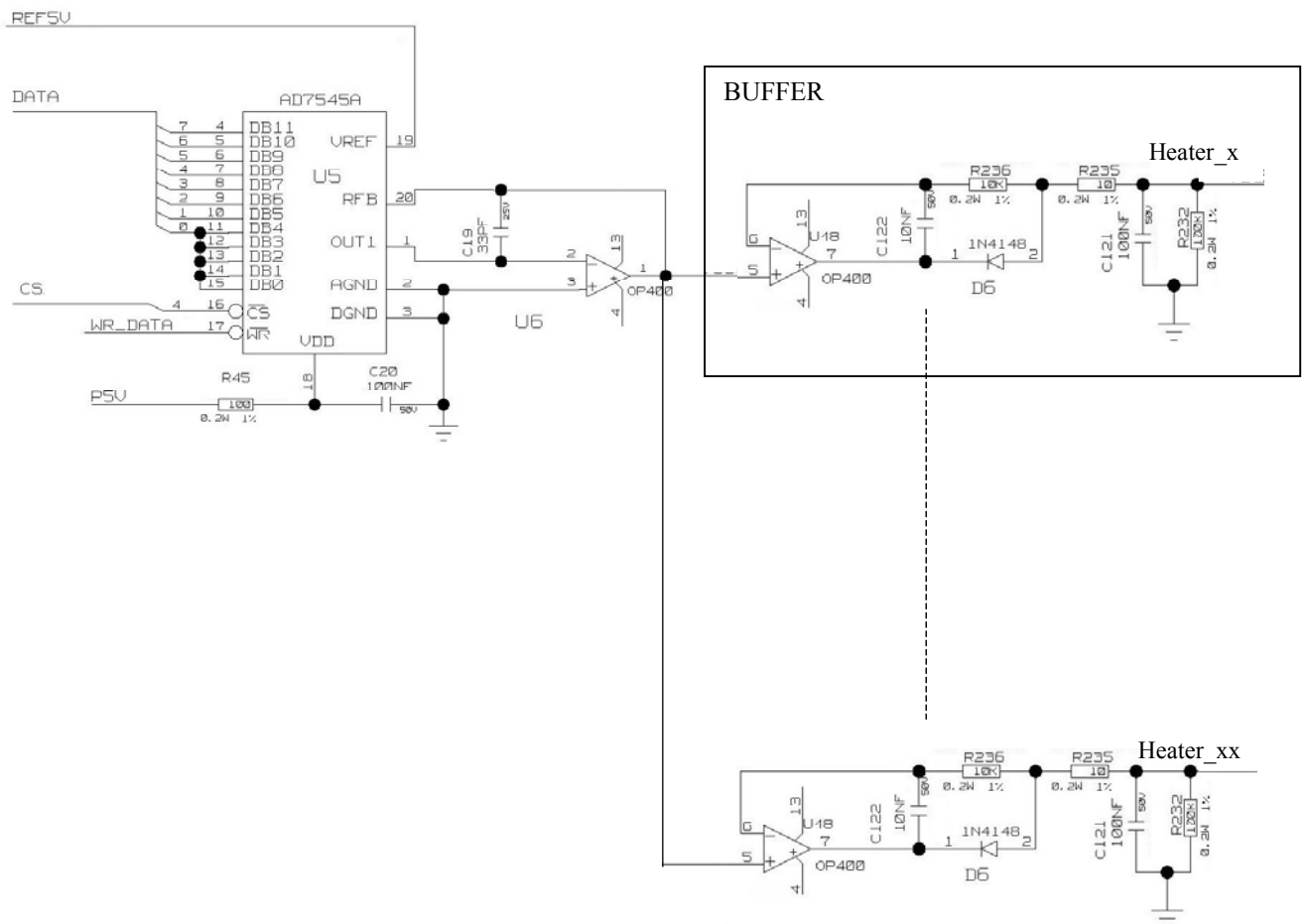
Figure 3-28 Heater Bias Generator

3.7.3.5   Serial receiver

- All of the photometer DACs CS (chips select) and ON/OFF switches are connected to four 8-bit latched SIPO (Serial Input to Parallel Output) shift registers.
- The 17 photometer DACs are connected to the same write signal WR_DATA_P.
- The four 8-bit latch SIPO shift registers are connected to the same latch signal WR_ADRESS_P
- The photometer 8-bit parallel DATA_P bus is provided by one SIPO shift register.

BIT number	Command	BIT number	Command
A1	CS Sine bias generator	A17	CS VSS12_P
A2	CS PSW bias attenuator	A18	CS HEATER_P
A3	CS PLW bias attenuator	A19	ON/OFF VDD1_P
A4	CS T/C bias attenuator	A20	ON/OFF VDD2_P
A5	CS PMW bias attenuator	A21	ON/OFF VDD3_P
A6	CS VSS1_P	A22	ON/OFF VDD4_P
A7	CS VSS2_P	A23	ON/OFF VDD5_P
A8	CS VSS3_P	A24	ON/OFF VDD6_P
A9	CS VSS4_P	A25	ON/OFF VDD7_P
A10	CS VSS5_P	A26	ON/OFF VDD8_P
A11	CS VSS6_P	A27	ON/OFF VDD9_P
A12	CS VSS7_P	A28	ON/OFF VDD10_P
A13	CS VSS8_P	A29	ON/OFF VDD11_P
A14	CS VSS9_P	A30	ON/OFF VDD12_P
A15	CS VSS10_P	A31	ON/OFF VDD_TC
A16	CS VSS11_P	A32	CS VSS_TC

Figure 3-29 Photometer Bias serial link timing

- All of the spectrometer DACs chips select and ON/OFF switches are connected to two 8-bit latch SIPO (Serial Input to Parallel Output) shift registers.
- The 7 spectrometer DACs are connected to the same write signal WR_DATA_S.
- The two 8-bit latch SIPO shift registers are connected to the same latch signal WR_ADRESS_S
- The spectrometer 8-bit parallel DATA_S bus is provided by SIPO shift register.

BIT number	Command	BIT number	Command
A1	CS Sine bias generator spectro	A9	ON/OFF VDD1_S
A2	CS SSW bias attenuator	A10	ON/OFF VDD2_S
A3	CS SLW bias attenuator	A11	ON/OFF VDD3_S
A4	CS VSS1_S	A12	-
A5	CS VSS2_S	A13	-
A6	CS VSS3_S	A14	-
A7	CS HEATER_S	A15	-
A8	-	A16	-
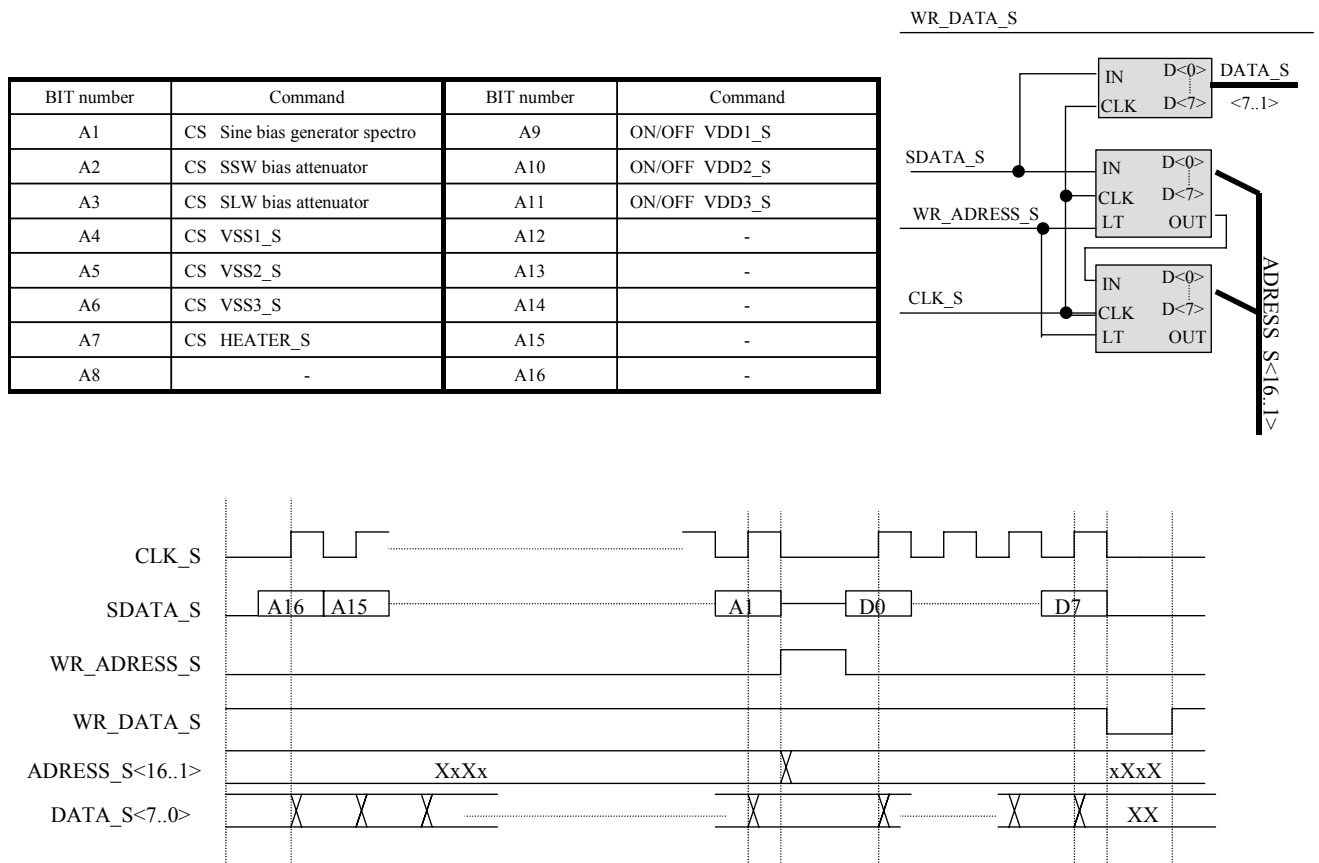
Figure 3-30 Spectrometer Bias serial link timing

3.7.3.6 JFET BIAS Noise

See DCU BIAS Test plan result.

3.8   DAQ+IF BOARD

3.8.1   DAQ+IF Board Overview
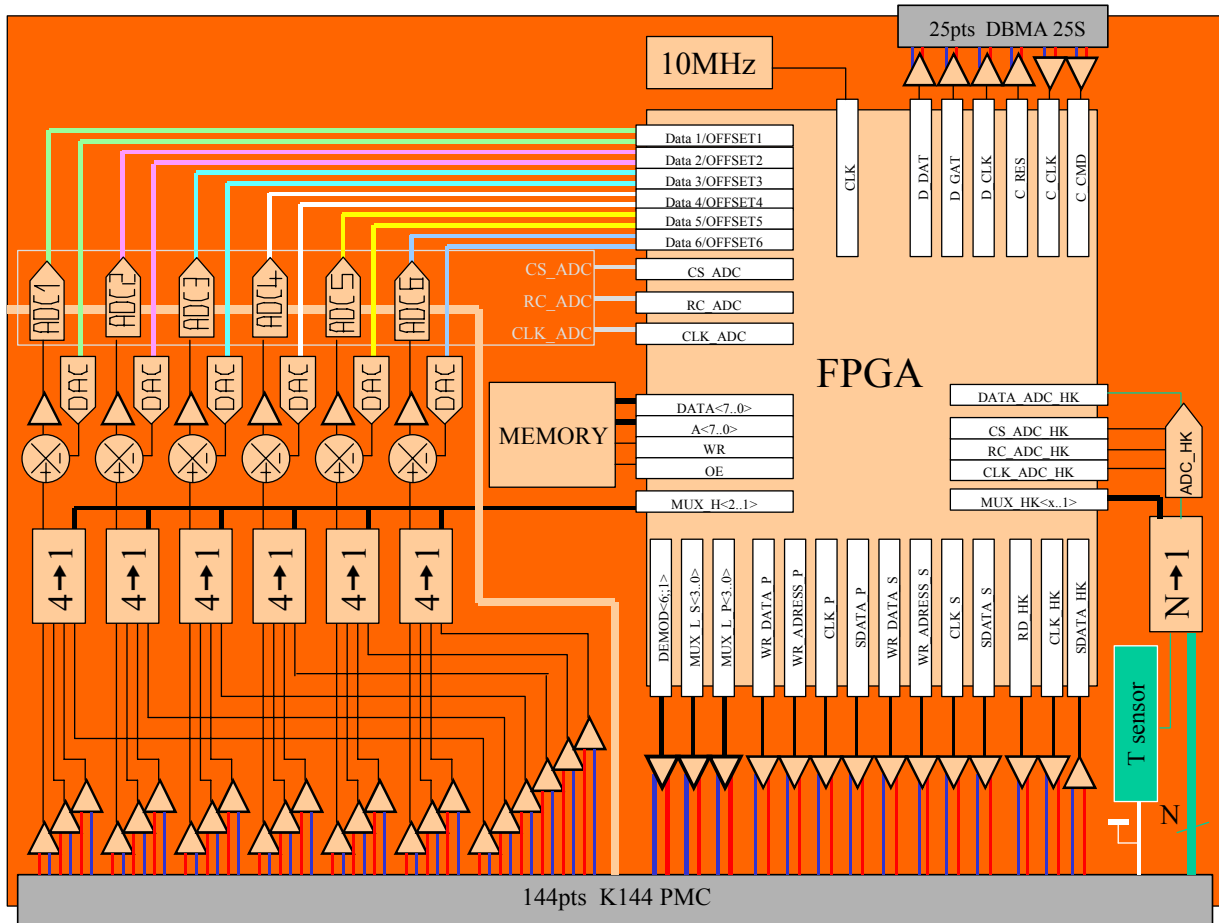
Figure 3-31 DAQ+IF Board Overview

- The DAQ+IF boards receive the bolometer analog signal for all LIA boards output, apply an offset on each bolometer signal, amplify them a last time, and then digitize them.

-The digitized data are embedded in a frame sent to the DPU through the fast link.

-The FPGA carries digital functions like:
- Low level command decoding
- Low level command acknowledge + HK parameters transfer
- The timestamp generation

-It provides all the digital signals needed by LIA and BIAS boards, and as well as the internal DAQ+IF board signals.

3.8.2 DAQ+IF Board Interface

Interface	Name	Description	Type	Level	In/Out	Frequency
DATA	D_CLK_DCU_P+	Data clock	Numeric	-0,3Vto	OUT	2.5MHz
	D_CLK_DCU_P-	Differential Signal		0,3V		
	D_GAT_DCU_P+	Data gate	Numeric	-0,3Vto	OUT	2.5MHz
	D_GAT_DCU_P-	Differential Signal		0,3V		
	D_DAT_DCU_P+	Data	Numeric	-0,3Vto	OUT	2.5MHz
	D_DAT_DCU_P-	Differential Signal		0,3V		
CMD_ ACK&STATUS	C_RES_DCU_P+	Commands response	Numeric	-0,3Vto	OUT	3.125 kHz
	C_RES_DCU_P-	Differential Signal		0,3V		
CMD	C_CMD_DCU_P+	Commands	Numeric	-0,3Vto	IN	3.125 kHz
	C_CMD_DCU_P-	Differential Signal		0,3V		
	C_CLK_DCU_P+	Commands clock	Numeric	-0,3Vto	IN	3.125 kHz
	C_CLK_DCU_P-	Differential Signal		0,3V		
MUX_CHANNEL	POUT x	channels Multiplexed in	Analogic	0 to 5V	IN	0-25Hz at mux freq.
	NOUT x	a Differential Signal				
CMD_MUX_H LIA_P & LIA_S	Ax-	BIT Command Mux (PRIME)	Numeric	-0,3Vto	OUT	~10kHz
	Ax+	Differential Signal		0,3V		
DEMOD_x	DEMODx-	Demodulation	Numeric	-0,3Vto	OUT	50-300Hz
	DEMODx+	Differential Signal (PRIME) for Channels One to Twenty-four		0,3V		
SERIAL LINK PHOTOMETER	CLK_P+	Serial link clock	Numeric	-0,3Vto	OUT	0-10MHz
	CLK_P-	Differential Signal		0,3V		
	SDATA_P+	Serial link data	Numeric	-0,3Vto	OUT	0-10MHz
	SDATA_P-	Differential Signal		0,3V		
	WR_DATA_P+	Serial link data write	Numeric	-0,3Vto	OUT	0-768kHz
	WR_DATA_P-	Differential Signal		0,3V		
	WR_ADRESS_P+	Serial link address write	Numeric	-0,3Vto	OUT	0-48kHz
	WR_ADRESS_P-	Differential Signal		0,3V		
SERIAL LINK SPECTROMETER	CLK_S+	Serial link clock	Numeric	-0,3Vto	OUT	0-10MHz
	CLK_S-	Differential Signal		0,3V		
	SDATA_S+	Serial link data	Numeric	-0,3Vto	OUT	0-10MHz
	SDATA_S-	Differential Signal		0,3V		
	WR_DATA_S+	Serial link data write	Numeric	-0,3Vto	OUT	0-768kHz
	WR_DATA_S-	Differential Signal		0,3V		
	WR_ADRESS_S+	Serial link address write	Numeric	-0,3Vto	OUT	0-48kHz
	WR_ADRESS_S-	Differential Signal		0,3V		
SERIAL LINK HK	CLK_HK+	Serial link clock	Numeric	-0,3Vto	OUT	0-xMHz
	CLK_HK-	Differential Signal		0,3V		
	SDATA_HK+	Serial link data	Numeric	-0,3Vto	OUT	0-xMHz
	SDATA_HK-	Differential Signal		0,3V		
	RD_HK+	Serial link data read	Numeric	-0,3Vto	OUT	0-xkHz
	RD_HK-	Differential Signal		0,3V		
BIAS&LIA_ TEMPERATURE	T_P9V	Sensor PRIME Bias	Analogic	9V	OUT	DC
	T	Output Sensor PRIME	Analogic	1 to 2V	IN	-
POWER	P9V	9V Power Supply	Power	9V	IN	DC
	N9V	-9V Power Supply	Power	-9V	IN	DC
	P5V	5V Power Supply	Power	5V	IN	DC
POWER_LIA_P	P9V_LIA_P	9V Power Supply	Power	9V	IN	DC
	N9V_LIA_P	-9V Power Supply	Power	-9V	IN	DC
	P5V_LIA_P	5V Power Supply	Power	5V	IN	DC
POWER_LIA_S	P9V_LIA_S	9V Power Supply	Power	9V	IN	DC
	N9V_LIA_S	-9V Power Supply	Power	-9V	IN	DC
	P5V_LIA_S	5V Power Supply	Power	5V	IN	DC

3.8.3   DAQ+IF BOARD FUNCTIONS

3.8.3.1   LIA Channel Digitization Overview
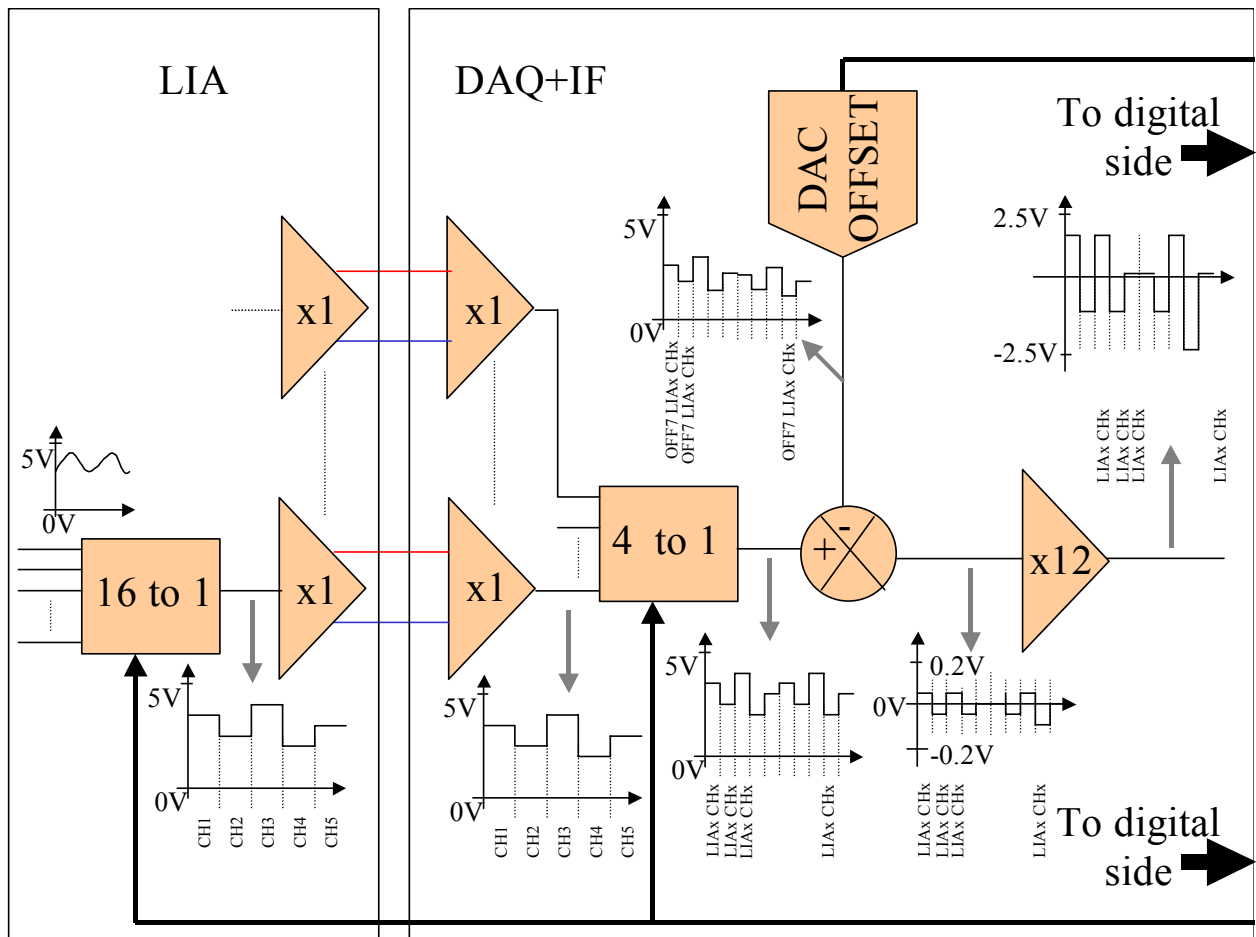
Channel way to digitization:

1. After the LIA_P (or LIA_S) channel processing, a bolometer signal is multiplexed with 15 (or 11) other bolometer signals on the same board.
2. Then the multiplexed signal goes out the LIA board through a differential amplifier with one unit gain.
3. The differential multiplexed signal goes into the DAQ+IF board through a differential receiver with one unit gain.
4. DAQ+IF board multiplexing stage:
   o If this multiplexed signal comes from the photometer it is then multiplexed with 2 other signals which come from 2 other LIA_P multiplexers. There are 48 photometer bolometer signals that are multiplexed.
   o If this multiplexed signal comes from the spectrometer then it goes straight through the multiplexer.
5. For each bolometer signal a predetermined offset signal is subtracted.
6. Afterwards, the signal is amplified by 12 and digitized.

3.8.3.2   Analog Receiver and Multiplexer FUNC-02-8

On a DAQ+IF board there are:
- 18 photometer analog receivers for the 18 LIA_P board output.
- 6   "Spectrometer" Analog receivers for the 6 LIA_S board output.
- 6 muxplexers
- Each multiplexer handles
  o   1 spectrometer analog receiver output.
  o   3 photometer analog receiver output.

3.8.3.2.1 Circuit
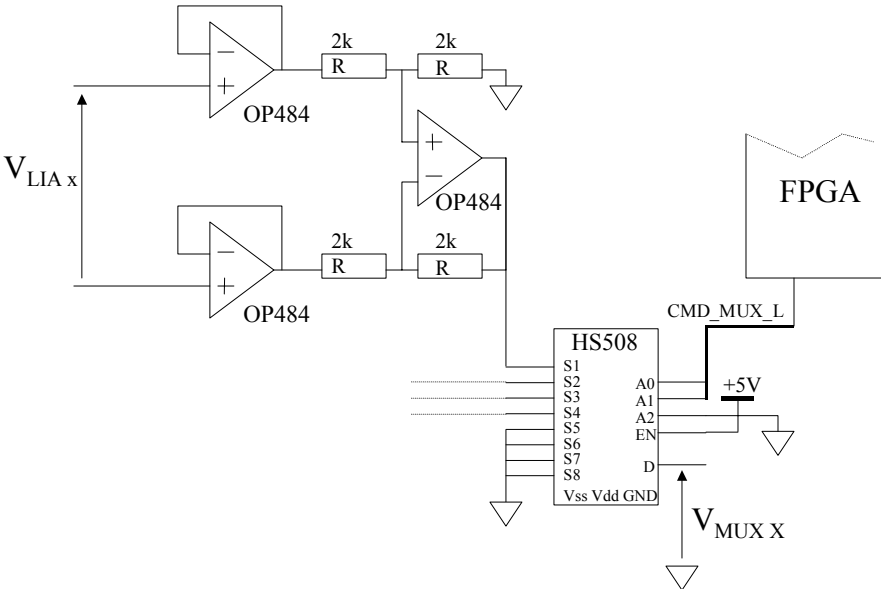
3.8.3.2.2 Noise

See noise synthesis section (on DAQ+IF).

3.8.3.2.3 Timing

See FPGA section.

3.8.3.2.4 Simulation

The following simulation determines the maximum time that an input ADC signal needs to be stabilized after different kinds of multiplexer switching:
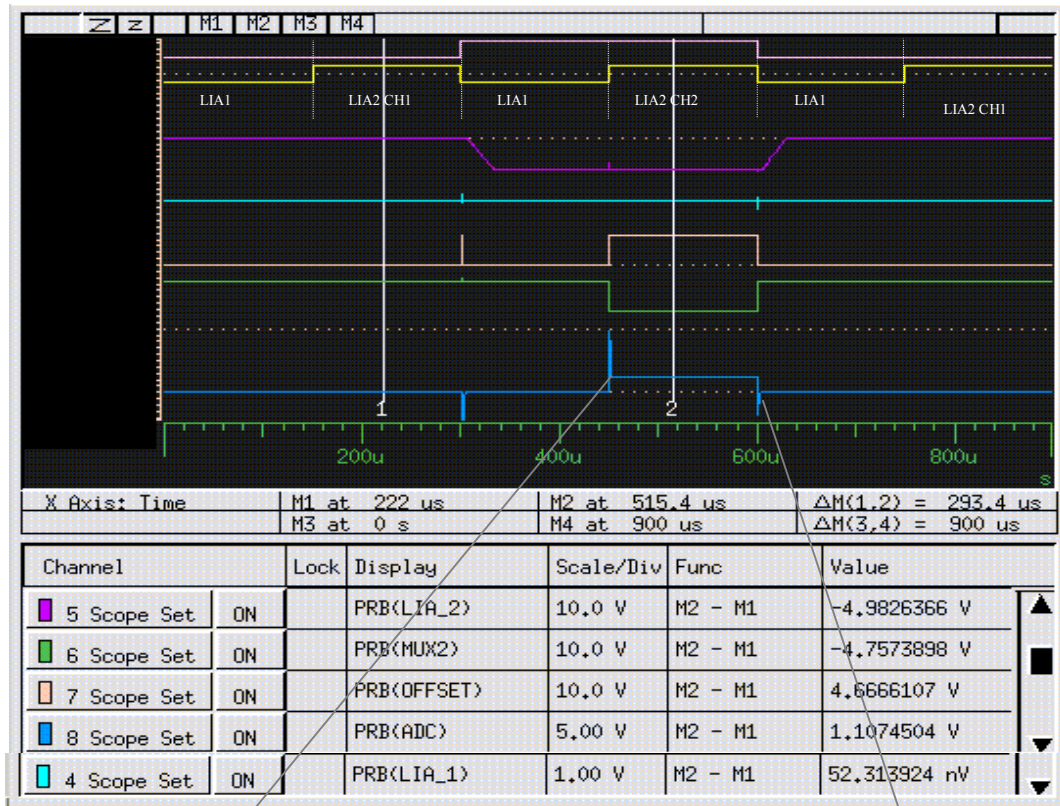
DETAIL N°1

DETAIL N°2

- When the LIA multiplexer and the DAQ multiplexer are switched at the same time, the ADC input signal is established and stabilized after 50 μs. (DETAIL N°2)
- When only the DAQ multiplexer is switched. The ADC input signal is established and stabilized after 20 μs. (DETAIL N°1)

3.8.3.3 Offset and Gain FUNC-02-6 and FUNC-02-7

After each mulptiplexer the channel signals that are going to be digitized are added with their 4-bit predetermined offset signal and the result is multiplied by -12 before to be digitized.
Each ADC is associated to one offset generator and gain amplifier.
2 multiplexers with an OP as follower build the 4-bit offset generators.

Note: In reality the output signal of a receiver is negative between 0v and –5V.
So we have (-channel +offset)x(-12) which it equivalent to (channel-offset)x(12).
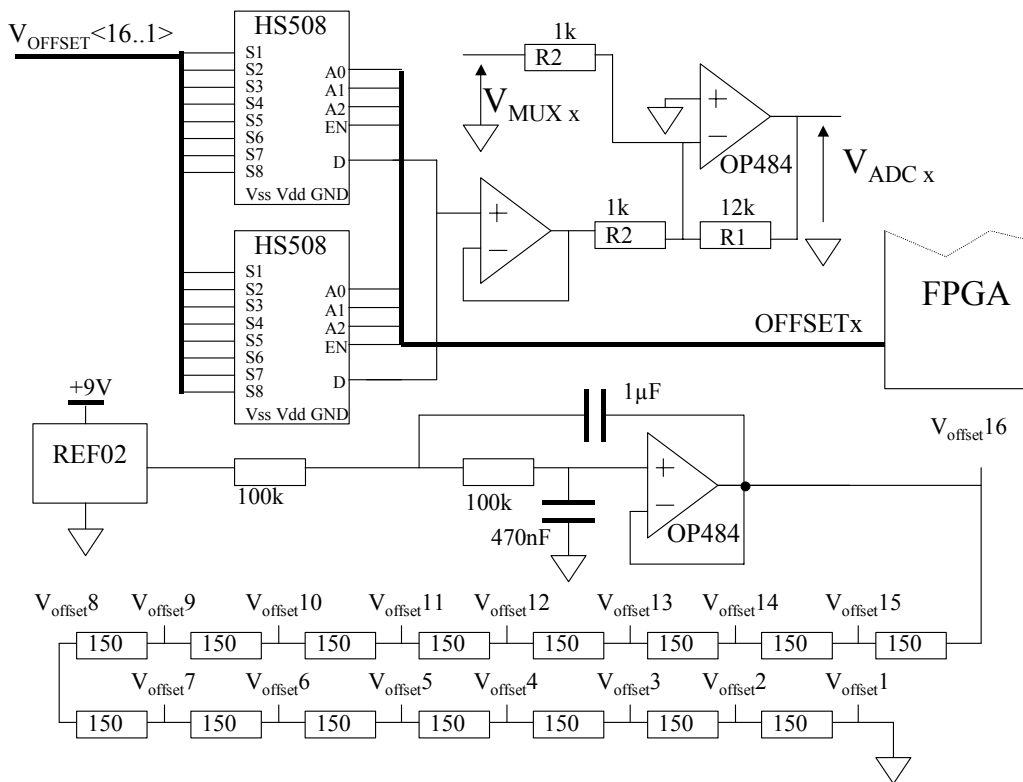
3.8.3.3.1 Circuit

Figure 3-32 Offset and Gain Circuit

3.8.3.3.2 Noise

See noise synthesis section (on DAQ+IF).

3.8.3.3.3 Timing

See FPGA section.

3.8.3.4   ADCs FUNC-03

The 6 ADC how make the function FUNC-03 are ADS7809 from SEI on a –2.5 to 2.5V scale and an external clock.

3.8.3.4.1 Circuit
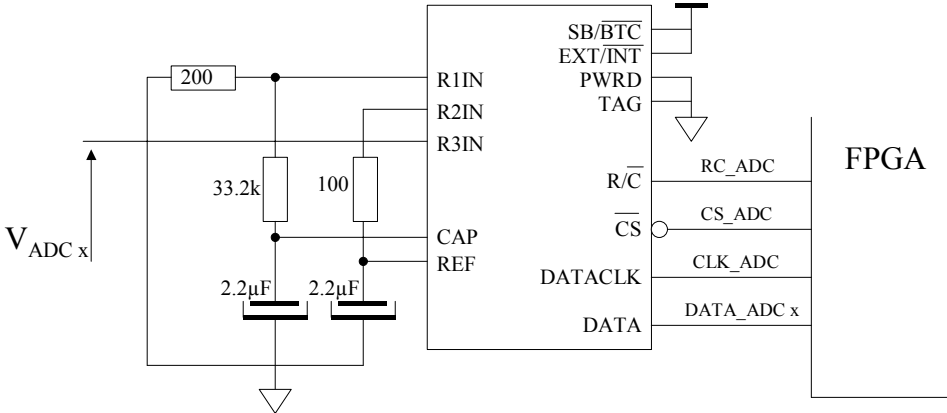
3.8.3.4.2 Noise

See noise synthesis section (on DAQ+IF).

3.8.3.4.3 Timing

See FPGA section.

3.8.3.5   Boards Temperature and power supplies Acquisition FUNC-09-1, FUNC-09-2 and FUNC-09-2

- MUX_HK selects the board temperature and power supplies voltage, that will to be digitized.
    o Board temperature:
        • The temperature range is –40°C to 80°C.
        • The digitized signal voltage range is 1.165V to 1.8V.
        • The ADC is 16-bit with a -2.5V to 2.5V input range.
        • The ADC voltage resolution is 76µV.
        • So the temperature resolution is 0.0144°C.
    o Power supplies voltage
        • All the power supplies are divided by 10 before digitization
        • The ADC is 16-bit with a -2.5V to 2.5V input range.
        • The voltage resolution for each power supplies voltage is 0,760mV.
        • The power supplies voltage range is –25V to 25V

MUX_HK					Board temperature
5	4	3	2	1	
0	0	0	0	0	BIAS temperature
0	0	0	0	1	LIA_S1 temperature
0	0	0	1	0	LIA_S2 temperature
0	0	0	1	1	LIA_S3 temperature
0	0	1	0	0	LIA_P9 temperature
0	0	1	0	1	LIA_P8 temperature
0	0	1	1	0	LIA_P7 temperature
0	0	1	1	1	LIA_P6 temperature
0	1	0	0	0	LIA_P5 temperature
0	1	0	0	1	LIA_P4 temperature
0	1	0	1	0	LIA_P3 temperature
0	1	0	1	1	LIA_P2 temperature
0	1	1	0	0	LIA_P1 temperature
0	1	1	0	1	DAQ+IF temperature
0	1	1	1	0	BIAS/DAQ_IF +5V
0	1	1	1	1	BIAS/DAQ_IF +9V
1	0	0	0	0	BIAS/DAQ_IF –9V
1	0	0	0	1	LIA_P +5V
1	0	0	1	0	LIA_P +9V
1	0	0	1	1	LIA_P –9V
1	0	1	0	0	LIA_S +5V
1	0	1	0	1	LIA_S +9V
1	0	1	1	0	LIA_S –9V
1	0	1	1	1	--

3.8.3.5.1 Circuit
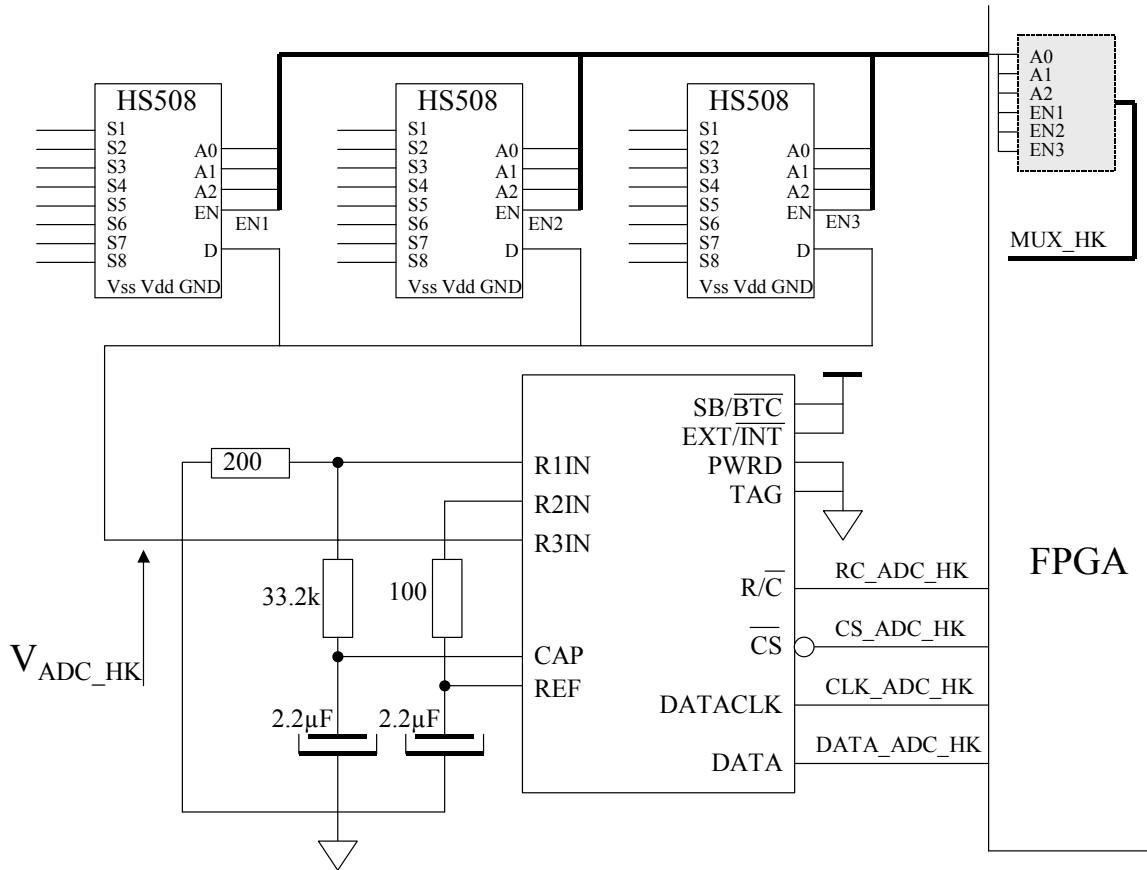
3.8.3.6 Noise Synthesis

cut off frequency	70000
BW	109955,7429
OP484 0-10Hz in Vrms	7,50E-08
OP484 10-1000Hz in Vrms/rtHz	5,00E-09
OP484 1000-xHz in Vrms/rtHz	3,90E-09
OP484 0-10Hz in Arms	1,00E-10
OP484 1000-xHz in Arms/rtHz	4,00E-13
OP484 total voltage noise in Vrms	1,52E-06
OP484 total current noise in Arms	2,33E-10
4KT	1,60E-20

last gain stage on DAQ+IF (FUNC-02-7)	
R1in ohm	12000
R2 in ohm	1000
total noise in Vrms	**2,51397E-06**
offset stage on DAQ+IF (FUNC-02-06)	
REF02	1,80E-06
Rtot in ohm	2250
total noise in Vrms	**2,68298E-06**
Substractor stage on DAQ+IF (Analog receiver)	
R in ohm	2000
total noise in Vrms	**2,42529E-06**
Differential receiver stage on DAQ+IF (Analog receiver)	
total noise in Vrms	**2,14911E-06**

Differential Transmitter stage on LIA	
R1 in ohm	100
R2 in ohm	1000
total noise in Vrms	**2,8715E-06**
LIA photometer channel (FUNC-02-05,*-04,*-03,-02,*-01)	
total noise in Vrms	**3,70E-06**
LIA spectrometer channel (FUNC-02-05,*-04,*-03,-02,*-01)	
total noise in Vrms	**6,13E-06**

ADC (FUNC-03)	
total noise in Vrms	**5,80E-05**

Photometer ADC input noise Vrms	**8,13E-05**
Spectrometer ADC input noise Vrms	**1,00E-04**

Photometer input noise V/rtHz	**8,20E-09**
Spectrometer input noise V/rtHz	**6,57E-09**

3.9 DAQ+IF FPGA

3.9.1 DAQ+IF FPGA Overview
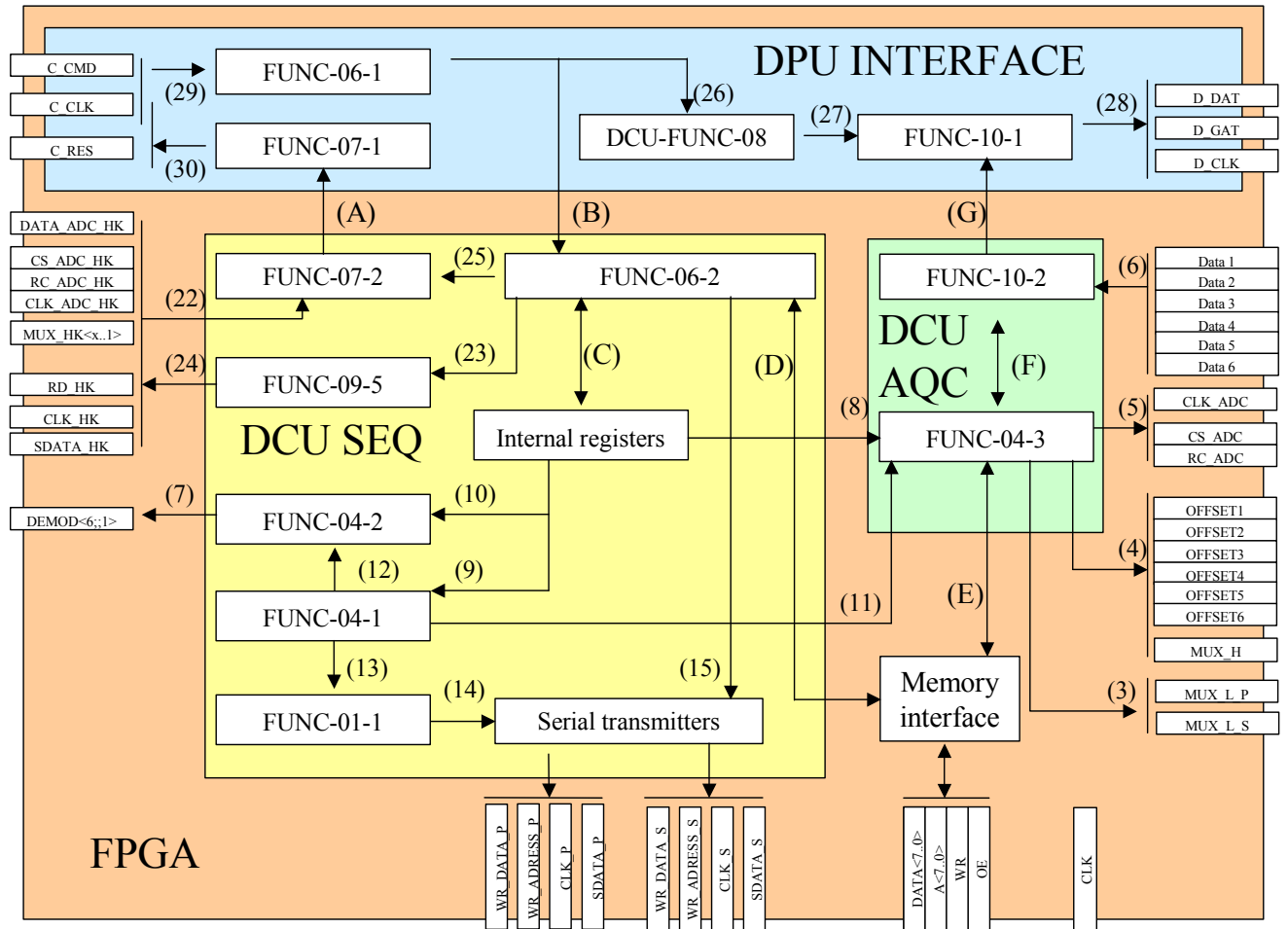
Figure 3-33 DAQ+IF FPGA Overview

This FPGA is divided into 3 main parts:
- One handles the communication with the DPU (DPU inteface)
- One handles the command executions and the "high-level sequencer" (DCU SEQ)
  - Bias generator management (Frequency, amplitude, demodulation signals phase shift…
  - Mode management (picture acquisition Number and frequency, Spectrometer or photometer mode, offset set up…
  - Board Temperature acquisition.
- The last one handles the sequencing of picture acquisition and the offset set up (DCU AQC)

3.9.2 DAQ+IF FPGA Interfaces

TBC

3.9.3 DAQ+IF FPGA FUNCTIONS

3.9.3.1 DCU SEQ: DECODAGE (FUNC-06-2)

This process is divided in three parts:
- Part one does the commands checking.
- Part two sequence the commands execution and the associate response sending.
- Part three decodes the commands from groups dedicated to the load of the internal register.

3.9.3.1.1 Part one: Commands check Diagram
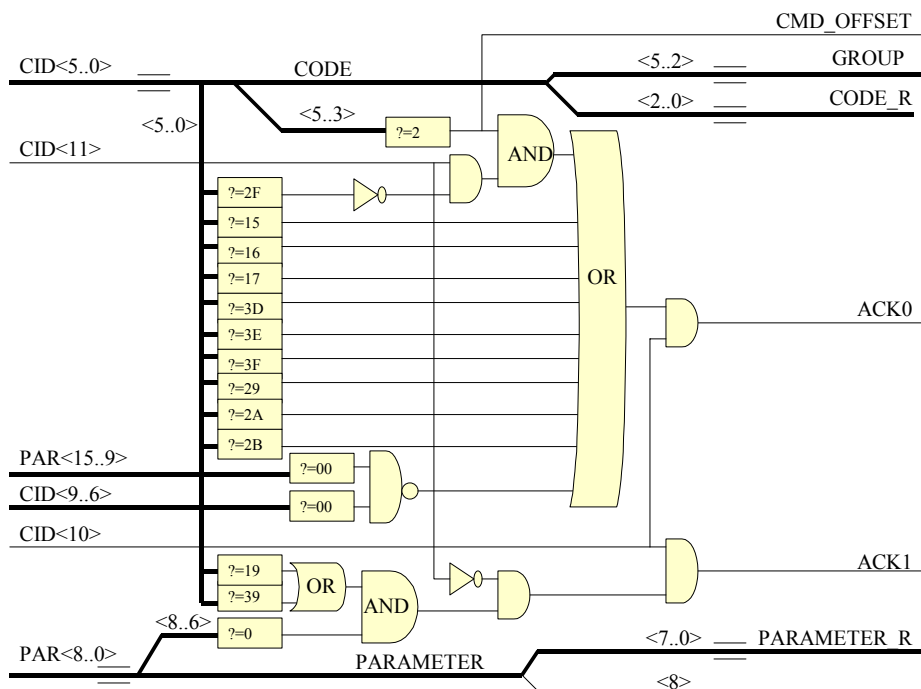
For CID<10>=1, PAR<15..9>="00" and CID<9..6>="0"					
Unknown commands (ACK0=1 and ACK1=0)				Forbidden commands (ACK0=0 and ACK1=1)	
READ/WRITE (CID<11>)		READ(CID<11>=1)		WRITE (CID<11>=0)	
CID<5..0>	PAR<8..0>	CID<5..0>	PAR<8..0>	CID<5..0>	PAR<8..6>
15	xx	20	xx	19	000
16	xx	21	xx	39	000
17	xx	22	xx		
29	xx	23	xx		
2A	xx	24	xx		
2B	xx	25	xx		
3D	xx	26	xx		
3E	xx	27	xx		
3F	xx	28	xx		
		2C	xx		
		2D	xx		
		2E	xx		

3.9.3.1.2 Part two: Commands and response sequence diagram
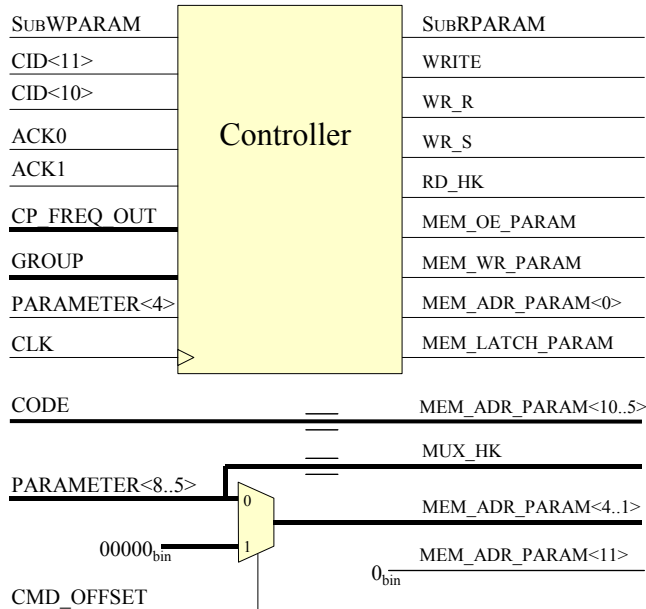
TIMINGS:

If ACK0=0,ACK1=0 and CID<10>=1 Then

For GROUP = 000 or 001 or 010:

TBW

For GROUP = 011 or 111:

TBW

For GROUP = 110:

TBW

For GROUP = 100 or 101:

3.9.3.1.3   Part three: Internal registers load diagram
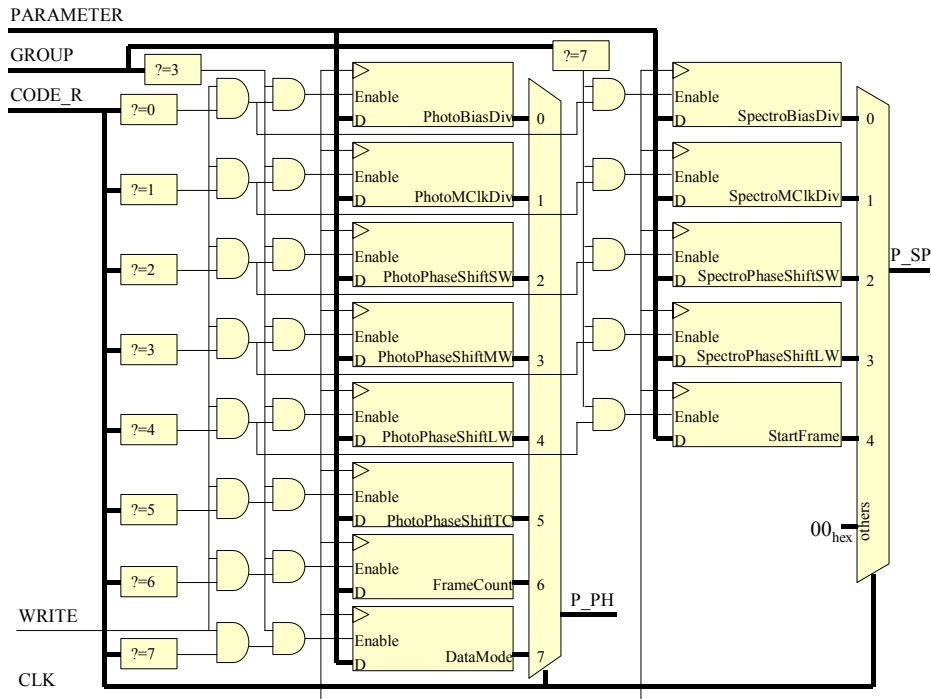
REGISTER RESET POSITION:

PhotoBiasDiv=0F
SpectroBiasDiv=0F
PhotoMClkDiv=1FF
SpectroMClkDiv=1FF

All the others register are set to "00".

TIMING:
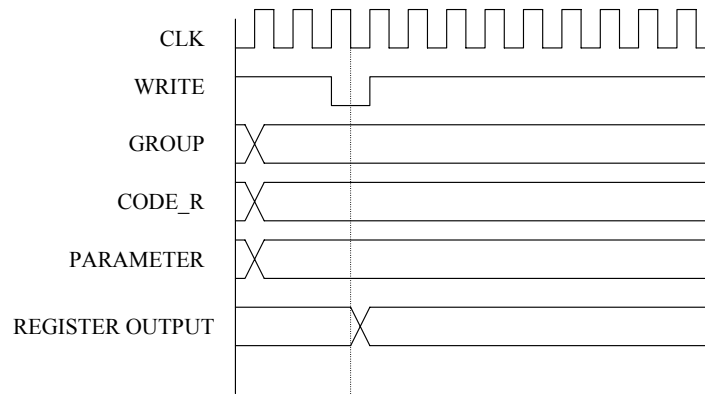
3.9.3.2 DCU SEQ: BIAS (FUNC-01-1, FUNC-04-1 and FUNC-04-2)
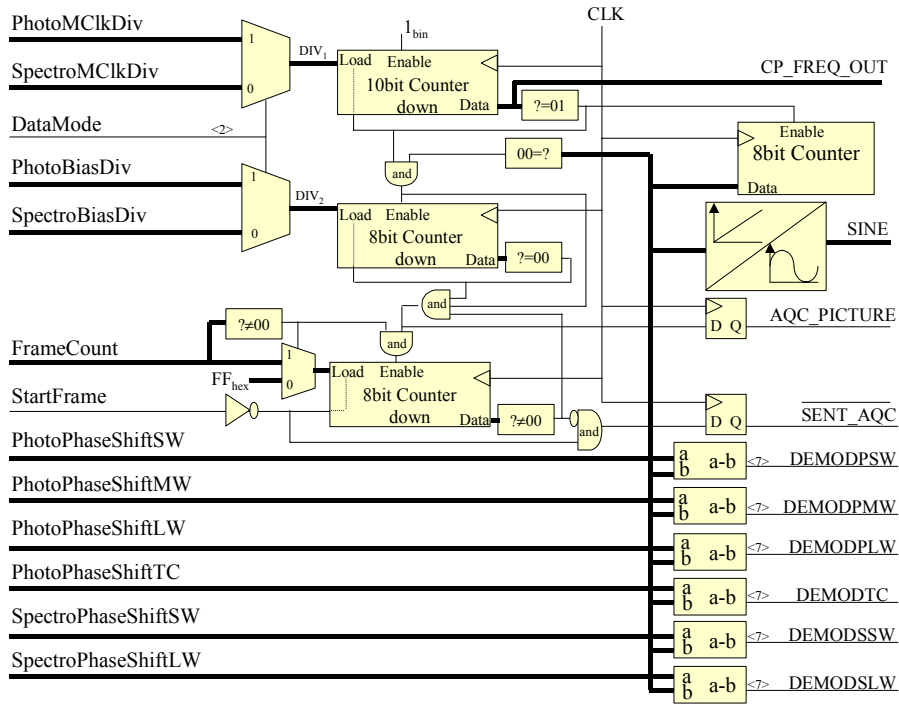
REGISTER and COUNTER RESET POSITION:

CP_FREQ_OUT ="001"
All the others are set to "00"

TIMING:
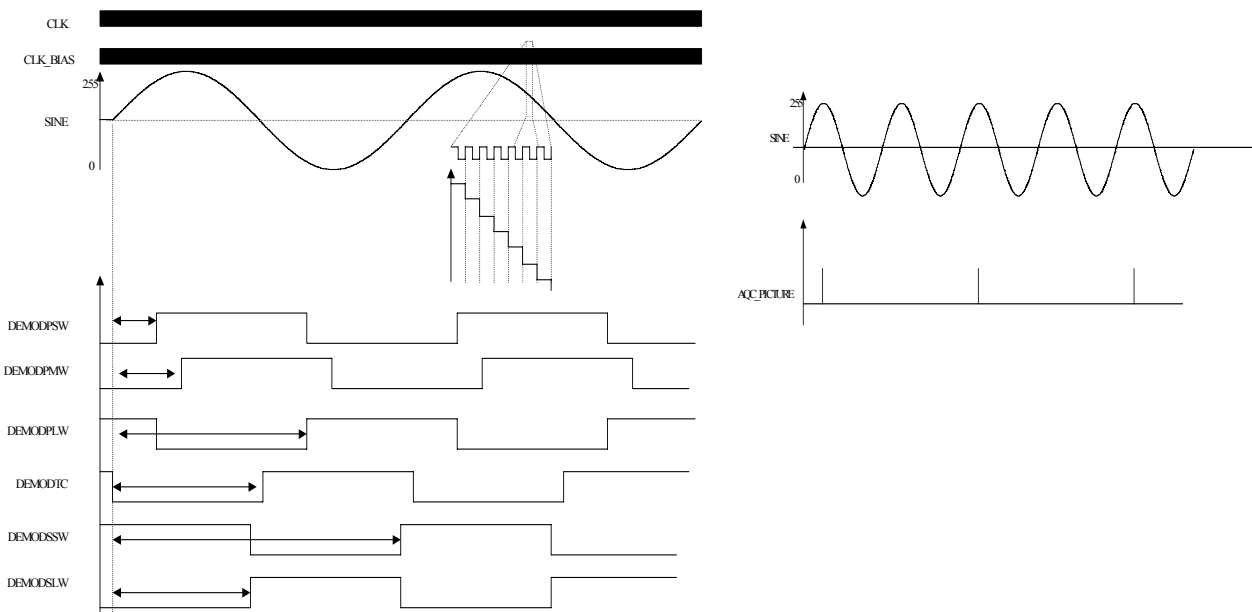
3.9.3.3 DCU SEQ: SERIAL LINK PHOTOMETER
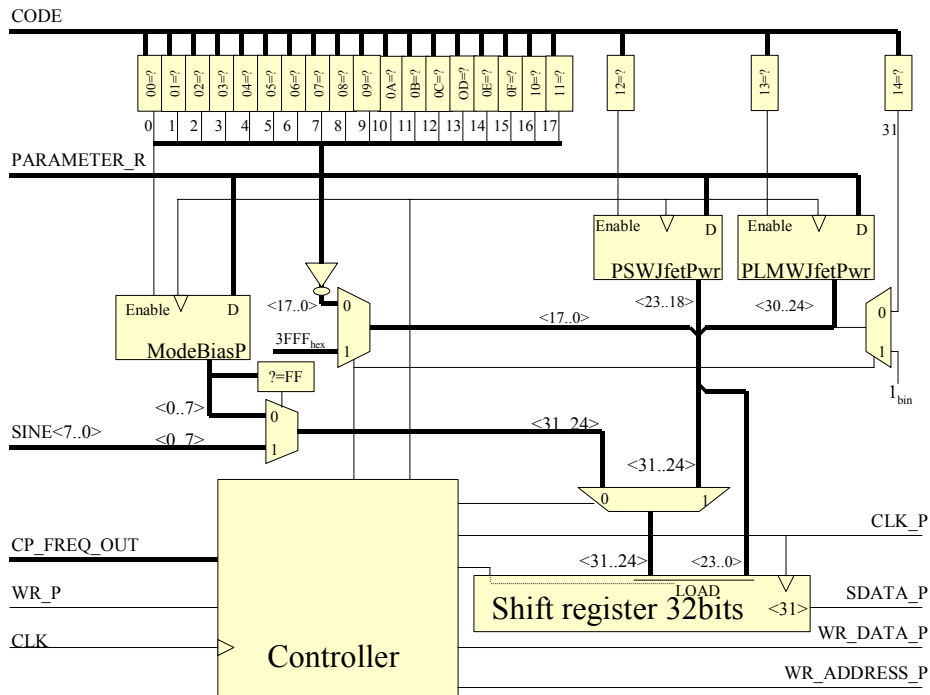
REGISTER RESET POSITION:

TWB

TIMING:

TWB

3.9.3.4 DCU SEQ: SERIAL LINK SPECTROMETER
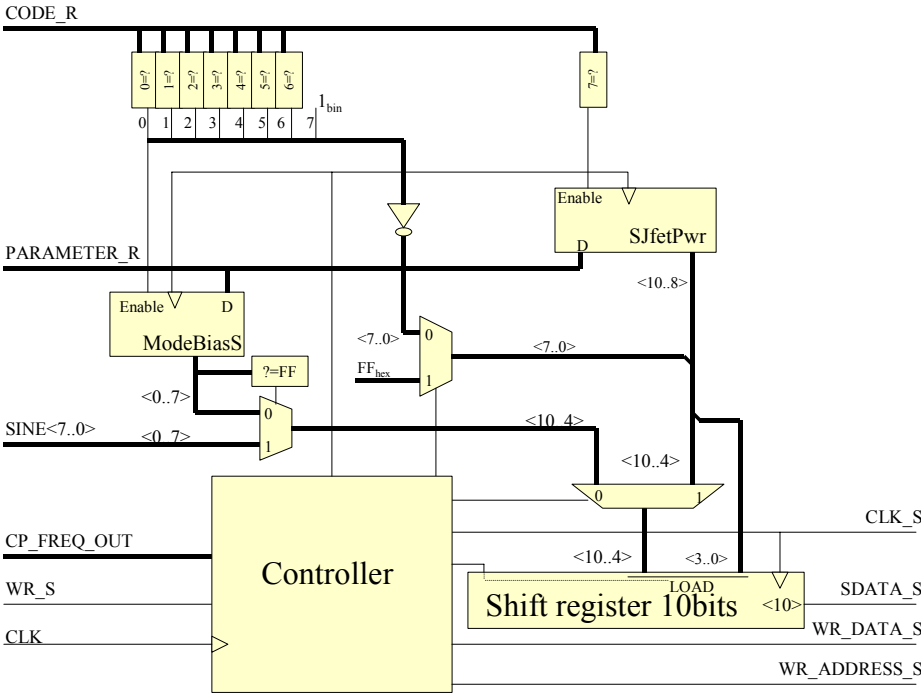
REGISTER RESET POSITION:

TWB

TIMING:

TWB

3.9.3.5   DCU SEQ: HK ACQUISITION and COMMANDS RESPONSE (FUNC-07-2 and FUNC-09-5)
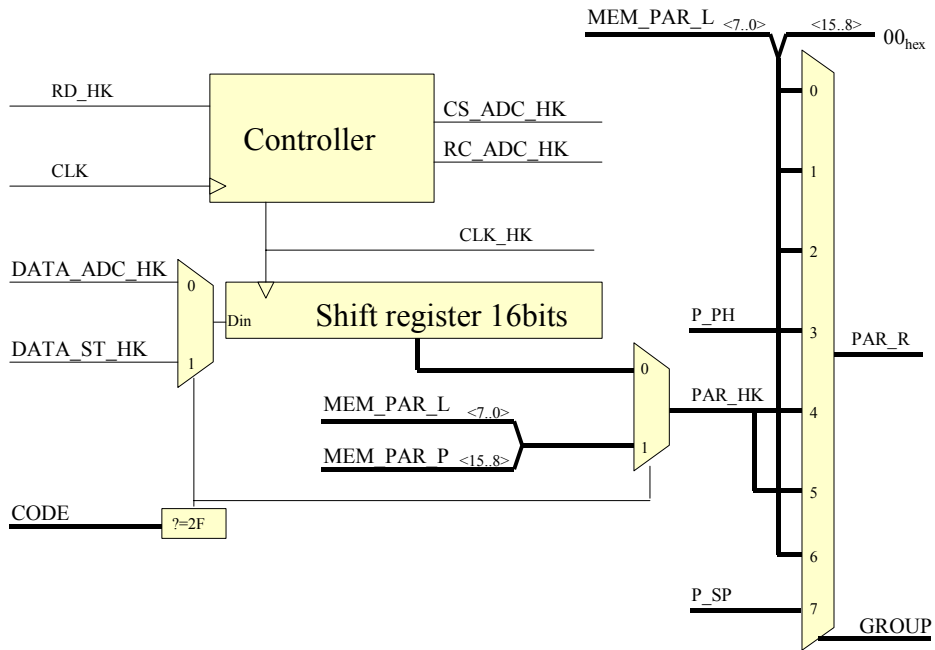
REGISTER RESET POSITION:

TWB

TIMING:

TWB

3.9.3.6   MEMORY INTERFACE
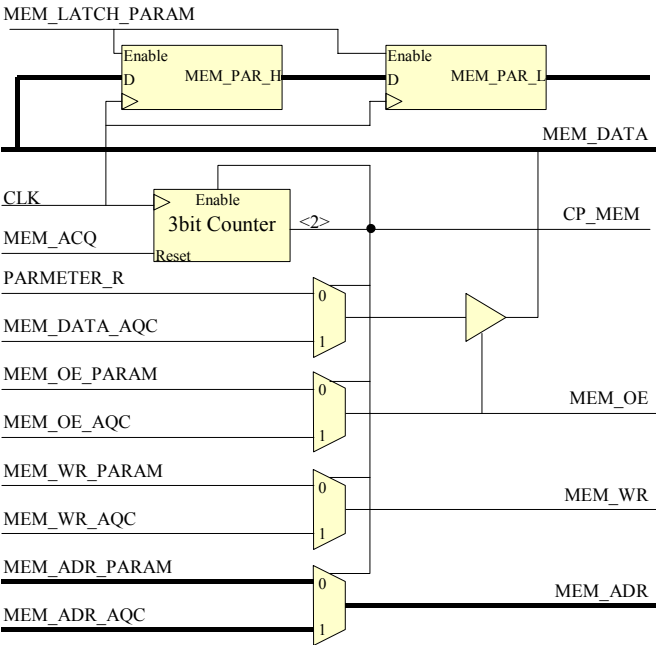
MEMORY MAPING:

TWB

TIMING:

TWB

3.9.3.7 DCU ACQ (FUNC-10-2 and FUNC-04-3)

3.9.3.7.1 Channel Multiplexing

Spectrometer mode:

The following table shows the chronological sequence of the spectrometer's picture acquisition mode:
- The indicated times show when the digitization occurs. These times are given with reference to the beginning of the picture acquisition.
- The six ADCs work in parallel.
- The LIA_S MUX line specifies the LIA_S board's multiplexer positions at the digitization time.
- The DAQ+IF board multiplexer position is 0 during the spectrometer mode.
- The table shows for each ADC which board's channel is associated with each digitization time.

Time in ms		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
ADC1	channel	1	2	3	4	5	6	7	8	9	10	11	12
	Lia_s	1	1	1	1	1	1	1	1	1	1	1	1
ADC2	channel	13	14	15	16	17	18	19	20	21	22	23	24
	Lia_s	1	1	1	1	1	1	1	1	1	1	1	1
ADC3	channel	1	2	3	4	5	6	7	8	9	10	11	12
	Lia_s	2	2	2	2	2	2	2	2	2	2	2	2
ADC4	channel	13	14	15	16	17	18	19	20	21	22	23	24
	Lia_s	2	2	2	2	2	2	2	2	2	2	2	2
ADC5	channel	1	2	3	4	5	6	7	8	9	10	11	12
	Lia_s	3	3	3	3	3	3	3	3	3	3	3	3
ADC6	channel	13	14	15	16	17	18	19	20	21	22	23	24
	Lia_s	3	3	3	3	3	3	3	3	3	3	3	3
LIA_S	MUX	0	1	2	3	4	5	6	7	8	9	10	11
DAQ	MUX	0	0	0	0	0	0	0	0	0	0	0	0

Photometer mode:

The following tables show the chronological sequence of the photometer's picture acquisition mode:
- The times point out digitization times. These times are given with reference to the beginning of the picture acquisition.
- The six ADCs work in parallel.
- The LIA_P MUX specifies multiplexer positions at the digitization time
- The DAQ MUX specifies DAQ+IF board's multiplexer positions at the digitization time.
- The table shows for each ADC which board's channel of which is associated with each digitization time.

Time in ms		0.15	0.25	0.35	0.5	0.6	0.7	0.85	0.95	1.05	1.3	1.4	1.5	1.65	1.75	1.85	2
ADC1	channel	1	17	1	2	18	2	3	19	3	4	20	4	5	21	5	6
	Lia_p	1	1	2	1	1	2	1	1	2	1	1	2	1	1	2	1
ADC2	channel	17	1	17	18	2	18	19	3	19	20	4	20	21	5	21	22
	Lia_p	2	3	3	2	3	3	2	3	3	2	3	3	2	3	3	2
ADC3	channel	1	17	1	2	18	2	3	19	3	4	20	4	5	21	5	6
	Lia_p	4	4	5	4	4	5	4	4	5	4	4	5	4	4	5	4
ADC4	channel	17	1	17	18	2	18	19	3	19	20	4	20	21	5	21	22
	Lia_p	5	6	6	5	6	6	5	6	6	5	6	6	5	6	6	5
ADC5	channel	1	17	1	2	18	2	3	19	3	4	20	4	5	21	5	6
	Lia_p	7	7	8	7	7	8	7	7	8	7	7	8	7	7	8	7
ADC6	channel	17	1	17	18	2	18	19	3	19	20	4	20	21	5	21	22
	Lia_p	8	9	9	8	9	9	8	9	9	8	9	9	8	9	9	8
LIA_P	MUX	0	0	0	1	1	1	2	2	2	3	3	3	4	4	4	5
DAQ	MUX	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1

Time in ms		2.1	2.2	2.35	2.45	2.55	2.7	2.8	2.9	3.05	3.15	3.25	3.4	3.5	3.6	3.75	3.85
ADC1	channel	22	6	7	23	7	8	24	8	9	25	9	10	26	10	11	27
	Lia_p	1	2	1	1	2	1	1	2	1	1	2	1	1	2	1	1
ADC2	channel	6	22	23	7	23	24	8	24	25	9	25	26	10	26	27	11
	Lia_p	3	3	2	3	3	2	3	3	2	3	3	2	3	3	2	3
ADC3	channel	22	6	7	23	7	8	24	8	9	25	9	10	26	10	11	27
	Lia_p	4	5	4	4	5	4	4	5	4	4	5	4	4	5	4	4
ADC4	channel	6	22	23	7	23	24	8	24	25	9	25	26	10	26	27	11
	Lia_p	6	6	5	6	6	5	6	6	5	6	6	5	6	6	5	6
ADC5	channel	22	6	7	23	7	8	24	8	9	25	9	10	26	10	11	27
	Lia_p	7	8	7	7	8	7	7	8	7	7	8	7	7	8	7	7
ADC6	channel	6	22	23	7	23	24	8	24	25	9	25	26	10	26	27	11
	Lia_p	9	9	8	9	9	8	9	9	8	9	9	8	9	9	8	9
LIA_P	MUX	5	5	6	6	6	7	7	7	8	8	8	9	9	9	10	10
DAQ	MUX	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2

Time in ms		3.95	4.1	4.2	4.3	4.45	4.55	4.65	4.8	4.9	5	5.15	5.25	5.35	5.5	5.6	5.7
ADC1	channel	11	12	28	12	13	29	13	14	30	14	15	31	15	16	32	16
	Lia_p	2	1	1	2	1	1	2	1	1	2	1	1	2	1	1	2
ADC2	channel	27	28	12	28	29	13	29	30	14	30	31	15	31	32	16	32
	Lia_p	3	2	3	3	2	3	3	2	3	3	2	3	3	2	3	3
ADC3	channel	11	12	28	12	13	29	13	14	30	14	15	31	15	16	32	16
	Lia_p	5	4	4	5	4	4	5	4	4	5	4	4	5	4	4	5
ADC4	channel	27	28	12	28	29	13	29	30	14	30	31	15	31	32	16	32
	Lia_p	6	5	6	6	5	6	6	5	6	6	5	6	6	5	6	6
ADC5	channel	11	12	28	12	13	29	13	14	30	14	15	31	15	16	32	16
	Lia_p	8	7	7	8	7	7	8	7	7	8	7	7	8	7	7	8
ADC6	channel	27	28	12	28	29	13	29	30	14	30	31	15	31	32	16	32
	Lia_p	9	8	9	9	8	9	9	8	9	9	8	9	9	8	9	9
LIA_P	MUX 3	10	11	11	11	12	12	12	13	13	13	14	14	14	15	15	15
DAQ	MUX	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3

3.9.3.7.2 Channel Acquisition

Spectrometer Mode Digitization Timing Diagram:

Time in µS	200	300	400
Clk_ADC			
CS_ADC			
RC_ADC			
MUX_DAQ		0	
MUX_LIA_S	1	2	3	4
OFFSET_ADC1		OFFSET CH3 LIA_S1	OFFSET CH4 LIA_S1	CH5_LIA_S1
OFFSET_ADC2		OFFSET CH15 LIA_S1	OFFSET CH16 LIA_S1	CH17_LIA_S1
OFFSET_ADC3		OFFSET CH3 LIA_S2	OFFSET CH4 LIA_S2	CH5_LIA_S2
OFFSET_ADC4		OFFSET CH15 LIA_S2	OFFSET CH16 LIA_S2	CH17_LIA_S2
OFFSET_ADC5		OFFSET CH3 LIA_S3	OFFSET CH4 LIA_S3	CH5_LIA_S3
OFFSET_ADC6		OFFSET CH15 LIA_S3	OFFSET CH16 LIA_S3	CH17_LIA_S3
A_OFF_MEM		Adr_offset CH15 LIA_S3	Adr_offset CH16 LIA_S3	
D_OFF_MEM		OFFSET CH15 LIA_S3	OFFSET CH16 LIA_S3	
OE_OFF_MEM			
WR_OFF_MEM			
DATA_ADC1			
DATA_ADC2			
DATA_ADC3			
DATA_ADC4			
DATA_ADC5			
DATA_ADC6			

SEE DETAILED TIMING N°2

SEE DETAILED TIMING N°1

DETAILED TIMING N°1

Time in µS	300	310	314
Clk_ADC			
CS_ADC			
RC_ADC			
MUX_DAQ			
MUX_LIA_S		2	
OFFSET_ADC1		OFFSET CH3 LIA_S1	
OFFSET_ADC2		OFFSET CH15 LIA_S1	
OFFSET_ADC3		OFFSET CH3 LIA_S2	
OFFSET_ADC4		OFFSET CH15 LIA_S2	
OFFSET_ADC5		OFFSET CH3 LIA_S3	
OFFSET_ADC6		OFFSET CH15 LIA_S3	
A_OFF_MEM		Adr_offset CH15 LIA_S3	
D_OFF_MEM		OFFSET CH15 LIA_S3	
OE_OFF_MEM			
WR_OFF_MEM			
DATA_ADC1			
DATA_ADC2			
DATA_ADC3			
DATA_ADC4			
DATA_ADC5			
DATA_ADC6			

DETAILED TIMING N°2

Time in µS	310		314
Clk_ADC			
CS_ADC			
RC_ADC			
MUX_DAQ			
MUX_LIA_S		3	
OFFSET_ADC1		OFFSET CH4 LIA_S1	
OFFSET_ADC2	CH15 LIA_S1	OFFSET CH16 LIA_S1	
OFFSET_ADC3	OFFSET CH3 LIA_S2	OFFSET CH4 LIA_S2	
OFFSET_ADC4	OFFSET CH15 LIA_S2	OFFSET CH16 LIA_S2	
OFFSET_ADC5	OFFSET CH3 LIA_S3	OFFSET CH4 LIA_S3	
OFFSET_ADC6	OFFSET CH15 LIA_S3	OFFSET CH16 LIA_S3	
A_OFF_MEM	AC4 S1 X A C16 S X A C4 S2 X A C16 S2 X A C4 S3	Adr_offset CH16 LIA_S3	
D_OFF_MEM	OC4 S1 X O C16 S1 X O C4 S2 X O C16 S2 X O C4 S3	OFFSET CH16 LIA_S3	
OE_OFF_MEM			
WR_OFF_MEM			
DATA_ADC1	D1		D0
DATA_ADC2	D1		D0
DATA_ADC3	D1		D0
DATA_ADC4	D1		D0
DATA_ADC5	D1		D0
DATA_ADC6	D1		D0

Photometer Mode Digitization Timing Diagram:

Time in µS	350	450	600	
Clk_ADC				
CS_ADC				
RC_ADC				
MUX_DAQ	2	3	1	2
MUX_LIA_P		0	1	
OFFSET_ADC1		OFFSET CH1 LIA_P2	OFFSET CH2 LIA_P1	CH18 LIA_P1
OFFSET_ADC2		OFFSET CH17 LIA_P3	OFFSET CH18 LIA_P2	CH2 LIA_P3
OFFSET_ADC3		OFFSET CH1 LIA_P5	OFFSET CH2 LIA_P4	CH18 LIA_P4
OFFSET_ADC4		OFFSET CH17 LIA_P6	OFFSET CH18 LIA_P5	CH2 LIA_P6
OFFSET_ADC5		OFFSET CH1 LIA_P8	OFFSET CH2 LIA_P7	CH18 LIA_P7
OFFSET_ADC6		OFFSET CH17 LIA_P9	OFFSET CH18 LIA_P8	CH2 LIA_P9
A_OFF_MEM		Adr_offset CH17 LIA_P9	Adr_offset CH18 LIA_P8	
D_OFF_MEM		OFFSET CH17 LIA_P9	OFFSET CH18 LIA_P8	
OE_OFF_MEM				
WR_OFF_MEM				
DATA_ADC1				
DATA_ADC2				
DATA_ADC3				
DATA_ADC4				
DATA_ADC5				
DATA_ADC6				

3.9.3.8   Offset

For each channel, the following algorithm determines its offset:

Offset Calculation for Ch X lia X
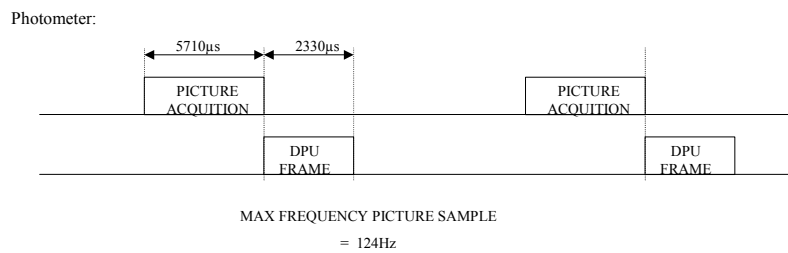
3.9.3.9   Data Transmission

the data are transmitted to the DPU through a serial link at 2Mb/s after a complete PICTURE ACQUISITION is as follow:

Spectrometer:

Photometer:
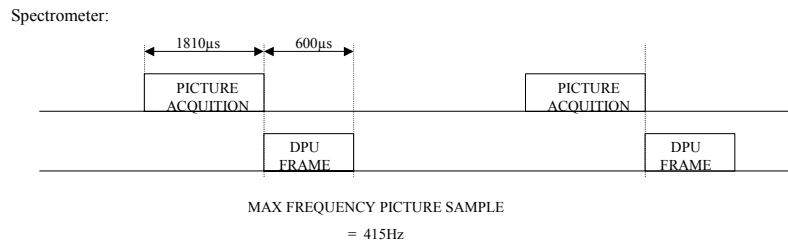
3.9.3.10   DPU INTERFACE (FUNC-06-1, FUNC-07-1, FUNC-10-1 and DCU-FUNC-08)

SEE Generic DPU Interface for spire DRCU Subsystems

3.10 DCU Power Supply

3.10.1 DCU POWER SUPPLY OVERVIEW

3.10.2 LIA SUPPLIES POST-REGULATOR

3.10.2.1 Function

TBC

3.10.2.2 Performances

TBC

4   PHYSICAL CARACTERISTCS

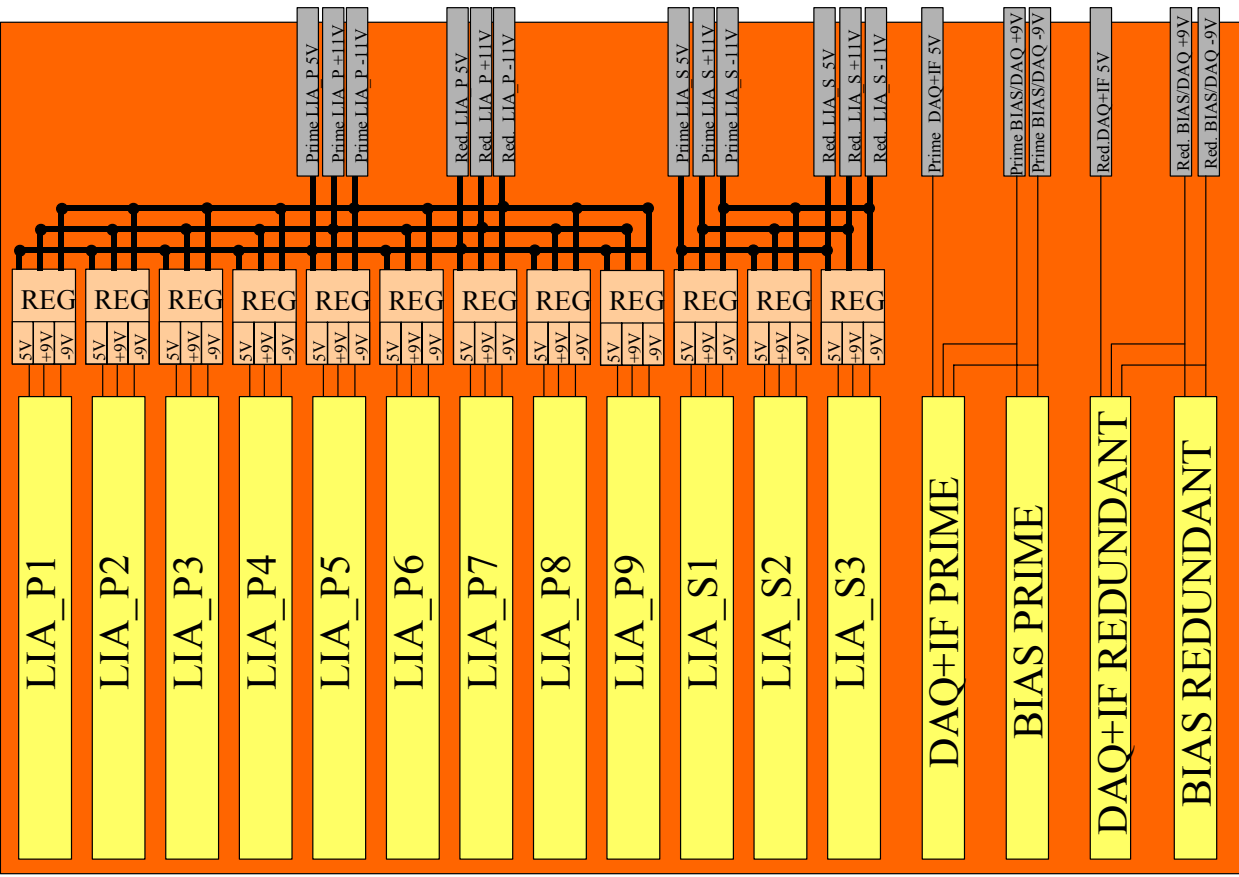## 4.1   PHYSICAL DESCRIPTION

4.1.1   DCU housing

4.1.1.1   QM2 and FM

All of the DCU electronics are housed in one box. A back plane printed circuit board insures the internal DCU connections.
The DCU is composed in its QM2 and FM versions of:
- 9 LIA_P boards
- 3 LIA_S boards
- 2 BIAS boards (PRIME and REDUNDANT)
- 2 DAQ+I/F boards (PRIME and REDUNDANT)

The layout of these boards is organized as shown in Figure 4-1 DCU Front Panel.
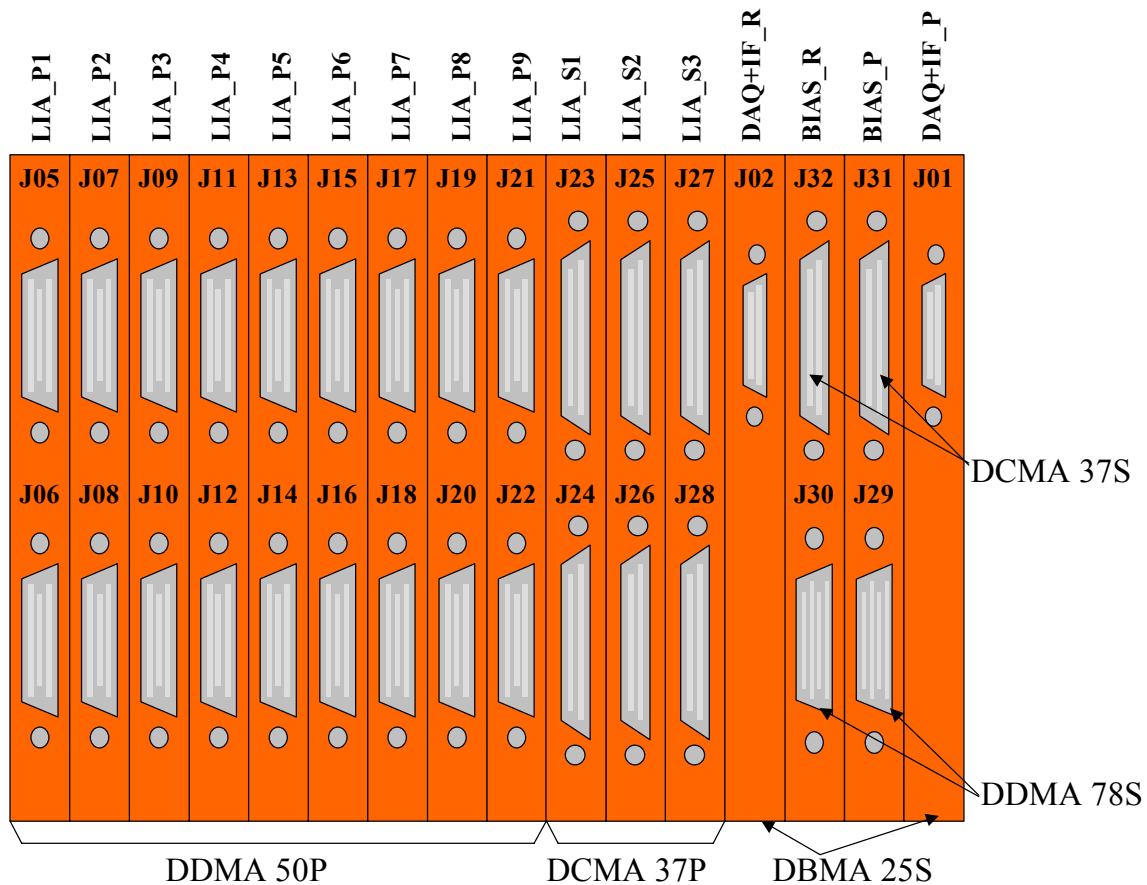

Figure 4-1 DCU Front Panel for QM2 and FM

4.1.2 Back plane

4.1.2.1 QM2 and FM

QM2, and FM all have the same kind of back plane.
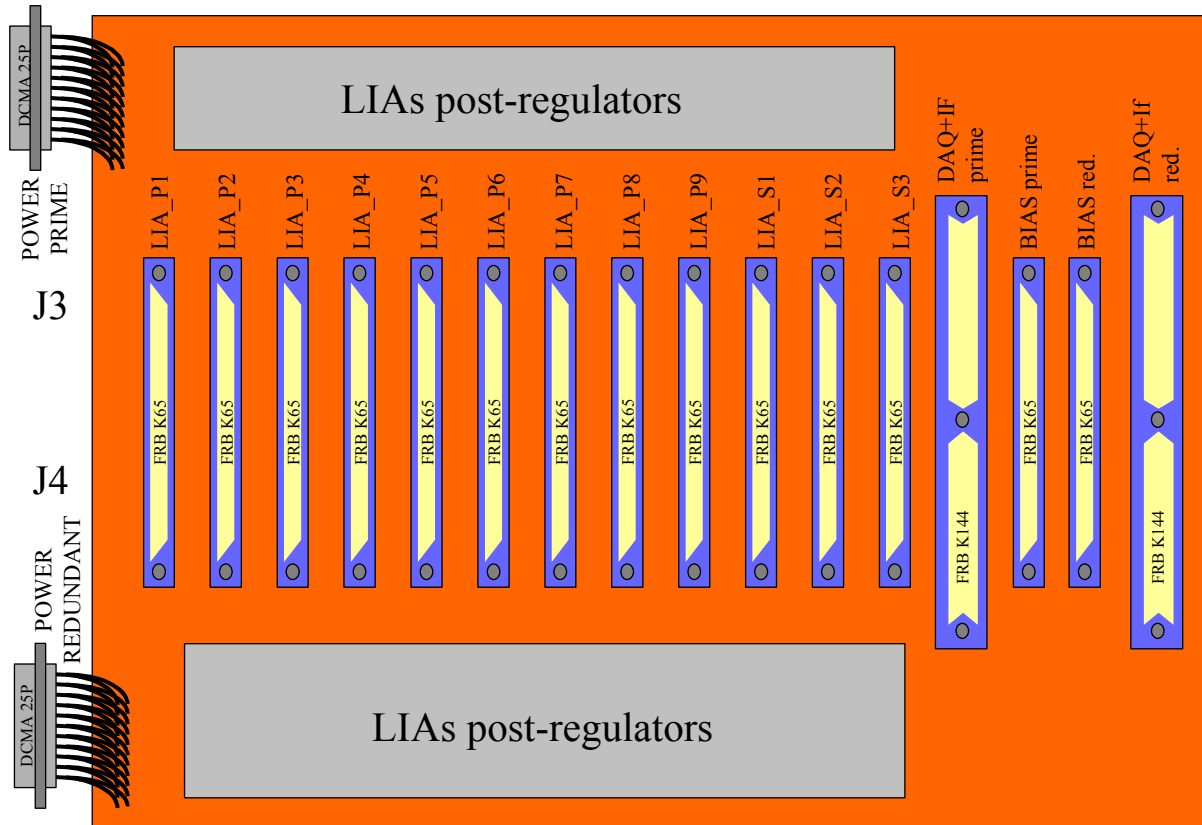The back plane is organized as shown in Figure 4-2 Back Plane.

Figure 4-2 Back Plane

5 TRACEABILITY MATRIX

DRCU Subsystem Specification	FUNCTIONS	Description	Check by		
			Design	Simulation	Measurement
DRCU REQ-15	ALL	Number of channels	ok		
DRCU REQ-16	DCU-FUNC-11	Short circuit protection	ok		
DRCU REQ-17	DCU-FUNC-01	BIAS channels	ok		
DRCU REQ-18	DCU-FUNC-01	BIAS individually adjustable	ok		
DRCU REQ-19	FUNC-04-01	Bias frequency	ok		
DRCU REQ-20	DCU-FUNC-05	DC JFET/heater bias channels	ok		
DRCU REQ-21	FUNC-05-1 and FUNC-05-3	VDD/VSS ON/OFF	ok		
DRCU REQ-22	FUNC-05-5	Heater ON/OFF	ok		
DRCU REQ-23		BIAS redundancy	ok		
DRCU REQ-24		DAQ+IF redundancy	ok		
DRCU REQ-25	FUNC-04-1	Sampling frequency	ok		
DRCU REQ-26	FUNC-04-1	Number of blocks to be transferred	ok		
DRCU REQ-27	FUNC-09-3	Temperature measurement	ok		
DRCU REQ-28	FUNC-09-3	AD590	ok		
DRCU REQ-29	FUNC-09-2 and FUNC-09-1	Temperature range	ok		
DRCU REQ-30	FUNC-09-1, FUNC-09-5 and FUNC-09-4	HK	ok		
DRCU REQ-31		Conducted RF			
DRCU REQ-32-1	DCU-FUNC-02	Input Signal AC	ok		
DRCU REQ-32-2	FUNC-02-2, FUNC-02-3	Input Signal DC	ok		
DRCU REQ-32-3	FUNC-02-2, FUNC-02-3, FUNC-02-5	Output Signal AC	ok		
DRCU REQ-32-4	FUNC-02-2, FUNC-02-3	Common mode ofset			ok
DRCU REQ-32-5	DCU-FUNC-02	Cross talk			x
DRCU REQ-32-6	DCU-FUNC-02	Noise<7nV/rt(Hz)			nok
DRCU REQ-32-7	FUNC-02-1	Input capa< 100pF	ok		
DRCU REQ-32-8	FUNC-02-1	Input impedance>1MΩ	ok		
DRCU REQ-32-9	FUNC-02-5	Bandwidth 0.03 to 5Hz 0.03 to 25Hz	ok		
DRCU REQ-32-10	FUNC-02-1, FUNC-02-2, FUNC-02-3	BPF	ok		
DRCU REQ-32-11	FUNC-02-5	LPF	ok		
DRCU REQ-32-12	FUNC-02-1, FUNC-02-2, FUNC-02-3	Common mode rejection -60dB			ok
DRCU REQ-32-14	FUNC-02-1	Interface	ok		
DRCU REQ-33		NOISE with thermal drift			x

DRCU Subsystem Specification	FUNCTIONS	Description	Check by		
			Design	Simulation	Measurement
DRCU REQ-34	FUNC-01-4	Spec/ph: 0-200mVrms	ok		ok
	FUNC-01-4	TC : 0-500mVrms	ok		
	FUNC-04-1	50 to 300Hz	ok		
	FUNC-01-3	Amplitude resolution	ok		
		Load impedance			
		Interface type			
	FUNC-04-1	Sine wave	ok		
	FUNC-01-4	Noise 20nVrms/rtHz			x
	FUNC-04-2	Phase	ok		
DRCU REQ-35	FUNC-05-1	VSS amplidude	ok		
	FUNC-05-1	VSS resolution	ok		
	FUNC-05-2	VSS noise			ok
	FUNC-05-4	VDDamplitude	ok		
	FUNC-05-4	VDD noise			ok
	FUNC-05-4	Current range			ok
	FUNC-05-4	Voltage stability			x
		Load			
DRCU REQ-36	FUNC-05-2, FUNC-05-4	Overshoot<10%		ok	ok
DRCU REQ-37		Voltage	ok		
		Current	ok		
DRCU REQ-38	DCU-FUNC-03	ADC16bit	ok		
	FUNC-04-3	<6.2ms	ok		
	FUNC-04-3	<1.2ms	ok		
	FUNC-02-6	Offset	ok		
DRCU REQ-39	FUNC-04-3	frames	ok		