
	DCU Design document	 SAp-SPIRE- FP-0063-02 Issue : 0.2 Date : 05/07/02
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HERSCHEL/SPIRE

DETECTOR CONTROL UNIT

DESIGN DOCUMENT

	Function	Name	Date	Visa
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DOCUMENT STATUS and CHANGE RECORD

Date	Issue	Affected pages
08/11/2001	0.1	Creation
05/07/2002	0.2	Removed pin out description of connectors

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1 INTRODUCTION

1.1 PURPOSE

TBW

1.2 SCOPE

TBW

1.3 APPLICABLE DOCUMENTS

AD1	DRCU Interface Control DOCUMENT	Sap-SPIRE-CCA-	0.5
AD2	DRCU Subsystem Specification	Sap-SPIRE-CCA-25-00	0.9
AD3	Detector Subsystem Specification	FIRS-SPI-000103	Working / 7/9/01
AD4	Spire harness definition	SPIRE-RAL-PRJ-000608	0.8
AD5	Spire instrument block diagram	SPIRE-RAL-DWG-000646	3.8

1.4 REFERENCE DOCUMENTS

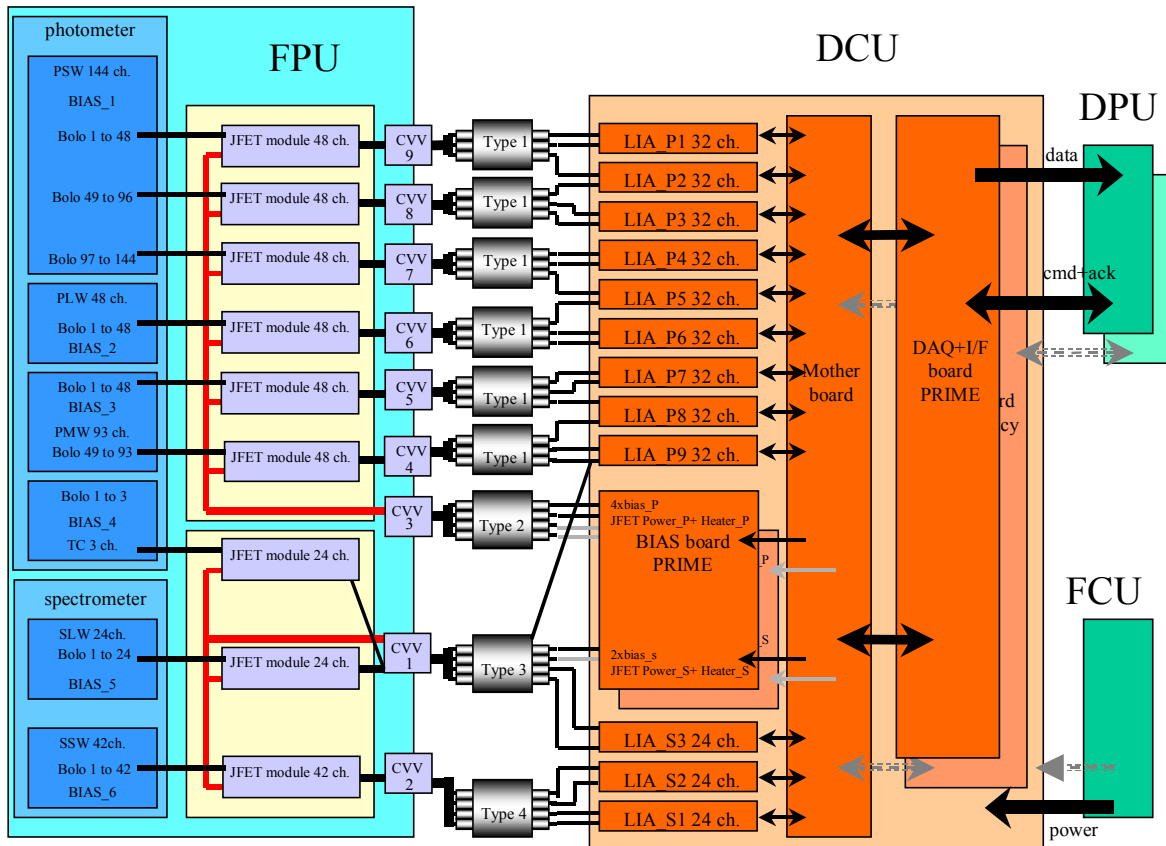
RD1	MAT02 data sheet		REV.C
RD2	OP-400 data sheet		
RD3			
RD4			
AD5			

2 GENERAL DESCRIPTION

2.1 OVERVIEW

The following drawing shows:

- How the DCU is connected to the FPU.
- The different harnesses types and their localization.
- That the DCU power supply is provided by FCU.
- The data exchange link with the DPU PRIME and REDUNDANT.



Picture 2-1: DCU Overview

3 PHYSICAL CHARACTERISTICS

3.1 PHYSICAL DESCRIPTION

3.1.1 DCU housing

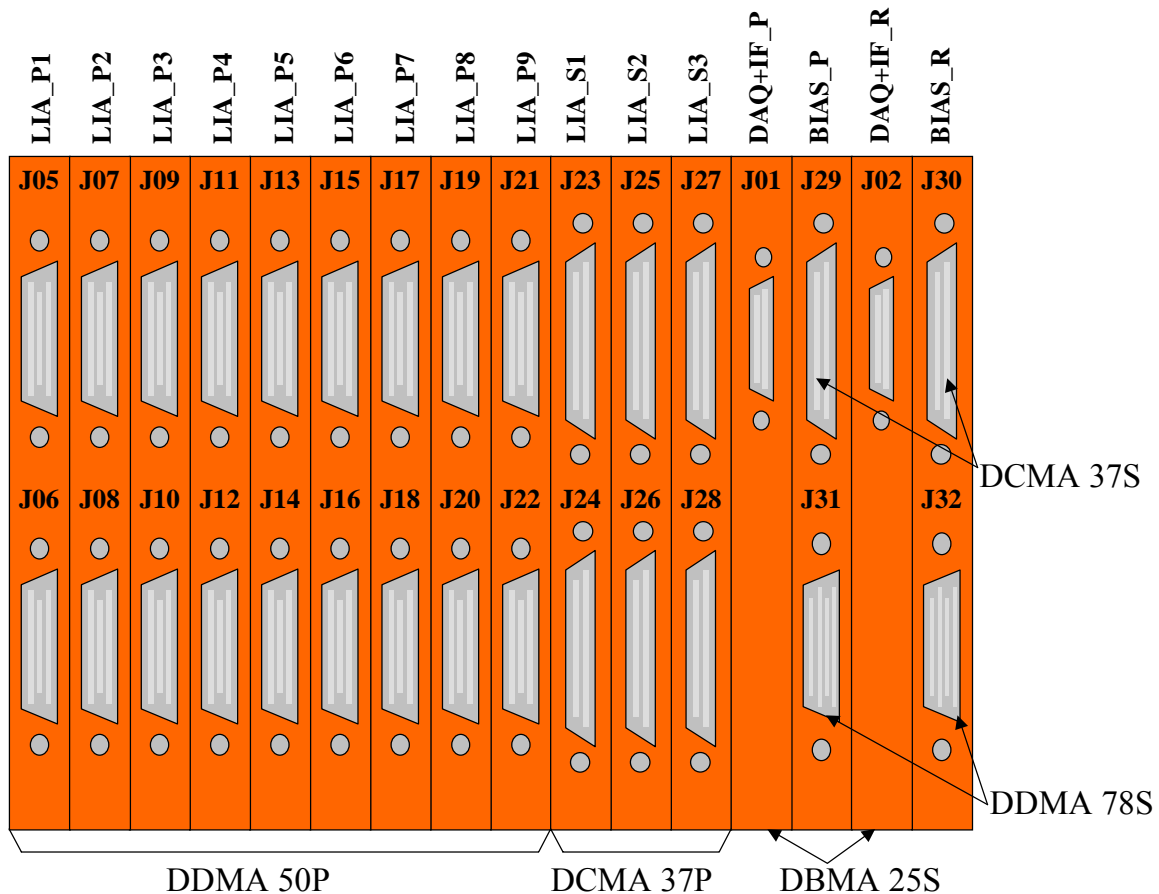
3.1.1.1 QM2 and FM

All of the DCU electronics are housed in one box. A back plane printed circuit board insures the internal DCU connections.

The DCU is composed in its QM2 and FM versions of:

- 9 LIA_P boards
- 3 LIA_S boards
- 2 BIAS boards (PRIME and REDUNDANT)
- 2 DAQ+I/F boards (PRIME and REDUNDANT)

The layout of these boards is organized as shown in Picture 3-1 DCU Front Panel.



Picture 3-1 DCU Front Panel for QM2 and FM

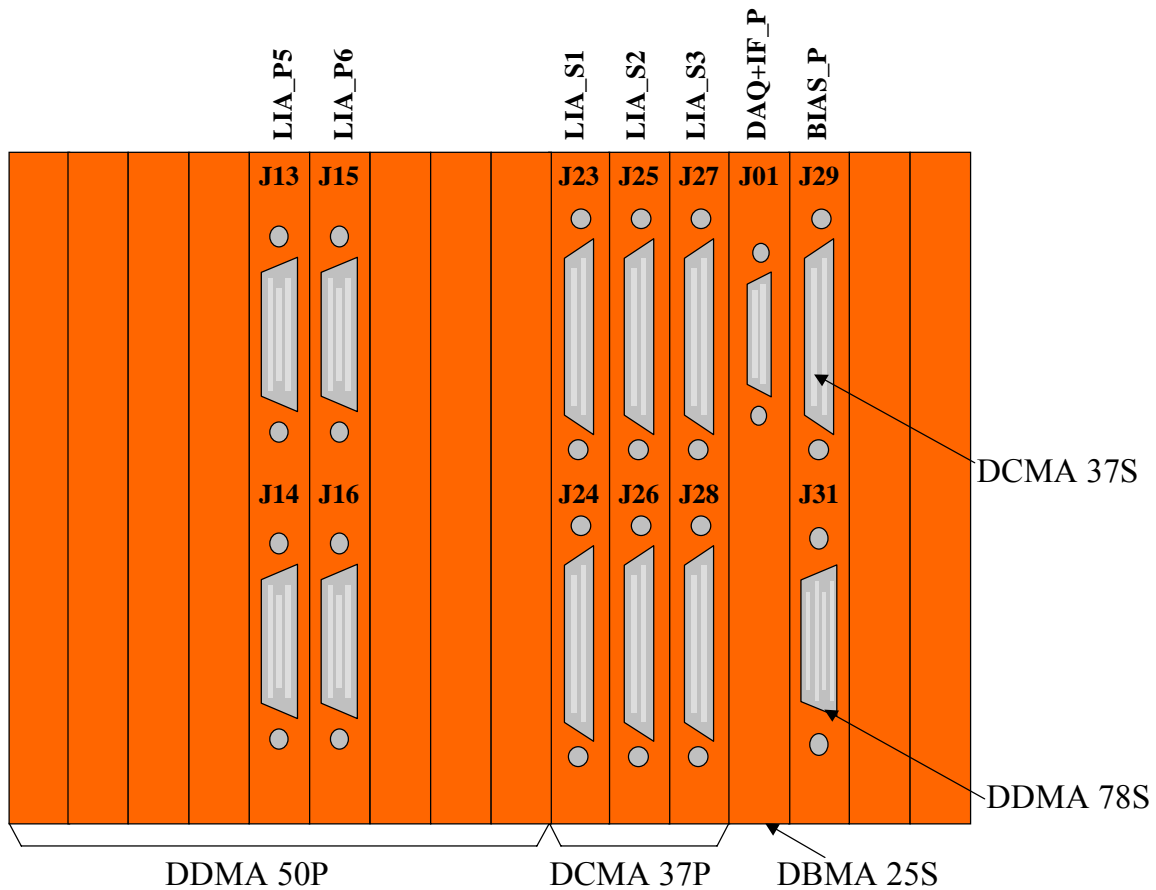
3.1.1.2 QM1

All of the DCU electronics are housed in a prototype box. A QM1 back plane printed circuit board insures the internal DCU connections.

The DCU is composed in its QM1 version of:

- 2 LIA_P boards
- 3 LIA_S boards
- 1 BIAS board (PRIME)
- 1 DAQ+I/F board (PRIME).

The layout of these boards is organized as shown in Picture 3-2 DCU Front Panel for QM1.

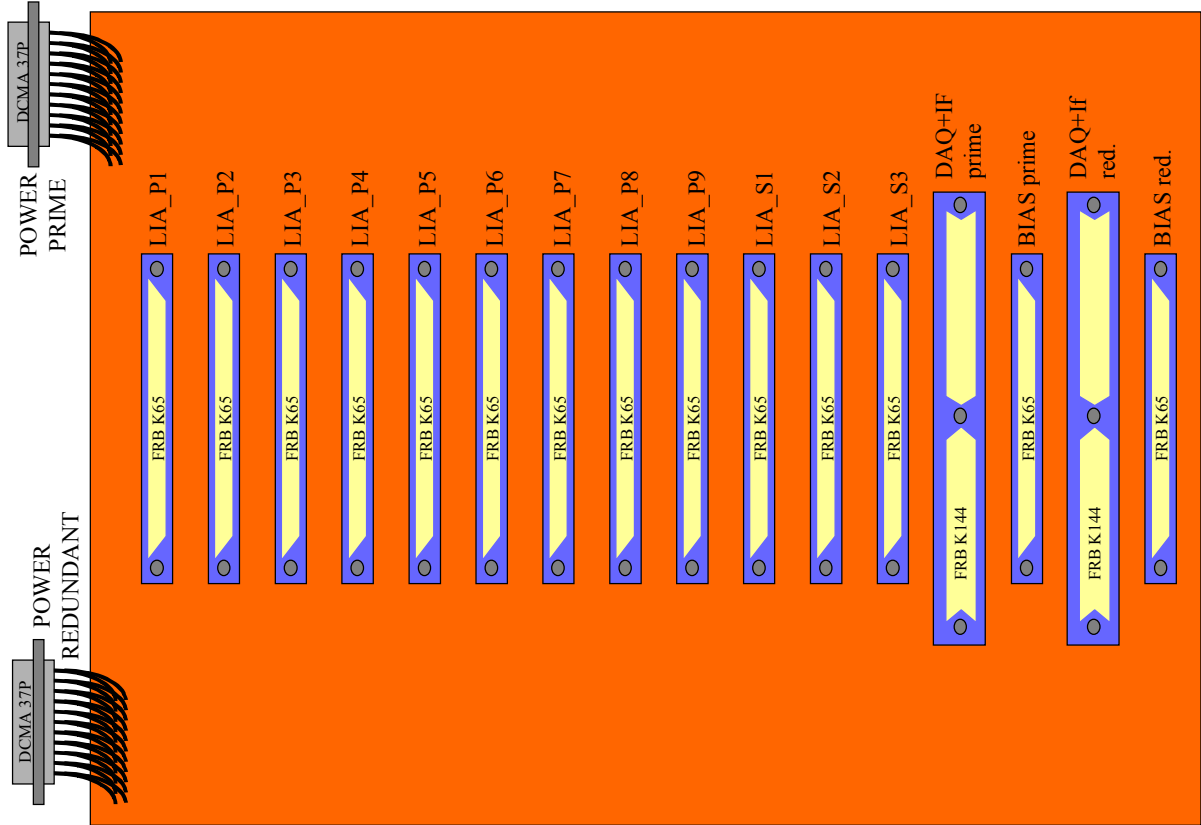


Picture 3-2 DCU Front Panel for QM1

3.1.2 Back plane

3.1.2.1 QM1,QM2 and FM

QM1,QM2, and FM all have the same kind of back plane.
The back plane is organized as shown in Picture 3-3 Back Plane.



Picture 3-3 Back Plane

3.2 NECESSARY POWER SUPPLY ESTIMATION

3.2.1.1 QM2, FM

	9 x LIA_P	3 x LIA_S	BIAS_P	BIAS_S	DAQ+I/F
+9V					
-9V					
5V					

3.2.1.2 QM1

	2 x LIA_P	3x LIA_S	BIAS_P	BIAS_S	DAQ+I/F
+9V					
-9V					
5V					

4 PERFORMANCE

4.1 Functional description

The **Detector Control Unit** supports all of the functions related to the detector's operation. This covers:

- | | |
|---|-------------|
| • The detector bias generation | DCU-FUNC-01 |
| • The bolometer signal processing | DCU-FUNC-02 |
| • The bolometer signal digitization | DCU-FUNC-03 |
| • The timing cycle | DCU-FUNC-04 |
| • The JFET box biasing | DCU-FUNC-05 |
| | |
| • The low-level command decoding | DCU-FUNC-06 |
| • The low-level command acknowledge | DCU-FUNC-07 |
| • The relative timestamp generation | DCU-FUNC-08 |
| • The housekeeping parameter digitisation | DCU-FUNC-09 |
| • The digitized data (bolometers + hk param. + rel. timestamp) transfer | DCU-FUNC-10 |

DCU-FUNC-01 and DCU-FUNC-05 are done by either the PRIME or REDUNDANT BIAS boards.

DCU-FUNC-02 is done by nine LIA_P boards for the photometer and three LIA_S boards for the spectrometer.

DCU-FUNC-03 is done by six ADC on either the PRIME or the REDUNDANT DAQ+IF board.

DCU-FUNC-04, DCU-FUNC-06, DCU-FUNC-07, DCU-FUNC-08 and DCU-FUNC-10 are done by an FPGA on either the PRIME or REDUNDANT DAQ+IF board.

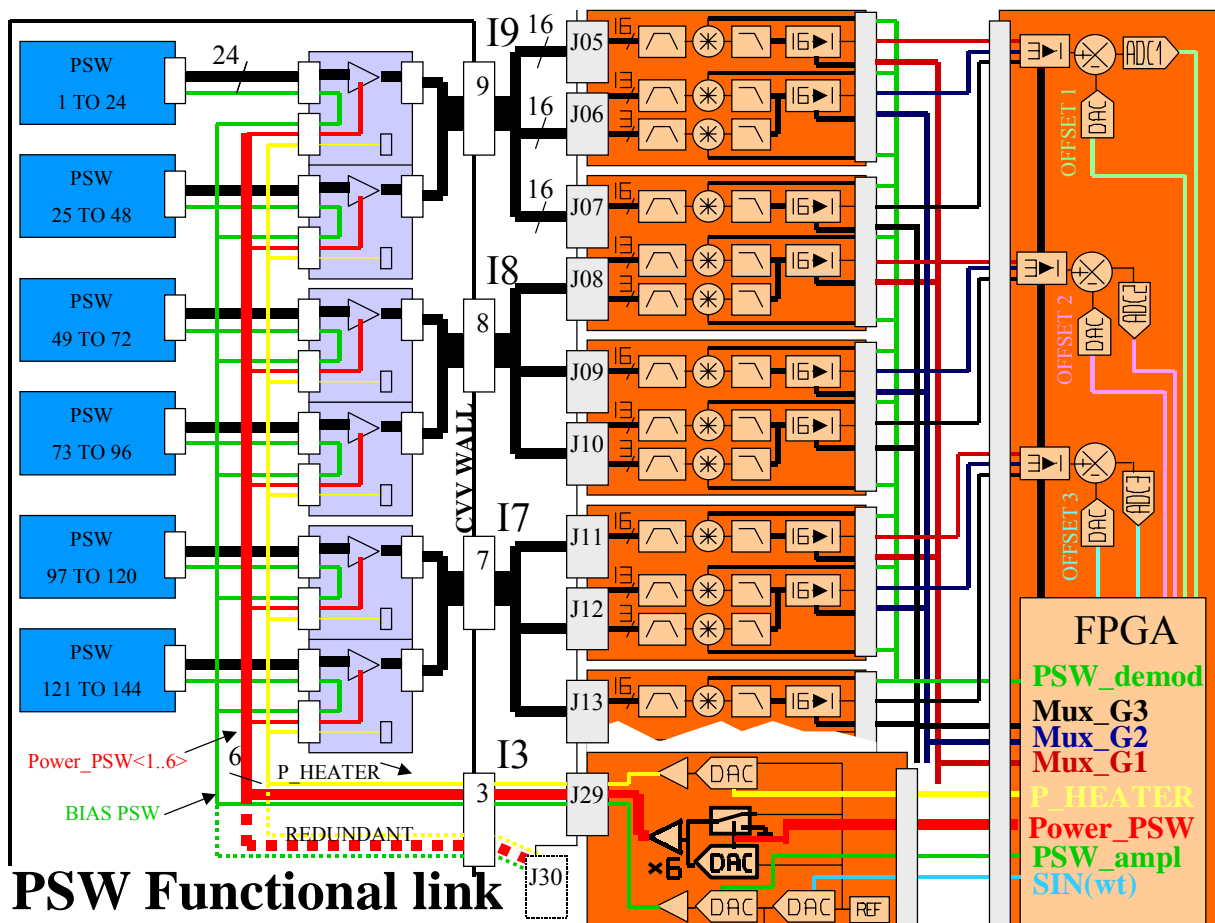
DCU-FUNC-09 is done by an ADC on either the PRIME or REDUNDANT DAQ+IF board.

4.1.1 LIAs PHOTOMETER

4.1.1.1 QM2, FM

Nine LIA_P boards make up the LIA photometer section.

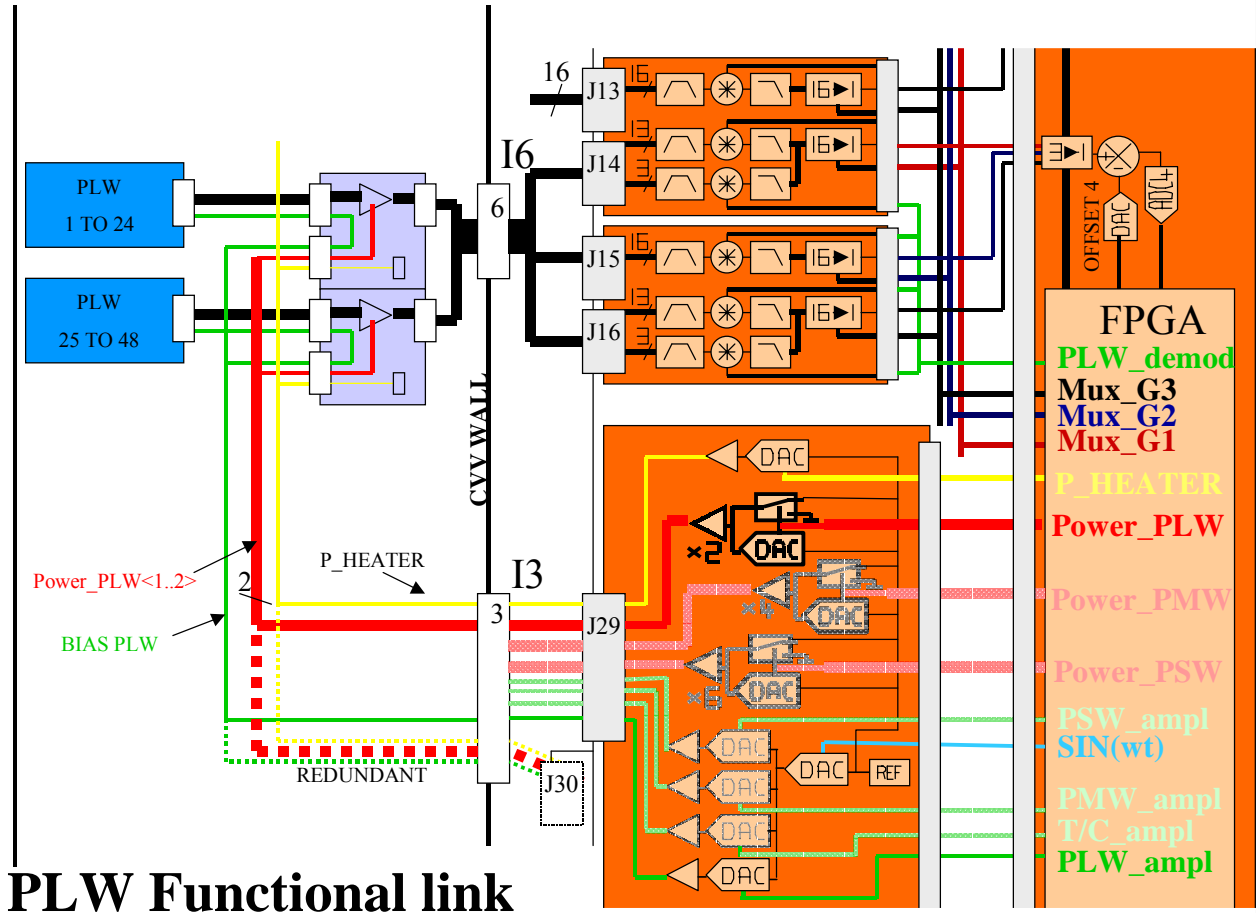
1. LIA_P1 to LIA_P4 and the first 16 channels of LIA_P5 will receive and process the signals from 144 “PSW bolometers.”



Picture 4-1 PSW Photometer Functional Links

- The 144 PSW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (PSW_demod.)
- All of the 144 channels are sent to the DAQ+IF board through 9 differential links that are digitized by 3 ADCs.

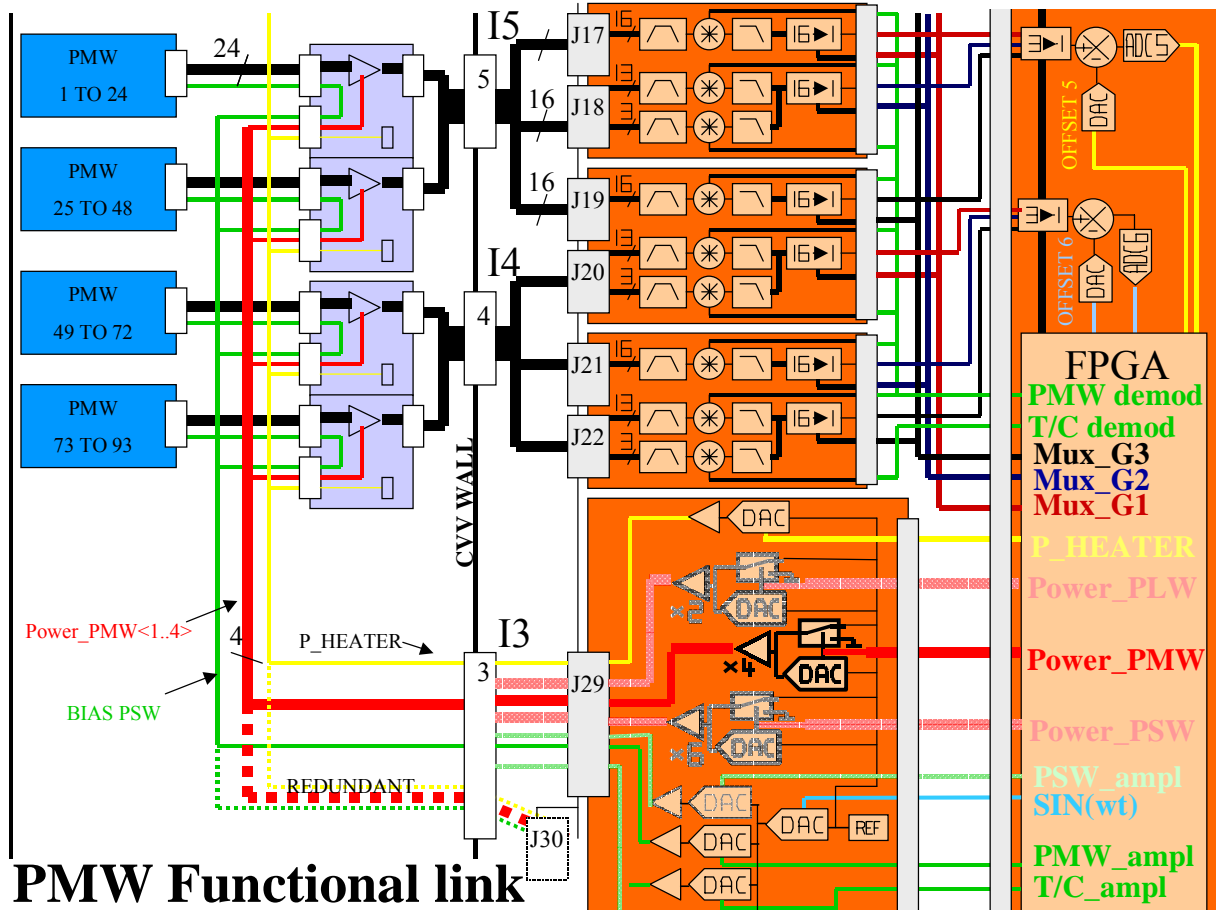
- The other 16 channels from LIA_P5 and LIA_P6 receive and process signals from 48 “PLW bolometers.”



Picture 4-2 PLW Photometer Functional Links

- The 48 PLW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (PLW_demod.)
- All of the 48 channels are sent to the DAQ+IF board through 3 differential links that are digitized by one ADC.

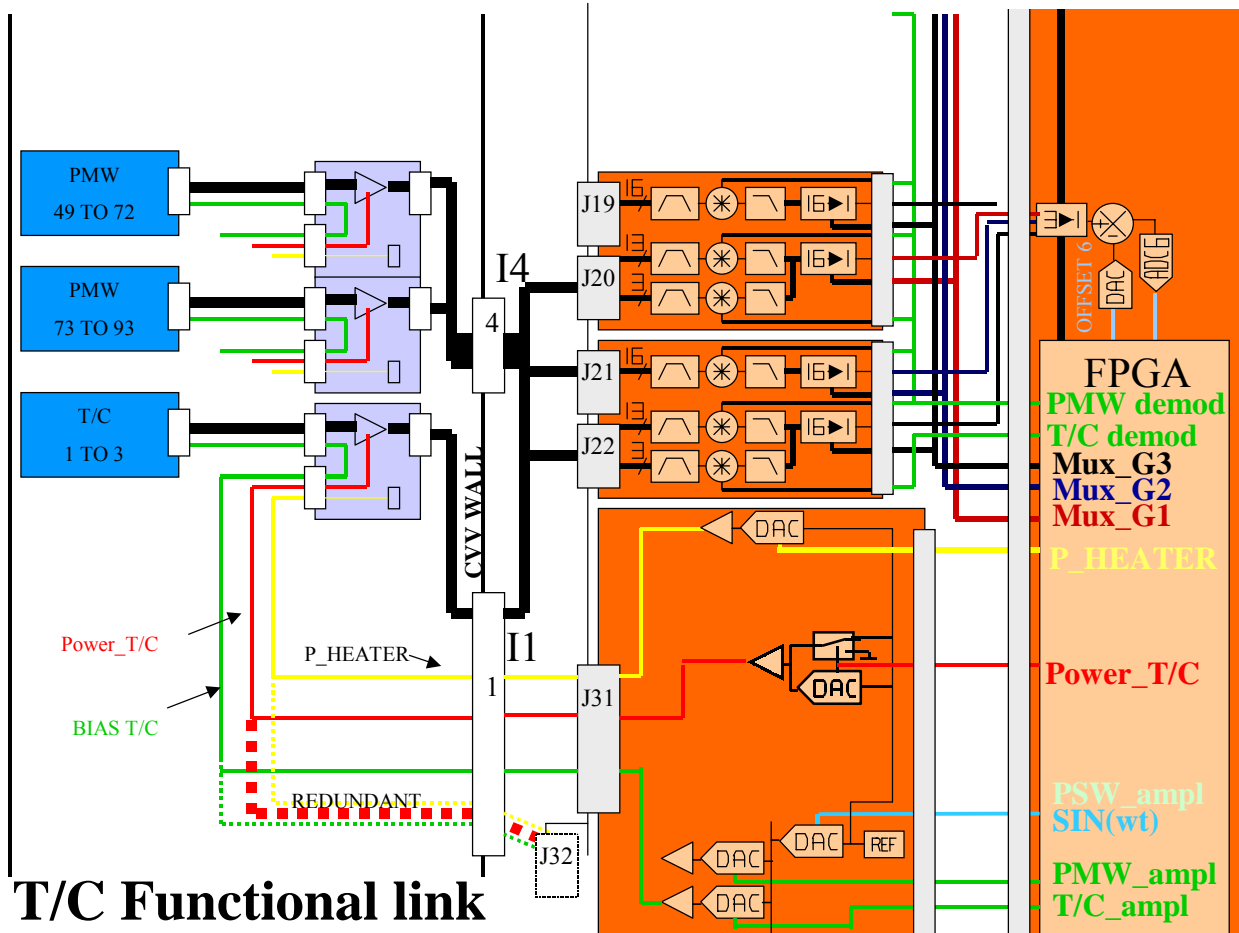
3. LIA_P7 to LIA_P8 and the first 29 channels of the LIA_P9 receive and process the signals from 93 “PMW bolometers.”



Picture 4-3 PMW Photometer Functional Links

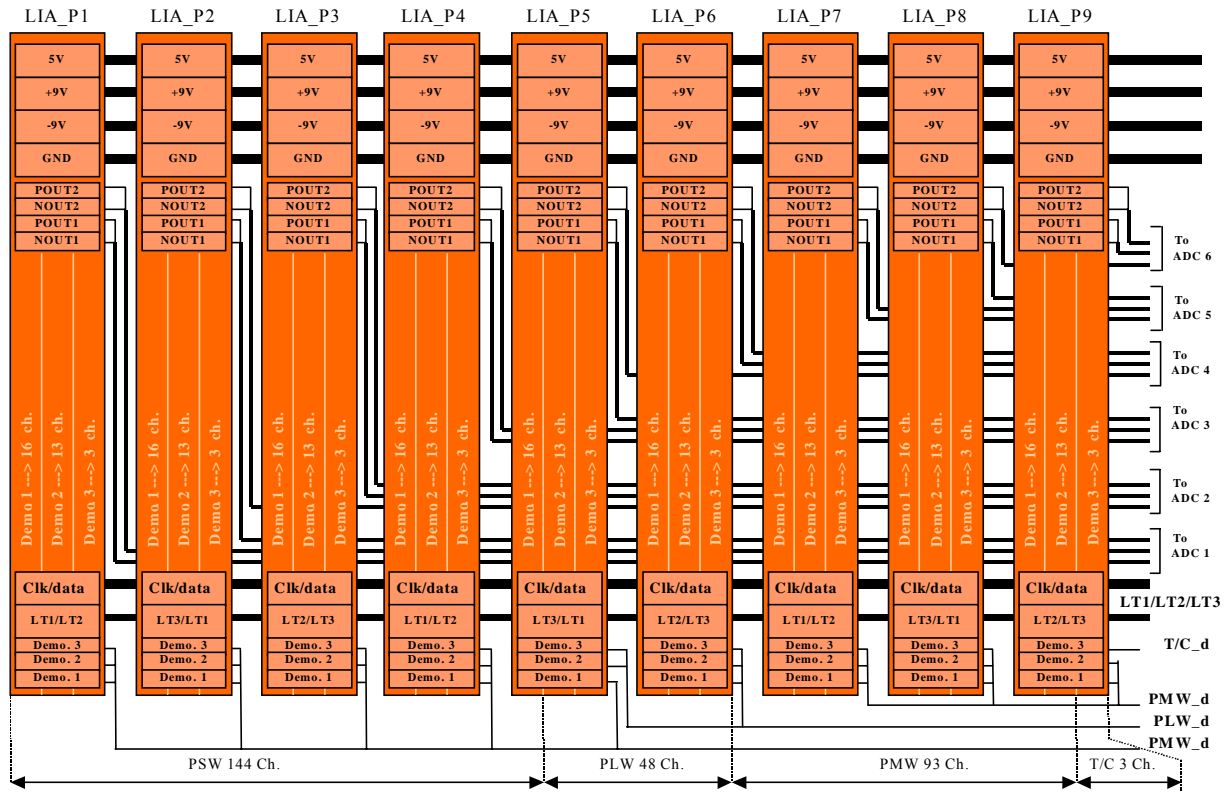
- The 93 PMW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (PMW_demod.)
- All of the 93 channels are sent to the DAQ+IF board through 6 differential links that are digitized by 2 ADCs.

4. The last 3 channels of the LIA_P9 receive and process signals from 3 “T/C bolometers.”



Picture 4-4 T/C Photometer Functional Links

- The 3 T/C channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (T/C_demod.)
- All 3 channels are sent to the DAQ+IF board through one differential link that is digitized by one ADC.
- Note: The T/C signals go through connectors J31 and J32 as well as harness I1 which are mainly used to carry the spectrometer signals. However, these T/C signals always refer to the photometer’s ground.



Picture 4-5 LIA Photometer Section

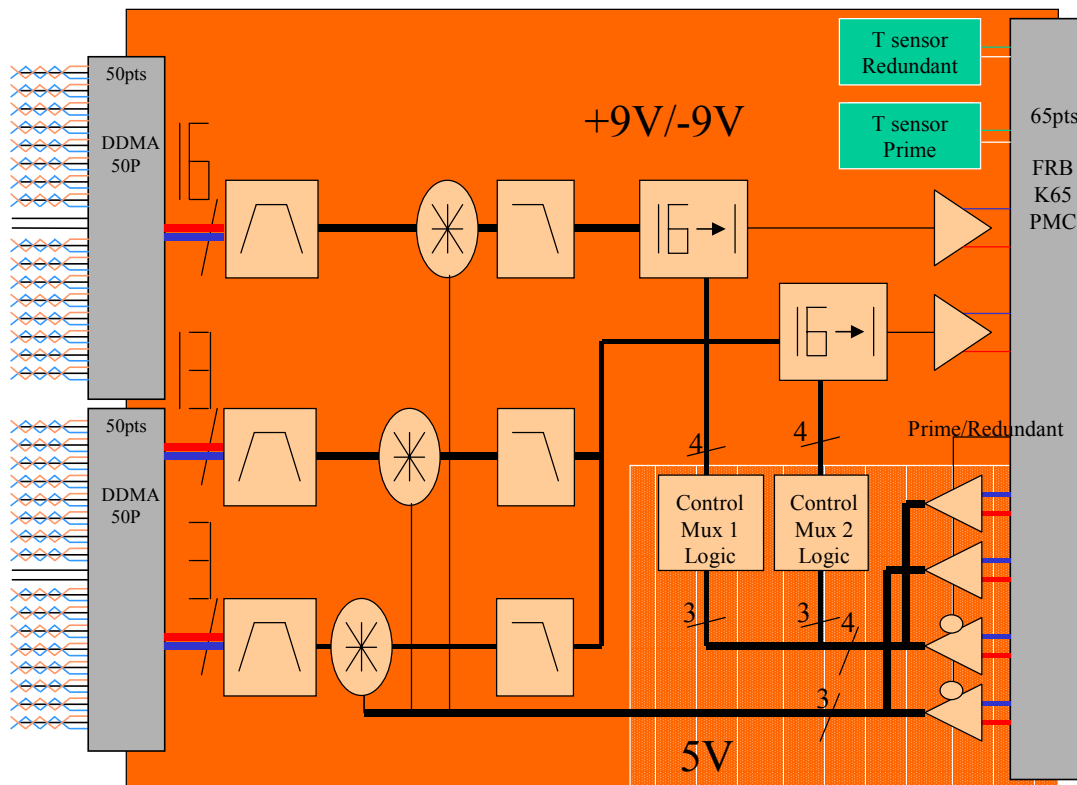
Each group receive its own respective demodulation signal: PSW_demod, PMW_demod, PLW_demod and T/C_demod. Each of these signals can have a different phase shift.

The LIA photometer is supplied only when the SPIRE instrument is running in the photometer mode.

Each LIA photometer board receive its own group of 3 supply lines (-9V, +9V and 5V) which be automatically shutdown if a error occurs on one of these three lines.

4.1.2 LIA PHOTOMETER BOARD

4.1.2.1 LIA Photometer Board Overview



Picture 4-6 LIA Photometer Board Overview

- **The LIA_P board has thirty-two channels that are divided into three groups:**



- A group of sixteen channels which go to the first multiplexer.
- A group of thirteen channels which go to the second multiplexer.
- A group of three channels which also go to the second multiplexer.

- **Each of the three groups can receive its own demodulation signals.**

- **The receivers that relay the multiplexer command signals as well as the demodulation signals are redundant:**

- A PRIME/REDUNDANT signal from the PSU activates the PRIME receivers when the PRIME power supply turns on and the REDUNDANT receivers when the REDUNDANT power supply turns on.
- The LIA PRIME receivers are connected to the PRIME DAQ+IF board.
- The LIA REDUNDANT receivers are connected to the REDUNDANT DAQ+IF board.

- **Each multiplexer's command is independent.**

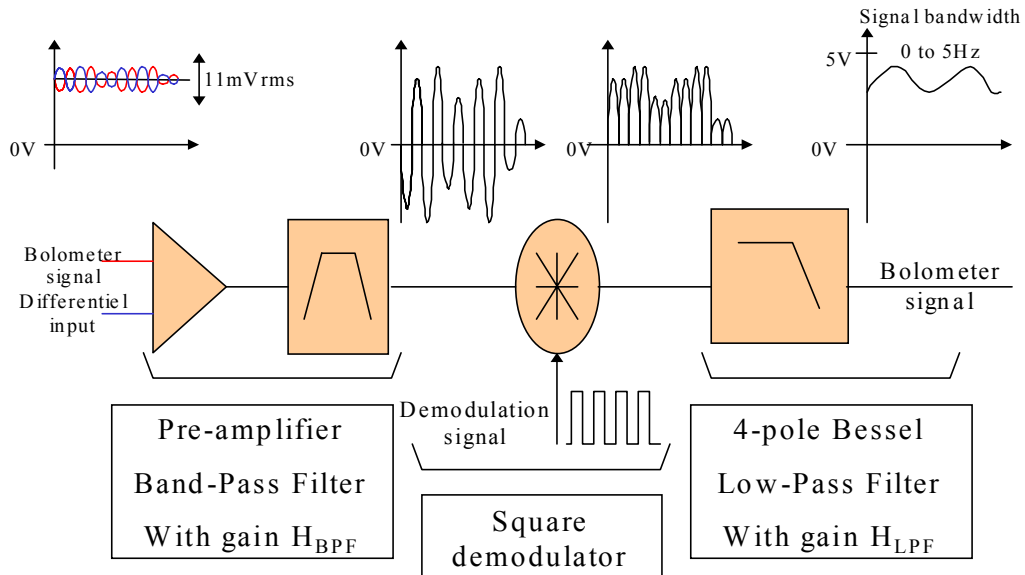
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4.1.2.2 LIA Photometer Board Interface

Name	Description	Type	Level	In/Out	Frequency
IN+ xx	Bolometer Differential Signal	Analogic	11mVrms (AC) + 1.5V (DC)	IN	50-300Hz
IN- xx					
POUT x	sixteen LIA_P channels multiplexed in one differential signal	Analogic	0 to 5V	OUT	0-5Hz at mux freq. ~2.5kHz
NOUT x					
PCLK-	Serial Clock for the LIA_P /DAQ+IF PRIME Interface, (differential signal)	Numeric	-0,3Vto 0,3V	IN	5MHz max
PCLK+					
PDATA-	Serial Data for the LIA_P /DAQ+IF PRIME interface, (differential signal)	Numeric	-0,3Vto 0,3V	IN	5MHz max
PDATA+					
PLTx-	Data LATCH for the LIA_P /DAQ+IF PRIME Interface, (differential signal)	Numeric	-0,3Vto 0,3V	IN	5MHz max
PLTx+					
PDEMOD1-	Demodulation Differential Signal (PRIME) for Channels One to Sixteen	Numeric	-0,3Vto 0,3V	IN	50-300Hz
PDEMOD1+					
PDEMOD2-	Demodulation Differential Signal (PRIME) for Channels Seventeen to Twenty-nine	Numeric	-0,3Vto 0,3V	IN	50-300Hz
PDEMOD2+					
PDEMOD3-	Demodulation Differential Signal for Channels One to Sixteen	Numeric	-0,3Vto 0,3V	IN	50-300Hz
PDEMOD3+					
RCLK-	Serial Clock for the LIA_P /DAQ+IF REDUNDANT Interface	Numeric	-0,3Vto 0,3V	IN	5MHz max
RCLK+					
RDATA-	Serial Data for the LIA_P /DAQ+IF REDUNDANT Interface	Numeric	-0,3Vto 0,3V	IN	5MHz max
RDATA+					
RLTx-	Data LATCH for the LIA_P /DAQ+IF REDUNDANT Interface	Numeric	-0,3Vto 0,3V	IN	5MHz max
RLTx+					
RDEMOD1-	Demodulation Differential signal (REDUNDANT) for Channels One to Sixteen	Numeric	-0,3Vto 0,3V	IN	50-300Hz
RDEMOD1+					
RDEMOD2-	Demodulation Differential Signal (REDUNDANT) for Channels Seventeen to Twenty-nine	Numeric	-0,3Vto 0,3V	IN	50-300Hz
RDEMOD2+					
RDEMOD3-	Demodulation Differential Signal for (REDUNDANT) channels One to Sixteen	Numeric	-0,3Vto 0,3V	IN	50-300Hz
RDEMOD3+					
PT_P9V	Sensor PRIME Bias	Analogic	9V	IN	DC
PT	Output Sensor PRIME	Analogic	2 to 4V	OUT	-
RT_P9V	Sensor REDUNDANT Bias	Analogic	9V	IN	DC
RT	Output Sensor REDUNDANT	Analogic	2 to 4V	OUT	-
P9V	9V Power Supply	Power	9V	IN	DC
N9V	-9V Power Supply	Power	-9V	IN	DC
P9V_P	PRIME/REDUNDANT Signal	Analogic	0 to 9V	IN	DC
P5V	5V Power Supply	Power	5V	IN	DC
GND	Grounding	Power	0V	-	DC

4.1.3 LIA PHOTOMETER CHANNELS

4.1.3.1 LIA Photometer Channel Overview



Picture 4-7 LIA Photometer Board Overview

The input differential signal that comes from a bolometer is amplified and its DC component is eliminated by the pre-amplifier BPF. Then, it is demodulated by a squared signal. Afterwards, it is filtered by a four-pole Bessel LPF.

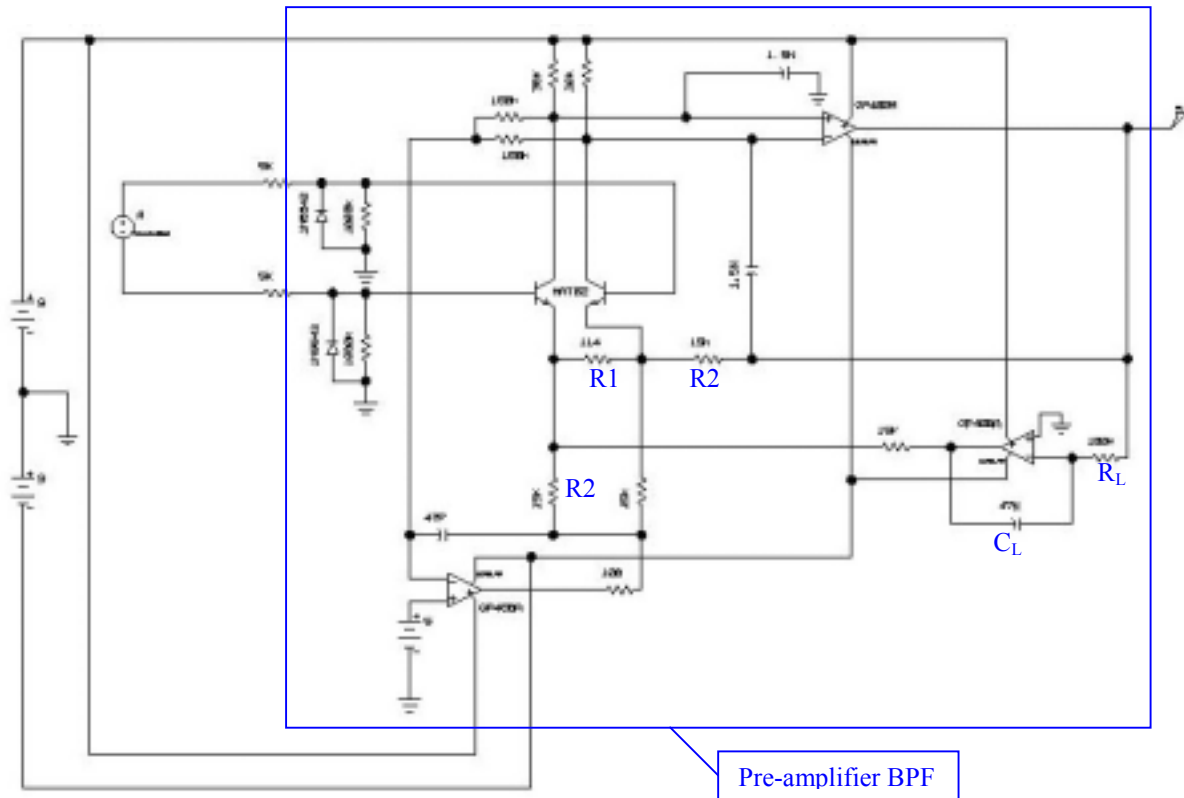
The four-pole Bessel low pass filter has a structural gain of $H_{LPF} = 1.9$

The square demodulation signal will introduce a gain of $2/\pi$

Note: To be sure that a photometer channel won't be saturated with a 11mVrms input, the output signal cannot be more than 5V.

This is why the band pass filter gain H_{BPF} cannot be larger than $\frac{5V}{11mV \cdot \frac{2\sqrt{2}}{\pi} \cdot 1.9} = 264$

4.1.3.2 LIA Photometer Channel Pre-amplifier BPF



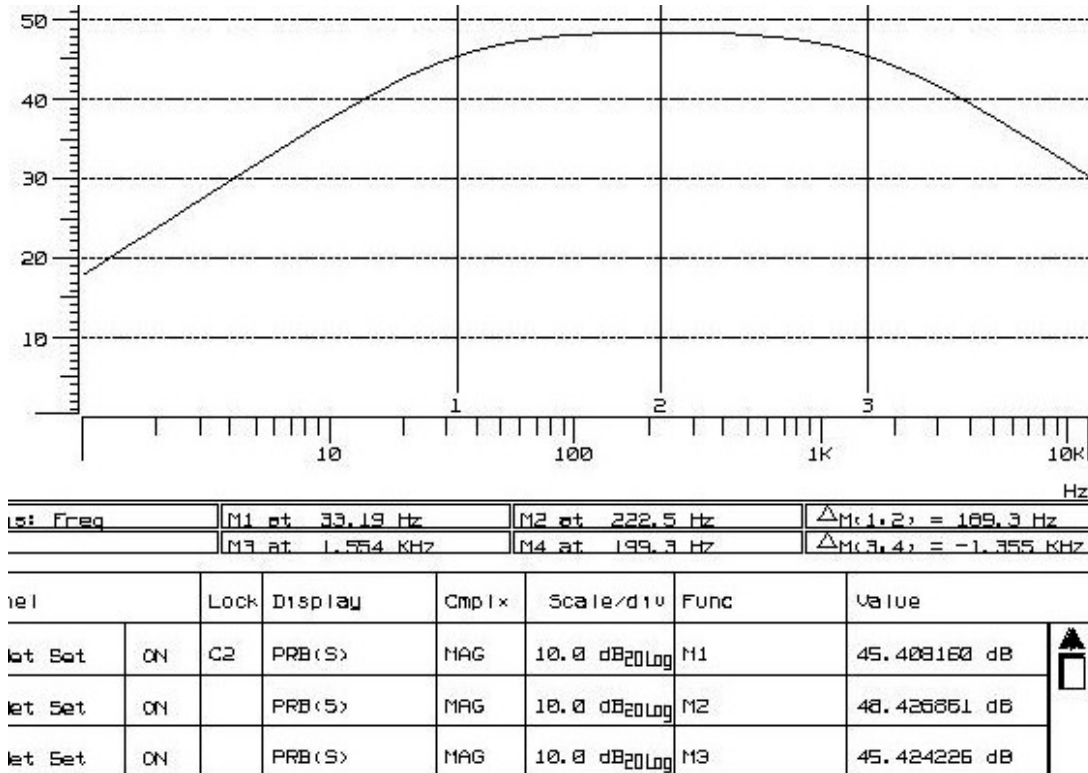
Picture 4-8 LIA Photometer Pre-amplifier BPF

The gain of this pre-amplifier is found by employing the following calculation: $2 \times R2 / R1 = 2 \times 15K / 114 = 263$.

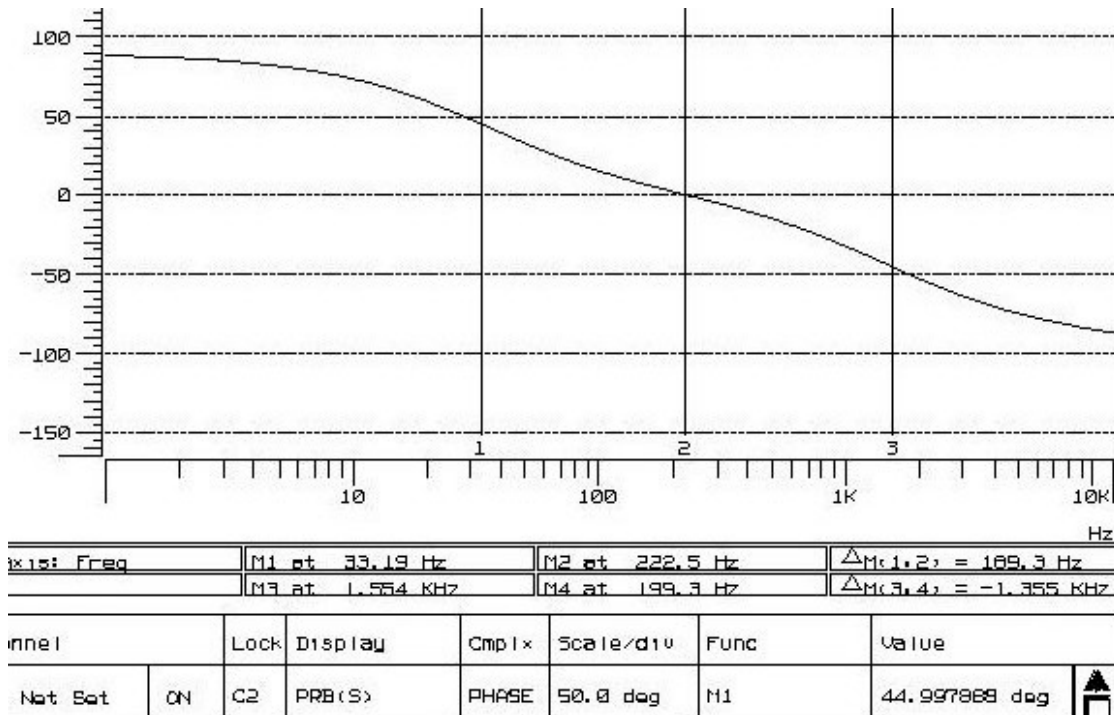
The BPF's low frequency cut-off is found by employing the following calculation:

$$F_{CL} = \frac{1}{2\pi \cdot R_L \cdot C_L} = \frac{1}{2\pi \cdot 100K \times 47nF} = 33,8Hz$$

The two following simulation results show respectively the magnitude and the phase transfer function of LIA Photometer Pre-amplifier BPF:

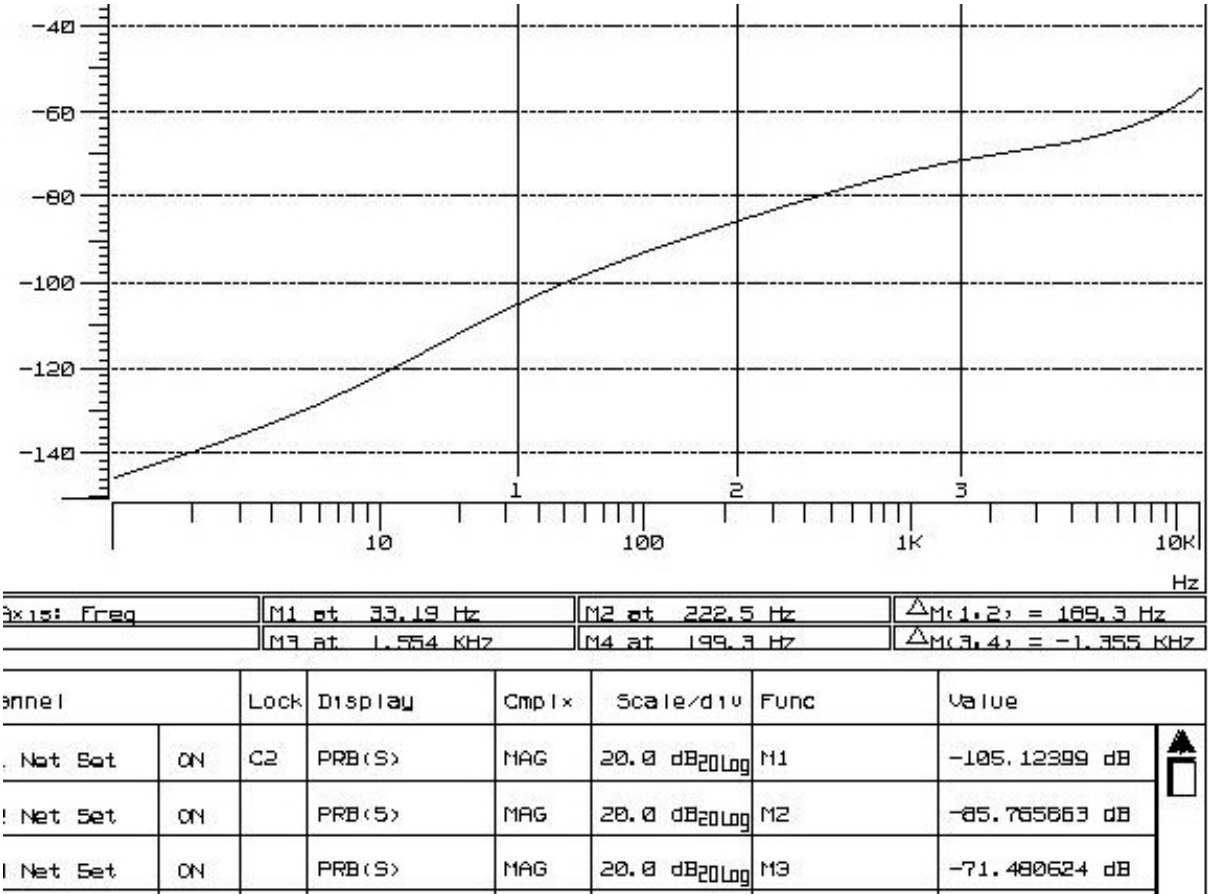


Picture 4-9 LIA Photometer Pre-amplifier BPF Magnitude Transfer Function



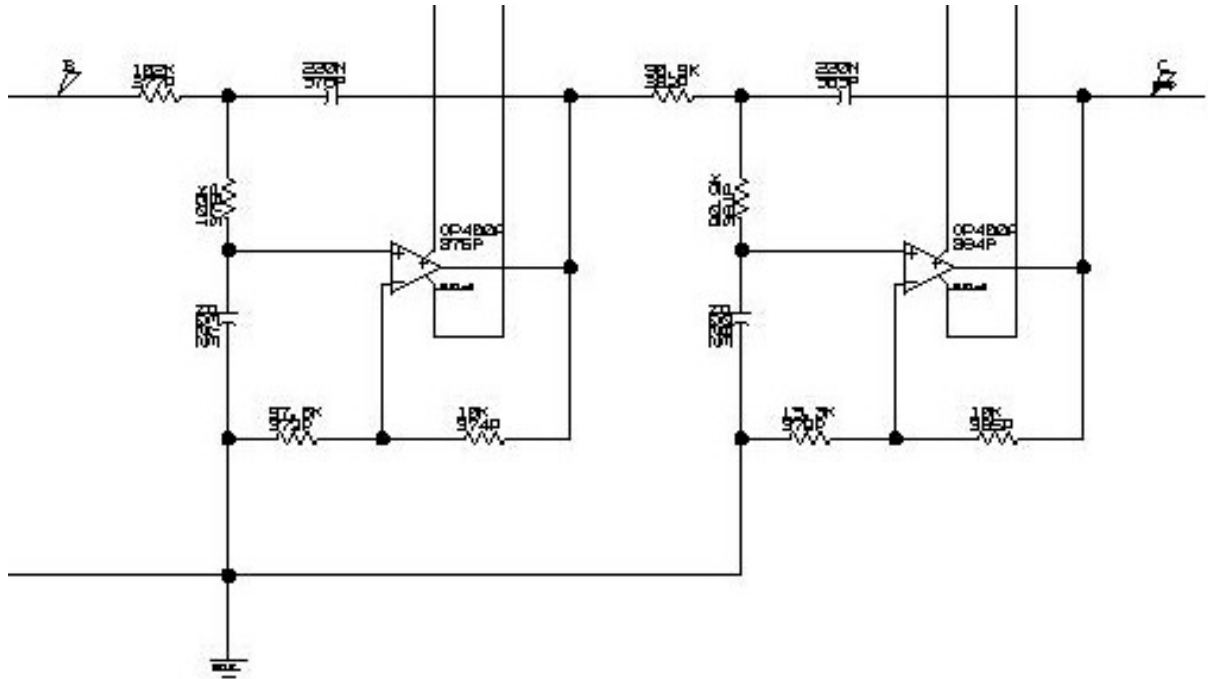
Picture 4-10 LIA Photometer Pre-amplifier BPF Phase Transfer Function

The following simulation result shows the common mode transfer function. It shows that we have at least -80dB common mode rejection between 50Hz and 300Hz . In other words, there is some leeway with the -60dB requirement.



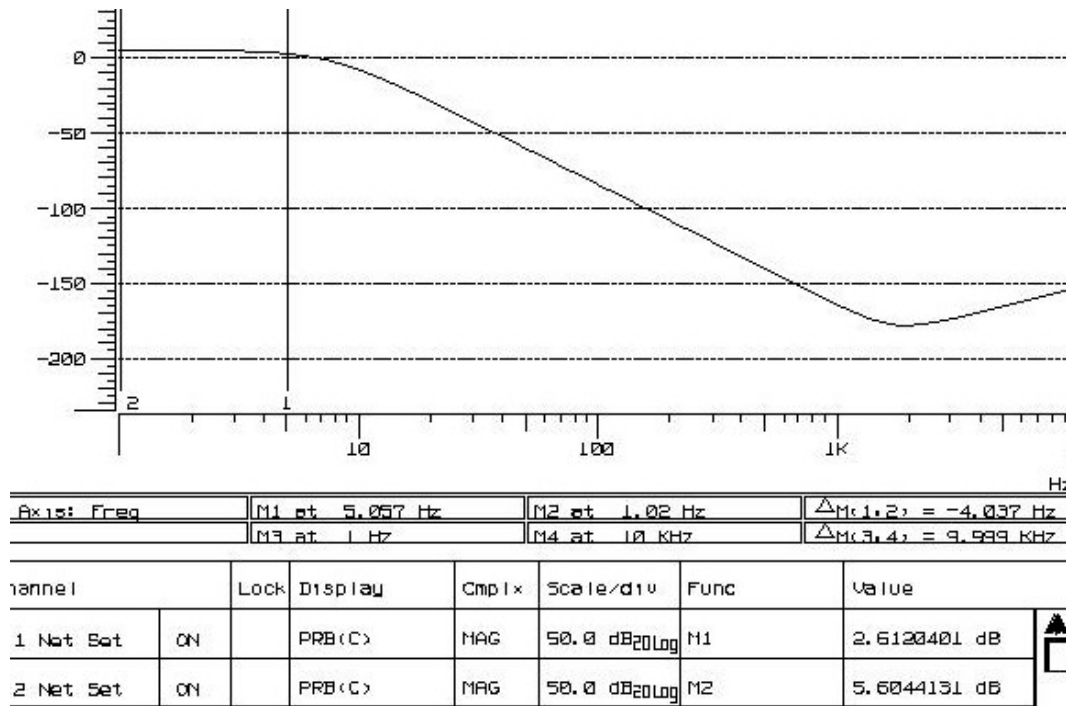
Picture 4-11 LIA Photometer Pre-amplifier BPF Common Mode Rejection

4.1.3.3 LIA Photometer Channel LPF

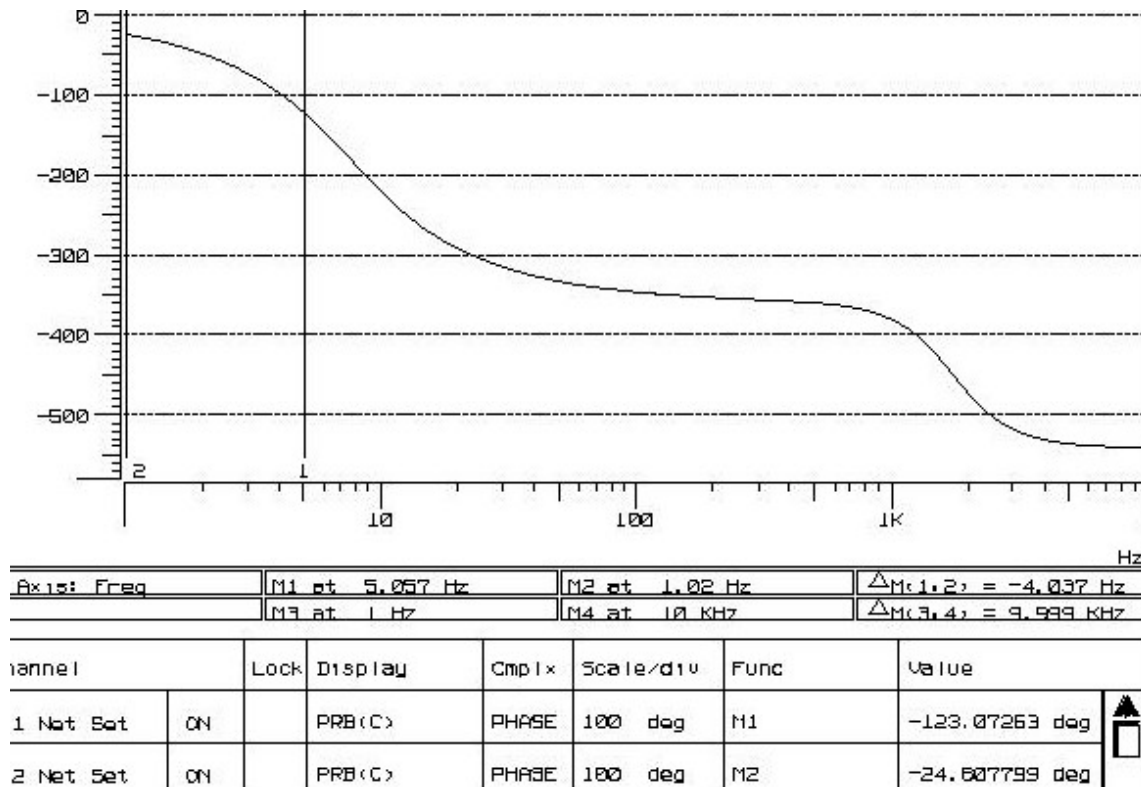


Picture 4-12 LIA Photometer Pre-amplifier BPF



The two following simulation results show respectively the magnitude and the phase transfer function of LIA Photometer four-pole Bessel LPF:



Picture 4-13 LIA Photometer LPF Magnitude Transfer Function



Picture 4-14 LIA Photometer LPF Phase Transfer Function

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4.1.3.4 LIA Photometer Channel Input Noise

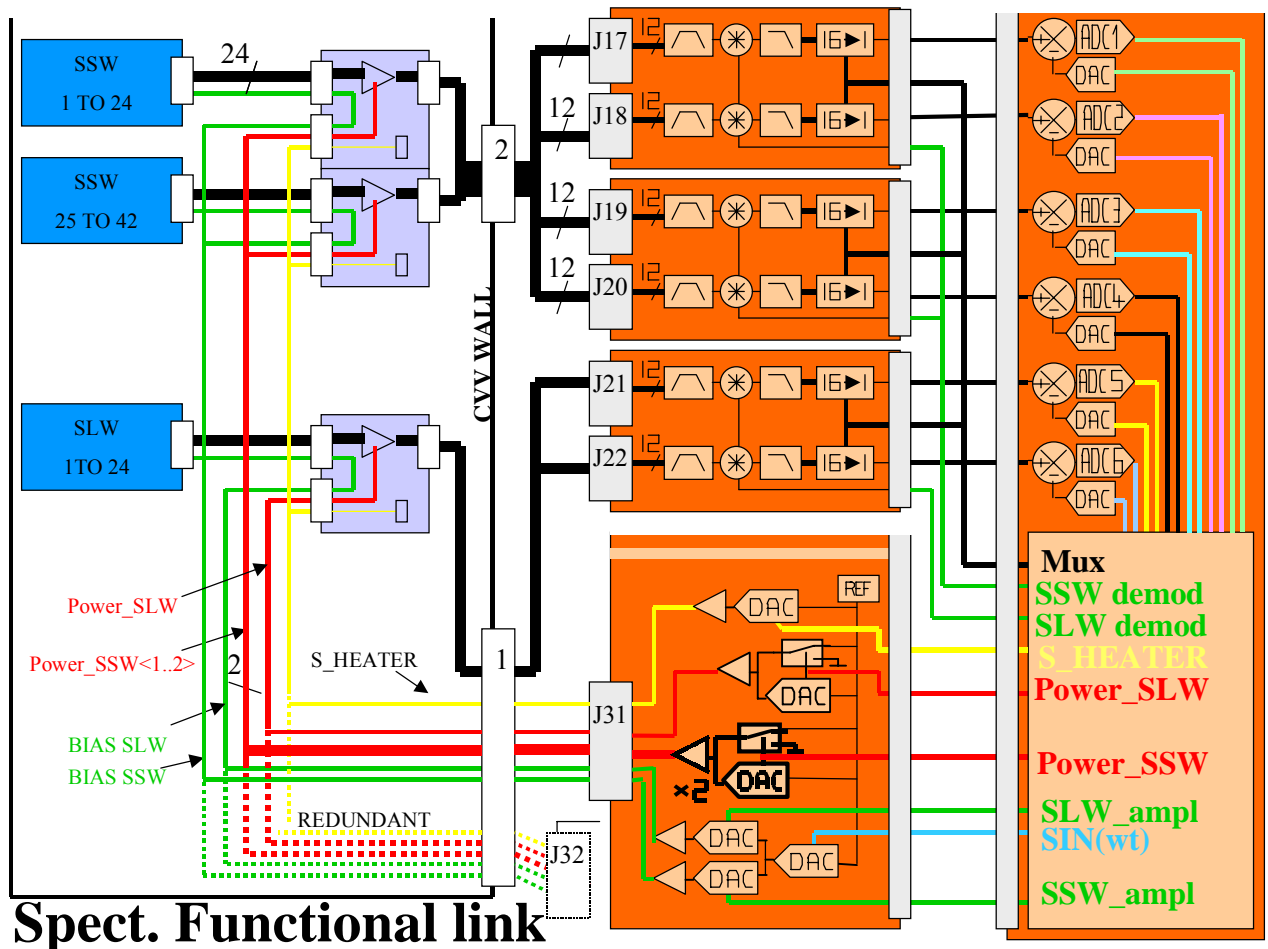
TBW

4.1.4 LIAs SPECTROMETER

4.1.4.1 QM1, QM2 and FM

Three LIA_S boards make up the LIA spectrometer section.

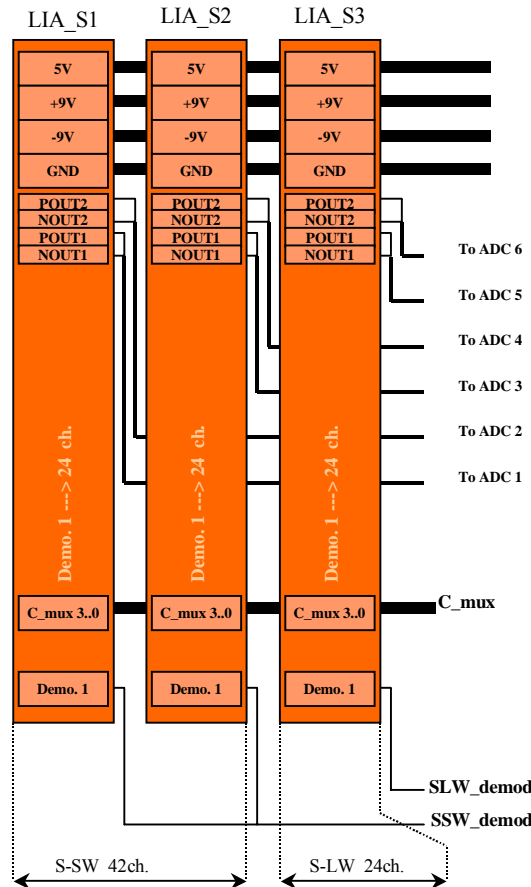
- LIA_S1 and LIA_S2 receive and process signals from forty-two “S-SW bolometers.”
- LIA_S3 receive and process signals from twenty-four “S-LW bolometers.”



Picture 4-15 Spectrometer Functional Links

The 24 SLW channels receive the same sinus bias signal (the same frequency and the same amplitude) and the same square demodulation signal (SLW_demod.) All of the 24 channels be sent to the DAQ+IF board through two differential links that are digitized by two ADCs.

The 42 SSW channels + six spare channels receive the same sinus bias signal (the same frequency and the same amplitude) and the same square demodulation signal (SSW_demod.) All of the 42 channels are sent to the DAQ+IF board through four differential links that are digitized by four ADCs.



Picture 4-16 LIA Spectrometer Section

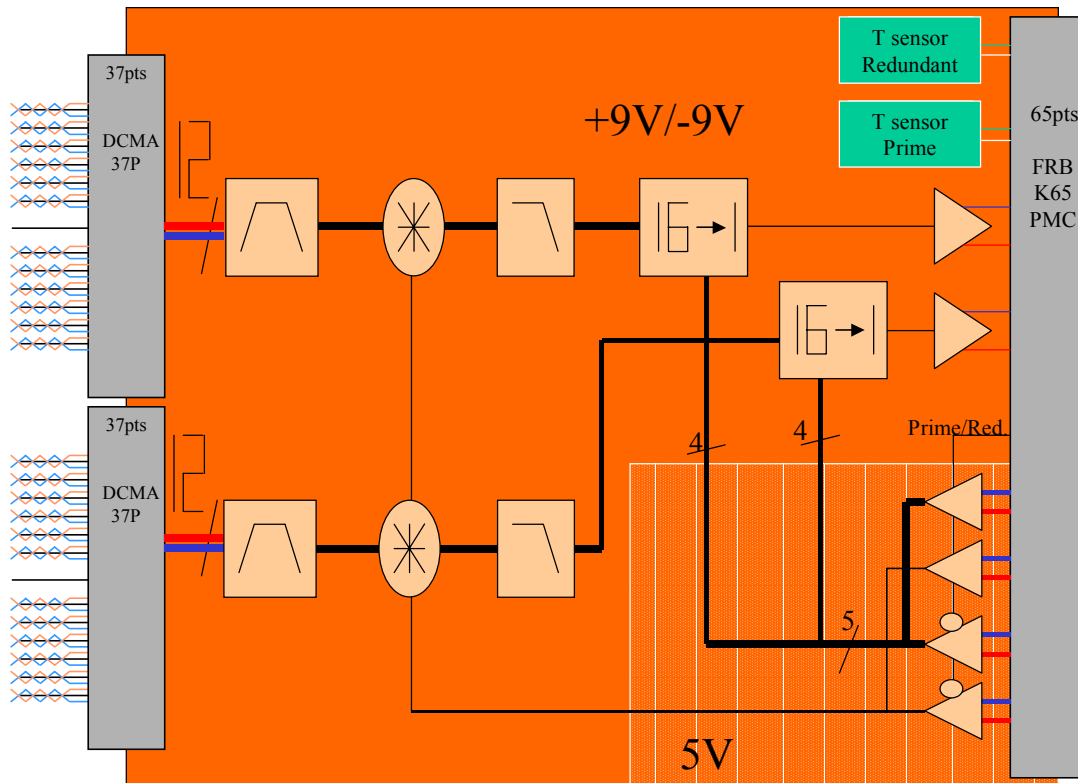
Each group receive its own respective demodulation signal: SSW_demod and SLW_demod. These signals can each have a different phase shift.

The LIA spectrometer is supplied only when the SPIRE instrument is running in spectrometer mode.

Each LIA spectrometer board receive its own group of 3 supply lines (-9V, +9V and 5V) which are automatically shutdown if a error occurs in on one of these three lines.



4.1.5 LIA SPECTROMETER BOARD

4.1.5.1 LIA Spectrometer Board Overview



Picture 4-17 LIA Spectrometer Board Overview

- Each LIA_S board has twenty-four channels which are divided into two groups.
Each group of 12 channels goes to a multiplexer.
- The two groups receive the same demodulation signal.
- The receivers that relay the multiplexer command signal and demodulation signal are redundant as they are on the LIA photometer boards.
- The two multiplexers receive the same command signals.

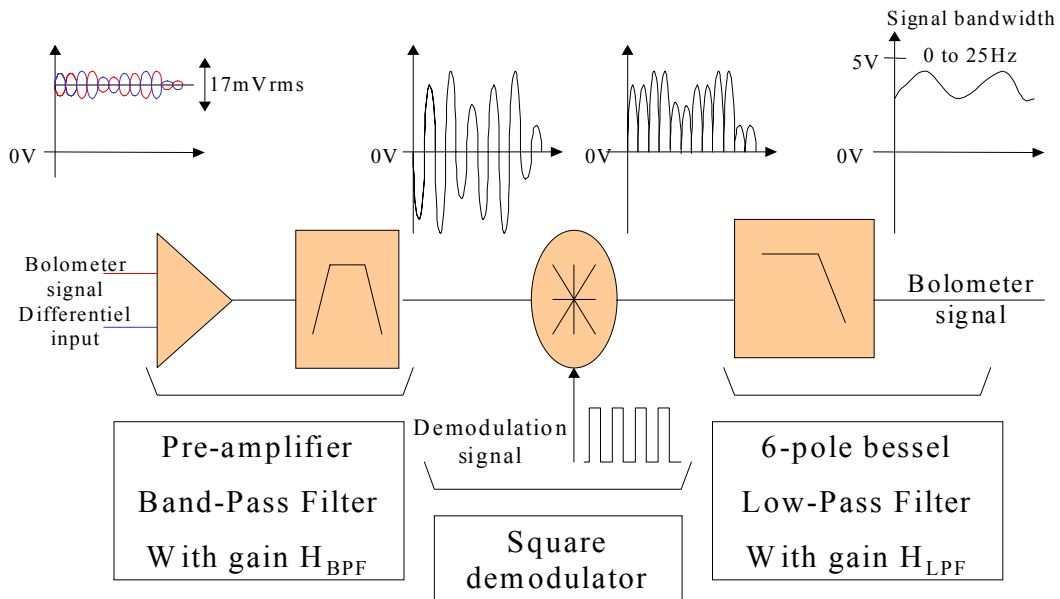
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4.1.5.2 LIA Spectrometer Board Interface

Name	Description	Type	Level	In/Out	Frequency
IN+ <i>xx</i>	Bolometer Differential Signal	Analogic	11mVrms (AC) + 1.5V (DC)	IN	50-300Hz
IN- <i>xx</i>					
POUT <i>x</i>	The twelve LIA_S channels Multiplexed in a Differential Signal	Analogic	0 to 5V	OUT	0-25Hz at mux freq.
NOUT <i>x</i>					
PAX-	BIT Command Mux (PRIME) Differential Signal	Numeric	-0,3Vto 0,3V	IN	~2.5kHz
PAX+					
RAX-	BIT Command Mux (REDUNDANT) Differential Signal	Numeric	-0,3Vto 0,3V	IN	~2.5kHz
RAX+					
PDEMOD1-	Demodulation Differential Signal (PRIME) for Channels One to Twenty- four	Numeric	-0,3Vto 0,3V	IN	50-300Hz
PDEMOD1+					
RDEMOD1-	Demodulation Differential Signal (REDUNDANT) for Channels One to Twenty-four	Numeric	-0,3Vto 0,3V	IN	50-300Hz
RDEMOD1+					
PT_P9V	Sensor PRIME Bias	Analogic	9V	IN	DC
PT	Output Sensor PRIME	Analogic	2 to 4V	OUT	-
RT_P9V	Sensor REDUNDANT Bias	Analogic	9V	IN	DC
RT	Output Sensor REDUNDANT	Analogic	2 to 4V	OUT	-
P9V	9V Power Supply	Power	9V	IN	DC
N9V	-9V Power Supply	Power	-9V	IN	DC
P9V_P	PRIME/REDUNDANT Signal	Analogic	0 to 9V	IN	DC
P5V	5V Power Supply	Power	5V	IN	DC
GND	Grounding	Power	0V	-	DC

4.1.6 LIA SPECTROMETER CHANNELS

4.1.6.1 LIA Spectrometer Channel Overview



The input differential signal that comes from a bolometer is amplified and its DC component is eliminated by the pre-amplifier BPF. Then, it is demodulated by a squared signal. Afterwards it is filtered by a six-pole Bessel LPF.

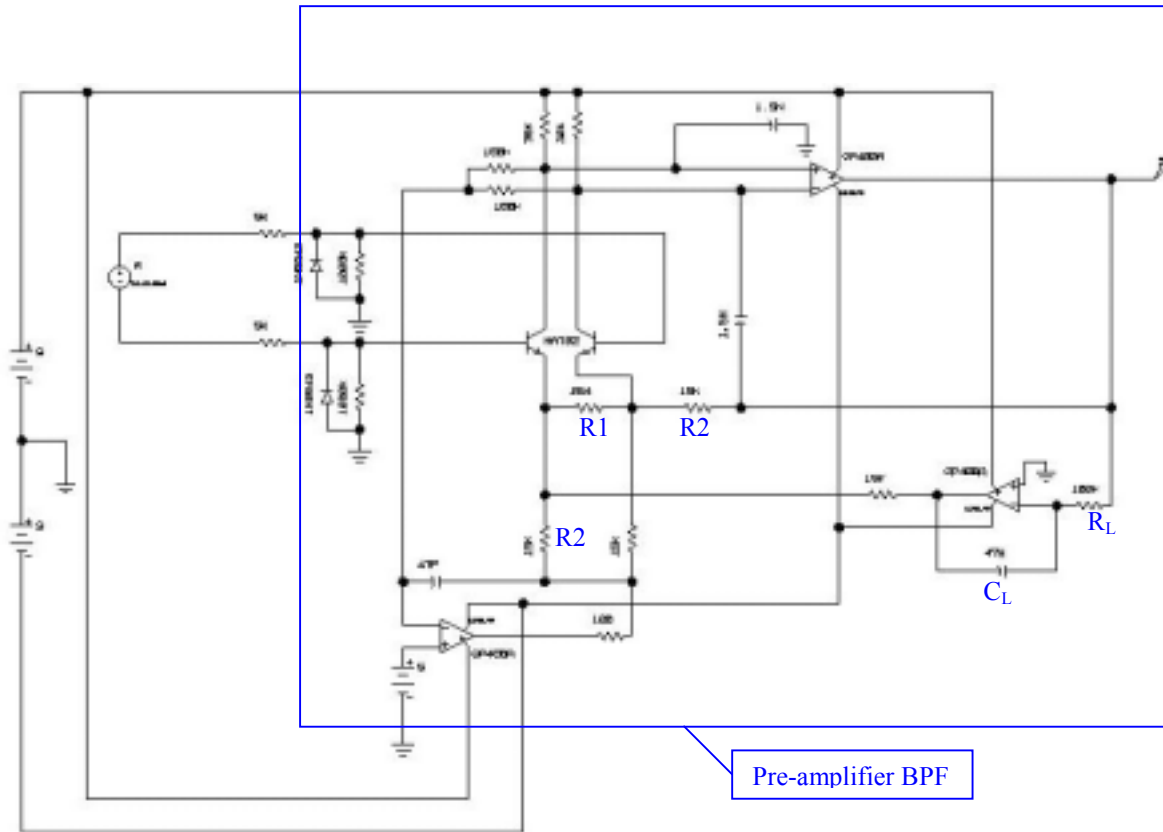
The six-pole besel low pass filters have a structural gain of $H_{LPF} = 2,87$

The square demodulation introduces a gain of $2/\pi$

Note: To be sure that a photometer channel won't be saturated with a 17mVrms input, the output signal cannot not be more than 5V.

This is why the band pass filter gain H_{BPF} cannot be more than $\frac{5V}{17mV \cdot \frac{2\sqrt{2}}{\pi} \cdot 2,87} = 114$

4.1.6.2 LIA Spectrometer Channel BPF



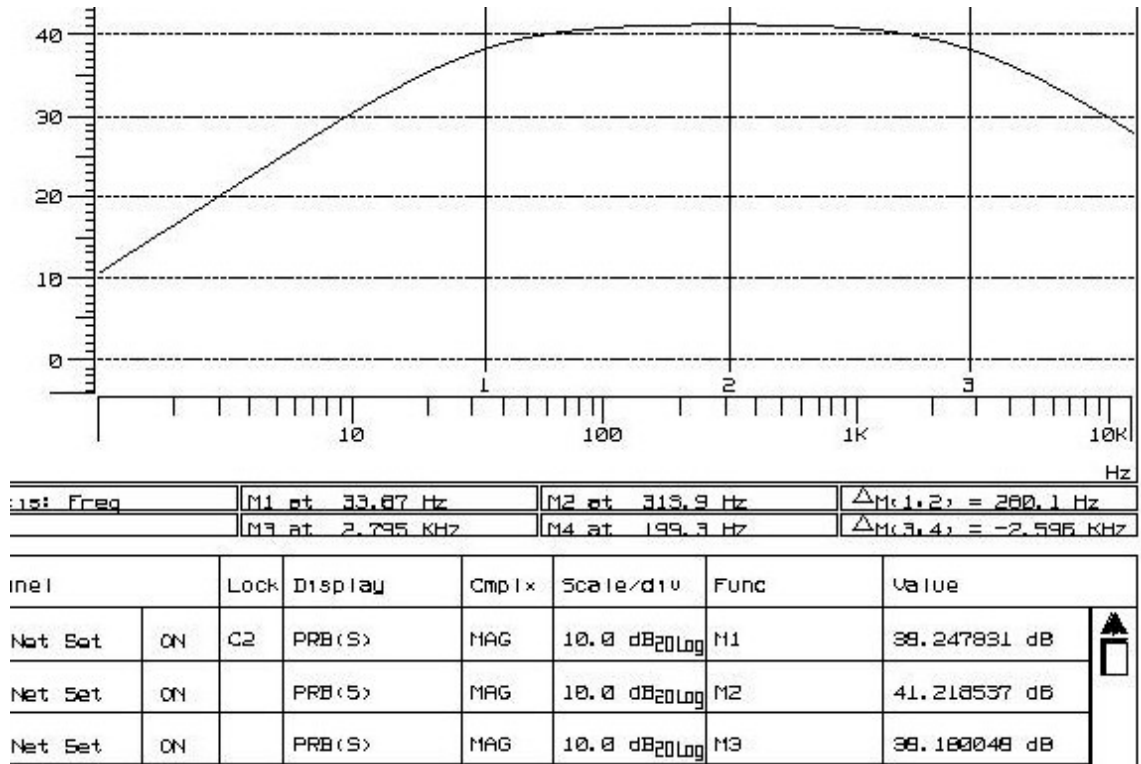
Picture 4-18 LIA Spectrometer Pre-amplifier BPF

The gain of this pre-amplifier is found by employing the following calculation: $2 \times R_2 / R_1 = 2 \times 15K / 263 = 114$.

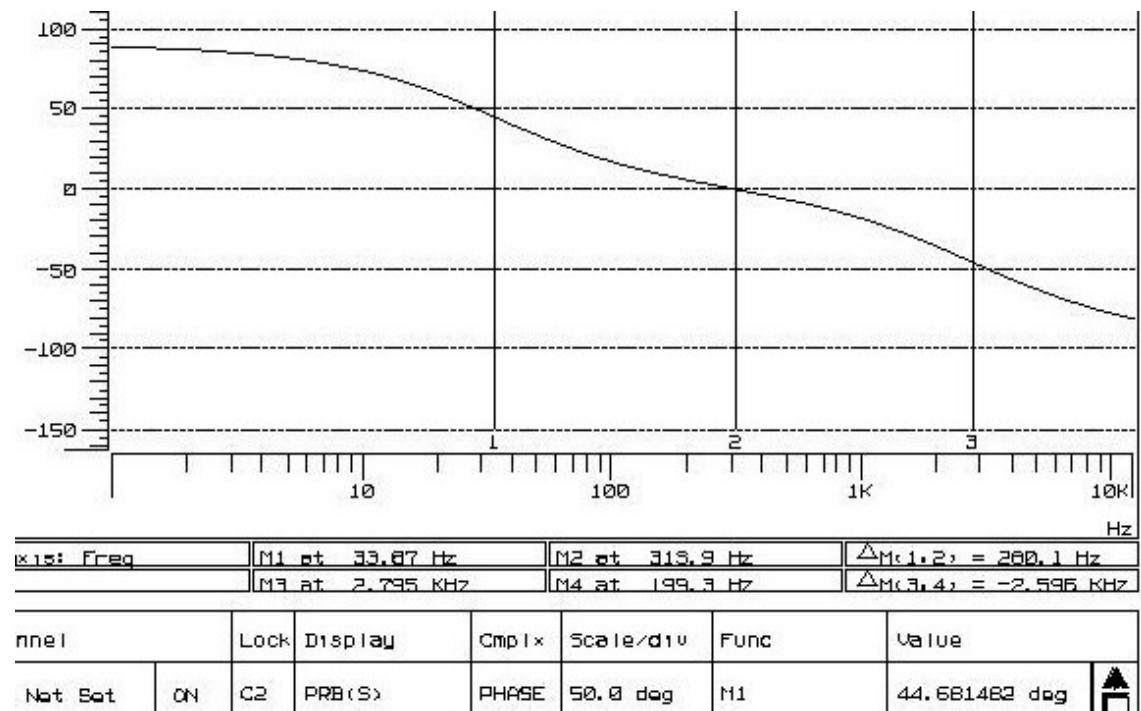
The BPF's low frequency cut-off is found by employing the following calculation:

$$F_{CL} = \frac{1}{2\pi \cdot R_L \cdot C_L} = \frac{1}{2\pi \cdot 100K \cdot 47nF} = 33,8Hz$$

The two following simulation results show respectively the magnitude and the phase transfer function of LIA Spectrometer Pre-amplifier BPF:

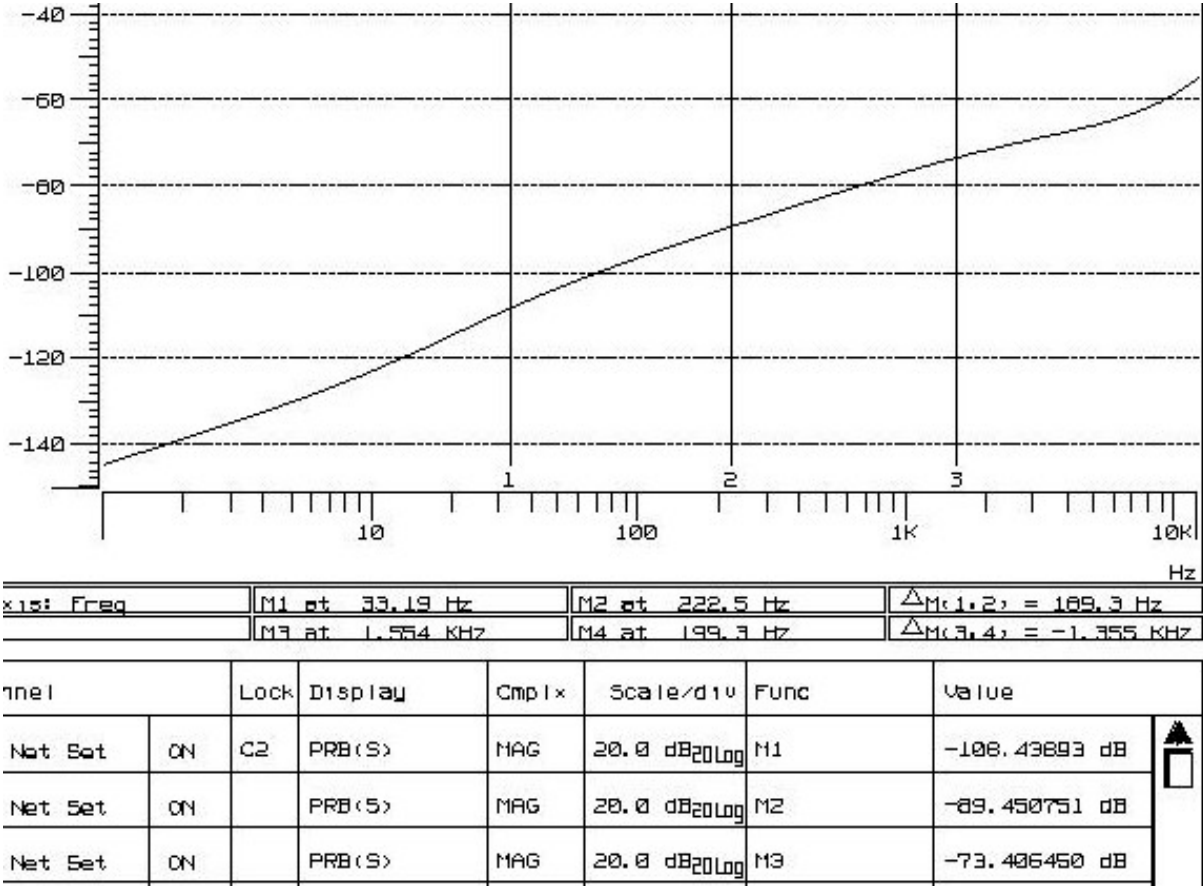


Picture 4-19 LIA Spectrometer Pre-amplifier BPF Magnitude Transfer Function



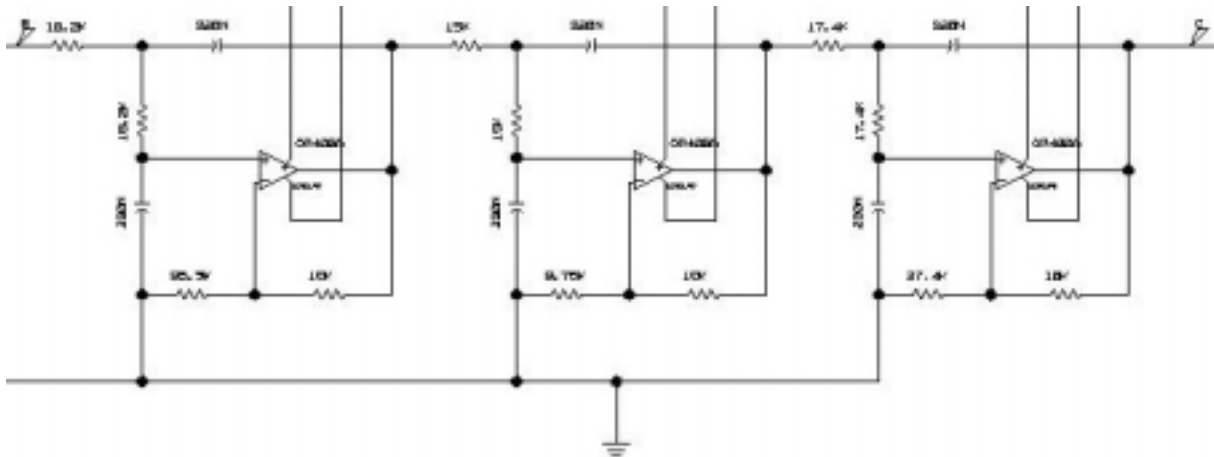
Picture 4-20 LIA Spectrometer Pre-amplifier BPF Phase Transfer Function

The following simulation result shows the common mode transfer function. It shows that we have at least -80dB common mode rejection between 50Hz and 300Hz . In other words, there is some leeway with the -60dB requirement.



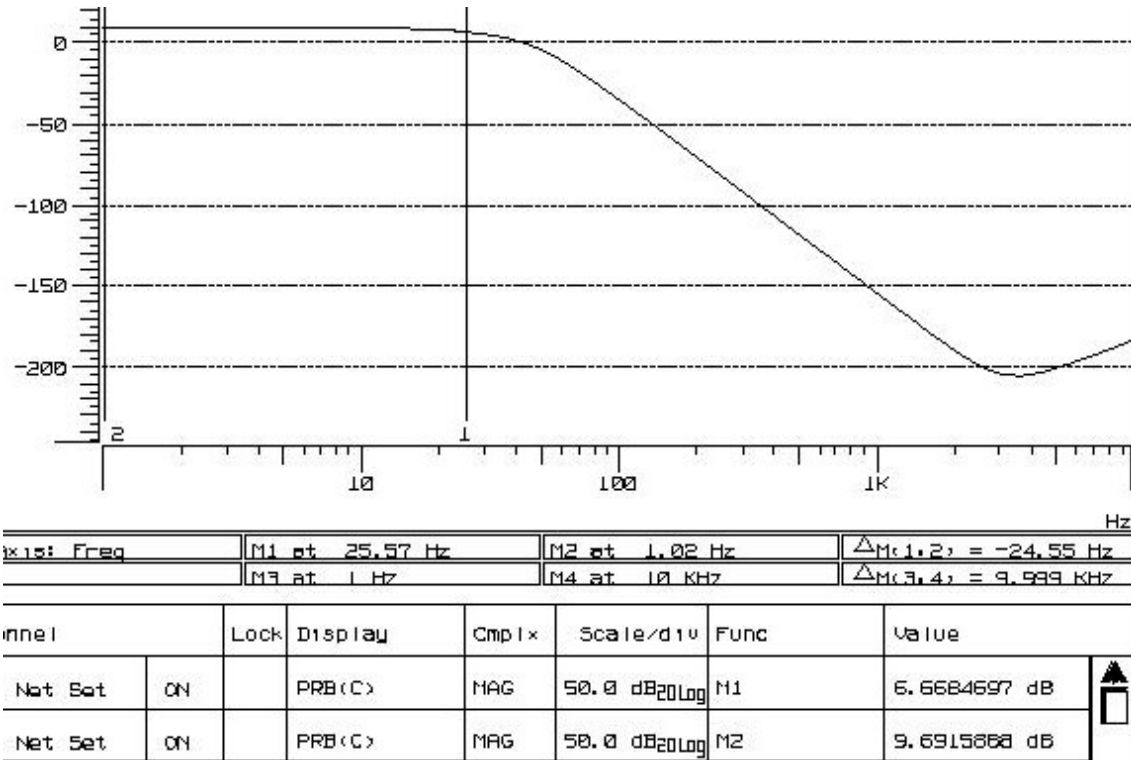
Picture 4-21 LIA Spectrometer Pre-amplifier BPF Common Mode Rejection

4.1.6.3 LIA Spectrometer Channel LPF

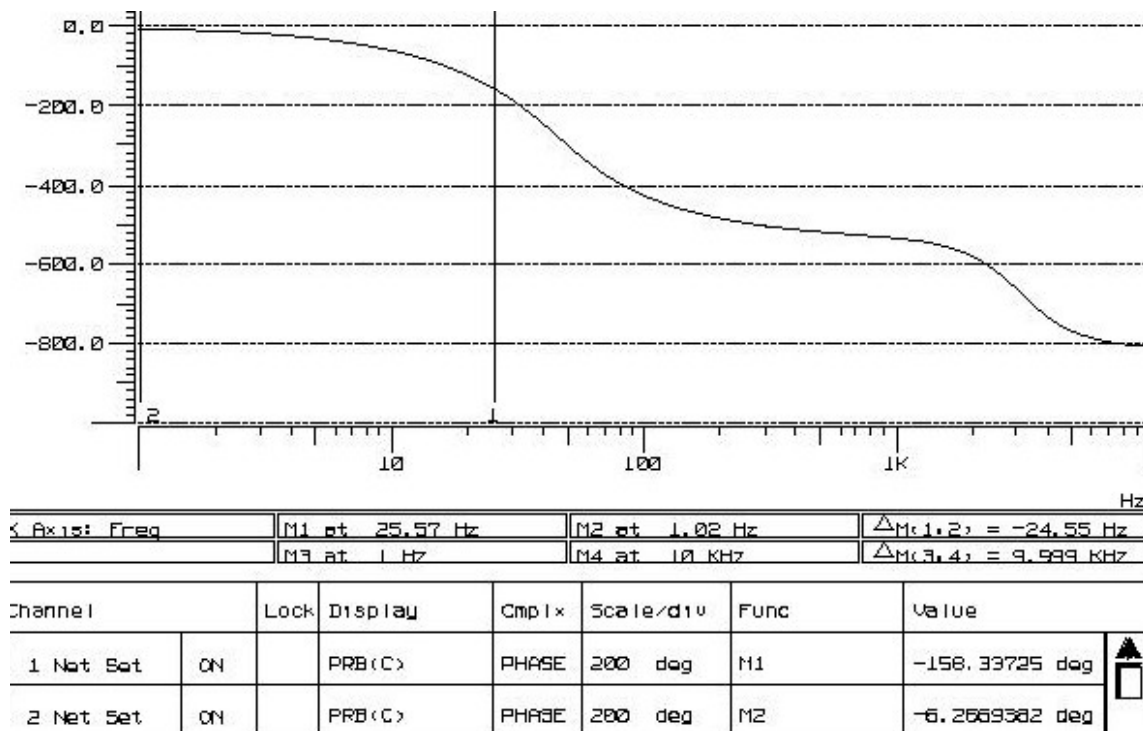


Picture 4-22 LIA Spectrometer Pre-amplifier BPF



The two following simulation results show respectively the magnitude and the phase transfer function of LIA Spectrometer six-pole Bessel LPF:



Picture 4-23 LIA Spectrometer LPF Magnitude Transfer Function



Picture 4-24 LIA Spectrometer LPF Phase Transfer Function

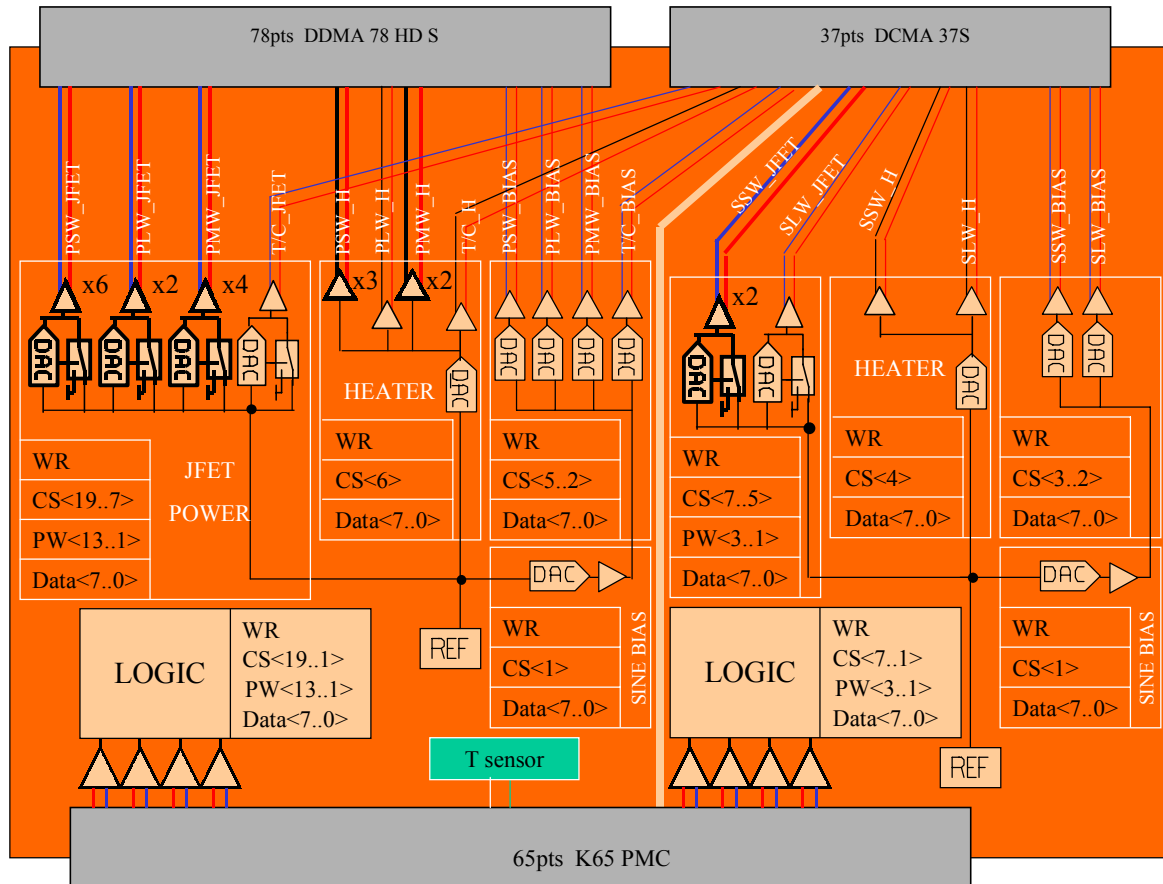
	<p>DCU Design document</p>	 <p>SAP-SPIRE- FP-0063-02 Issue: 0.2 Date : 05/07/02</p>
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4.1.6.4 LIA Photometer Channel Input Noise

TBW

4.1.7 BIAS BOARDS

4.1.7.1 BIAS Board Overview



Picture 4-25 BIAS Board Overview

The BIAS boards generate sine biases for the bolometers and DC biases for JFETs and heaters.

- Adjustable sine biases:
 - Photometer: 1sine generator/ 4 channels with independent amplitudes
 - Spectrometer: 1sine generator/ 2 channels with independent amplitudes
 - Voltage range: 0 to 200 mVrms for the bolometers 0 to 500 mVrms for the thermometers
 - Accuracy: 256 levels
 - Frequency range: 50 to 300Hz
- Adjustable DC JFET biases:
 - Photometer: 13 generators for JFET
 - Spectrometer: 3 generators for JFET
 - Voltage range: 0 to –5V for VSS with 256 levels and VDD is set between 0 and 4V by two resistors
 - Output currents: 5mA max
- Adjustable DC heater biases:
 - Photometer: 1heater generator and 7 buffers
 - Spectrometer: 1 heater generator and 3 buffers
 - Voltage range: 0 to –5V with 256 levels
 - Output currents: 5mA max for each buffer

Note: Each buffer biases at most 2 JFET module* heaters. (*JFETmodule = 24 channels)

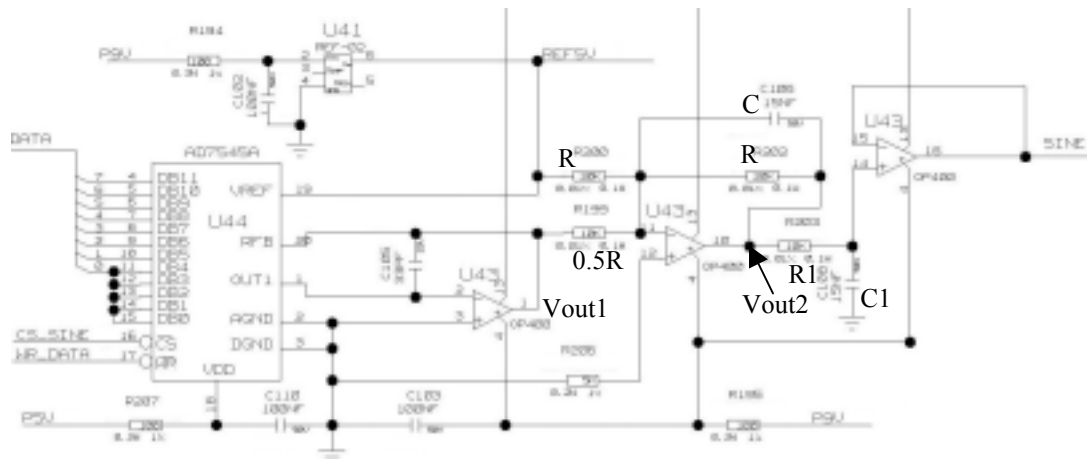
4.1.7.2 BIAS Board Interface

TBW

4.1.8 BIAS BOARD FUNCTIONS

4.1.8.1 Bolometer BIAS

The following circuit is used to generate a sinusoidal signal with amplitude of 5V and a 0V center.
There are two identical sine generators on the BIAS board (1 for the photometer and 1 for the spectrometer.)



Picture 4-26 Sine Generator

- From a +5V precision voltage reference, the DAC and the first OP generate a tension proportional to the numeric 8 bits signal DATA: $V_{out1} = -REF5V(DATA/256)$.
- The second OP adds half the reference voltage to V_{out1} and multiplies the result by 2 as well as filters: $V_{out2} = REF5V(1-DATA/128)/(1+j\omega/\omega_c)$ with $\omega_c = 1/RC \Rightarrow Fc = 530Hz$
- Afterward the signal go through another low pass filter: $SINE = V_{out2}/(1+j\omega/\omega_c1)$ with $\omega_c1 = 1/R1C1 \Rightarrow Fc1 = 1061Hz$

DATA is an integer between 0 and 255

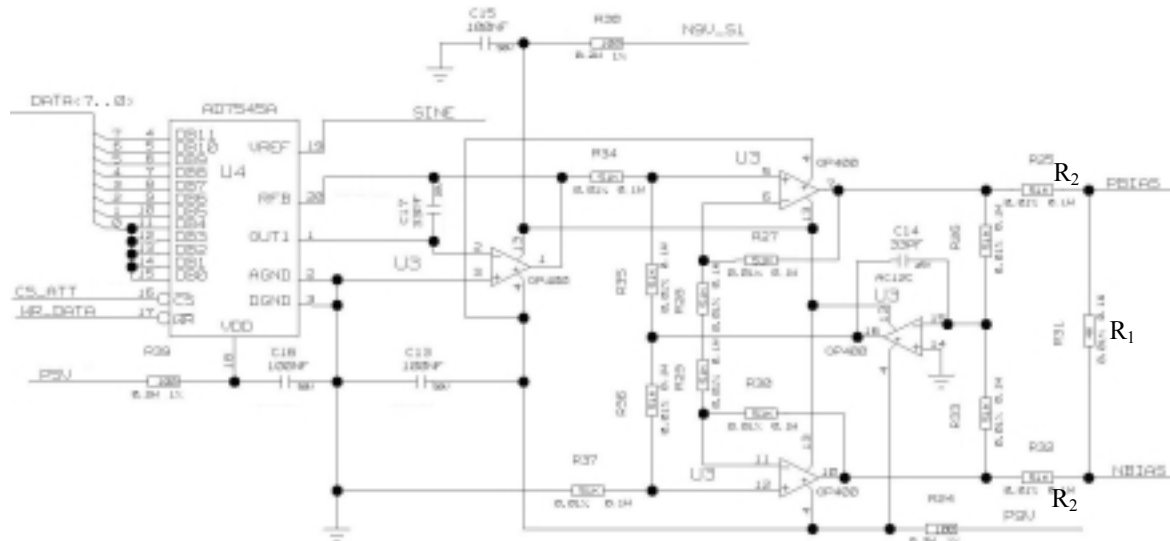
To generate sinusoidal signal (SINE) with frequency F_{sine} the 256 integers, which describe a sine, should be wrote in the digital to analog converter with a frequency for $256.F_{sine}$.

The 256 values can be calculated by taken the nearest integer of $[127.SIN(2\pi(n+1/2)/256)+128]$ with n between 0 and 255.

Each bolometer group has his own bias attenuator.

- The 4 bias attenuators of the photometer receive at their input the signal coming from the photometer sine generator.
- As well as The 2 bias attenuators of the spectrometer receive at their input the signal coming from the spectrometer sine generator.

The bias attenuator circuit is as follow:

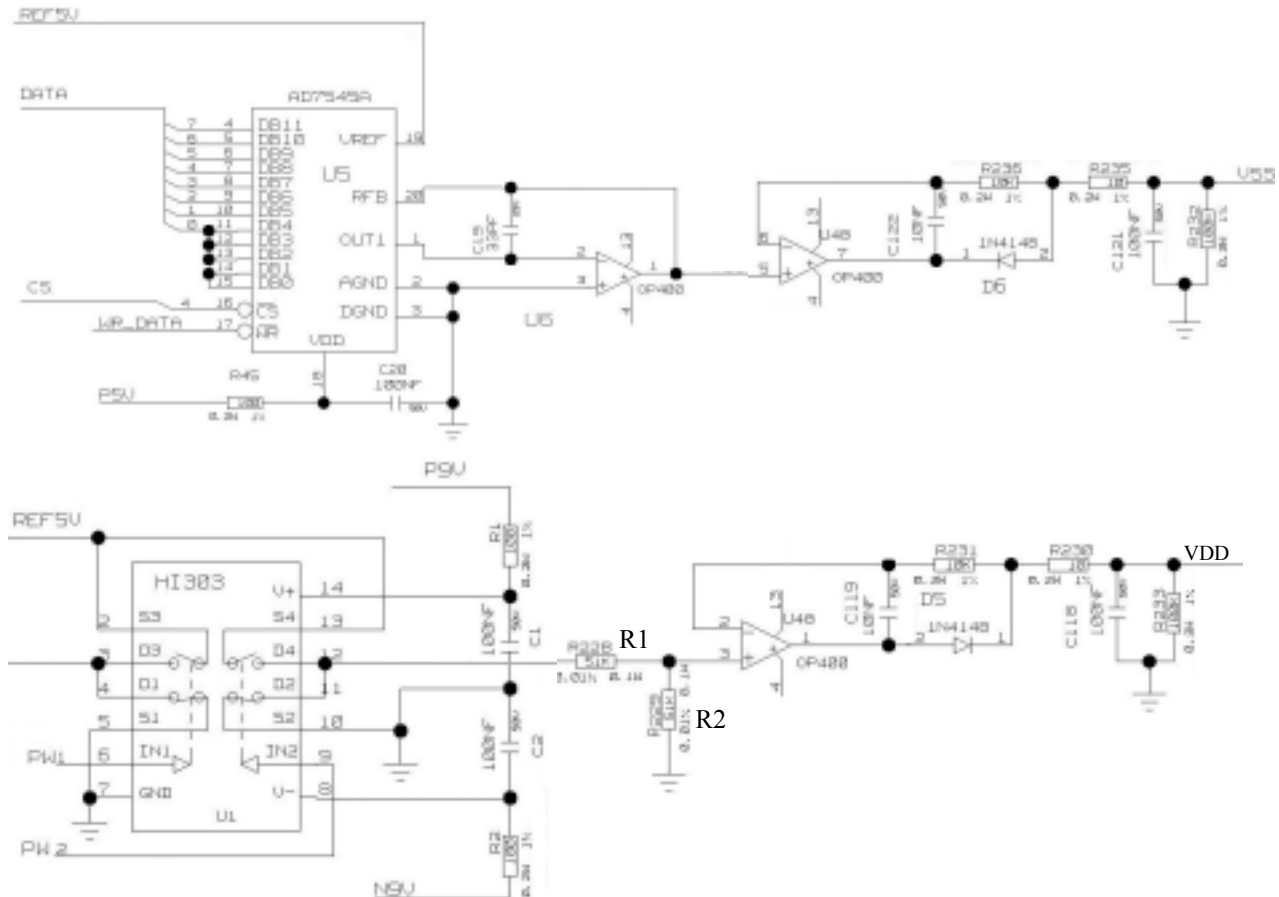


Picture 4-27 Bias Attenuator

- From the output of a sine generator (SINE) the DAC and the first OP generate a tension proportional to the numeric 8 bit signal DATA: $V_{out1} = -SINE(DATA/256)$.
- The three others OP make the signal differential with a 0V center by filtering the DC component.
- The 3 last resistors divide the differential signal by $\frac{R_1/2}{2.R_2+R_1/2}$ if the redundant and prime bias boards are connected together or by $\frac{R_1}{2.R_2+R_1}$ if they are not.

4.1.8.2 JFET BIAS

Each JFET module has its own bias generator. A JFET bias generator provide a negative DC tension VSS and a positive DC tension VDD



Picture 4-28 JFET Bias Generator

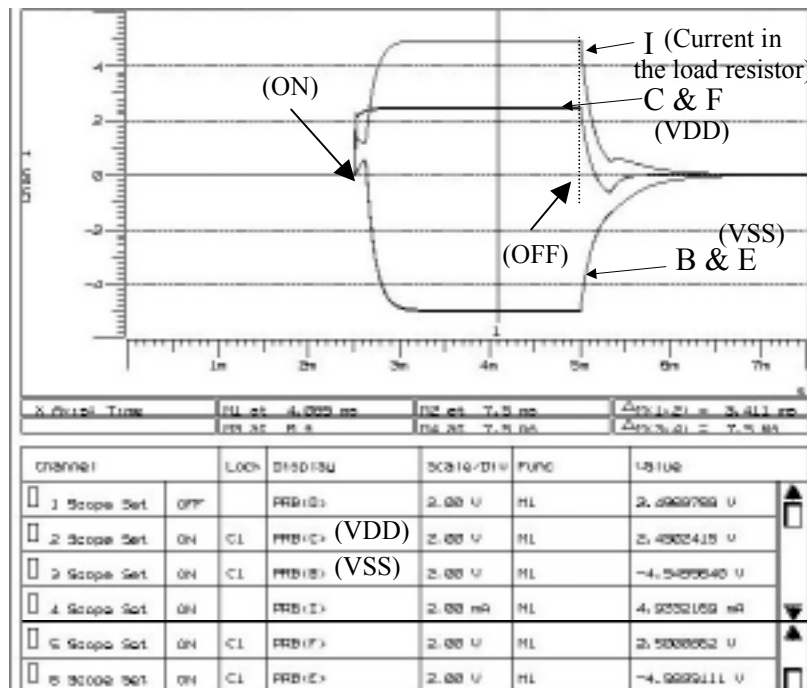
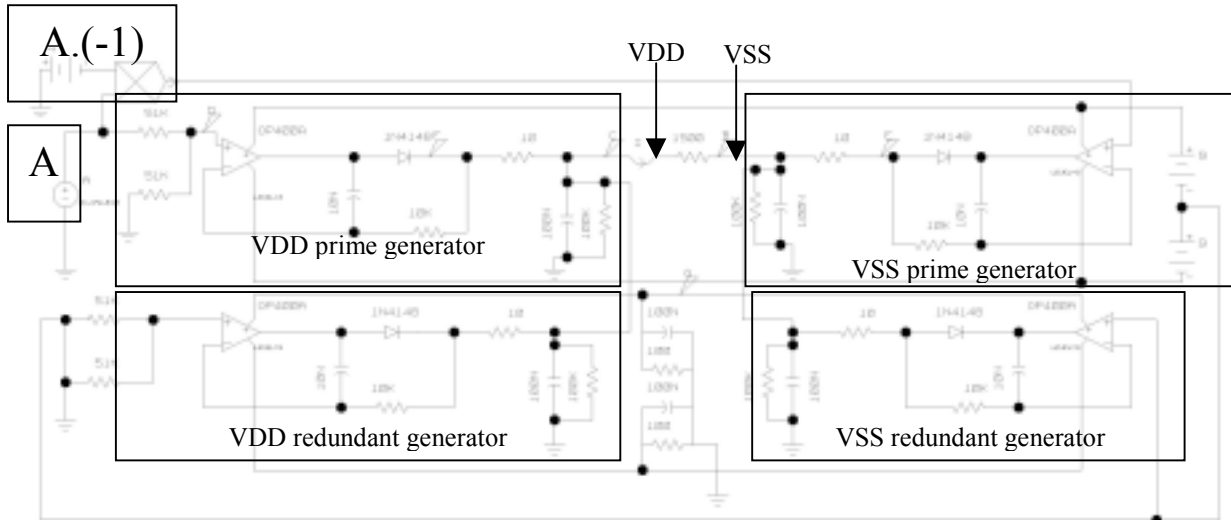
- VSS generator:
 - From a +5V precision voltage reference, the DAC and the first OP generate a tension proportional to the digital 8 bits DATA: $VSS = -REF5V(DATA/256)$.
 - The second OP and his following components are there to:
 - o Avoid overshoot when VSS is set ON from OFF or the other way
 - o Make the connection with the empowered redundant bias board safe and use full
 - o Provide the 5mA required.
- VDD generator:
 - When the switch is **ON** a +5V precision voltage reference is applied on two resistors R1 and R2 so $VDD = REF5V.R2/(R1+R2)$.
 - When the switch is **OFF** the ground is applied on two resistors R1 and R2 so $VDD= 0V$.
 - The second OP and his following components are there to:
 - o Avoid overshoot when VDD is set ON from OFF or the other way
 - o Make the connection with the empowered redundant bias board safe and use full
 - o Provide the 5mA required.

The following simulation shows the switching ON and OFF of VSS, VDD.

- VSS switched ON 0V to -5V. (A=5V)
- VSS switched OFF -5V to 0V. (A=0V)
- VDD switched ON 0V to 2.5V. (A=5V)
- VDD switched OFF 2.5V to 0V. (A=0V)

The prime generators are powered, the redundant ones are not.

The load resistor is set for a nominal generator output current of 5mA.



Picture 4-29 JFET Bias Generator Simulation

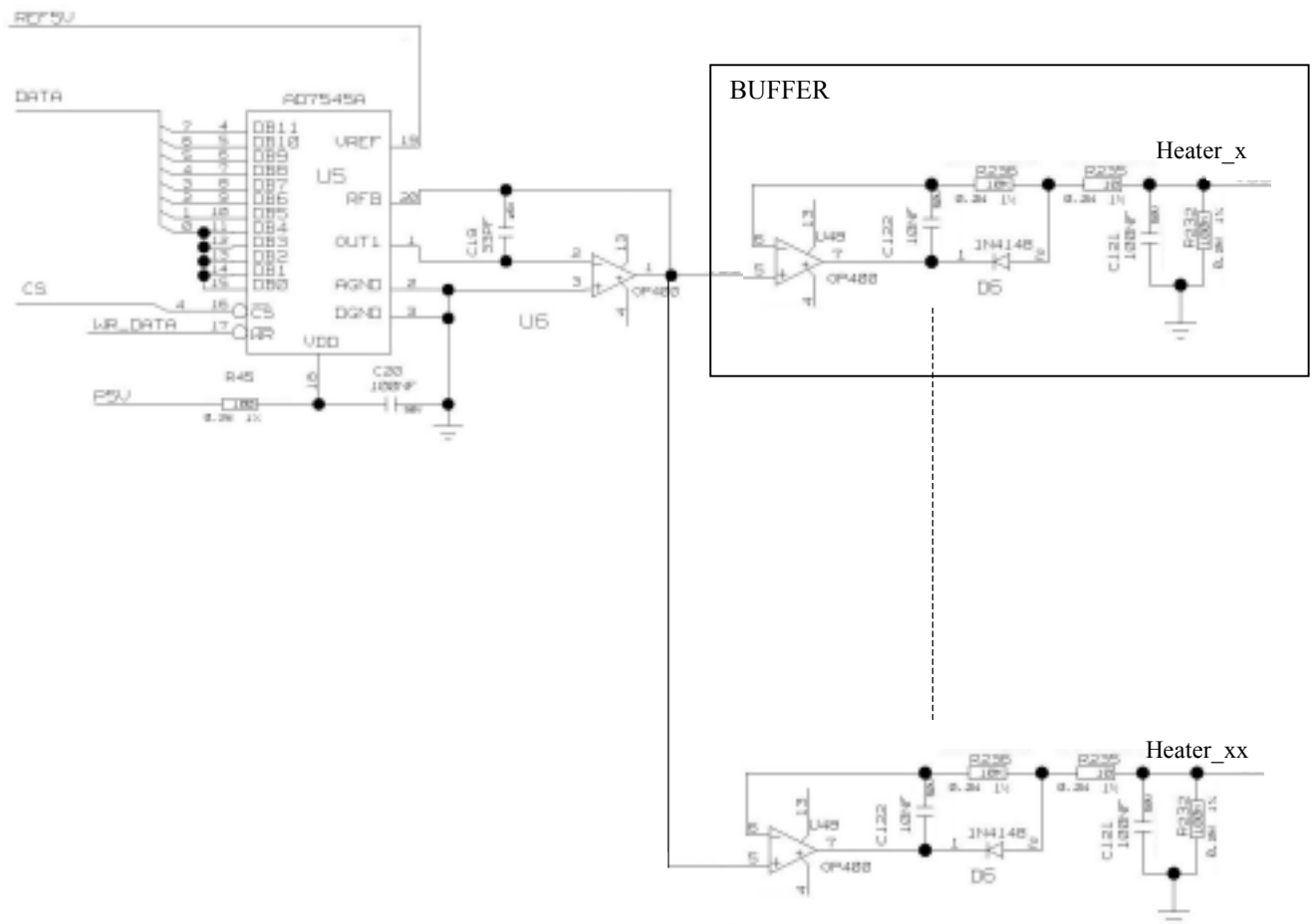
4.1.8.3 Heater

To bias the photometer heaters there are:

- A bias generator and 7 buffers (the buffer heater is similar to a VSS buffer) of which:
 - o each 6 buffers bias each 2 JFET module heaters
 - o 1 buffer biases only the T/C JFET module

To bias the spectrometer heaters there are:

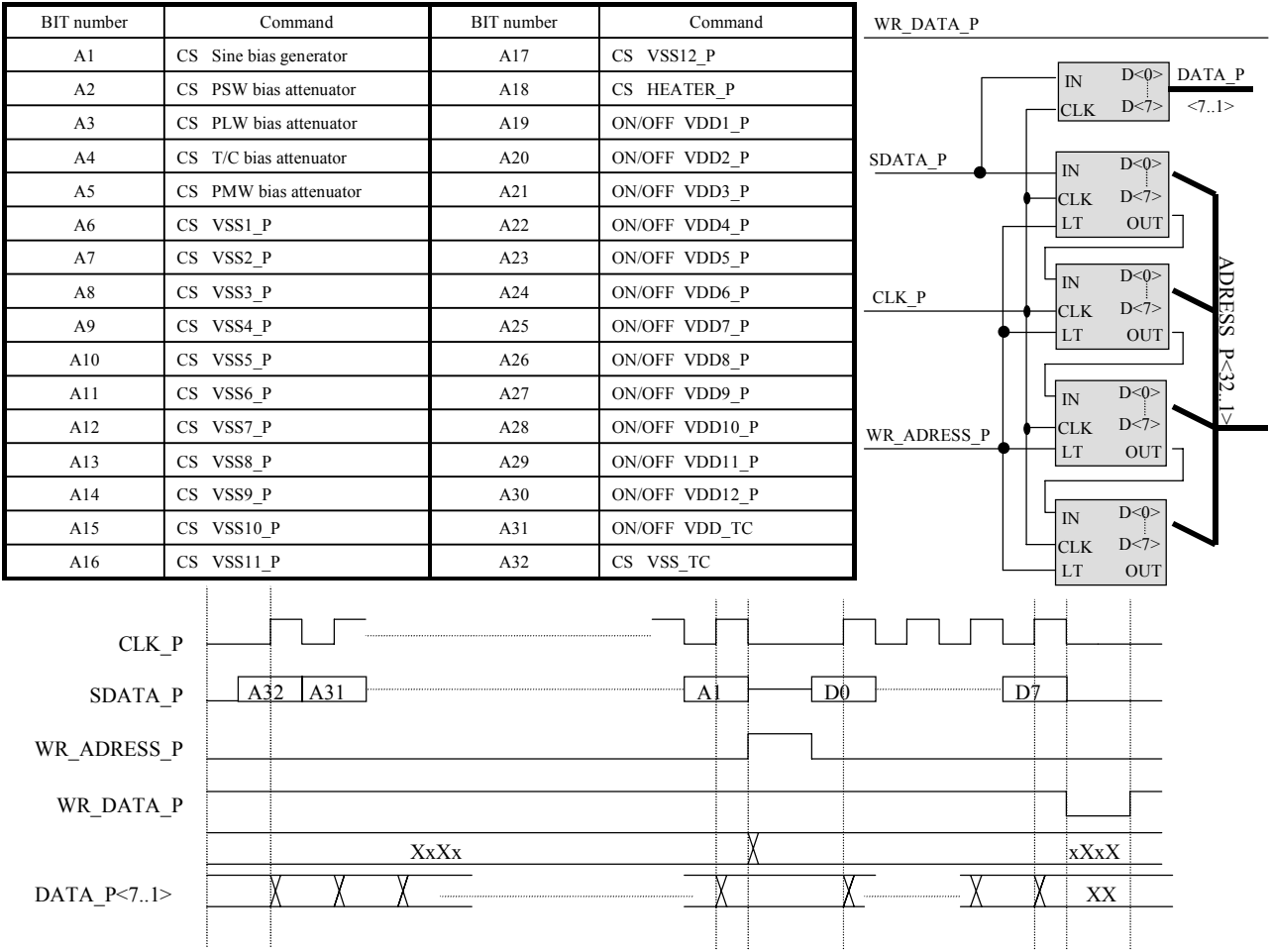
- A bias generator and 2 buffers (the buffer heater is similar to a VSS buffer) of which:
 - o 1 buffer biases 2 JFET module heaters
 - o 1 buffer biases only 1 JFET module heater



Picture 4-30 Heater Bias Generator

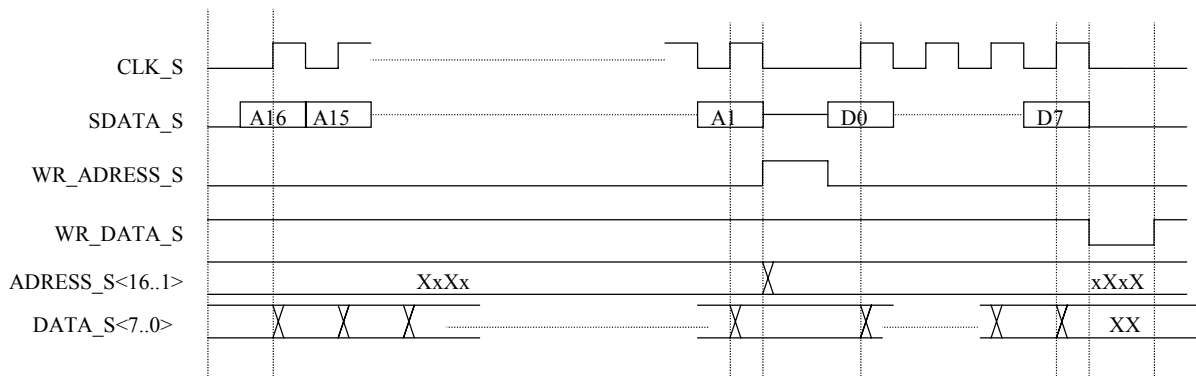
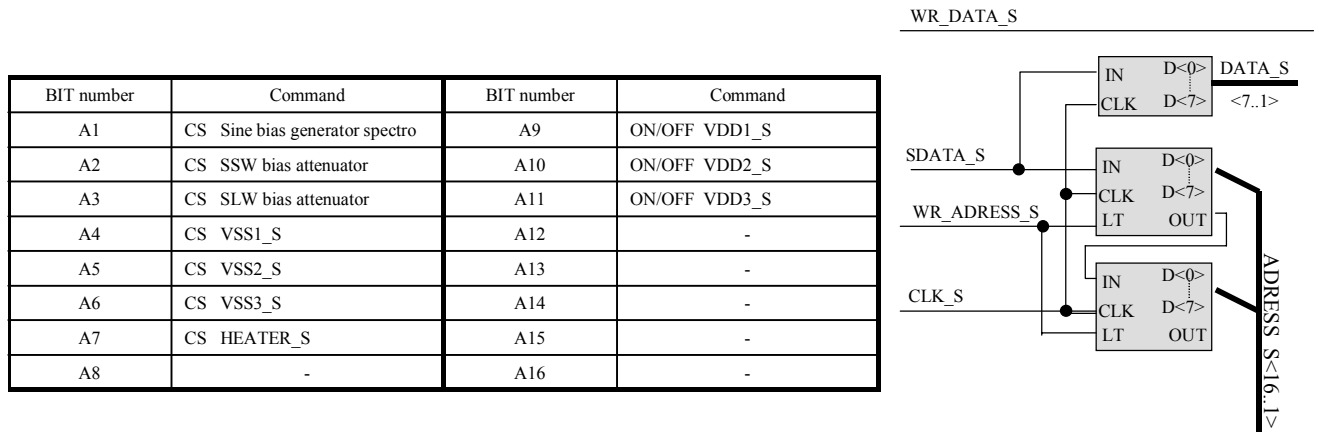
4.1.8.4 Commands

- All of the photometer ADCs CS (chips select) and ON/OFF switches are connected to four 8-bit latched SIPO (Serial Input to Parallel Output) shift registers.
- The 17 photometer ADCs are connected to the same write signal WR_DATA_P.
- The four 8-bit latch SIPO shift registers are connected to the same latch signal WR_ADRESS_P
- The photometer 8-bit parallel DATA_P bus is provided by one SIPO shift register.



Picture 4-31 Photometer Bias Command

- All of the spectrometer ADCs chips select and ON/OFF switches are connected to two 8-bit latch SIPO (Serial Input to Parallel Output) shift registers.
- The 7 spectrometer ADCs are connected to the same write signal WR_DATA_S.
- The two 8-bit latch SIPO shift registers are connected to the same latch signal WR_ADDRESS_S
- The spectrometer 8-bit parallel DATA_S bus is provided by SIPO shift register.



Picture 4-32 Spectrometer Bias Command

4.1.8.5 Bolometer Bias Noise

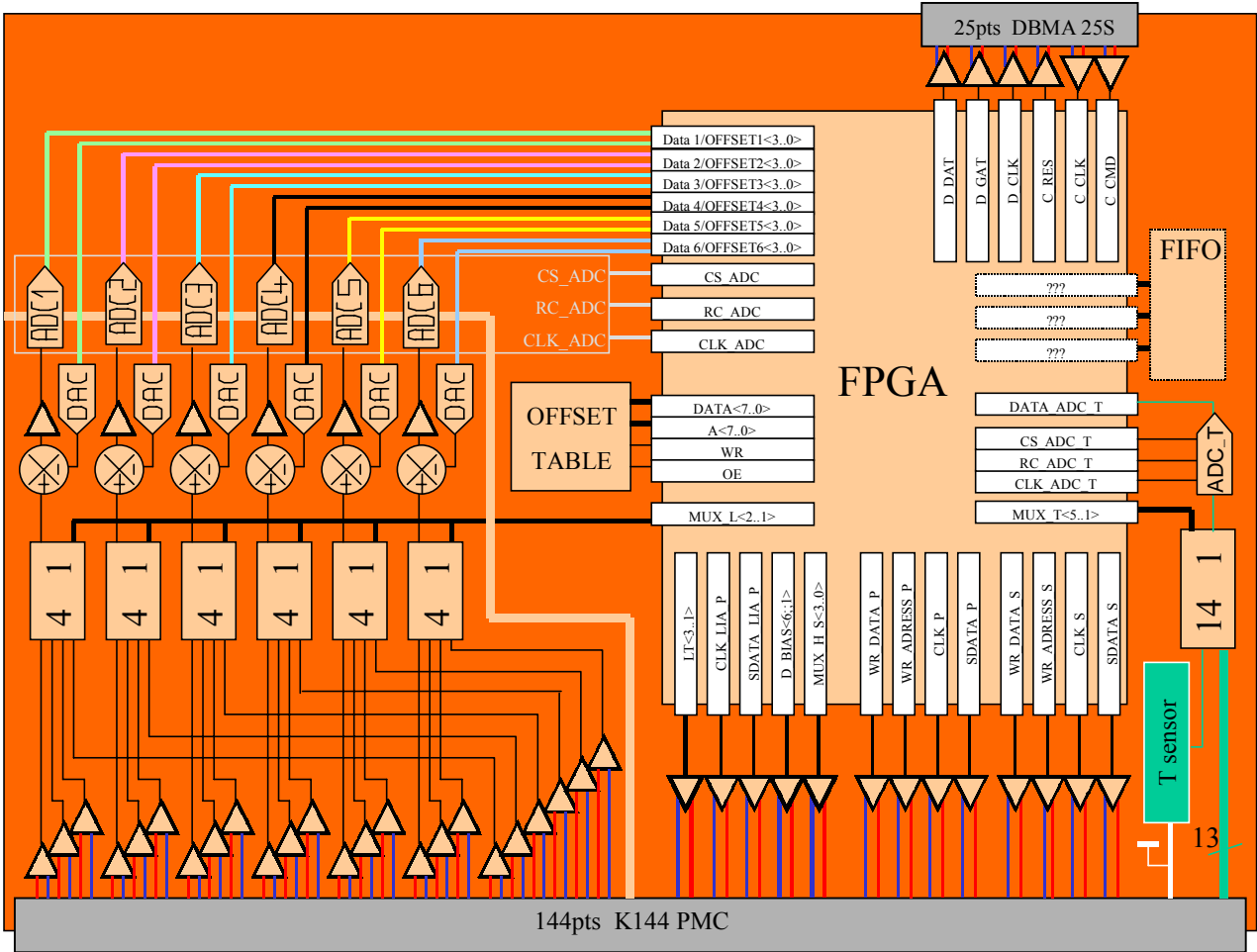
TBW

4.1.8.6 JFET BIAS Noise

TBW

4.1.9 DAQ+IF BOARD

4.1.9.1 DAQ+IF Board Overview



Picture 4-33 DAQ+IF Board Overview

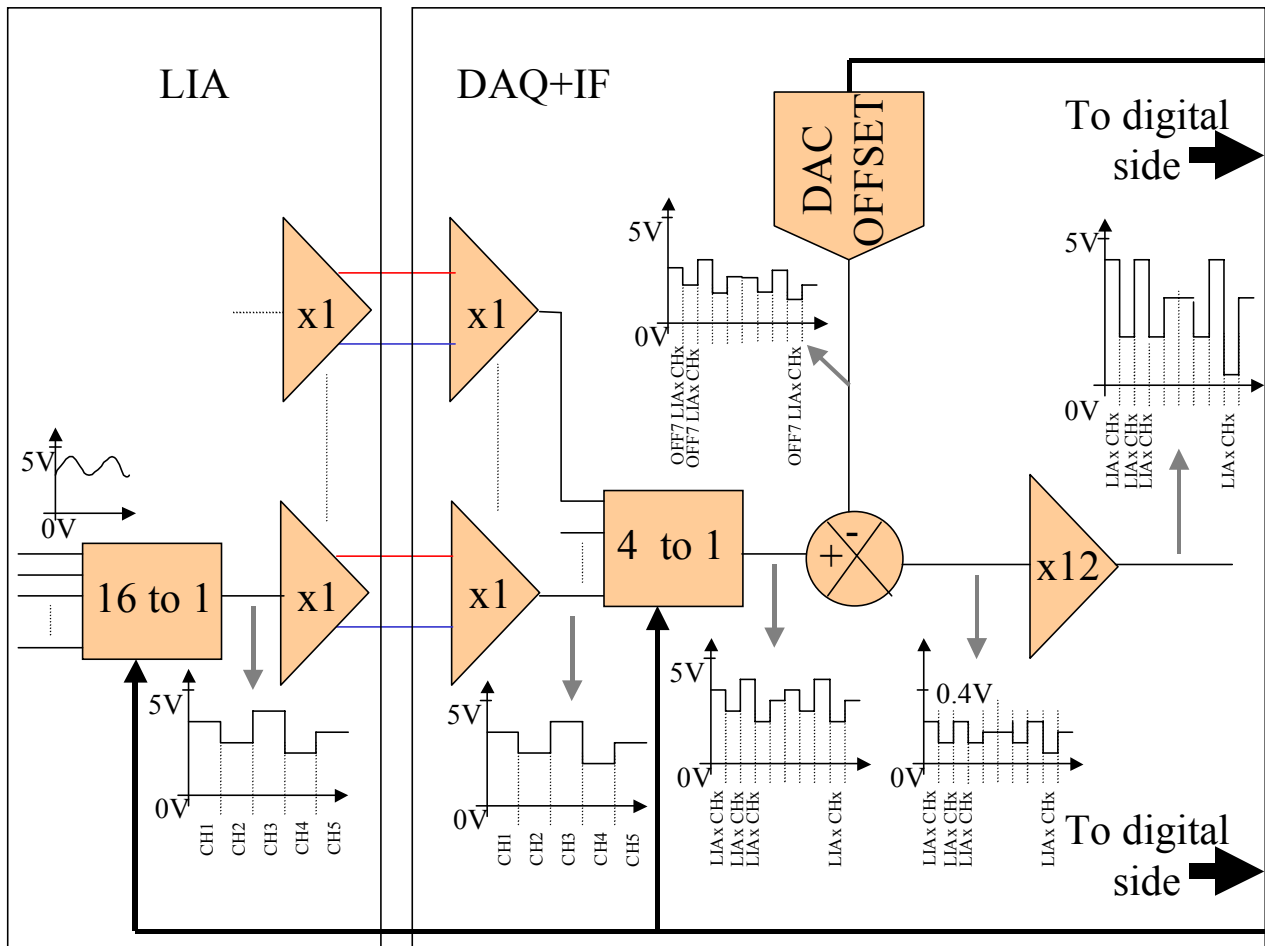
TBW

4.1.9.2 DAQ+IF Board Interface

TBW

4.1.10 DAQ+IF BOARD FUNCTIONS

4.1.10.1 LIA Channel Digitization Overview



Channel way to digitization:

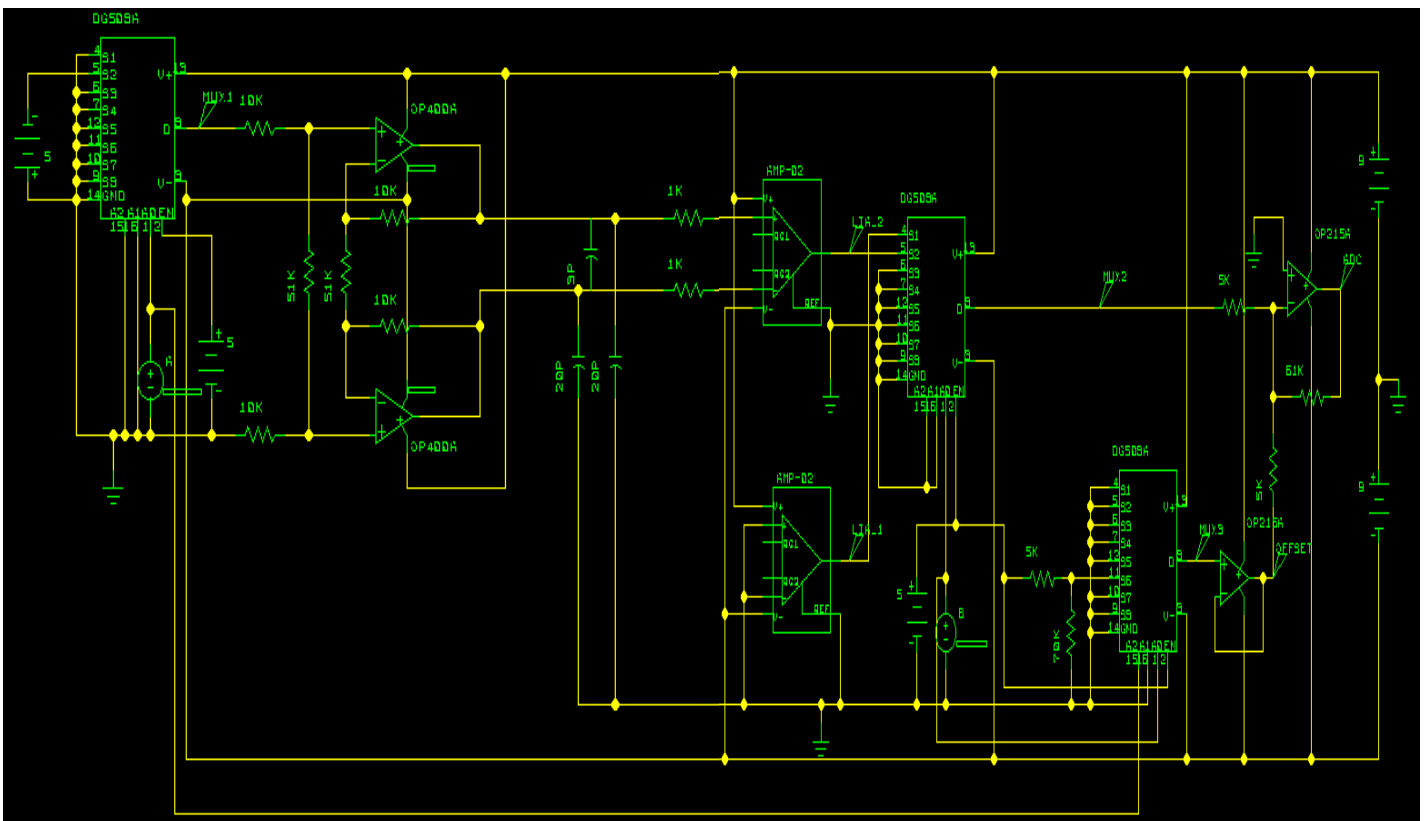
1. After the LIA_P (or LIA_S) channel processing, a bolometer signal is multiplexed with 15 (or 11) other bolometer signals on the same board.
2. Then the multiplexed signal goes out the LIA board through a differential amplifier with one unit gain.
3. The differential multiplexed signal goes into the DAQ+IF board through a differential receiver with one unit gain.
4. DAQ+IF board multiplexing stage:
 - If this multiplexed signal comes from the photometer it is then multiplexed with 2 other signals which come from 2 other LIA_P multiplexers. There are 48 photometer bolometer signals that are multiplexed.
 - If this multiplexed signal comes from the spectrometer then it goes straight through the multiplexer.
5. For each bolometer signal a predetermined offset signal is subtracted.
6. Afterwards, the signal is amplified by 12 and digitized.

4.1.10.2 Analog Receiver and Multiplexer

On a DAQ+IF board there are:

- 18 photometer analog receivers for the 18 LIA_P board output.
- 6 “Spectrometer” Analog receivers for the 6 LIA_S board output.
- 6 muxplexers
- Each multiplexer handles
 - o 1 spectrometer analog receiver output.
 - o 3 photometer analog receiver output.

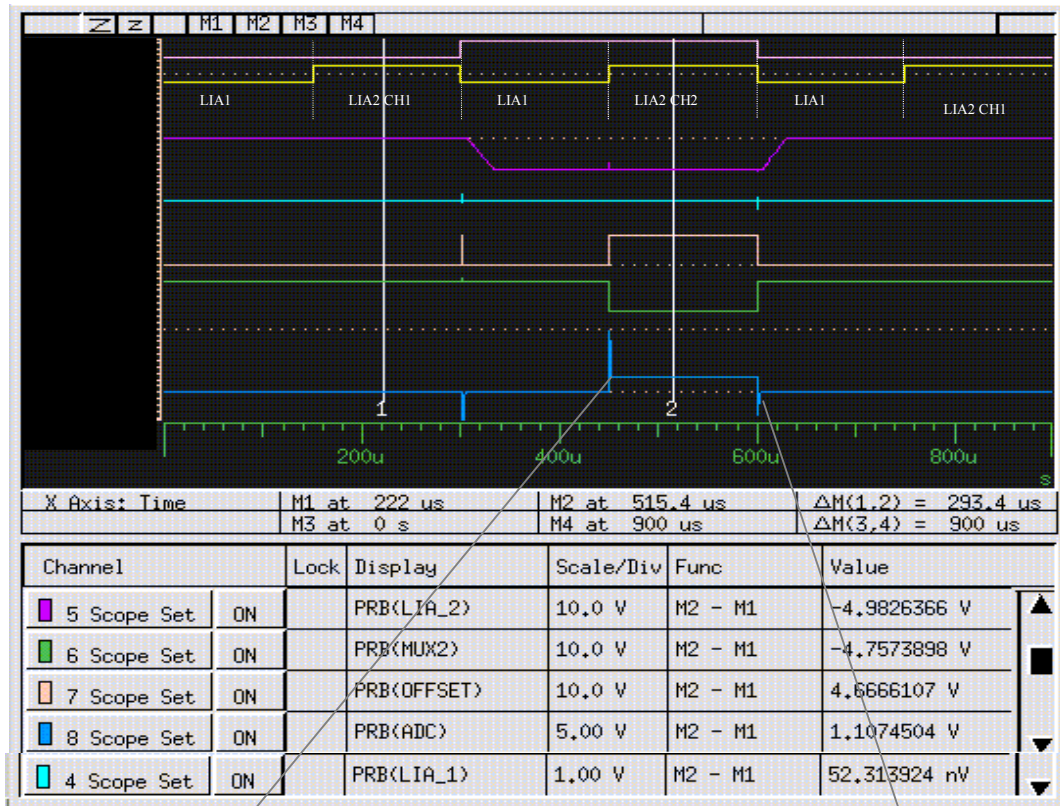
The following simulation circuit shows how to determine the maximum time that an input ADC signal needs to be stabilized after different kinds of multiplexer switching:



There is a small difference between the real design and the previous Channel Digitization Overview, however result is the same:

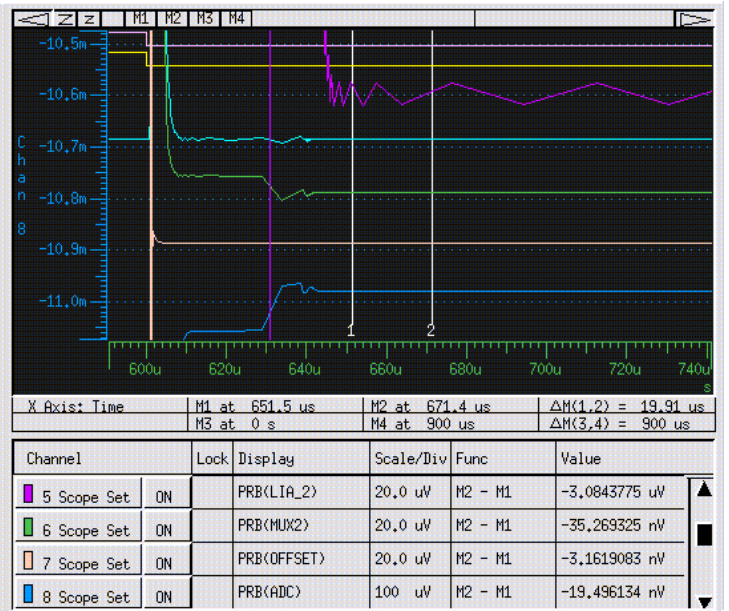
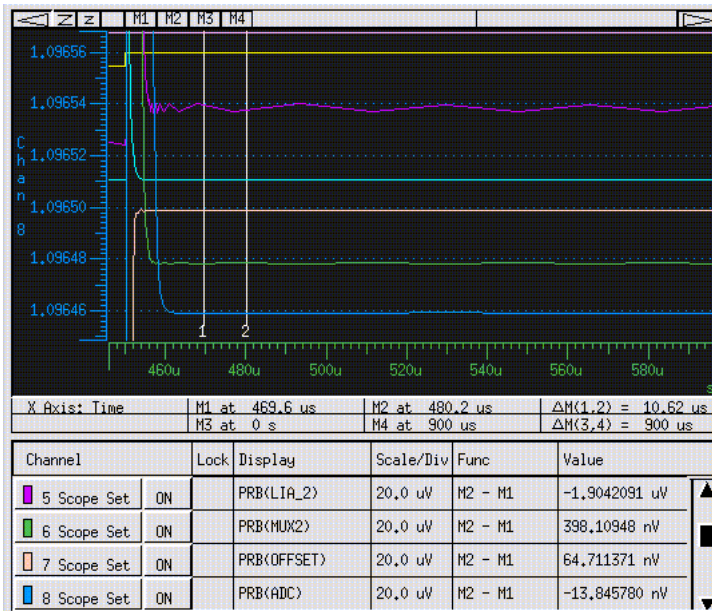
- In reality the output signal of a receiver is negative between 0v and -5V.
- After the DAQ Multiplexer, it is added to a positive offset between 0v and 5V and multiplied by a negative gain of -12.

So we have $(-\text{channel} + \text{offset}) \times (-12)$ which is equivalent to $(\text{channel} - \text{offset}) \times (12)$.



DETAIL N°1

DETAIL N°2

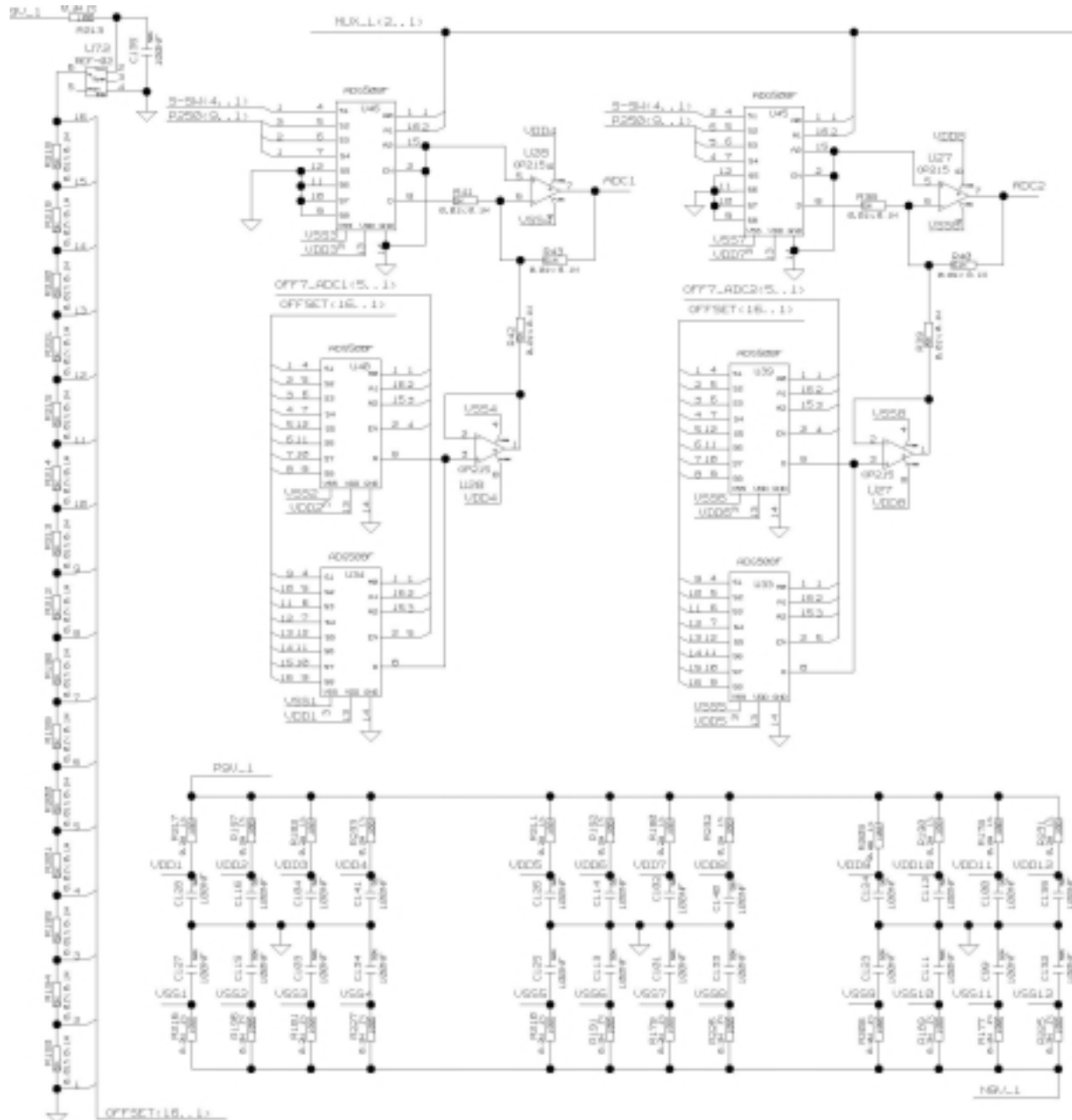


- When the LIA multiplexer and the DAQ multiplexer are switched at the same time, the ADC input signal is established and stabilized after 50 μ s. (DETAIL N°2)
- When only the DAQ multiplexer is switched. The ADC input signal is established and stabilized after 20 μ s. (DETAIL N°1)



4.1.10.3 Offset and Gain

After each multiplexer the channel signals that are going to be digitized are added with their 4-bit predetermined offset signal and the result is multiplied by -12 before to be digitized. Each ADC is associated to one offset generator and gain amplifier. 2 multiplexers with an OP as follower build the 4-bit offset generators.

See the following circuit:



Picture 4-34 Offset and Gain Circuit

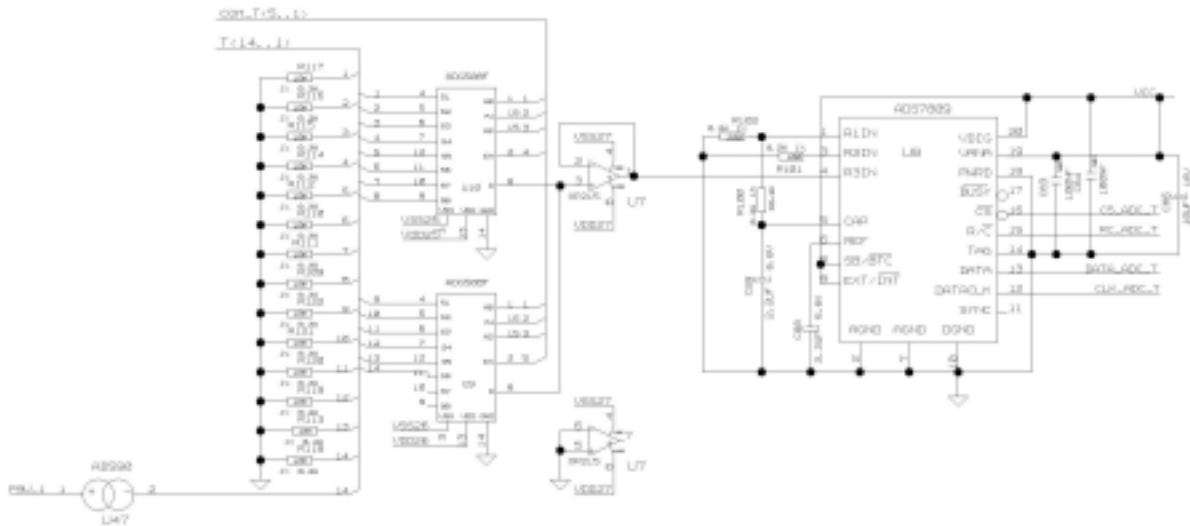
	<p>DCU Design document</p>	 <p>SAP-SPIRE- FP-0063-02 Issue: 0.2 Date : 05/07/02</p>
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4.1.10.4 ADC

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4.1.10.5 Boards Temperature Acquisition

See the following circuit:

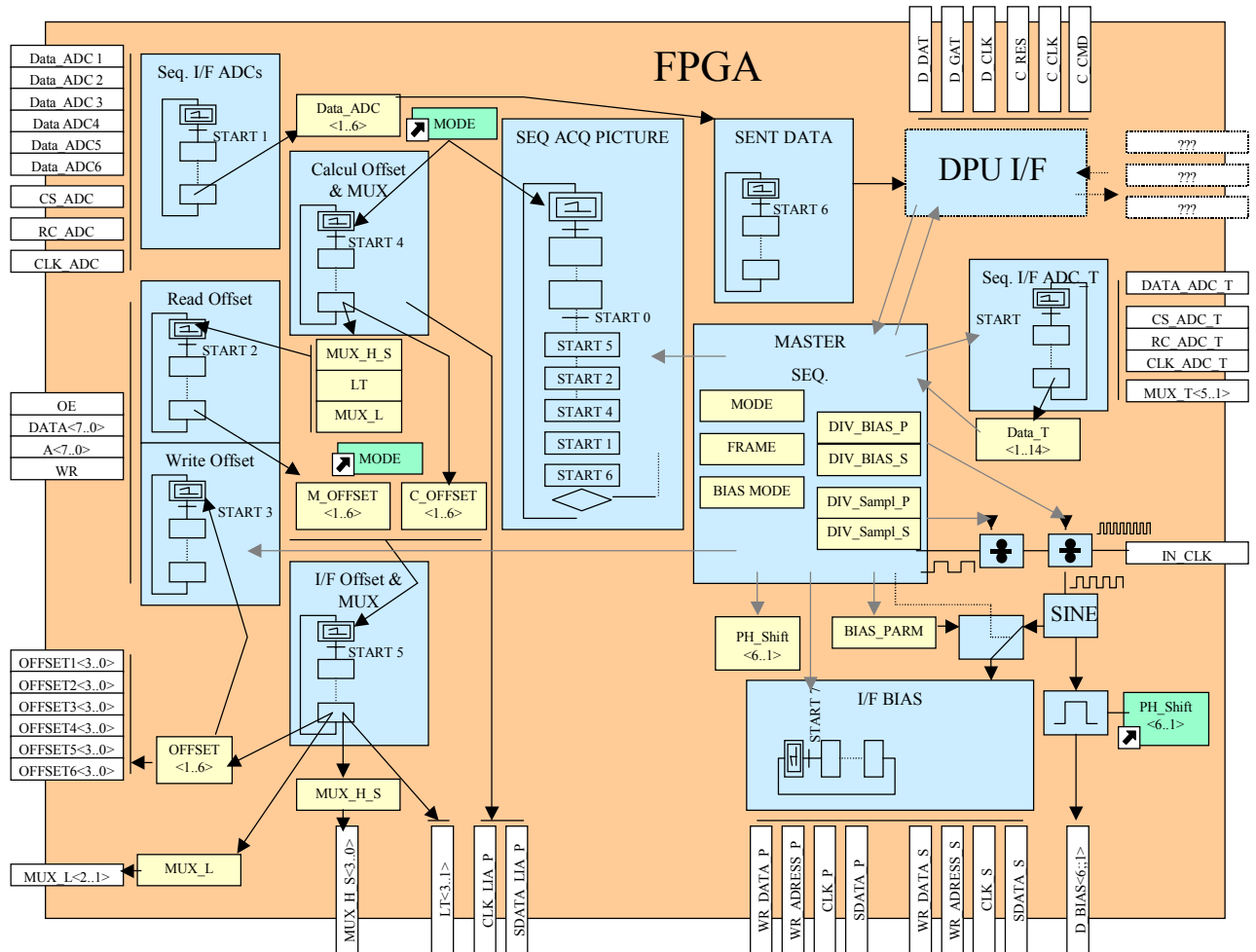


- COM_T selects the board temperature, that will to be digitized.
- The temperature range is -40°C to 80°C .
- The digitized signal voltage range is 2.33V to 3.61V.
- The ADC is 16-bit with a 0V to 5V input range.
- So, the voltage resolution is $76\mu\text{V}$.
- And the temperature resolution is 0.008°C .
- The 10 most significant bits give a resolution of 0.48°C

COM_T<5..1>					Board temperature
5	4	3	2	1	
0	1	0	0	0	BIAS
0	1	0	0	1	LIA S1
0	1	0	1	0	LIA S2
0	1	0	1	1	LIA S3
0	1	1	0	0	LIA P9
0	1	1	0	1	LIA P8
0	1	1	1	0	LIA P7
0	1	1	1	1	LIA P6
1	0	0	0	0	LIA P5
1	0	0	0	1	LIA P4
1	0	0	1	0	LIA P3
1	0	0	1	1	LIA P2
1	0	1	0	0	LIA P1
1	0	1	0	1	DAQ+IF

4.1.11 DAQ+IF FPGA

4.1.11.1 DAQ+IF FPGA Overview



Picture 4-35 DAQ+IF FPGA Overview

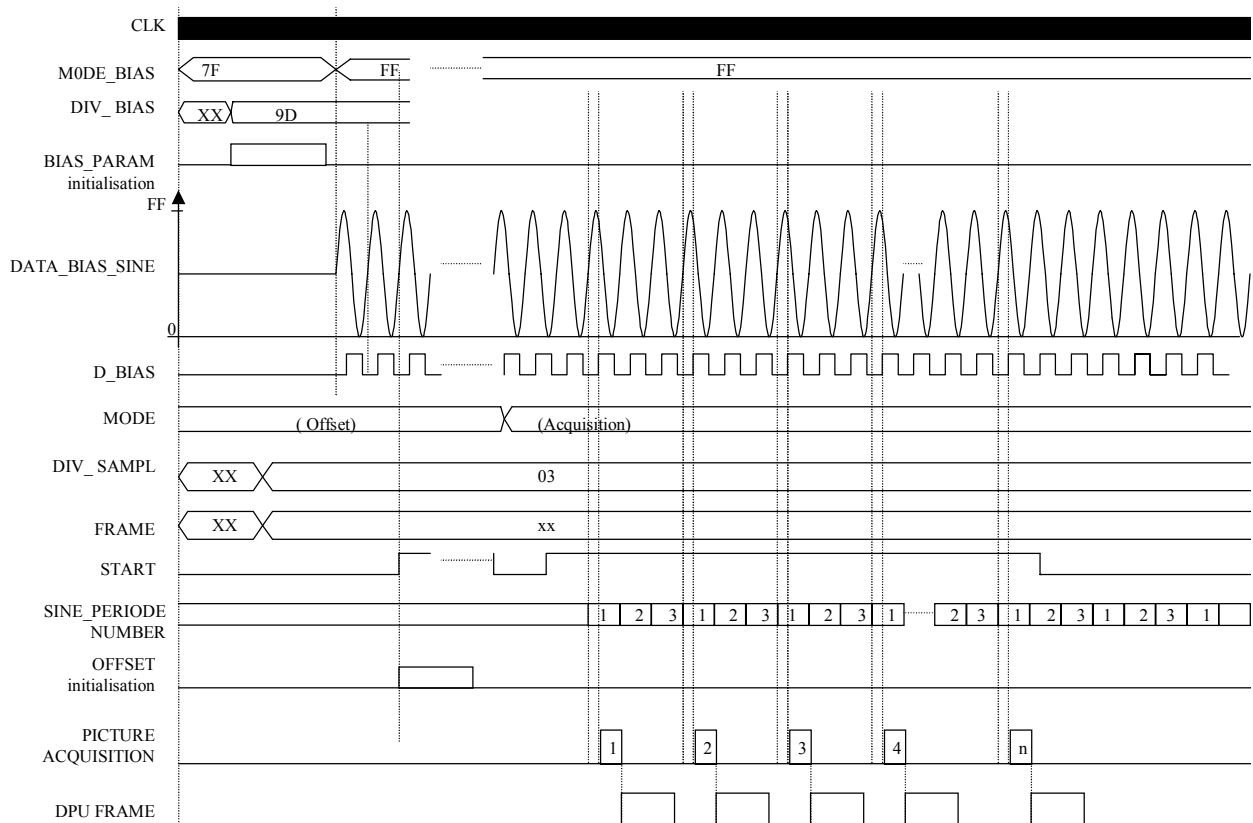
This FPGA is divided into 3 main parts:

- One handles the communication with the DPU (DPU I/F)
- One handles the command executions and the “high-level sequencer”(MATER SEQ)
 - o Bias generator management (Frequency, amplitude, demodulation signals phase shift...)
 - o Mode management (picture acquisition Number and frequency, Spectrometer or photometer mode, offset set up...)
 - o Board Temperature acquisition.
- The last one handles the sequencing of picture acquisition and the offset set up (SEQ ACQ PICTURE)

4.1.12 DAQ+IF FPGA FUNCTIONS

4.1.12.1 Mode Overview and Timing

This timing diagram shows how this instrument works:



1. Bias parameters are set (JFET power, heater, demodulation signal phase shift, bias frequency and Amplitude...) See detail in 4.1.12.4 Bias Control.
2. Then the sine bias signal starts.
3. The offsets are determined and memorized. See detail in 4.1.12.5 Offset.
4. After each x^* bias period a picture is digitized (PICTURE ACQUISITION) and sent to the DPU (DPU FRAME.) For the picture acquisition detail see 4.1.12.2 Channel Multiplexing and 4.1.12.3 Channel Acquisition
5. The acquisition stops when the start signal become low or in photometer mode when the programmed number of FRAME (between 1 and 255) has been acquired.

* x is determined by DIV_SAMPL

4.1.12.2 Channel Multiplexing

Spectrometer mode:

The following table shows the chronological sequence of the spectrometer's picture acquisition mode:

- The indicated times show when the digitization occurs. These times are given with reference to the beginning of the picture acquisition.
- The six ADCs work in parallel.
- The LIA_S MUX line specifies the LIA_S board's multiplexer positions at the digitization time.
- The DAQ+IF board multiplexer position is 0 during the spectrometer mode.
- The table shows for each ADC which board's channel is associated with each digitization time.

Time in ms		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
ADC1	channel	1	2	3	4	5	6	7	8	9	10	11	12
	Lia_s	1	1	1	1	1	1	1	1	1	1	1	1
ADC2	channel	13	14	15	16	17	18	19	20	21	22	23	24
	Lia_s	1	1	1	1	1	1	1	1	1	1	1	1
ADC3	channel	1	2	3	4	5	6	7	8	9	10	11	12
	Lia_s	2	2	2	2	2	2	2	2	2	2	2	2
ADC4	channel	13	14	15	16	17	18	19	20	21	22	23	24
	Lia_s	2	2	2	2	2	2	2	2	2	2	2	2
ADC5	channel	1	2	3	4	5	6	7	8	9	10	11	12
	Lia_s	3	3	3	3	3	3	3	3	3	3	3	3
ADC6	channel	13	14	15	16	17	18	19	20	21	22	23	24
	Lia_s	3	3	3	3	3	3	3	3	3	3	3	3
LIA S	MUX	0	1	2	3	4	5	6	7	8	9	10	11
DAQ	MUX	0	0	0	0	0	0	0	0	0	0	0	0

Photometer mode:

The following tables show the chronological sequence of the photometer's picture acquisition mode:

- The times point out digitization times. These times are given with reference to the beginning of the picture acquisition.
- The six ADCs work in parallel.
- The LIA_P MUX specifies multiplexer positions at the digitization time
- The DAQ MUX specifies DAQ+IF board's multiplexer positions at the digitization time.
- The table shows for each ADC which board's channel of which is associated with each digitization time.

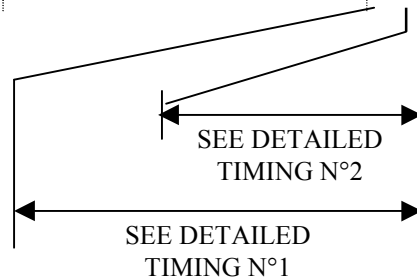
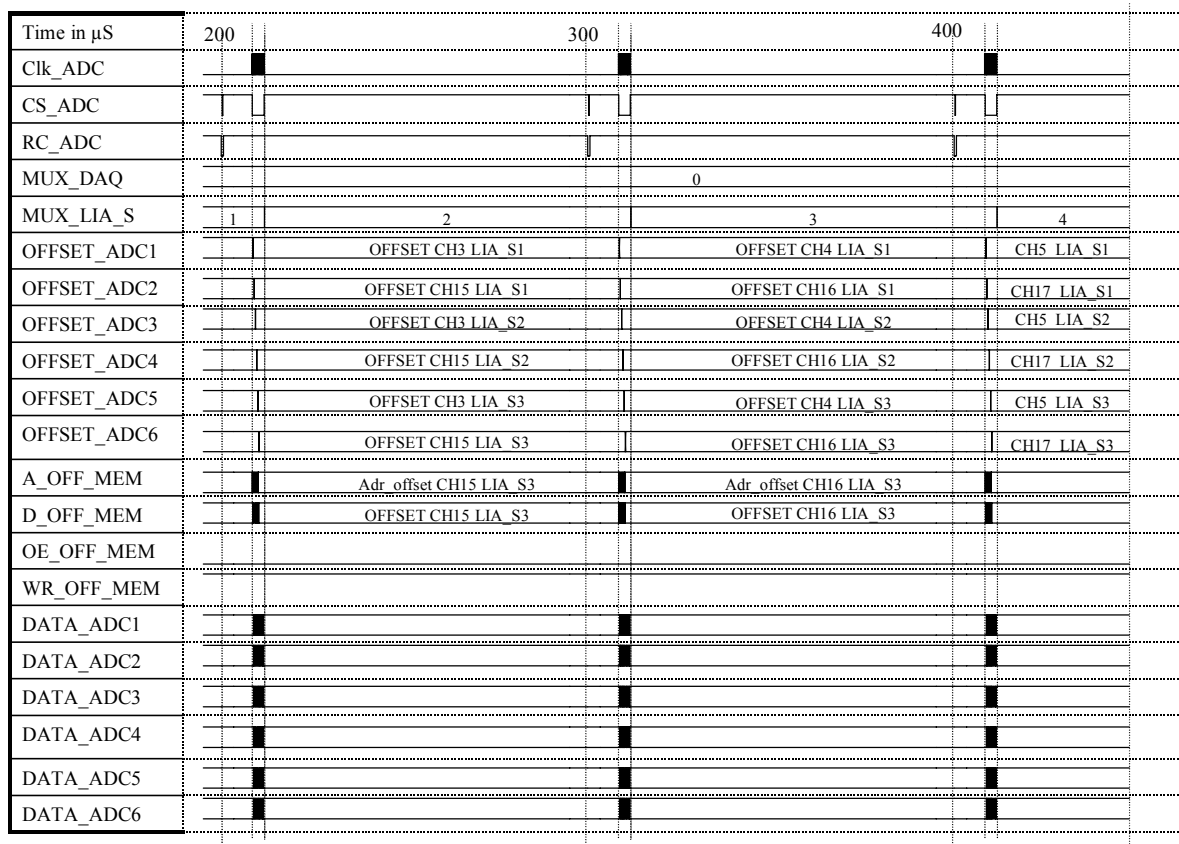
Time in ms		0.15	0.25	0.35	0.5	0.6	0.7	0.85	0.95	1.05	1.3	1.4	1.5	1.65	1.75	1.85	2
ADC1	channel	1	17	1	2	18	2	3	19	3	4	20	4	5	21	5	6
	Lia p	1	1	2	1	1	2	1	1	2	1	1	2	1	1	2	1
ADC2	channel	17	1	17	18	2	18	19	3	19	20	4	20	21	5	21	22
	Lia p	2	3	3	2	3	3	2	3	3	2	3	3	2	3	3	2
ADC3	channel	1	17	1	2	18	2	3	19	3	4	20	4	5	21	5	6
	Lia p	4	4	5	4	4	5	4	4	5	4	4	5	4	4	5	4
ADC4	channel	17	1	17	18	2	18	19	3	19	20	4	20	21	5	21	22
	Lia p	5	6	6	5	6	6	5	6	6	5	6	6	5	6	6	5
ADC5	channel	1	17	1	2	18	2	3	19	3	4	20	4	5	21	5	6
	Lia p	7	7	8	7	7	8	7	7	8	7	7	8	7	7	8	7
ADC6	channel	17	1	17	18	2	18	19	3	19	20	4	20	21	5	21	22
	Lia p	8	9	9	8	9	9	8	9	9	8	9	9	8	9	9	8
LIA P	MUX	0	0	0	1	1	1	2	2	2	3	3	3	4	4	4	5
DAQ	MUX	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1

Time in ms		2.1	2.2	2.35	2.45	2.55	2.7	2.8	2.9	3.05	3.15	3.25	3.4	3.5	3.6	3.75	3.85
ADC1	channel	22	6	7	23	7	8	24	8	9	25	9	10	26	10	11	27
	Lia p	1	2	1	1	2	1	1	2	1	1	2	1	1	2	1	1
ADC2	channel	6	22	23	7	23	24	8	24	25	9	25	26	10	26	27	11
	Lia p	3	3	2	3	3	2	3	3	2	3	3	2	3	3	2	3
ADC3	channel	22	6	7	23	7	8	24	8	9	25	9	10	26	10	11	27
	Lia p	4	5	4	4	5	4	4	5	4	4	5	4	4	5	4	4
ADC4	channel	6	22	23	7	23	24	8	24	25	9	25	26	10	26	27	11
	Lia p	6	6	5	6	6	5	6	6	5	6	6	5	6	6	5	6
ADC5	channel	22	6	7	23	7	8	24	8	9	25	9	10	26	10	11	27
	Lia p	7	8	7	7	8	7	7	8	7	7	8	7	7	8	7	7
ADC6	channel	6	22	23	7	23	24	8	24	25	9	25	26	10	26	27	11
	Lia p	9	9	8	9	9	8	9	9	8	9	9	8	9	9	8	9
LIA P	MUX	5	5	6	6	6	7	7	7	8	8	8	9	9	9	10	10
DAQ	MUX	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2

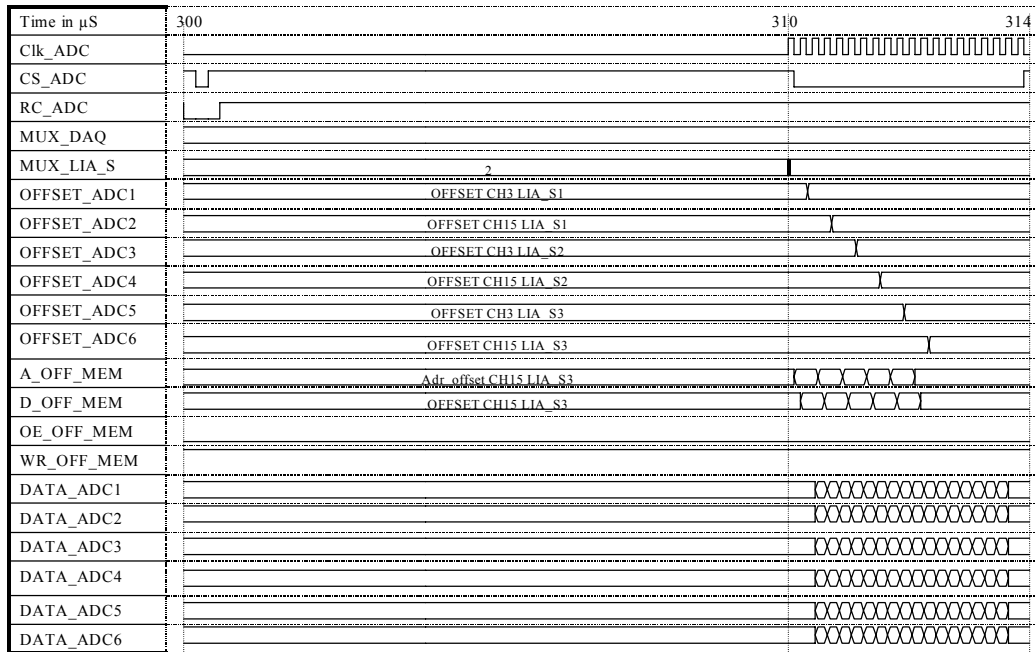
Time in ms		3.95	4.1	4.2	4.3	4.45	4.55	4.65	4.8	4.9	5	5.15	5.25	5.35	5.5	5.6	5.7
ADC1	channel	11	12	28	12	13	29	13	14	30	14	15	31	15	16	32	16
	Lia p	2	1	1	2	1	1	2	1	1	2	1	1	2	1	1	2
ADC2	channel	27	28	12	28	29	13	29	30	14	30	31	15	31	32	16	32
	Lia p	3	2	3	3	2	3	3	2	3	3	2	3	3	2	3	3
ADC3	channel	11	12	28	12	13	29	13	14	30	14	15	31	15	16	32	16
	Lia p	5	4	4	5	4	4	5	4	4	5	4	4	5	4	4	5
ADC4	channel	27	28	12	28	29	13	29	30	14	30	31	15	31	32	16	32
	Lia p	6	5	6	6	5	6	6	5	6	6	5	6	6	5	6	6
ADC5	channel	11	12	28	12	13	29	13	14	30	14	15	31	15	16	32	16
	Lia p	8	7	7	8	7	7	8	7	7	8	7	7	8	7	7	8
ADC6	channel	27	28	12	28	29	13	29	30	14	30	31	15	31	32	16	32
	Lia p	9	8	9	9	8	9	9	8	9	9	8	9	9	8	9	9
LIA P	MUX 3	10	11	11	11	12	12	12	13	13	13	14	14	14	15	15	15
DAQ	MUX	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3

4.1.12.3 Channel Acquisition

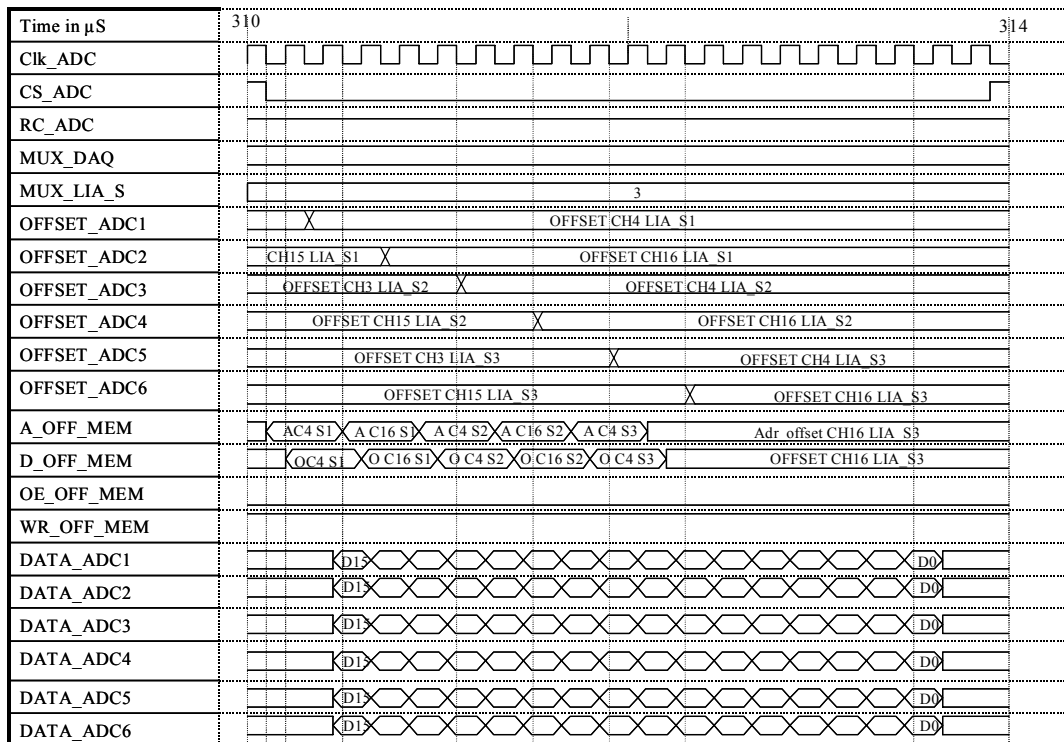
Spectrometer Mode Digitization Timing Diagram:



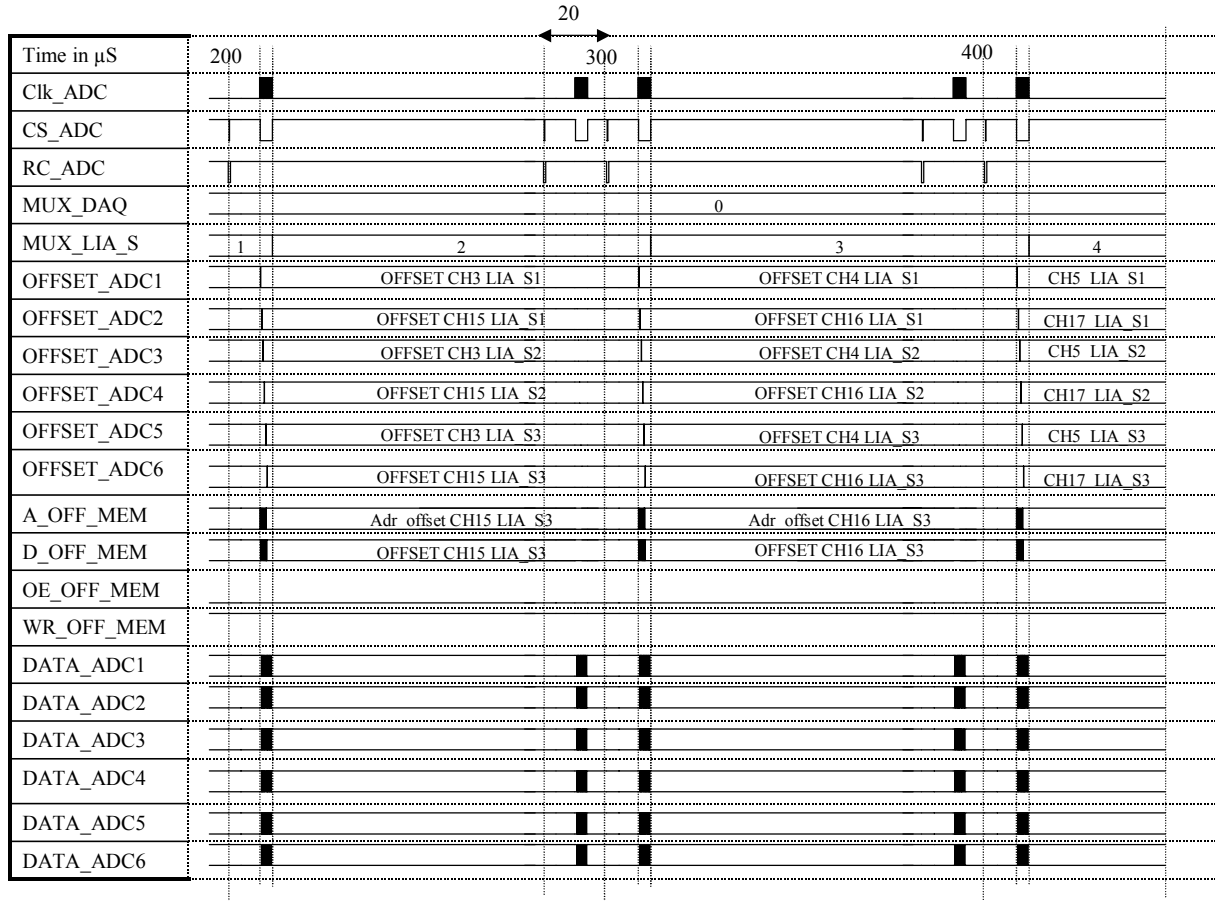
DETAILED TIMING N°1



DETAILED TIMING N°2



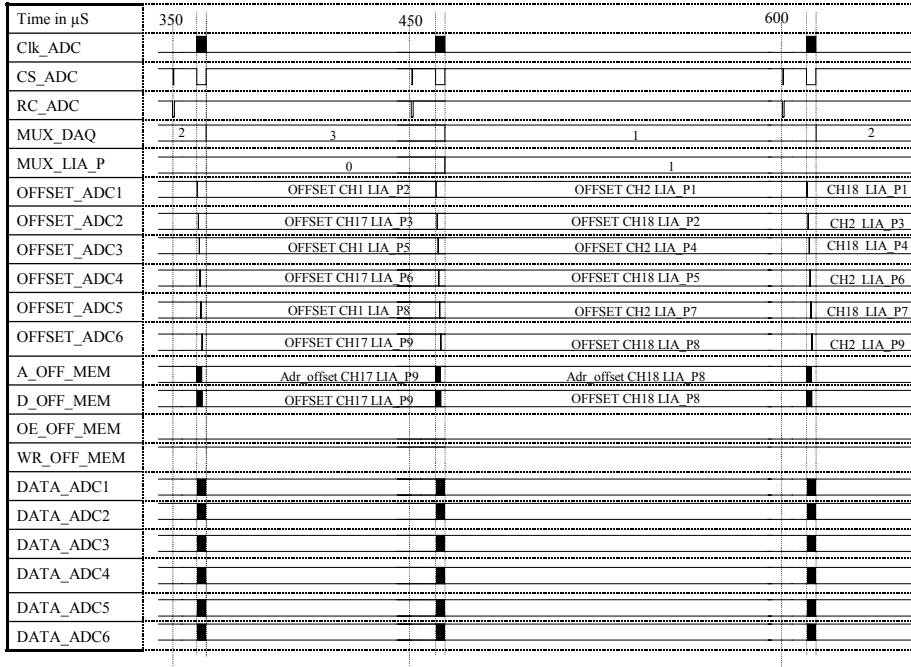
Spectrometer Mode Digitization Timing Diagram for the over sampling option:



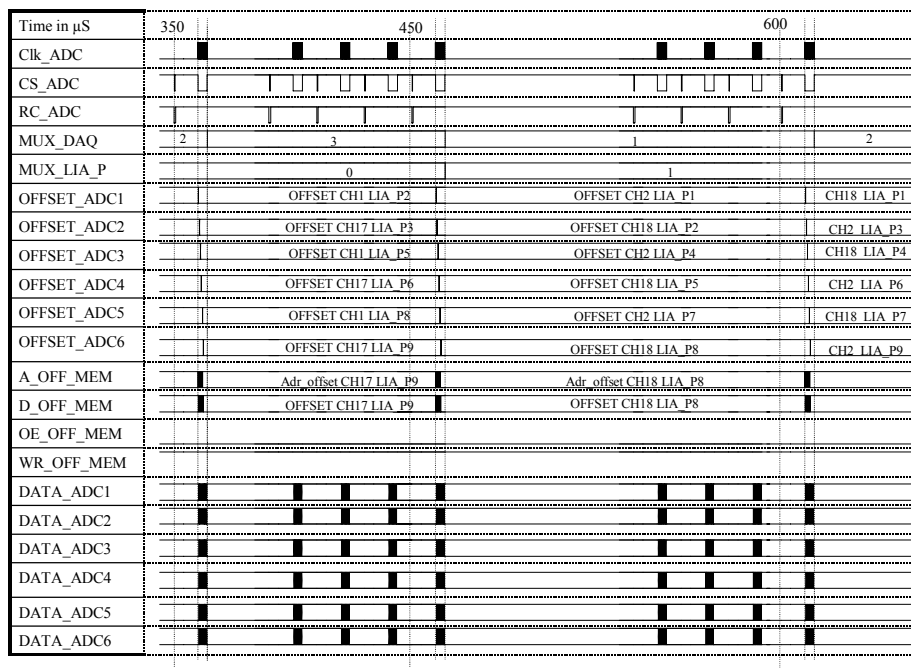
For each channel it is possible have 2 samples. A channel values of a will be the average of its 2 samples.

We will choose whether or not to implement this option after the QM1 test. At that point, the number of samples will be set and won't be able to be changed!!!

Photometer Mode Digitization Timing Diagram:



Photometer mode Digitization Timing Diagram for over sampling option:



For each channel, it is possible have 4 (or 2) samples. A channel values of a will be the average of its 4 (or 2) samples.

We will choose whether or not to implement this option after the QM1 test. At that point, the number of samples will be set and won't be able to be changed!!!

4.1.12.4 Bias Control

SINE BIAS generator:

The CLK_BIAS is the sine bias clock. This clock is determined by dividing the master clock's CLK_IN frequency by the parameter DIV_BIAS_PHOTO (or DIV_BIAS_SPECTRO.)

- 256 of this clock periods equal one sine period.

To write the Sine bias data on one of the BIAS board sine bias generator:

- All 32 (or 16) CS and ON/OFF positions are sent through a serial link (see BIAS § 4.1.8.4 Commands)
- For each the clock 256 periods a sine data is written in a sine bias generator.

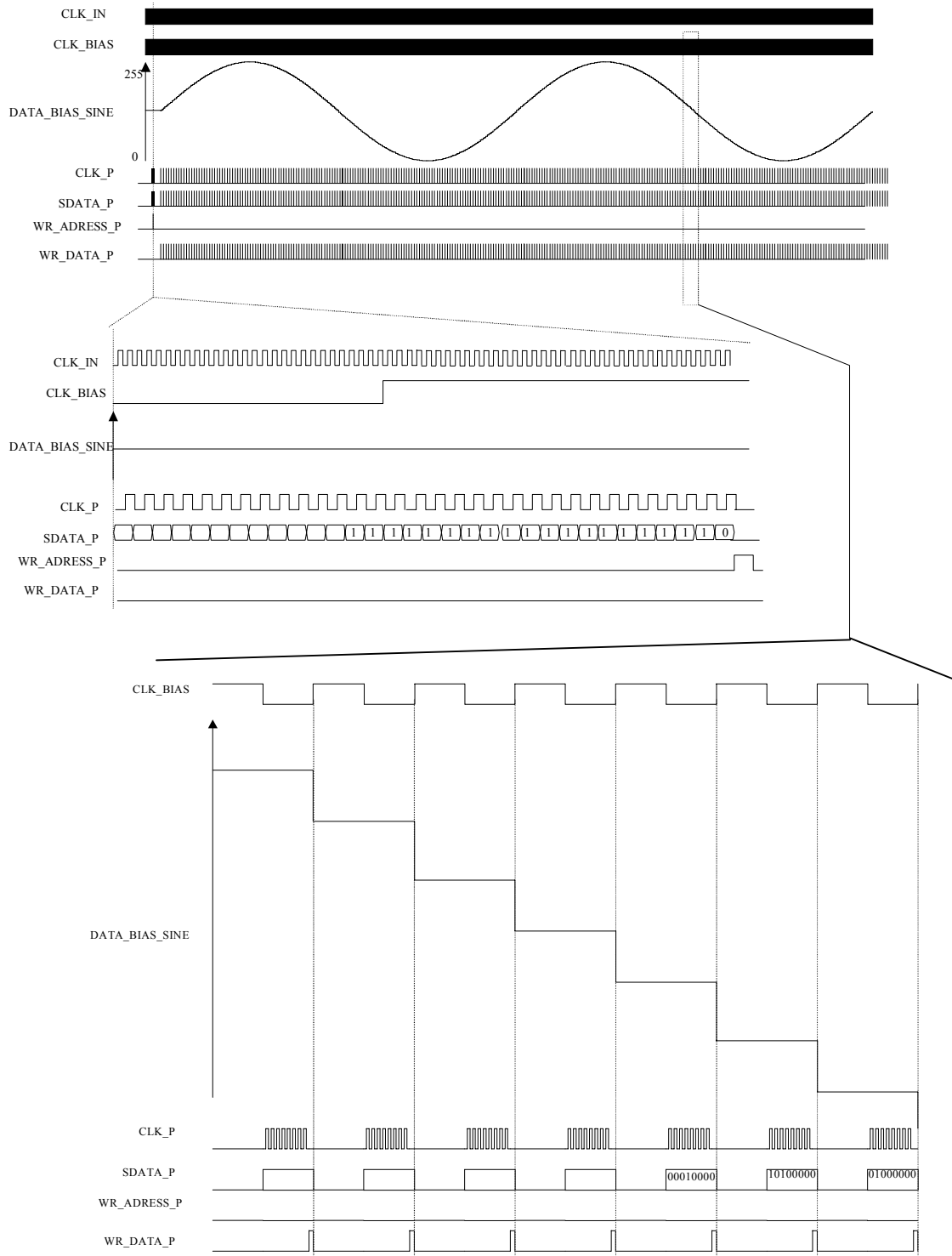
See next timing diagram

Demodulation signals:

TBW

BIAS parameter:

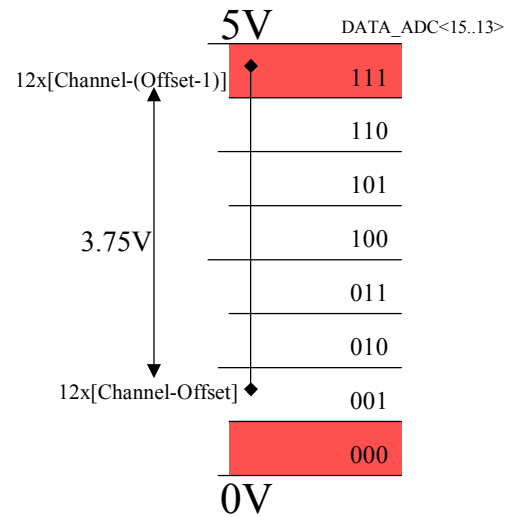
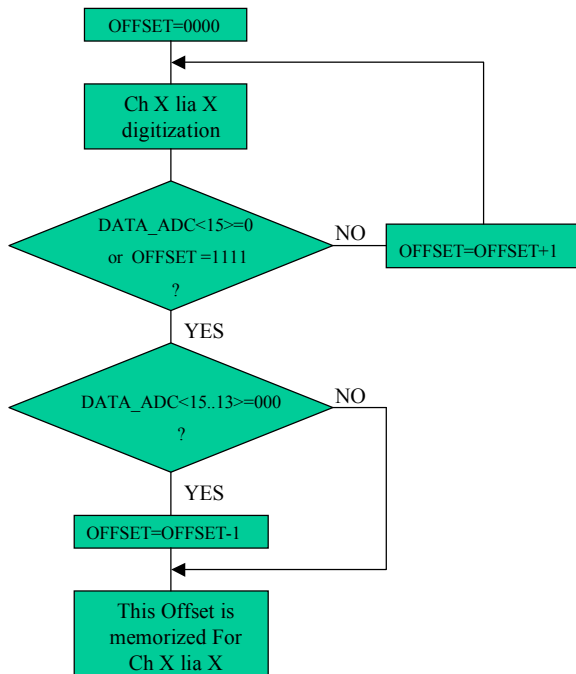
TBW





4.1.12.5 Offset

For each channel, the following algorithm determines its offset:

Offset Calculation for Ch X lia X



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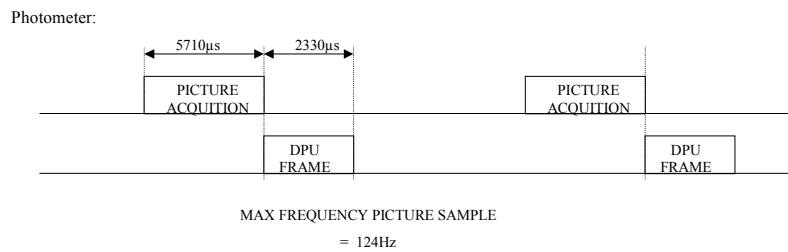
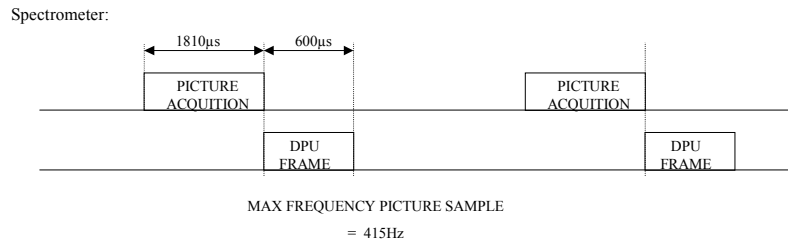
4.1.12.6 Command

See DCU/DRCU ICD

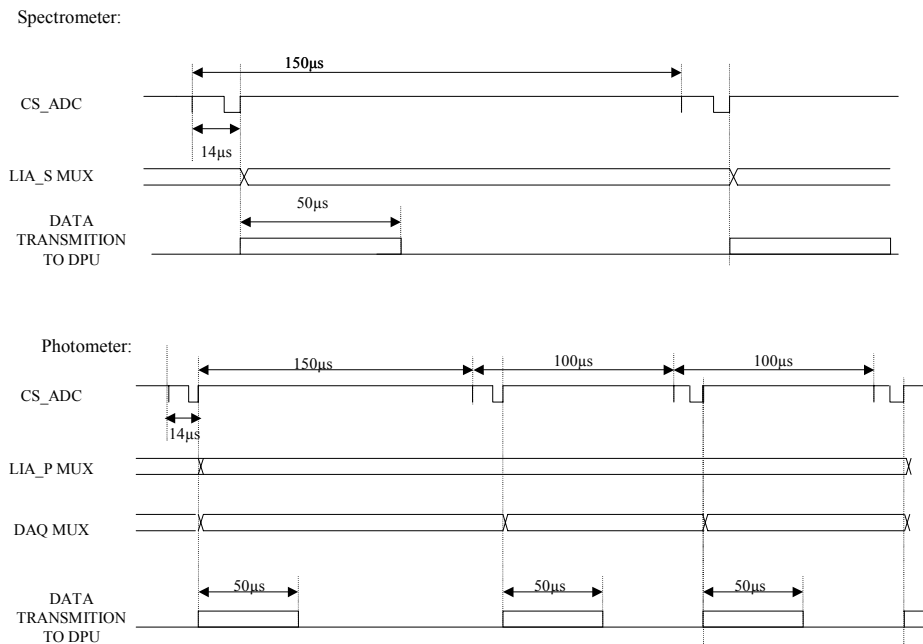
TBW

4.1.12.7 Data Transmission

1. With a FIFO the data are transmitted to the DPU through a serial link at 2Mb/s after a complete PICTURE AQUISION

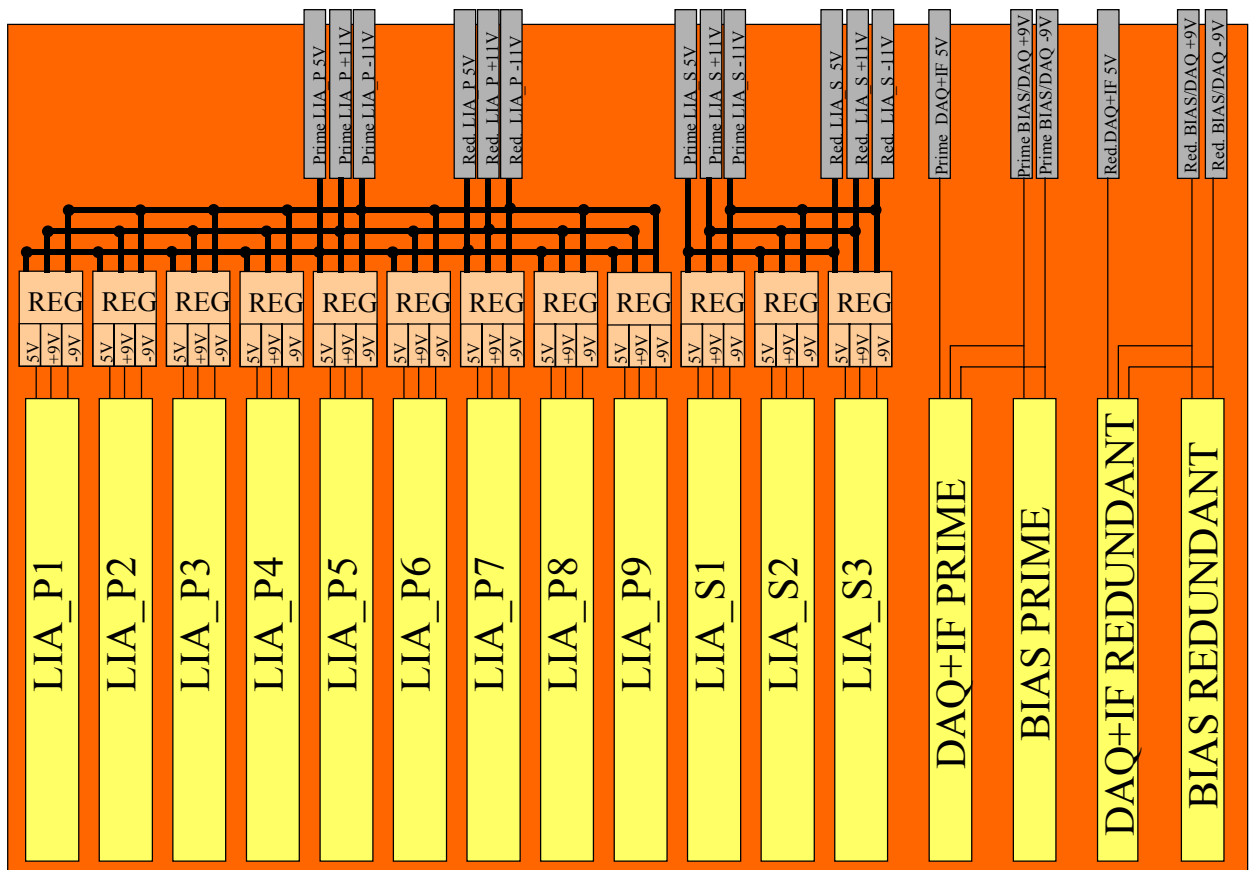


2. Without a FIFO data are transmitted to the DPU through a serial link at 2Mb/s after ADC digitization; this case, the over sample option is not possible.



4.2 DCU Power Supply

4.2.1 DCU POWER SUPPLY OVERVIEW

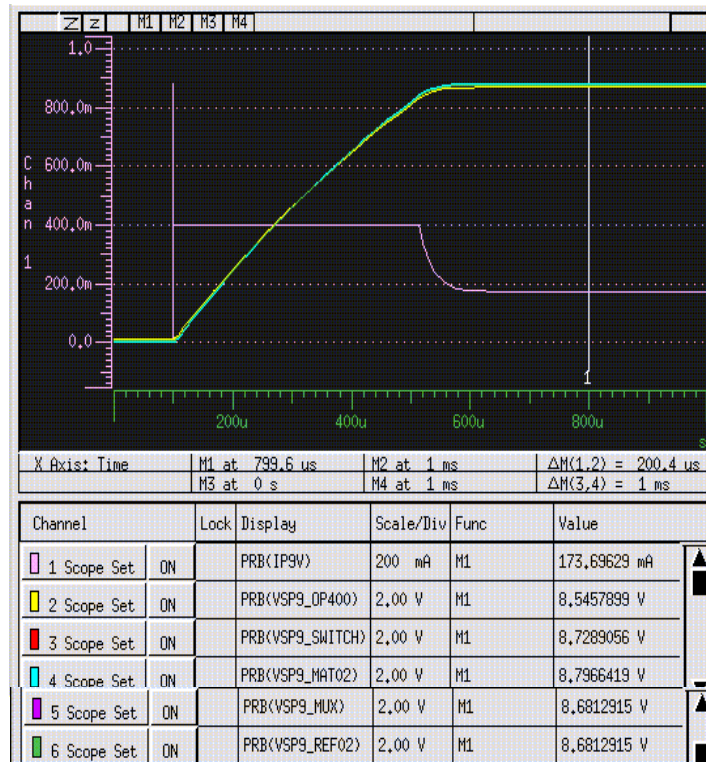
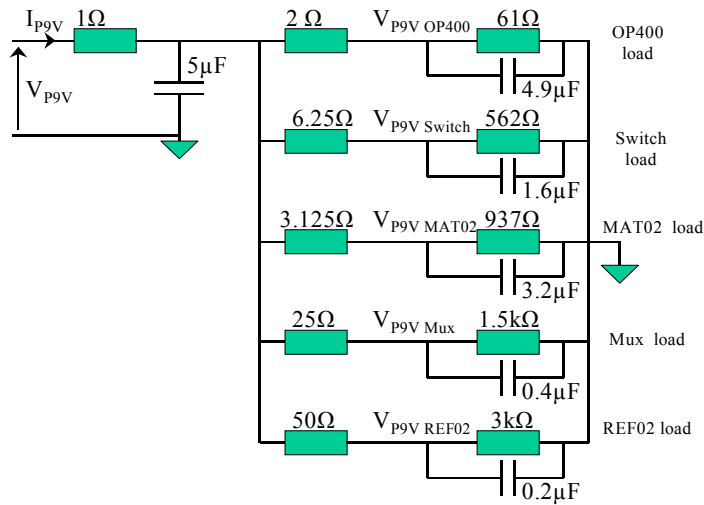


4.2.2 LIA PHOTOMETER POWER SUPPLY

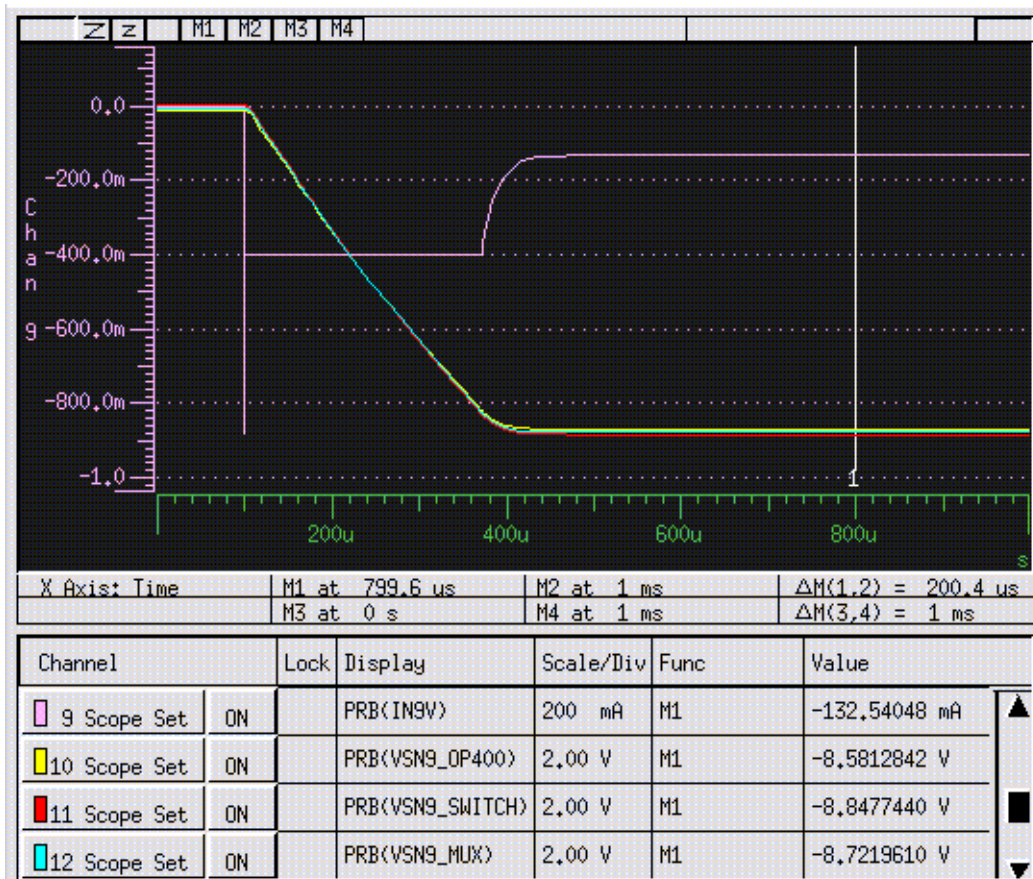
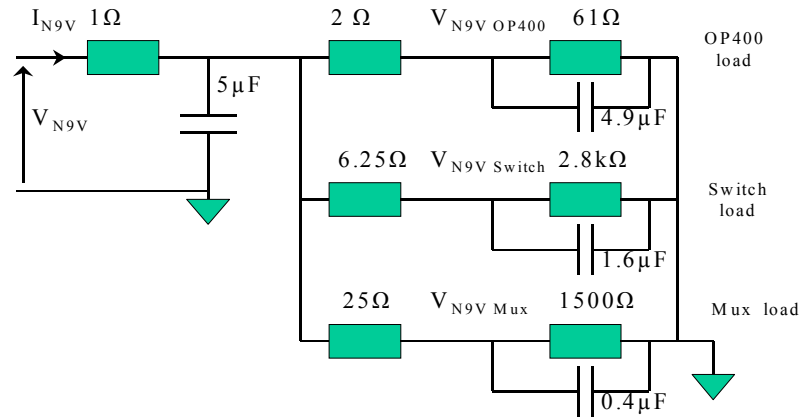
4.2.2.1 LIA Photometer Board Power Supply

A LIA board receives 3 different power supply line 5V,-9V and +9V. All regulators used to supply LIA boards have a limited electric current of 400mA.

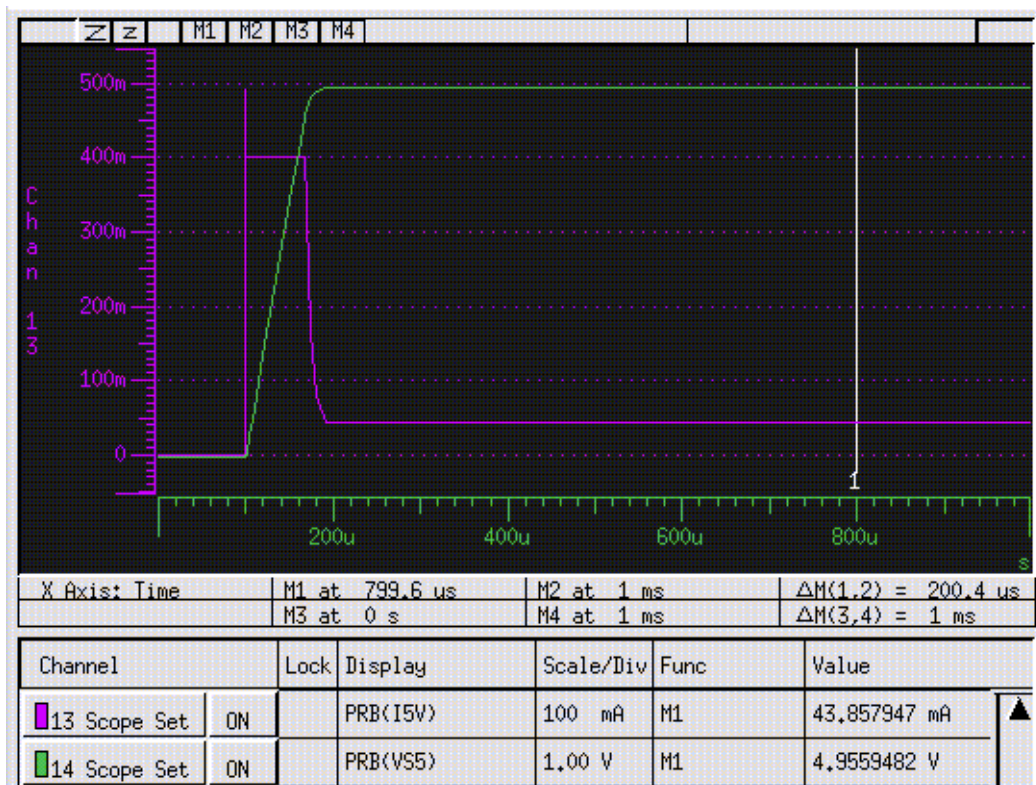
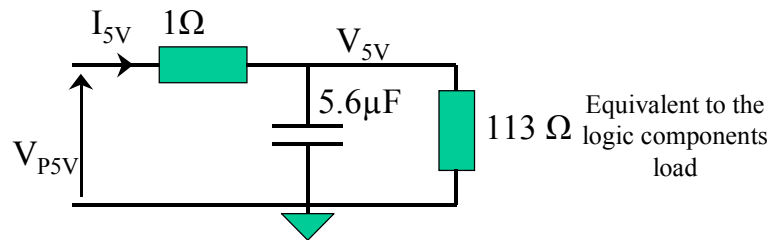
The following circuit is a simplified model of the LIA Photometer board seen from the +9V power supply line. The current is nominal around 175mA less than 1ms. See the following simulation result.



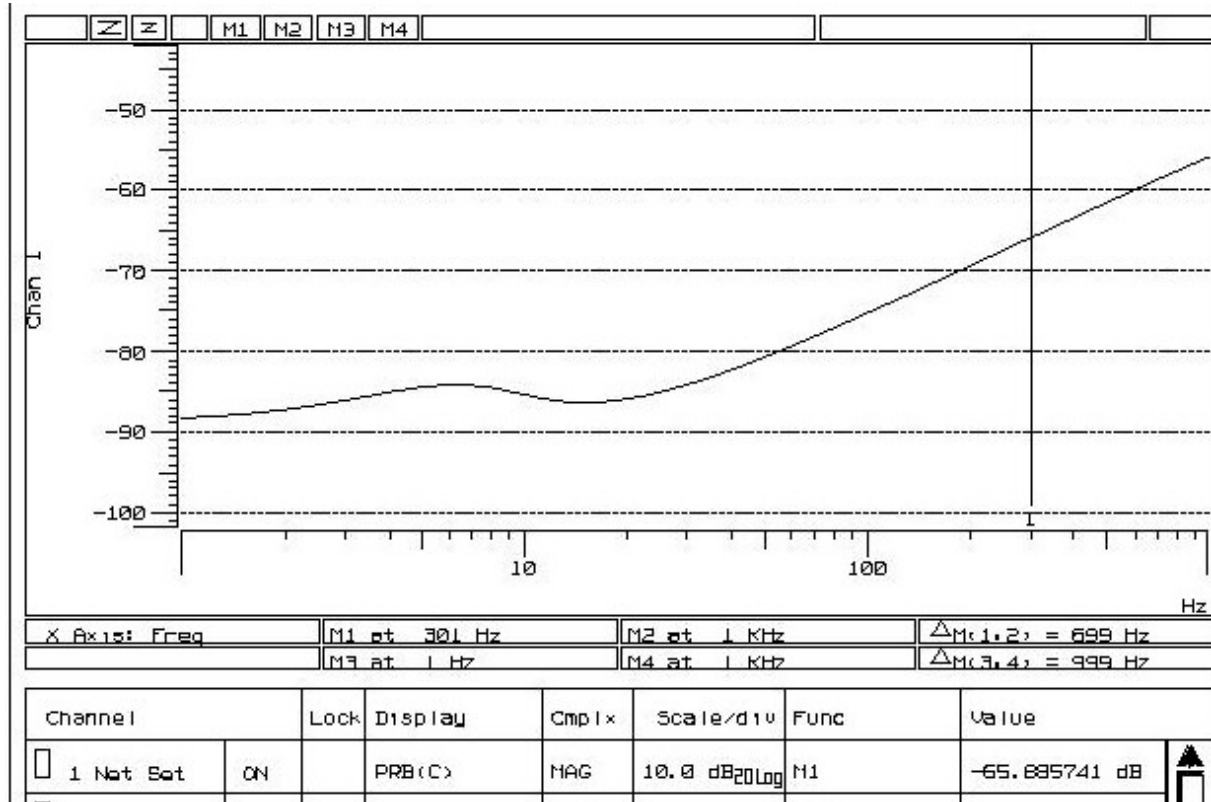
The following circuit is a simplified model of the LIA Photometer board seen from the -9V power supply line. The current is nominal around -150mA after less than 1ms. See the following simulation result.



The following circuit is a simplified model of the LIA Photometer board seen from the 5V power supply line. The current is nominal around 45mA after less than 1ms. See the following simulation result.



Power Supply Rejection Ratio:

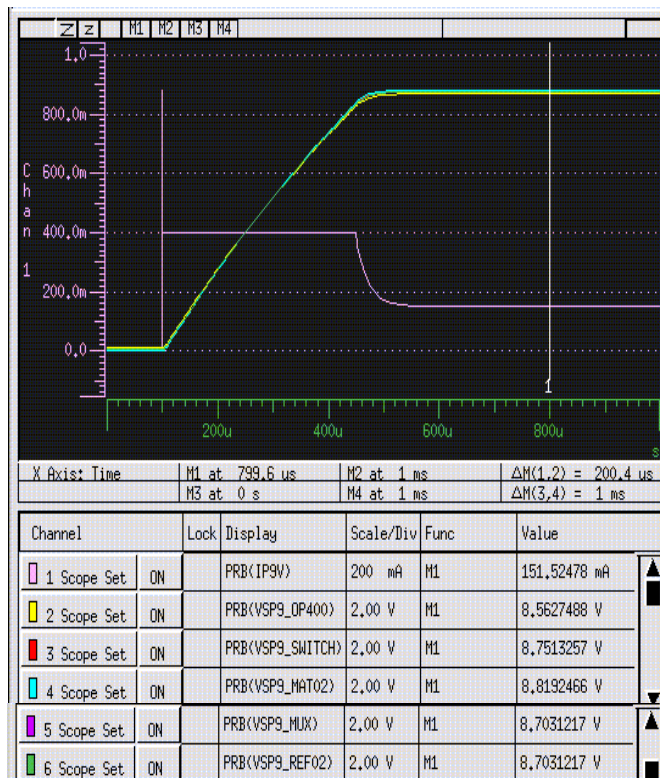
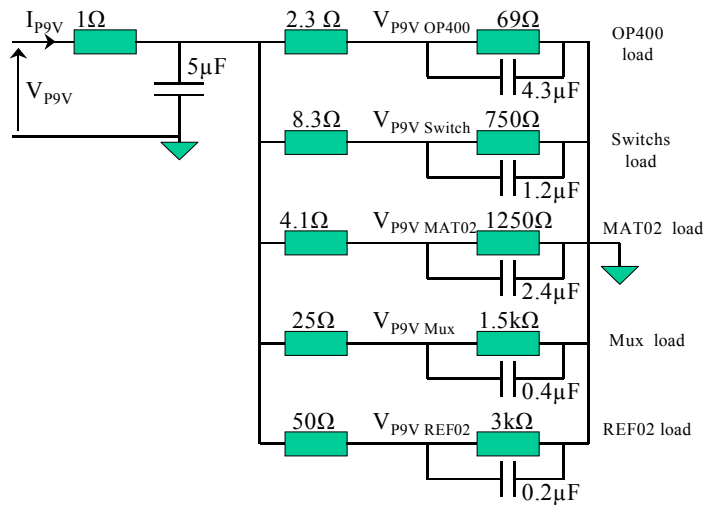


TBW

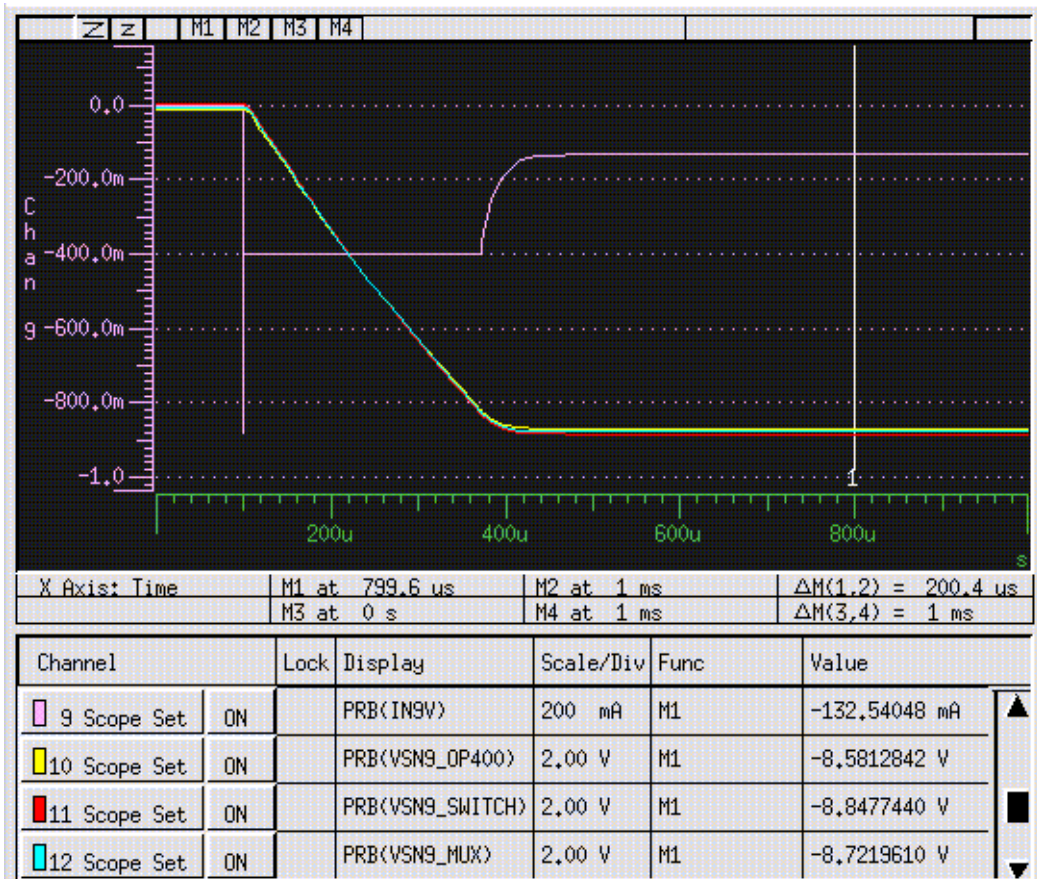
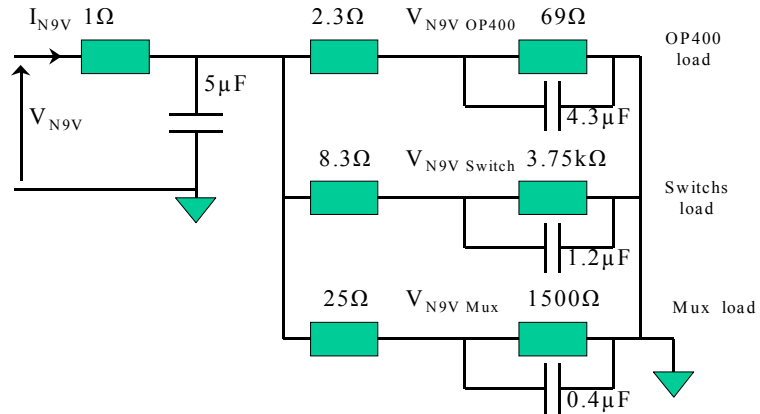
4.2.2.2 LIA Spectrometer Board Power Supply

A LIA board receives 3 different power supply line 5V,-9V and +9V. All regulators used to supply LIA boards have a limited electric current of 400mA.

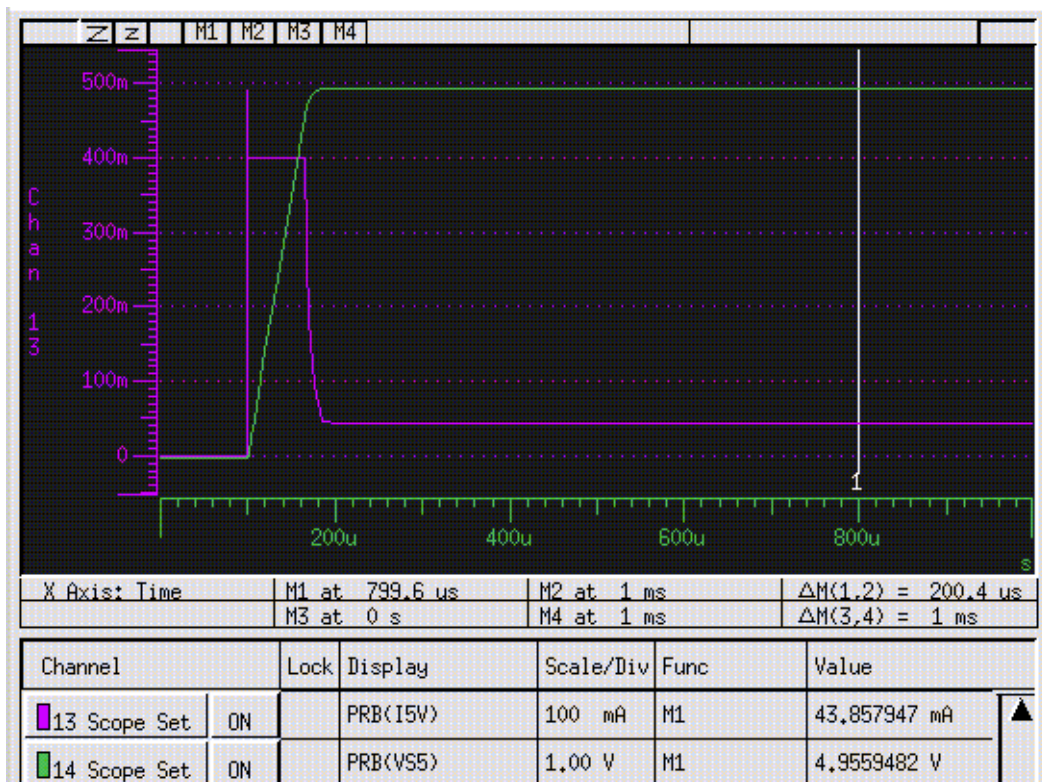
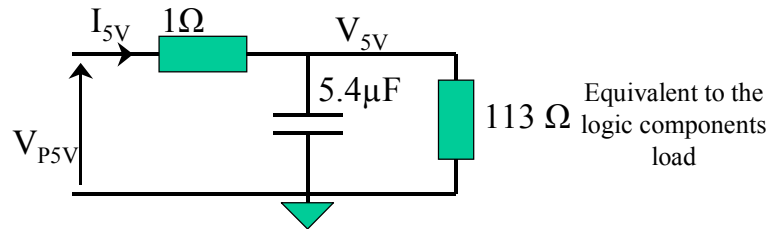
The following circuit is a simplified model of the LIA Spectrometer board seen from the +9V power supply line. The current is nominal around 155mA less than 1ms. See the following simulation result.



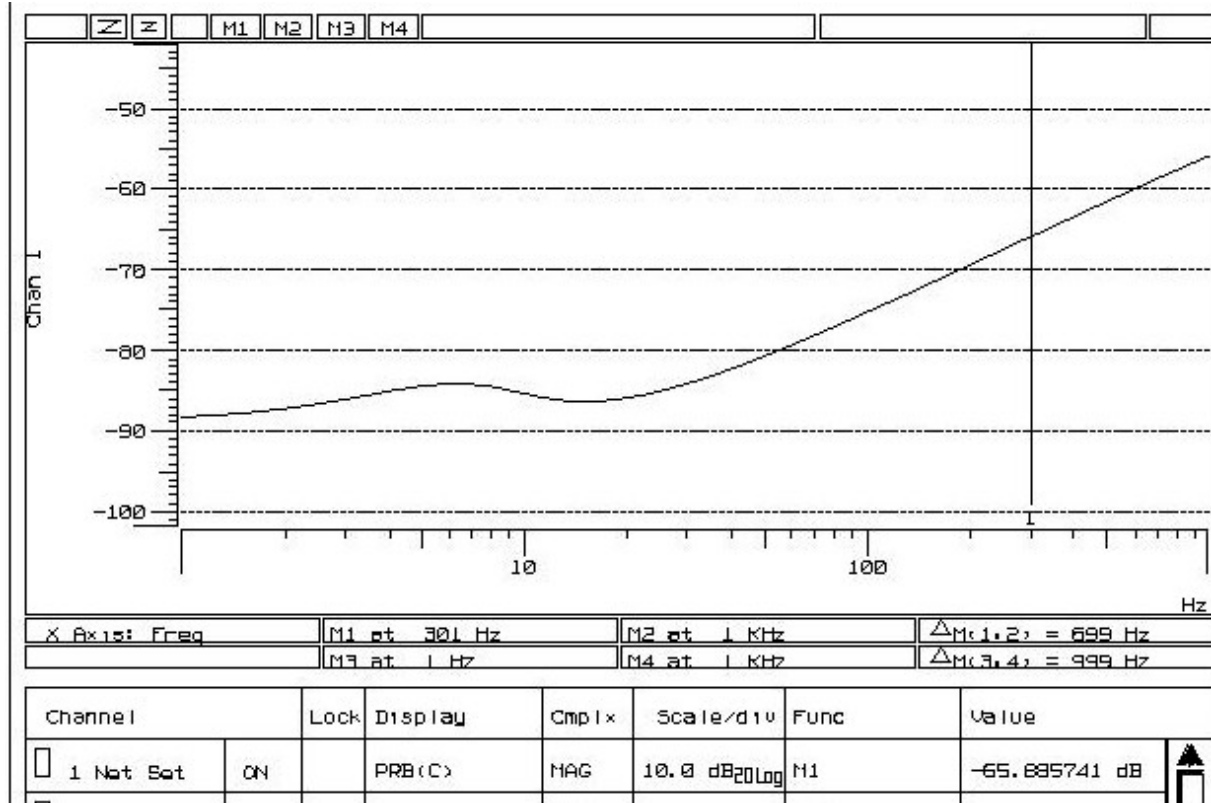
The following circuit is a simplified model of the LIA Spectrometer board seen from the -9V power supply line. The current is nominal around 135mA less than 1ms. See the following simulation result.





The following circuit is a simplified model of the LIA Spectrometer board seen from the 5V power supply line. The current is nominal around 45mA less than 1ms. See the following simulation result.



Power Supply Rejection Ratio:



TBW



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4.2.3 BIAS AND DAQ power SUPPLY

The PRIME (redundant) BIAS board and the PRIME(redundant) DAQ+IF board receive the same -9V and +9V power supply line.
A DAQ+IF board receives also a 5V power supply line.



The following circuit is a simplified model of one BIAS board with one DAQ+IF board seen from the 9V power supply line. The current is nominal around xx mA less than 1ms. See the following simulation result.

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The following circuit is a simplified model of one BIAS board with one DAQ+IF seen from the -9V power supply line. The current is nominal around xx mA less than 1ms. See the following simulation result.

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The following circuit is a simplified model of DAQ+IF board seen from the 5V power supply line. The current is nominal around xx mA less than 1ms. See the following simulation result.

TBW

 The logo for SPIRE, featuring the word "SPIRE" in a stylized, bold, blue font with a white outline, and the word "Spire" in a larger, orange, sans-serif font with a white outline.	<p data-bbox="683 152 922 230">DCU Design document</p>	 The logo for CEA DSM-DAPNIA SAp, featuring the text "cea" in a small, blue, sans-serif font, "DSM-DAPNIA" in a larger, blue, sans-serif font, and "SAp" in a large, grey, sans-serif font. <p data-bbox="1129 197 1380 280">SAp-SPIRE- FP-0063-02 Issue: 0.2 Date : 05/07/02</p>
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4.2.4 Grounding Network

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5 INTERFACES

5.1 INTERFACE WITH FPU



5.1.1 Harness

- The DCU will be connected to the FPU with four different types of harnesses.
- TYPE I will connect the LIA_P board with the FPU. Six TYPE I harnesses will connect the nine LIA_Ps.
- TYPE II will connect the photometer section of both the PRIME and REDUNDANT BIAS boards with the FPU.
- TYPE III will connect the spectrometer section of both the PRIME and REDUNDANT BIAS boards as well as a LIA_S board with the FPU.
- TYPE IV will connect the last two LIA_S boards with the FPU.

ANNEX A shows the composition of the TYPE I, TYPE II, TYPE III and TYPE IV harnesses.

ANNEX A shows how the nine harnesses are connected between the FPU and the DCU.

	Harness NAME	Harness type
Harness 1	H_FPU_BOLO_P1	TYPE I
Harness 2	H_FPU_BOLO_P2	TYPE I
Harness 3	H_FPU_BOLO_P3	TYPE I
Harness 4	H_FPU_BOLO_P4	TYPE I
Harness 5	H_FPU_BOLO_P5	TYPE I
Harness 6	H_FPU_BOLO_P6	TYPE I
Harness 7	H_FPU_BOLO_S	TYPE IV
Harness 8	H_FPU_BIAS_S	TYPE III
Harness 9	H_FPU_BIAS_P	TYPE II

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5.2 INTERFACE WITH THE DPU



5.2.1 Harness

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5.3 INTERFACE WITH THE FCU

5.3.1 Harness

TBW

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5.4 INTERFACE WITH THE TEST EQUIPEMENT

5.4.1 Harness

TBW

6 TRACEABILITY MATRIX

DRCU Subsystem Specification	Detector Subsystem Specification	DCU Design Document	Description	Check by		
				Design	Simulation	Measurement
DRCU REQ-36	BDA-DRCU-01	4.1.3.4	Noise<7nV/rt(Hz)			X
	BDA-DRCU-18	4.1.6.4				
	BDA-DRCU-03		Input capa< 100pF			X
	BDA-DRCU-04		Input impedance>1MΩ			X
	BDA-DRCU-11	4.1.3.2 4.1.6.2	CMR<-60dB		X	
	BDA-DRCU-13	4.1.3.3	Bandwidth photo		X	X
	BDA-DRCU-14	4.1.6.3	Bandwidth spectro		X	X
	BDA-DRCU-22	4.1.3.1 4.1.6.1	Channel saturation	X		
	BDA-DRCU-25		Cross talk<0.05%			X
	-	4.1.3.3 4.1.6.3	LPF (HR-SP-RAL-ERC-001)	X		
-	4.1.1.1 4.1.4.1	Channel number	X			
-	4.1.2.2 4.1.5.2	LIA Interface Balanced signal + Shield	X			
DRCU REQ-37	BDA-DRCU-19	4.1.3.4 4.1.6.4	NOISE with thermal drift			X
DRCU REQ-38	BDA-DRCU-05	4.1.7 4.1.12.4	BIAS	X		
DRCU REQ-39		4.1.8.1 4.1.8.4	Amplitude command	X		
DRCU REQ-40		4.1.12.4	Bias frequency	X		
-		4.1.8.5	Noise<20nV/rt(Hz)			X
DRCU REQ-41	BDA-DRCU-06	4.1.7	JFET BIAS	X		
	BDA-DRCU-07	4.1.8.2				
	BDA-DRCU-08	4.1.8.6	VSS and VDD Noise			X
DRCU REQ-42	BDA-DRCU-09	4.1.8.4 4.1.12.6	VSS and VDD ON/OFF command	X		
DRCU REQ-43		4.1.8.2	VSS and VDD overshoot		X	
	BDA-DRCU-21	4.1.8.6	JFET power NOISE with thermal drift			X
DRCU REQ-44	BDA-DRCU-10	4.1.8.3	heater	X		
DRCU REQ-45		4.1.8.4 4.1.12.6	heater command	X		
DRCU REQ-46	-	4.1.12.6	DCU data	X		
DRCU REQ-47	-	3.1.1.1	DAQ PRIME/ REDUNDANT	X		
DRCU REQ-48	BDA-DRCU-12	4.1.10.4	ADC resolution	X		
	-	4.1.12.2	TOTAL Acquisition time	X		
DRCU REQ-49	BDA-DRCU-15	4.1.12.1	Sample clock	X		
	BDA-DRCU-16	4.1.12.6				
DRCU REQ-50	-	4.1.12.1	Frame number	X		
	-	4.1.12.6				
DRCU REQ-51	-	4.1.12.6	Mode data frame	X		

DRCU Subsystem Specification	Detector Subsystem Specification	DCU Design Document	Description	Check by		
				Design	Simulation	Measurement
DRCU REQ-52	-	4.1.10.5	Temperature probe Location	X		
DRCU REQ-53	-	4.1.10.5	Temperature acquisition	X		
DRCU REQ-54	-	4.1.10.5	Temperature range	X		
DRCU REQ-55	-	4.1.12.6	Housekeeping parameter	X		
DRCU REQ-56	-	4.2	DCU power supply	X		
DRCU REQ-57	-					
DRCU REQ-58	-					
DRCU REQ-59	-					