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Draft

HERSCHEL/SPIRE

DETECTOR CONTROL UNIT
DESIGN DOCUMENT

	Function	Name	Date	Visa
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DOCUMENT STATUS and CHANGE RECORD

Date	Issue	Affected pages
8/11/2001	0.-	Creation

TABLE OF CONTENTS

PICTURES

List of Acronyms

ADC	Analog to Digital Converter
AMUX	Analog Multiplexer
DPU	Data Processing Unit
DCU	Detector Control Unit
DMUX	Digital Multiplexer
DRCU	Detector Readout & Control Unit
FPU	Focal Plane Unit
JFET	Junction Field Effect Transistor
LIA	Lock-in amplifier
LPF	Low Pass Filter
NA	Not Applicable
PDU	Power Distribution Unit
SCU	Sub-system Control Unit
PSU	Power Supply Unit
SMPS	Switching Mode Power Supply
SNR	Signal over Noise Ratio
S/W	Software
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
WIH	Warm Interconnect Harnesses

1 INTRODUCTION

1.1 PURPOSE

TBW

1.2 SCOPE

TBW

1.3 APPLICABLE DOCUMENTS

AD1	DRCU Interface Control DOCUMENT	Sap-SPIRE-CCA-	0.5
AD2	DRCU Subsystem Specification	Sap-SPIRE-CCA-25-00	0.9
AD3	Detector Subsystem Specification	FIRS-SPI-000103	Working / 7/9/01
AD4	Spire harness definition	SPIRE-RAL-PRJ-000608	0.8
AD5	Spire instrument block diagram	SPIRE-RAL-DWG-000646	3.8

1.4 REFERENCE DOCUMENTS

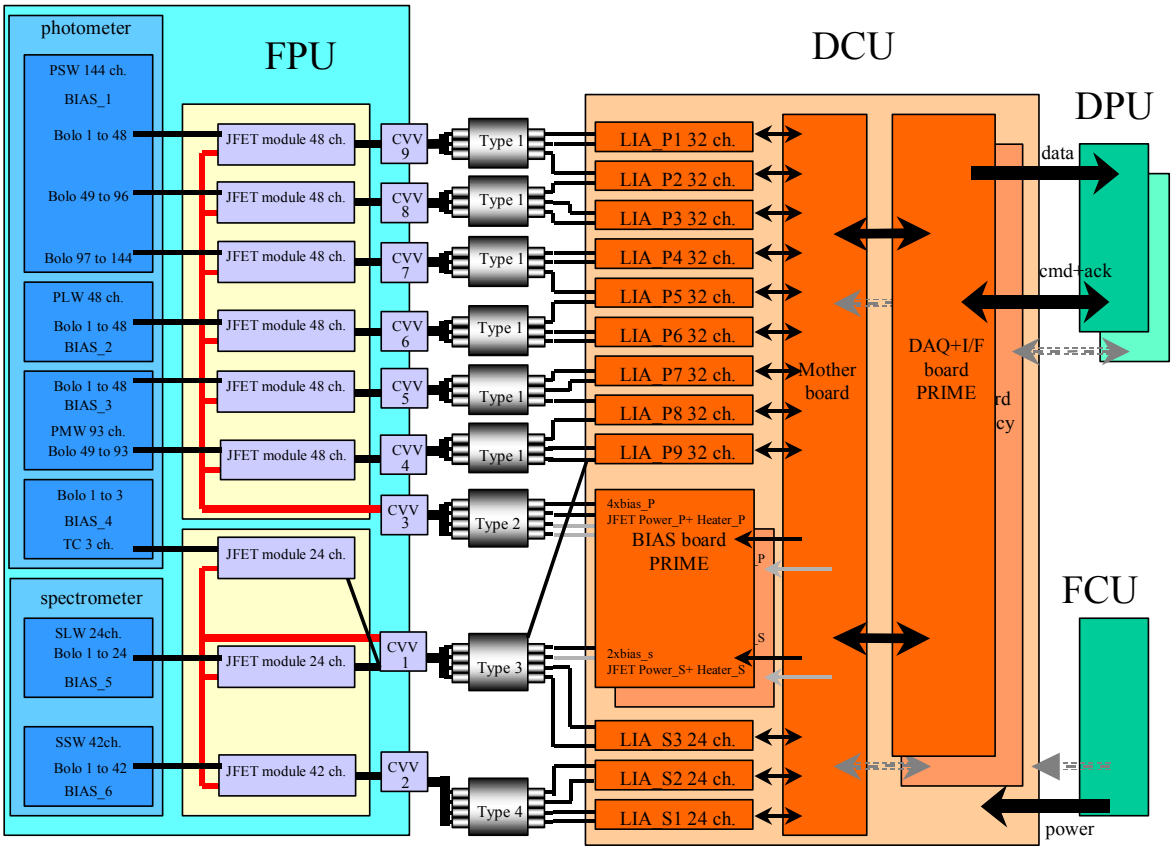
RD1	MAT02 data sheet		REV.C
RD2	OP-400 data sheet		
RD3			
RD4			
AD5			

2 GENERAL DESCRIPTION

2.1 OVERVIEW

The following drawing shows:

- How the DCU is connected to the FPU.
- The different harnesses types and their localization.
- That the DCU power supply is provided by FCU.
- The data exchange link with the DPU PRIME and REDUNDANT.



Picture 2-1: DCU Overview

3 PHYSICAL CARACTERISTCS

3.1 PHYSICAL DESCRIPTION

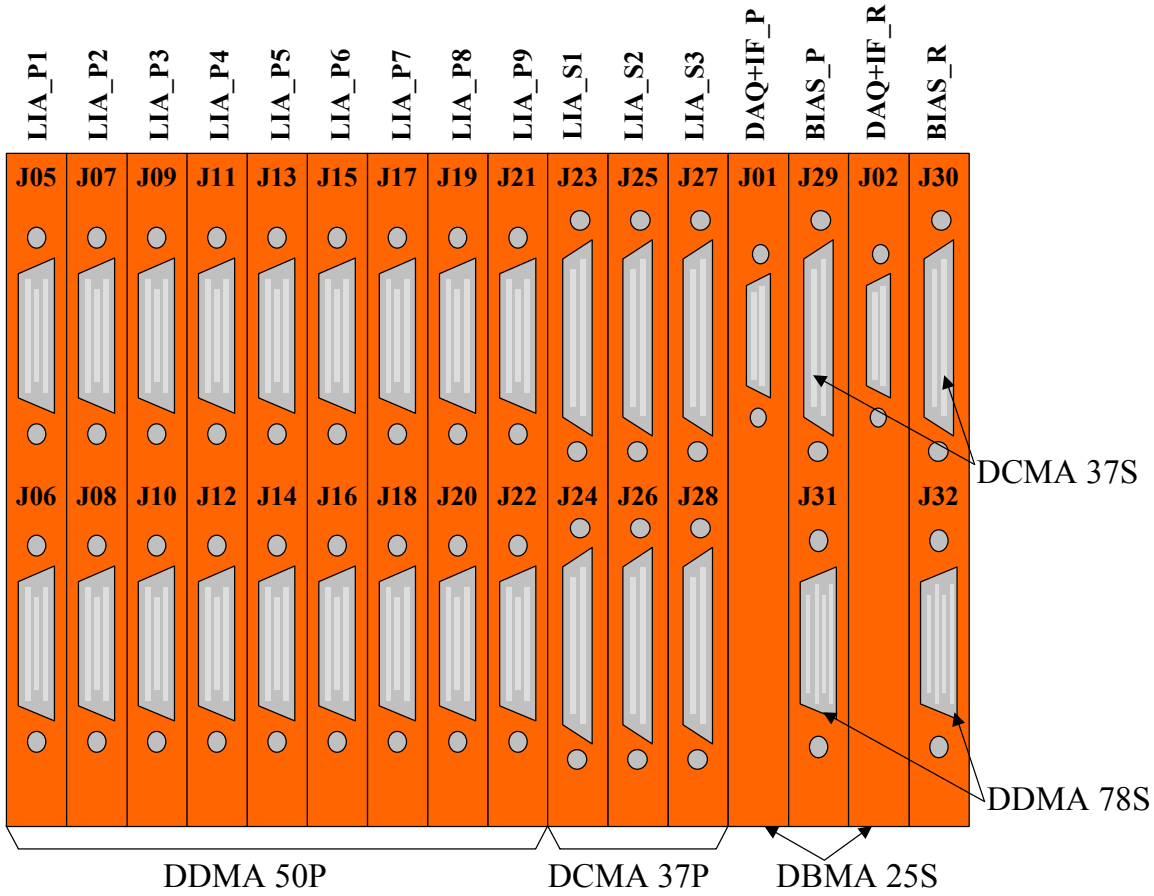
3.1.1 DCU housing

3.1.1.1 QM2 and FM

All of the DCU electronics are housed in one box. A back plane printed circuit board insures the internal DCU connections.
The DCU is composed in its QM2 and FM versions of:

- 9 LIA_P boards
- 3 LIA_S boards
- 2 BIAS boards (PRIME and REDUNDANT)
- 2 DAQ+I/F boards (PRIME and REDUNDANT)

The layout of these boards is organized as shown in Picture 3-1 DCU Front Panel.



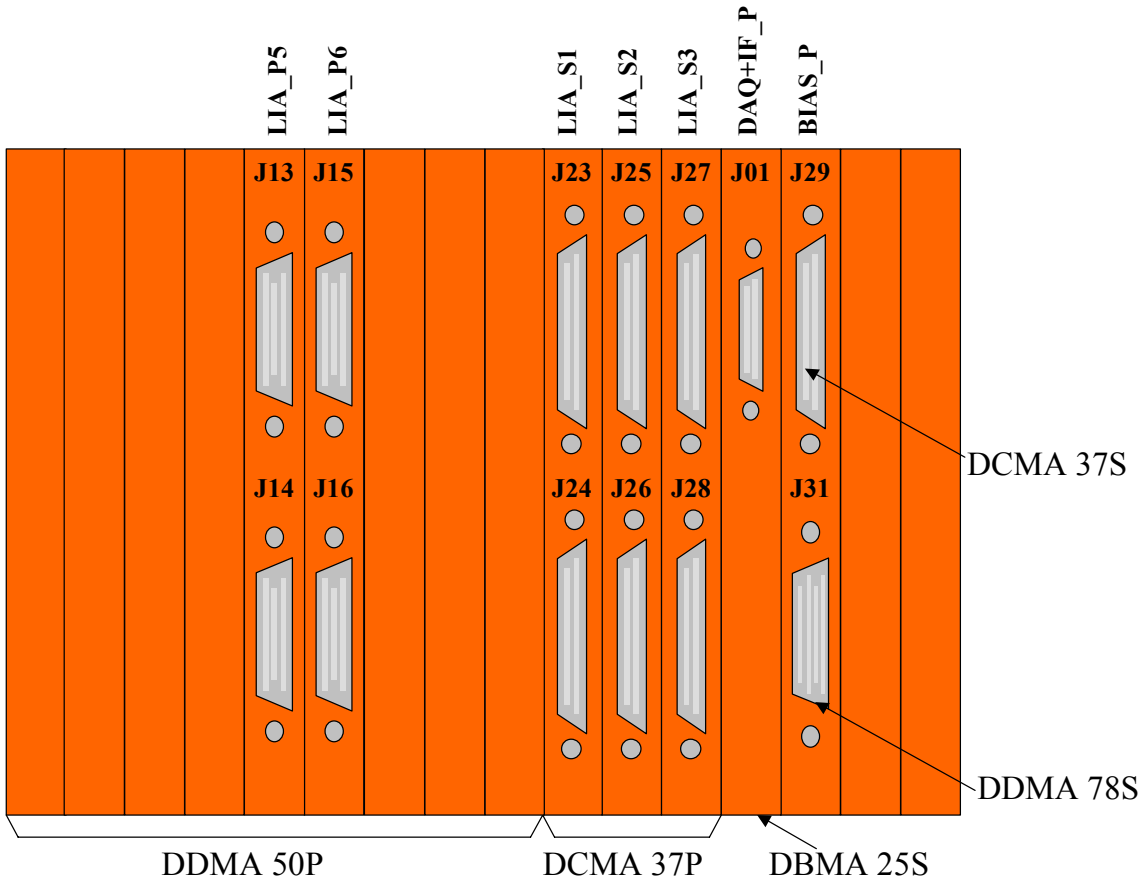
Picture 3-1 DCU Front Panel for QM2 and FM

3.1.1.2 QM1

All of the DCU electronics are housed in a prototype box. A QM1 back plane printed circuit board insures the internal DCU connections.
The DCU is composed in its QM1 version of:

- 2 LIA_P boards
- 3 LIA_S boards
- 1 BIAS board (PRIME)
- 1 DAQ+I/F board (PRIME).

The layout of these boards is organized as shown in Picture 3-2 DCU Front Panel for QM1.

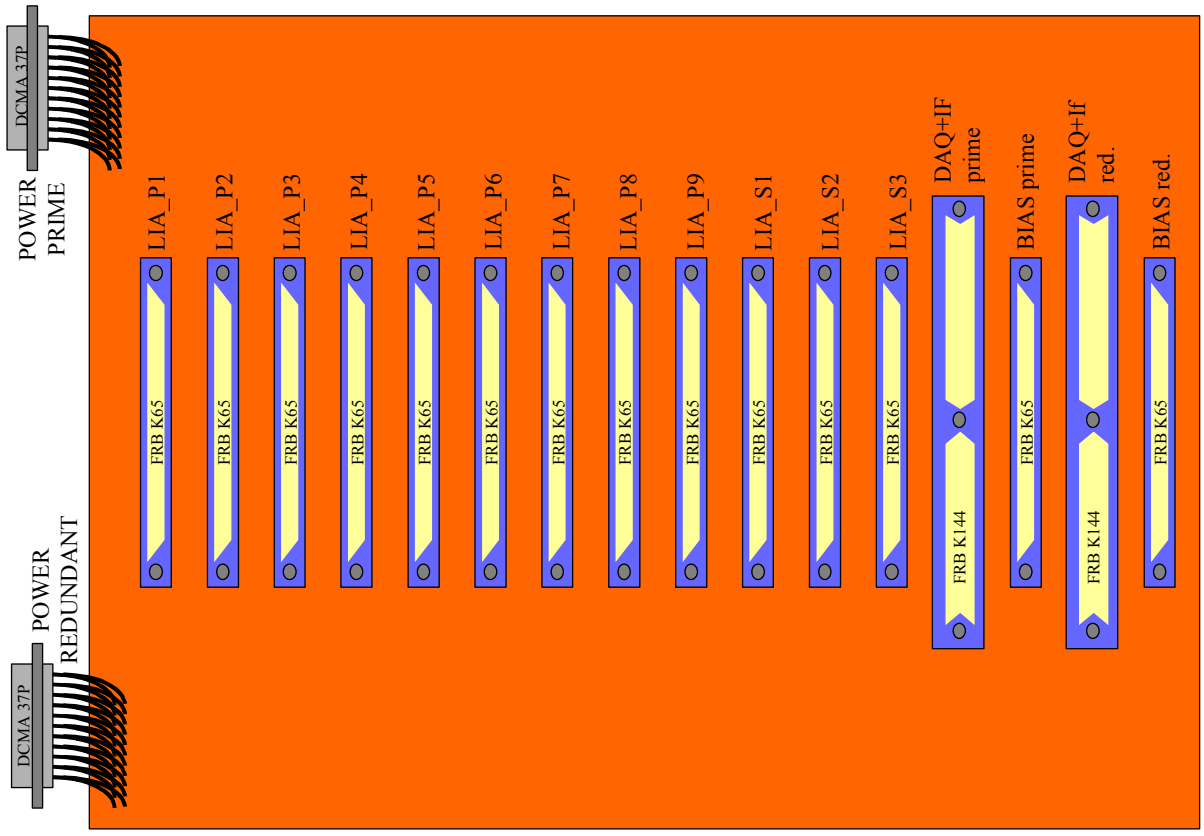


Picture 3-2 DCU Front Panel for QM1

3.1.2 Back plane

3.1.2.1 QM1,QM2 and FM

QM1,QM2, and FM all have the same kind of back plane.
The back plane is organized as shown in Picture 3-3 Back Plane.



Picture 3-3 Back Plane

3.2 NECESSARY POWER SUPPLY ESTIMATION

3.2.1.1 QM2, FM

	9 x LIA_P	3 x LIA_S	BIAS_P	BIAS_S	DAQ+I/F
+9V					
-9V					
5V					

3.2.1.2 QM1

	2 x LIA_P	3x LIA_S	BIAS_P	BIAS_S	DAQ+I/F
+9V					
-9V					
5V					

4 PERFOMANCE

4.1 Functional description

The **D**etector **C**ontrol **U**nit supports all of the functions related to the detector's operation. This covers:

• The detector bias generation	DCU-FUNC-01
• The bolometer signal processing	DCU-FUNC-02
• The bolometer signal digitization	DCU-FUNC-03
• The timing cycle	DCU-FUNC-04
• The JFET box biasing	DCU-FUNC-05
• The low-level command decoding	DCU-FUNC-06
• The low-level command acknowledge	DCU-FUNC-07
• The relative timestamp generation	DCU-FUNC-08
• The housekeeping parameter digitisation	DCU-FUNC-09
• The digitized data (bolometers + hk param. + rel. timestamp) transfer	DCU-FUNC-10

DCU-FUNC-01 and DCU-FUNC-05 are done by either the PRIME or REDUNDANT BIAS boards.

DCU-FUNC-02 is done by nine LIA_P boards for the photometer and three LIA_S boards for the spectrometer.

DCU-FUNC-03 is done by six ADC on either the PRIME or the REDUNDANT DAQ+IF board.

DCU-FUNC-04, DCU-FUNC-06, DCU-FUNC-07, DCU-FUNC-08 and DCU-FUNC-10 are done by an FPGA on either the PRIME or REDUNDANT DAQ+IF board.

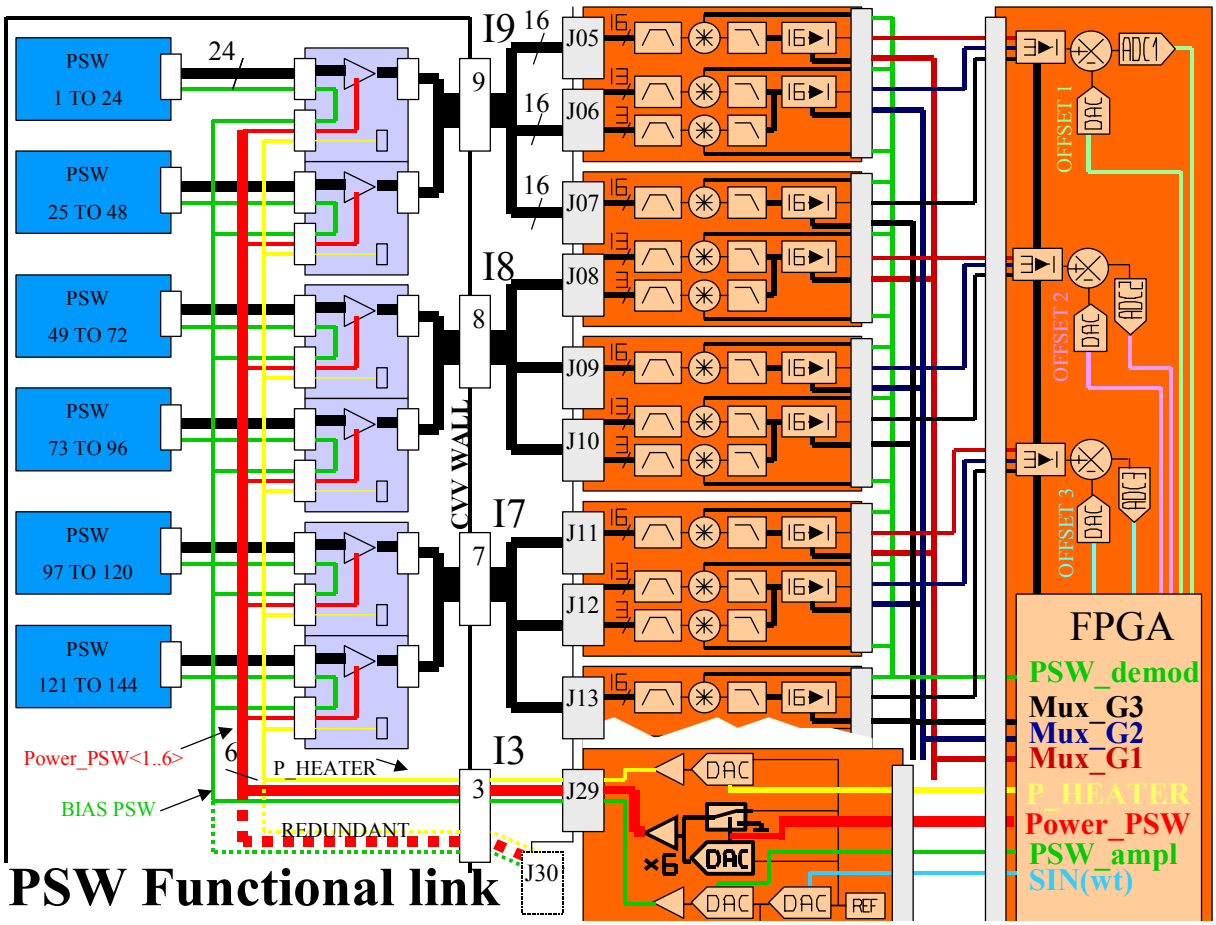
DCU-FUNC-09 is done by an ADC on either the PRIME or REDUNDANT DAQ+IF board.

4.1.1 LIAs PHOTOMETER

4.1.1.1 QM2, FM

Nine LIA_P boards make up the LIA photometer section.

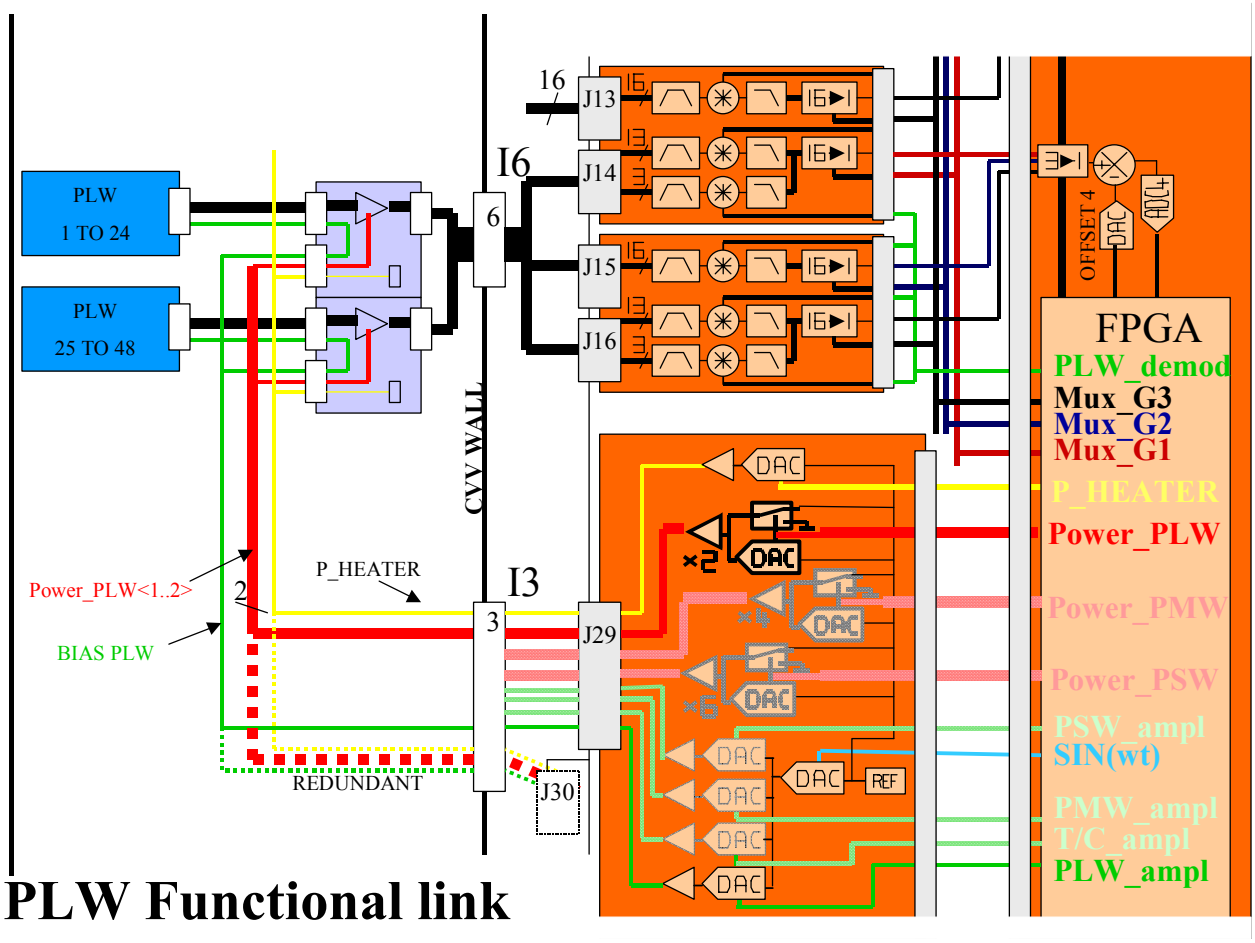
1. LIA_P1 to LIA_P4 and the first 16 channels of LIA_P5 will receive and process the signals from 144 "PSW bolometers."



Picture 4-1 PSW Photometer Functional Links

- The 144 PSW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (PSW_demod.)
- All of the 144 channels are sent to the DAQ+IF board through 9 differential links that are digitized by 3 ADCs.

2. The other 16 channels from LIA_P5 and LIA_P6 receive and process signals from 48 “PLW bolometers.”

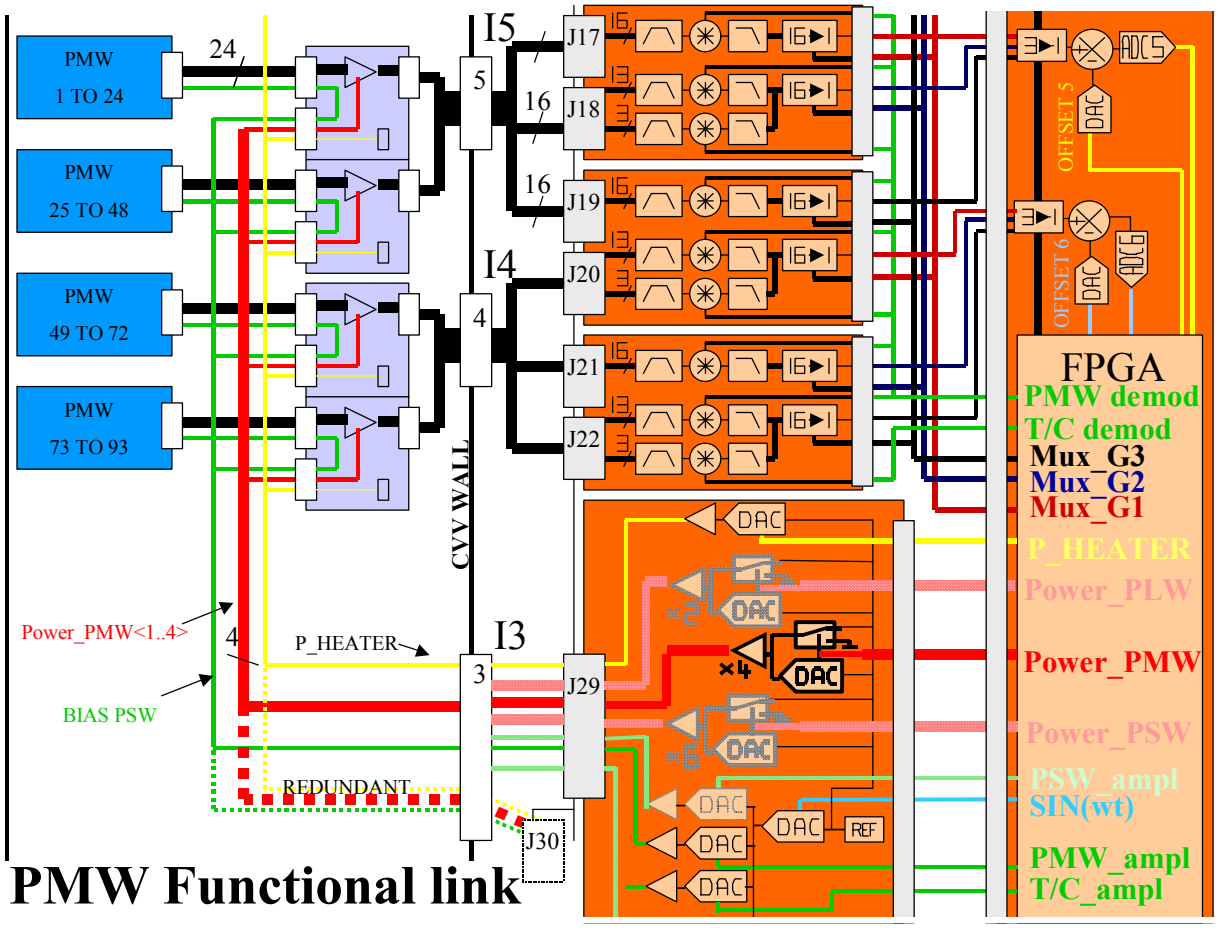


PLW Functional link

Picture 4-2 PLW Photometer Functional Links

- The 48 PLW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (PLW_demod.)
- All of the 48 channels are sent to the DAQ+IF board through 3 differential links that are digitized by one ADC.

3. LIA_P7 to LIA_P8 and the first 29 channels of the LIA_P9 receive and process the signals from 93 "PMW bolometers."

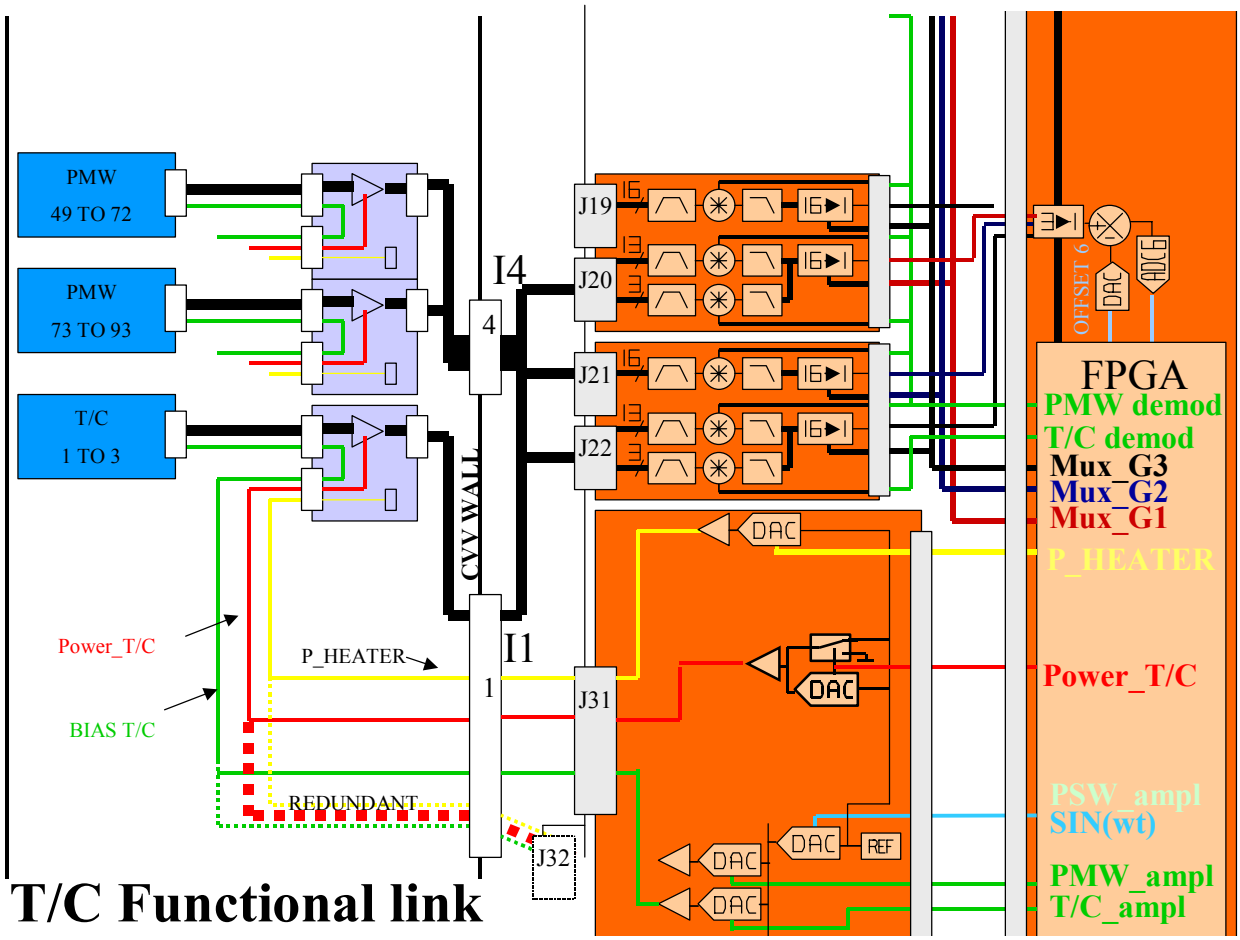


Picture 4-3 PMW Photometer Functional Links

- The 93 PMW channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (PMW_demod.)

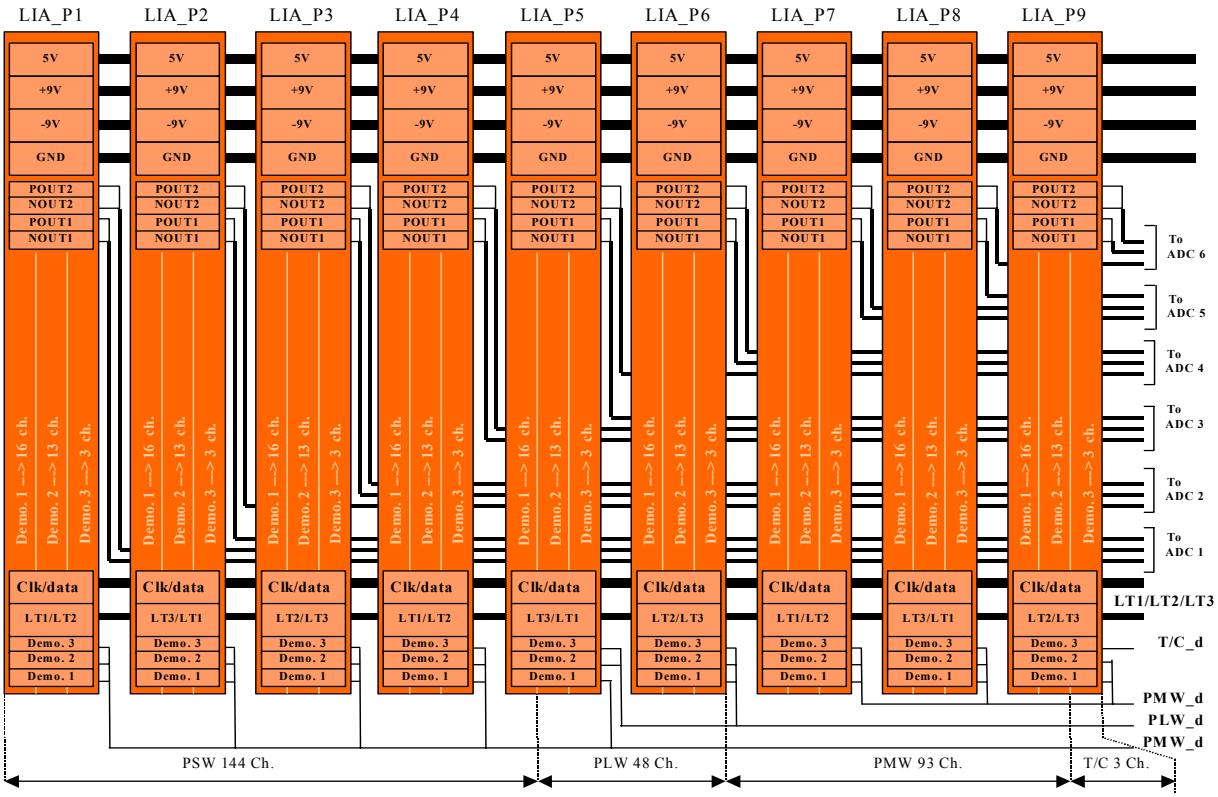
- All of the 93 channels are sent to the DAQ+IF board through 6 differential links that are digitized by 2 ADCs.

4. The last 3 channels of the LIA_P9 receive and process signals from 3 “T/C bolometers.’



Picture 4-4 T/C Photometer Functional Links

- The 3 T/C channels receive the same sinusoidal bias signal (the same frequency and the same amplitude) and the same square demodulation signal (T/C_demod.)
- All 3 channels are sent to the DAQ+IF board through one differential link that is digitized by one ADC.
- Note: The T/C signals go through connectors J31and J32 as well as harness I1 which are mainly used to carry the spectrometer signals. However, these T/C signals always refer to the photometer’s ground.



Picture 4-5 LIA Photometer Section

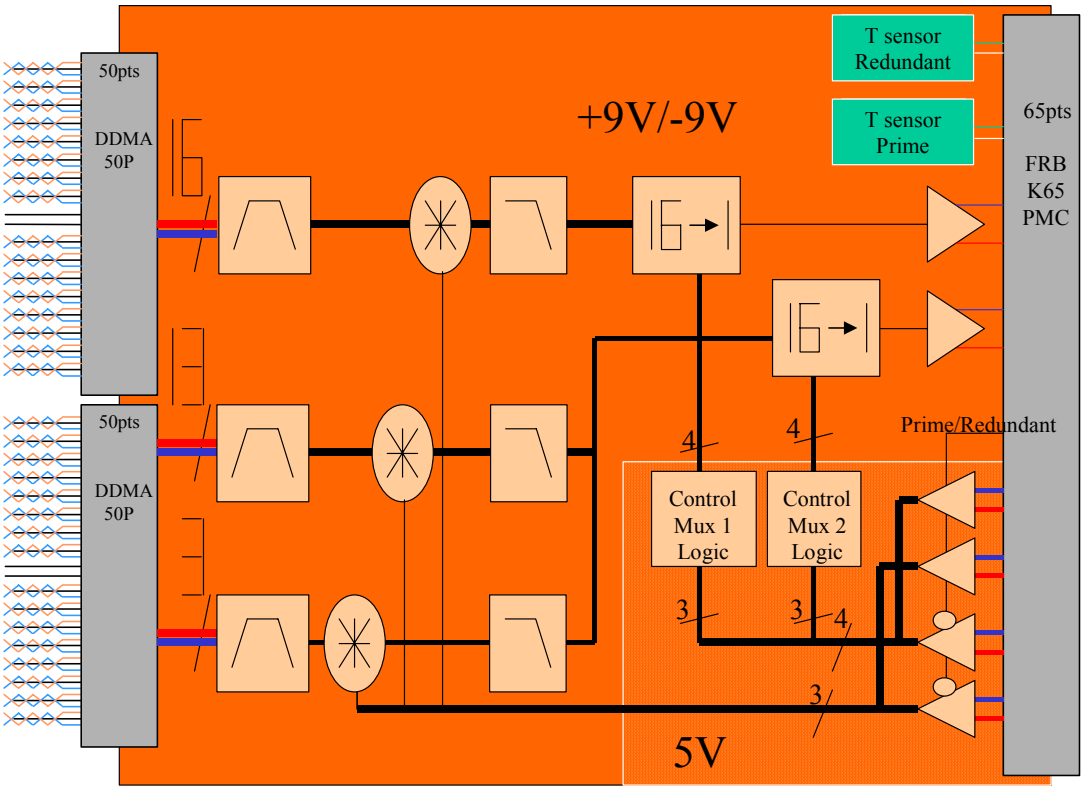
Each group receive its own respective demodulation signal: PSW_demod, PMW_demod, PLW_demod and T/C_demod. Each of these signals can have a different phase shift.

The LIA photometer is supplied only when the SPIRE instrument is running in the photometer mode.

Each LIA photometer board receive its own group of 3 supply lines (-9V, +9V and 5V) which be automatically shutdown if a error occurs on one of these three lines.

4.1.2 LIA PHOTOMETER BOARD

4.1.2.1 LIA Photometer Board Overview



Picture 4-6 LIA Photometer Board Overview

• The LIA_P board has thirty-two channels that are divided into three groups:

- A group of sixteen channels which go to the first multiplexer.
- A group of thirteen channels which go to the second multiplexer.
- A group of three channels which also go to the second multiplexer.

•Each of the three groups can receive its own demodulation signals.

•The receivers that relay the multiplexer command signals as well as the demodulation signals are redundant:

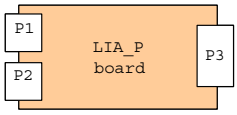
- A PRIME/REDUNDANT signal from the PSU activates the PRIME receivers when the PRIME power supply turns on and the REDUNDANT receivers when the REDUNDANT power supply turns on.
- The LIA PRIME receivers are connected to the PRIME DAQ+IF board.
- The LIA REDUNDANT receivers are connected to the REDUNDANT DAQ+IF board.

•Each multiplexer's command is independent.

4.1.2.2 LIA Photometer Board Interface

connector	P1				
type	DDMA 50 P				
pin	signal name	pin	signal name	pin	signal name
1	IN+1			34	SHLD1
2	IN+2	18	IN-1	35	SHLD2
3	IN+3	19	IN-2	36	SHLD3
4	IN+4	20	IN-3	37	SHLD4
5	IN+5	21	IN-4	38	SHLD5
6	IN+6	22	IN-5	39	SHLD6
7	IN+7	23	IN-6	40	SHLD7
8	IN+8	24	IN-7	41	SHLD8
9	GND	25	IN-8	42	GND
10	IN+9	26	IN-9	43	SHLD9
11	IN+10	27	IN-10	44	SHLD10
12	IN+11	28	IN-11	45	SHLD11
13	IN+12	29	IN-12	46	SHLD12
14	IN+13	30	IN-13	47	SHLD13
15	IN+14	31	IN-14	48	SHLD14
16	IN+15	32	IN-15	49	SHLD15
17	IN+16	33	IN-16	50	SHLD16

connector	P2				
type	DDMA 50 P				
pin	signal name	pin	signal name	pin	signal name
1	IN+17			34	SHLD17
2	IN+18	18	IN-17	35	SHLD18
3	IN+19	19	IN-18	36	SHLD19
4	IN+20	20	IN-19	37	SHLD20
5	IN+21	21	IN-20	38	SHLD21
6	IN+22	22	IN-21	39	SHLD22
7	IN+23	23	IN-22	40	SHLD23
8	IN+24	24	IN-23	41	SHLD24
9	GND	25	IN-24	42	GND
10	IN+25	26	IN-25	43	SHLD25
11	IN+26	27	IN-26	44	SHLD26
12	IN+27	28	IN-27	45	SHLD27
13	IN+28	29	IN-28	46	SHLD28
14	IN+29	30	IN-29	47	SHLD29
15	IN+30	31	IN-30	48	SHLD30
16	IN+31	32	IN-31	49	SHLD31
17	IN+32	33	IN-32	50	SHLD32



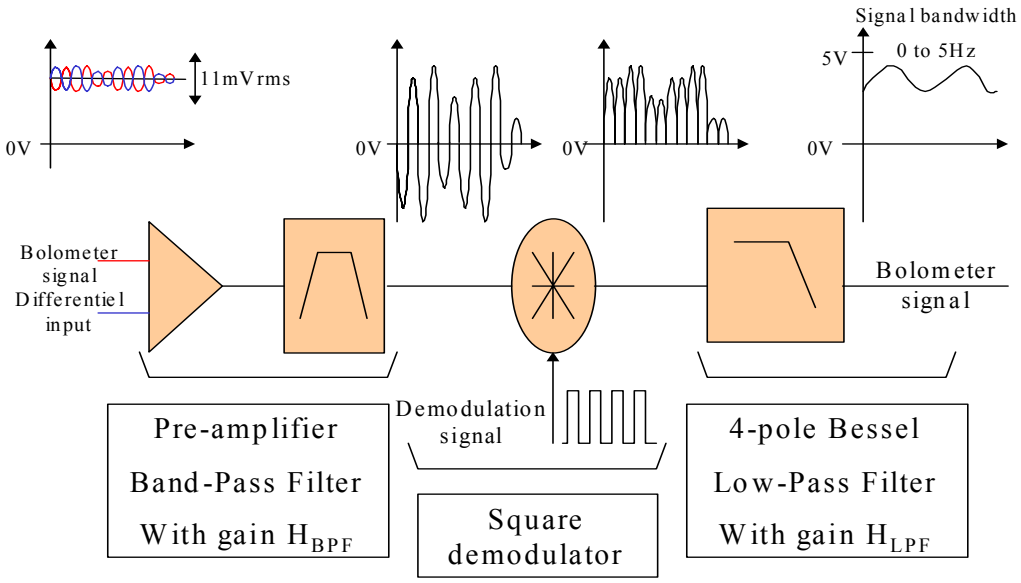
connector	P3		
type	KNB 65		
pin	signal name	pin	signal name
1	gnd		
3	NOUT1	2	POUT1
5	NOUT2	4	POUT2
7	gnd	6	gnd
9	N9V	8	N9V
11	P9V	10	P9V
13	P9V_P	12	P9V_P
15	gnd	14	gnd
17	PCLK-	16	RCLK-
19	PCLK+	18	RCLK+
21	PLT1-	20	RLT1-
23	PLT1+	22	RLT1+
25	PLT2-	24	RLT2-
27	PLT2+	26	RLT2+
29	PDATA_S-	28	RDATA_S-
31	PDATA_S+	30	RDATA_S+
33	P5V	32	P5V
35	gnd	34	gnd
37	PDEMOD1-	36	RDEMOD1-
39	PDEMOD1+	38	RDEMOD1+
41	PDEMOD2-	40	RDEMOD2-
43	PDEMOD2+	42	RDEMOD2+
45	PDEMOD3-	44	RDEMOD3-
47	PDEMOD3+	46	RDEMOD3+
49	gnd	48	gnd
51	gnd	50	gnd
53	-	52	-
55	-	54	-
57	-	56	-
59	RT_P9V	58	RT_P9V
61	RT	60	RT
63	PT_P9V	62	PT_P9V
65	PT	64	PT

Picture 4-7 LIA Photometer Board Interface

Name	Description	Type	Level	In/Out	Frequency
IN+ xx	Bolometer Differential Signal	Analogic	11mVrms (AC) + 1.5V (DC)	IN	50-300Hz
IN- xx					
POUT x	sixteen LIA_P channels multiplexed in one differential signal	Analogic	0 to 5V	OUT	0-5Hz at mux freq. ~2.5kHz
NOUT x					
PCLK-	Serial Clock for the LIA_P /DAQ+IF PRIME Interface, (differential signal)	Numeric	-0,3Vto 0,3V	IN	5MHz max
PCLK+					
PDATA-	Serial Data for the LIA_P /DAQ+IF PRIME interface, (differential signal)	Numeric	-0,3Vto 0,3V	IN	5MHz max
PDATA+					
PLTx-	Data LATCH for the LIA_P /DAQ+IF PRIME Interface, (differential signal)	Numeric	-0,3Vto 0,3V	IN	5MHz max
PLTx+					
PDEMOD1-	Demodulation Differential Signal (PRIME) for Channels One to Sixteen	Numeric	-0,3Vto 0,3V	IN	50-300Hz
PDEMOD1+					
PDEMOD2-	Demodulation Differential Signal (PRIME) for Channels Seventeen to Twenty-nine	Numeric	-0,3Vto 0,3V	IN	50-300Hz
PDEMOD2+					
PDEMOD3-	Demodulation Differential Signal for Channels One to Sixteen	Numeric	-0,3Vto 0,3V	IN	50-300Hz
PDEMOD3+					
RCLK-	Serial Clock for the LIA_P /DAQ+IF REDUNDANT Interface	Numeric	-0,3Vto 0,3V	IN	5MHz max
RCLK+					
RDATA-	Serial Data for the LIA_P /DAQ+IF REDUNDANT Interface	Numeric	-0,3Vto 0,3V	IN	5MHz max
RDATA+					
RLTx-	Data LATCH for the LIA_P /DAQ+IF REDUNDANT Interface	Numeric	-0,3Vto 0,3V	IN	5MHz max
RLTx+					
RDEMOD1-	Demodulation Differential signal (REDUNDANT) for Channels One to Sixteen	Numeric	-0,3Vto 0,3V	IN	50-300Hz
RDEMOD1+					
RDEMOD2-	Demodulation Differential Signal (REDUNDANT) for Channels Seventeen to Twenty-nine	Numeric	-0,3Vto 0,3V	IN	50-300Hz
RDEMOD2+					
RDEMOD3-	Demodulation Differential Signal for (REDUNDANT) channels One to Sixteen	Numeric	-0,3Vto 0,3V	IN	50-300Hz
RDEMOD3+					
PT_P9V	Sensor PRIME Bias	Analogic	9V	IN	DC
PT	Output Sensor PRIME	Analogic	2 to 4V	OUT	-
RT_P9V	Sensor REDUNDANT Bias	Analogic	9V	IN	DC
RT	Output Sensor REDUNDANT	Analogic	2 to 4V	OUT	-
P9V	9V Power Supply	Power	9V	IN	DC
N9V	-9V Power Supply	Power	-9V	IN	DC
P9V_P	PRIME/REDUNDANT Signal	Analogic	0 to 9V	IN	DC
P5V	5V Power Supply	Power	5V	IN	DC
GND	Grounding	Power	0V	-	DC

4.1.3 LIA PHOTOMETER CHANNELS

4.1.3.1 LIA Photometer Channel Overview



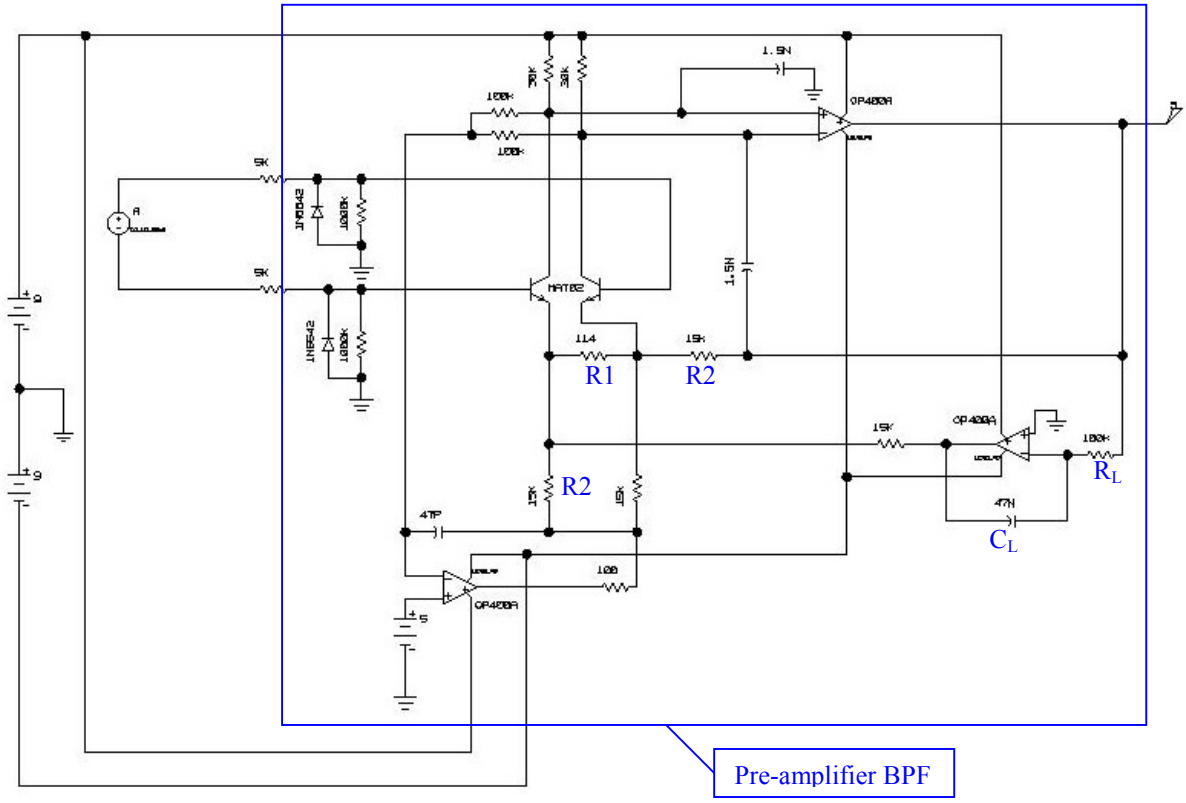
Picture 4-8 LIA Photometer Board Overview

The input differential signal that comes from a bolometer is amplified and its DC component is eliminated by the pre-amplifier BPF. Then, it is demodulated by a squared signal. Afterwards, it is filtered by a four-pole Bessel LPF.

The four-pole Bessel low pass filter has a structural gain of $H_{LPF} = 1.9$
The square demodulation signal will introduce a gain of $2/\pi$
Note: To be sure that a photometer channel won't be saturated with a 11mVrms input, the output signal cannot be more than 5V.

This is why the band pass filter gain H_{BPF} cannot be larger than $\frac{5V}{11mV.\frac{2\sqrt{2}}{\pi}.1,9}=264$

4.1.3.2 LIA Photometer Channel Pre-amplifier BPF



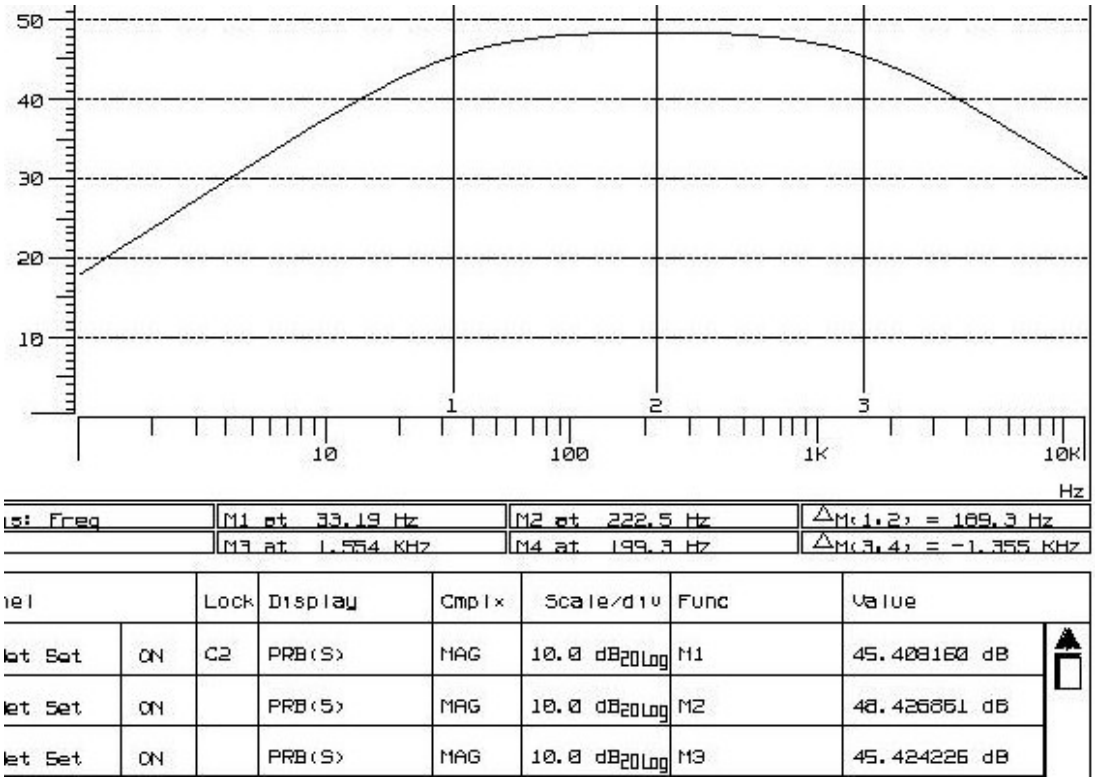
Picture 4-9 LIA Photometer Pre-amplifier BPF

The gain of this pre-amplifier is found by employing the following calculation: 2xR2/R1 = 2x15K/114 = 263.

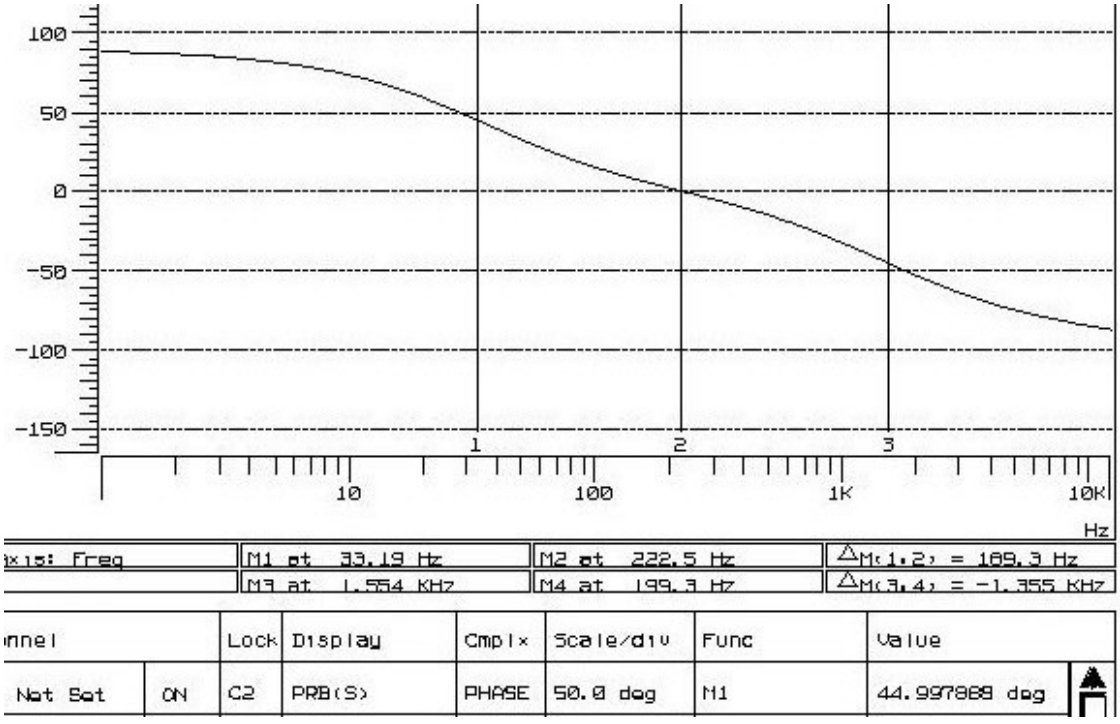
The BPF's low frequency cut-off is found by employing the following calculation:

$$F_{CL}=\frac{1}{2\pi.R_L.C_L}=\frac{1}{2\pi.100Kx47nF}=33,8Hz$$

The two following simulation results show respectively the magnitude and the phase transfer function of LIA Photometer Pre-amplifier BPF:

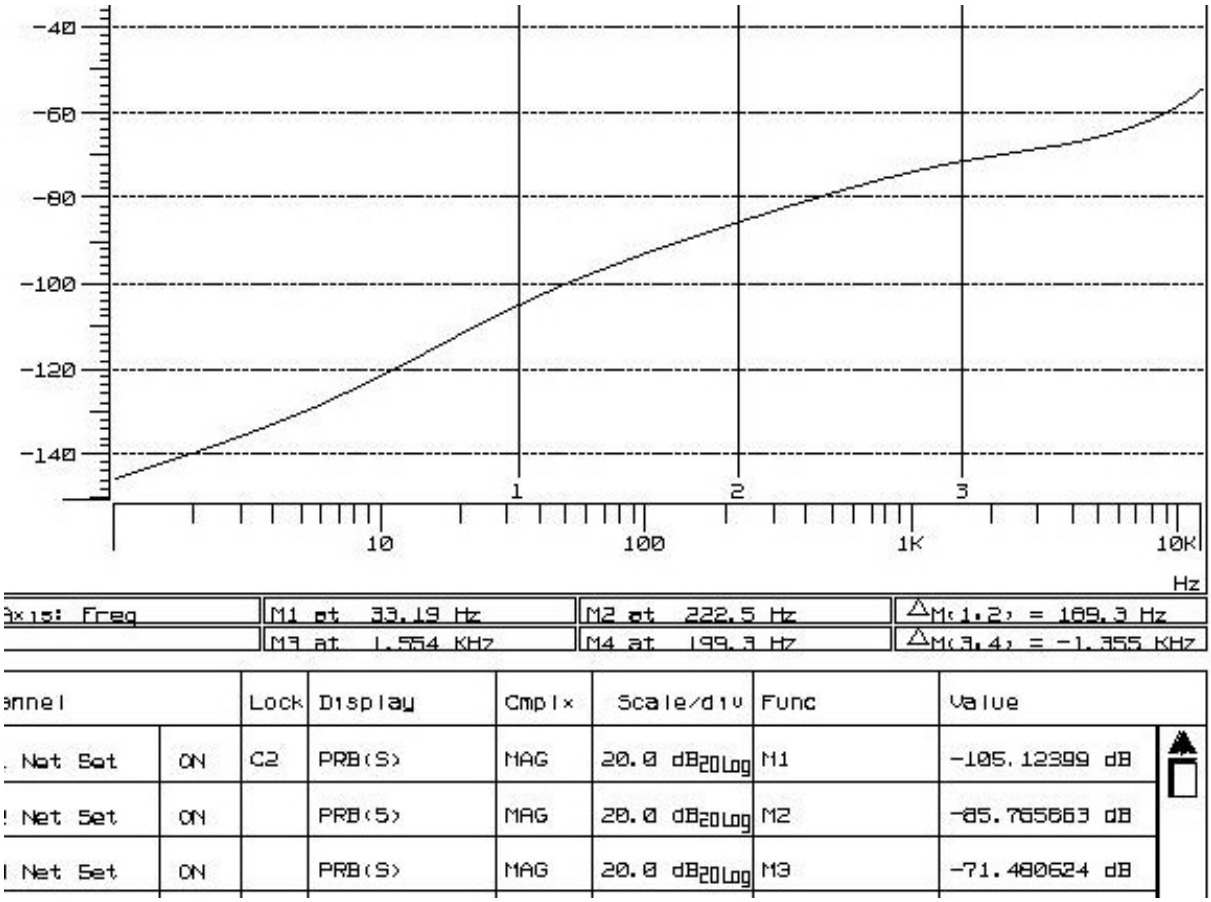


Picture 4-10 LIA Photometer Pre-amplifier BPF Magnitude Transfer Function



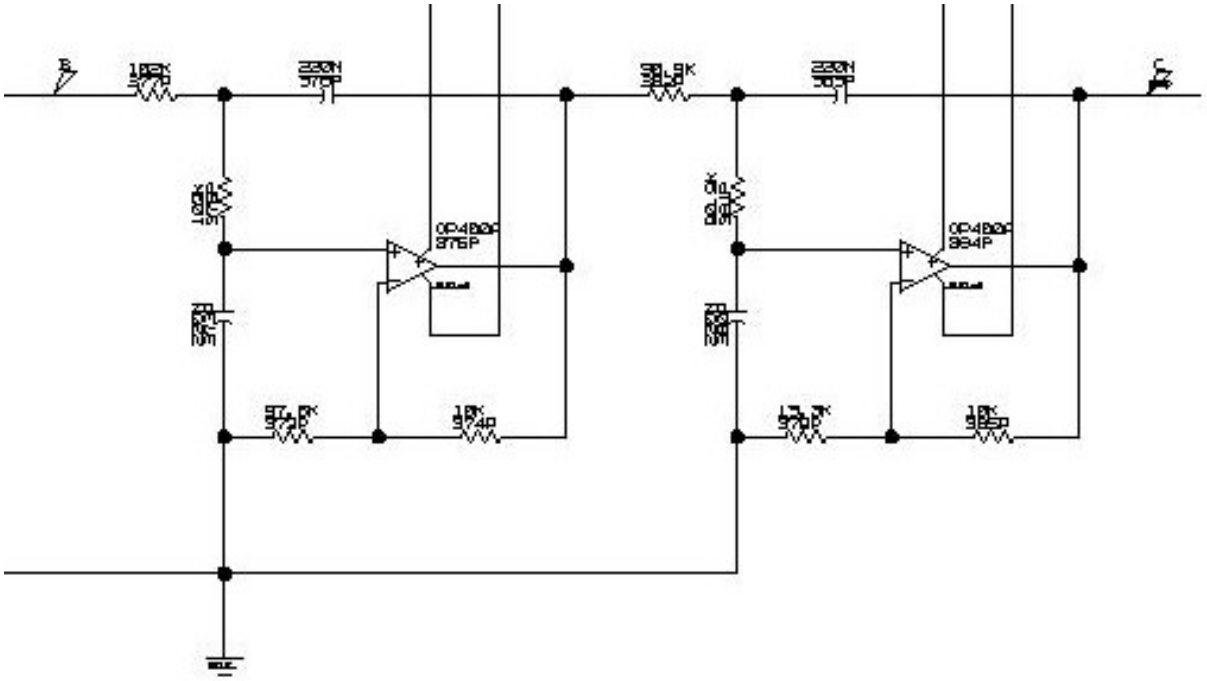
Picture 4-11 LIA Photometer Pre-amplifier BPF Phase Transfer Function

The following simulation result shows the common mode transfer function. It shows that we have at least –80dB common mode rejection between 50Hz and 300Hz.
In other words, there is some leeway with the –60dB requirement.



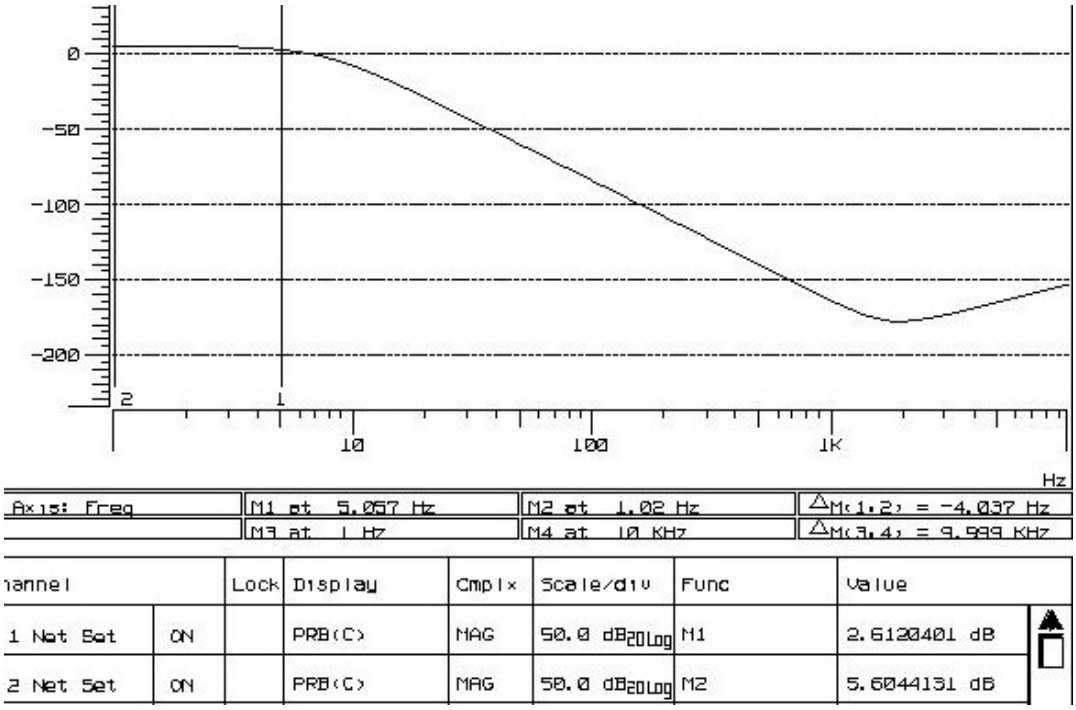
Picture 4-12 LIA Photometer Pre-amplifier BPF Common Mode Rejection

4.1.3.3 LIA Photometer Channel LPF

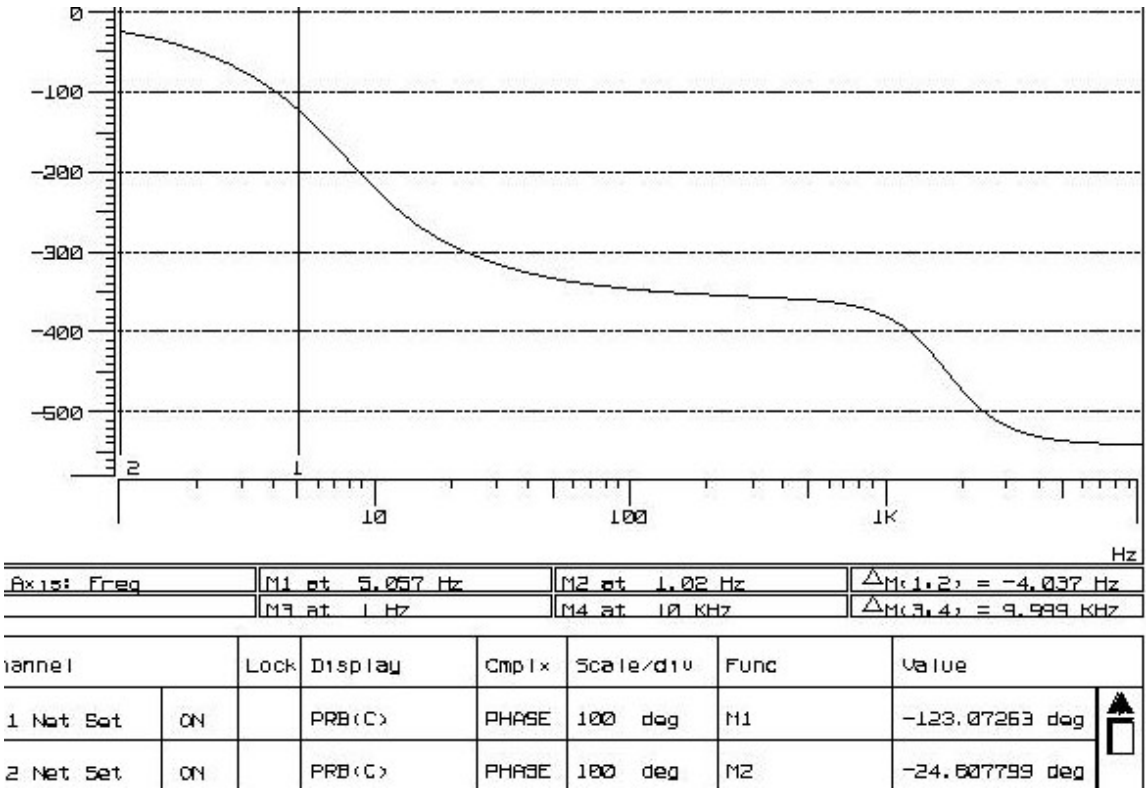


Picture 4-13 LIA Photometer Pre-amplifier BPF

The two following simulation results show respectively the magnitude and the phase transfer function of LIA Photometer four-pole Bessel LPF:



Picture 4-14 LIA Photometer LPF Magnitude Transfer Function



Picture 4-15 LIA Photometer LPF Phase Transfer Function

4.1.3.4 LIA Photometer Channel Input Noise

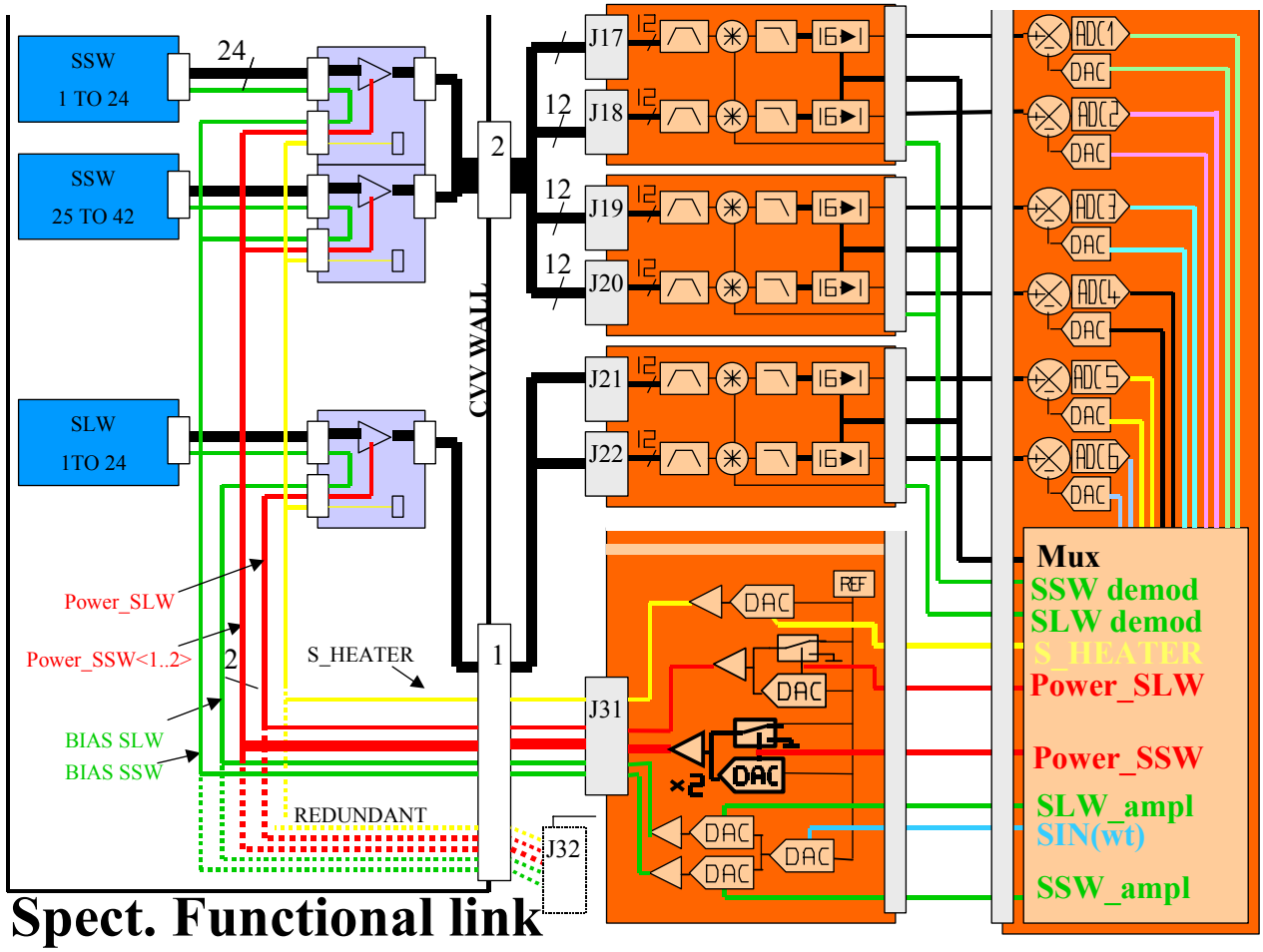
TBW

4.1.4 LIAs SPECTROMETER

4.1.4.1 QM1, QM2 and FM

Three LIA_S boards make up the LIA spectrometer section.

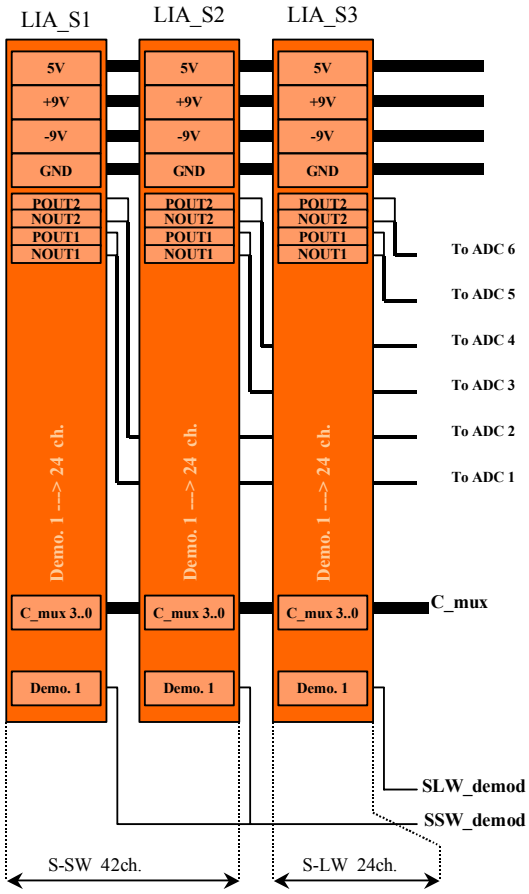
- LIA_S1 and LIA_S2 receive and process signals from forty-two "S-SW bolometers."
- LIA_S3 receive and process signals from twenty-four "S-LW bolometers."



Picture 4-16 Spectrometer Functional Links

The 24 SLW channels receive the same sinus bias signal (the same frequency and the same amplitude) and the same square demodulation signal (SLW_demod.)
All of the 24 channels be sent to the DAQ+IF board through two differential links that are digitized by two ADCs.

The 42 SSW channels + six spare channels receive the same sinus bias signal (the same frequency and the same amplitude) and the same square demodulation signal (SSW_demod.)
All of the 42 channels are sent to the DAQ+IF board through four differential links that are digitized by four ADCs.



Picture 4-17 LIA Spectrometer Section

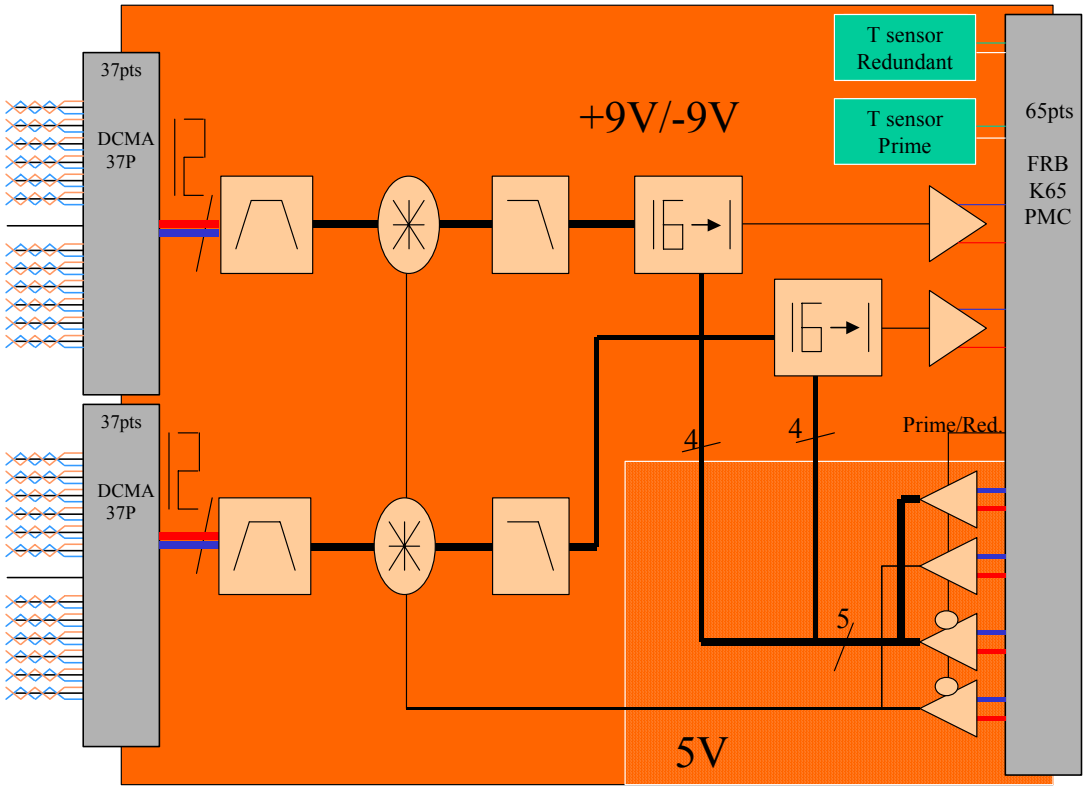
Each group receive its own respective demodulation signal: SSW_demod and SLW_demod. These signals can each have a different phase shift.

The LIA spectrometer is supplied only when the SPIRE instrument is running in spectrometer mode.

Each LIA spectrometer board receive its own group of 3 supply lines (-9V, +9V and 5V) which are automatically shutdown if a error occurs in on one of these three lines.

4.1.5 LIA SPECTROMETER BOARD

4.1.5.1 LIA Spectrometer Board Overview



Picture 4-18 LIA Spectrometer Board Overview

•Each LIA_S board has twenty-four channels which are divided into two groups.
Each group of 12 channels goes to a multiplexer.

•The two groups receive the same demodulation signal.

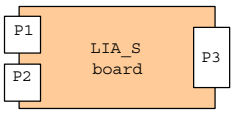
•The receivers that relay the multiplexer command signal and demodulation signal are redundant as they are on the LIA photometer boards.

•The two multiplexers receive the same command signals.

4.1.5.2 LIA Spectrometer Board Interface

connector	P1		
type	DCMA 37 P		
pin	signal name	pin	signal name
1	SHLD1		
2	IN-1	20	IN+1
3	IN+2	21	SHLD2
4	SHLD3	22	IN-2
5	IN-3	23	IN+3
6	IN+4	24	SHLD4
7	SHLD5	25	IN-4
8	IN-5	26	IN+5
9	IN+6	27	SHLD6
10	GND	28	IN-6
11	IN+7	29	IN-7
12	IN-8	30	SHLD7
13	SHLD8	31	IN+8
14	IN+9	32	IN-9
15	IN-10	33	SHLD9
16	SHLD10	34	IN+10
17	IN+11	35	IN-11
18	IN-12	36	SHLD11
19	SHLD12	37	IN+12

connector	P2		
type	DCMA 37 P		
pin	signal name	pin	signal name
1	SHLD13		
2	IN-13	20	IN+13
3	IN+14	21	SHLD14
4	SHLD15	22	IN-14
5	IN-15	23	IN+15
6	IN+16	24	SHLD16
7	SHLD17	25	IN-16
8	IN-17	26	IN+17
9	IN+18	27	SHLD18
10	GND	28	IN-18
11	IN+19	29	IN-19
12	IN-20	30	SHLD19
13	SHLD20	31	IN+20
14	IN+21	32	IN-21
15	IN-22	33	SHLD21
16	SHLD22	34	IN+22
17	IN+23	35	IN-23
18	IN-24	36	SHLD23
19	SHLD24	37	IN+24



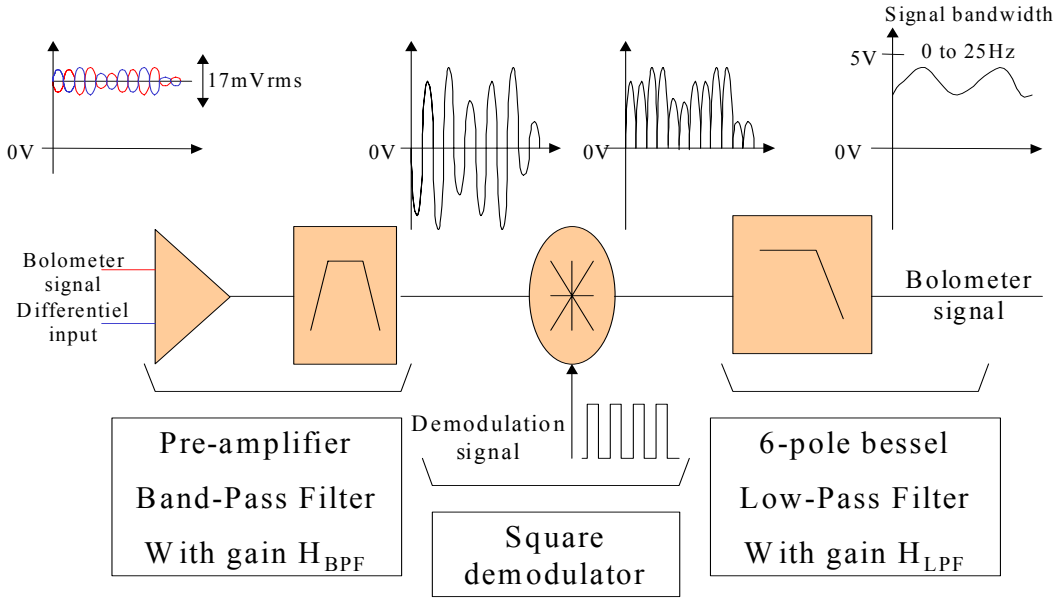
connector	P3		
type	KNB 65		
pin	signal name	pin	signal name
1	gnd		
3	NOUT1	2	POUT1
5	NOUT2	4	POUT2
7	gnd	6	gnd
9	N9V	8	N9V
11	P9V	10	P9V
13	P9V_P	12	P9V_P
15	gnd	14	gnd
17	PA0-	16	RA0-
19	PA0+	18	RA0+
21	PA1-	20	RA1-
23	PA1+	22	RA1+
25	PA2-	24	RA2-
27	PA2+	26	RA2+
29	PA3-	28	RA3-
31	PA3+	30	RA3+
33	P5V	32	P5V
35	gnd	34	gnd
37	PDEMOD1-	36	RDEMOD1-
39	PDEMOD1+	38	RDEMOD1+
41	gnd	40	gnd
43	gnd	42	gnd
45	-	44	-
47	-	46	-
49	-	48	-
51	-	50	-
53	-	52	-
55	-	54	-
57	-	56	-
59	RT P9V	58	RT P9V
61	RT	60	RT
63	PT_P9V	62	PT_P9V
65	PT	64	PT

Picture 4-19 LIA Spectrometer Board Interface

Name	Description	Type	Level	In/Out	Frequency
IN+ xx	Bolometer Differential Signal	Analogic	11mVrms (AC) + 1.5V (DC)	IN	50-300Hz
IN- xx					
POUT x	The twelve LIA_S channels Multiplexed in a Differential Signal	Analogic	0 to 5V	OUT	0-25Hz at mux freq.
NOUT x					
PAx-	BIT Command Mux (PRIME) Differential Signal	Numeric	-0,3Vto 0,3V	IN	~2.5kHz
PAx+					
RAx-	BIT Command Mux (REDUNDANT) Differential Signal	Numeric	-0,3Vto 0,3V	IN	~2.5kHz
RAx+					
PDEMOD1-	Demodulation Differential Signal (PRIME) for Channels One to Twenty-four	Numeric	-0,3Vto 0,3V	IN	50-300Hz
PDEMOD1+					
RDEMOD1-	Demodulation Differential Signal (REDUNDANT) for Channels One to Twenty-four	Numeric	-0,3Vto 0,3V	IN	50-300Hz
RDEMOD1+					
PT_P9V	Sensor PRIME Bias	Analogic	9V	IN	DC
PT	Output Sensor PRIME	Analogic	2 to 4V	OUT	-
RT_P9V	Sensor REDUNDANT Bias	Analogic	9V	IN	DC
RT	Output Sensor REDUNDANT	Analogic	2 to 4V	OUT	-
P9V	9V Power Supply	Power	9V	IN	DC
N9V	-9V Power Supply	Power	-9V	IN	DC
P9V_P	PRIME/REDUNDANT Signal	Analogic	0 to 9V	IN	DC
P5V	5V Power Supply	Power	5V	IN	DC
GND	Grounding	Power	0V	-	DC

4.1.6 LIA SPECTROMETER CHANNELS

4.1.6.1 LIA Spectrometer Channel Overview

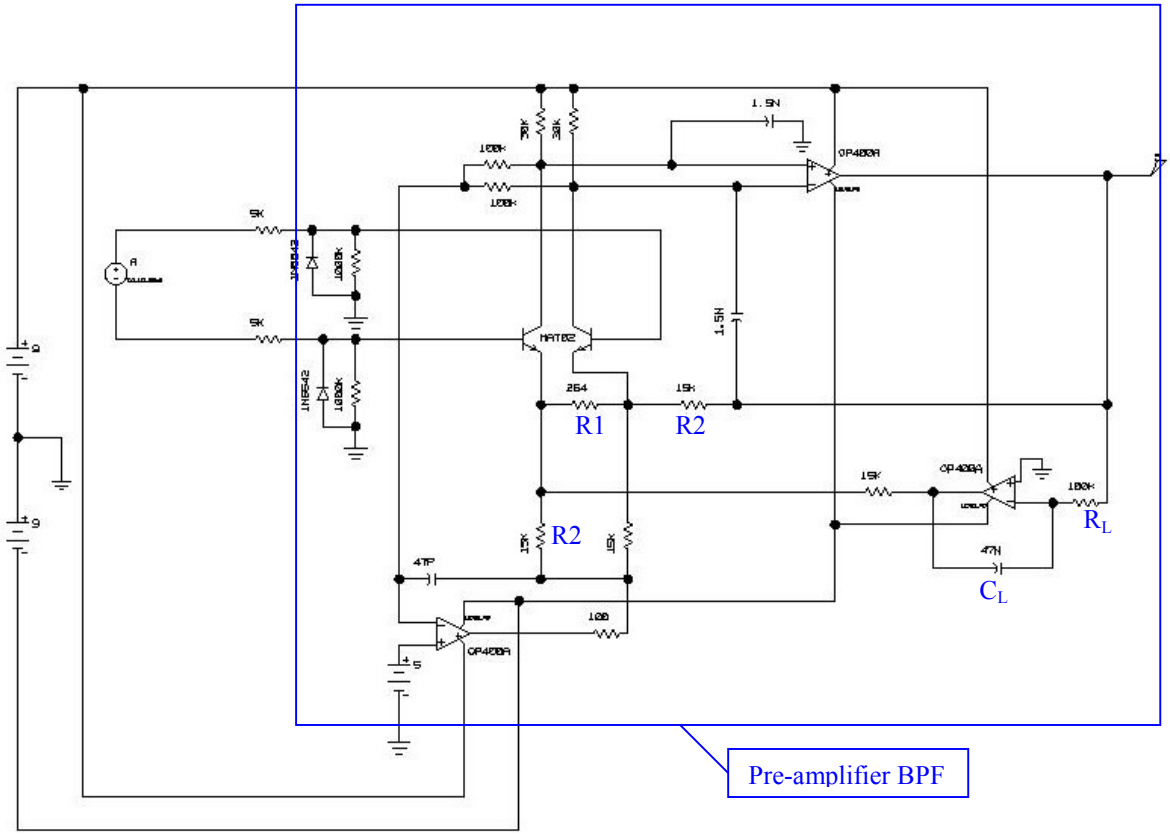


The input differential signal that comes from a bolometer is amplified and its DC component is eliminated by the pre-amplifier BPF. Then, it is demodulated by a squared signal. Afterwards it is filtered by a six-pole Bessel LPF.

The six-pole bessel low pass filters have a structural gain of H_{LPF} = 2,87
The square demodulation introduces a gain of $2/\pi$
Note: To be sure that a photometer channel won't be saturated with a 17mVrms input, the output signal cannot not be more than 5V.

This is why the band pass filter gain H_{BPF} cannot be more than $\frac{5V}{17mV.\frac{2\sqrt{2}}{\pi}.2,87}=114$

4.1.6.2 LIA Spectrometer Channel BPF



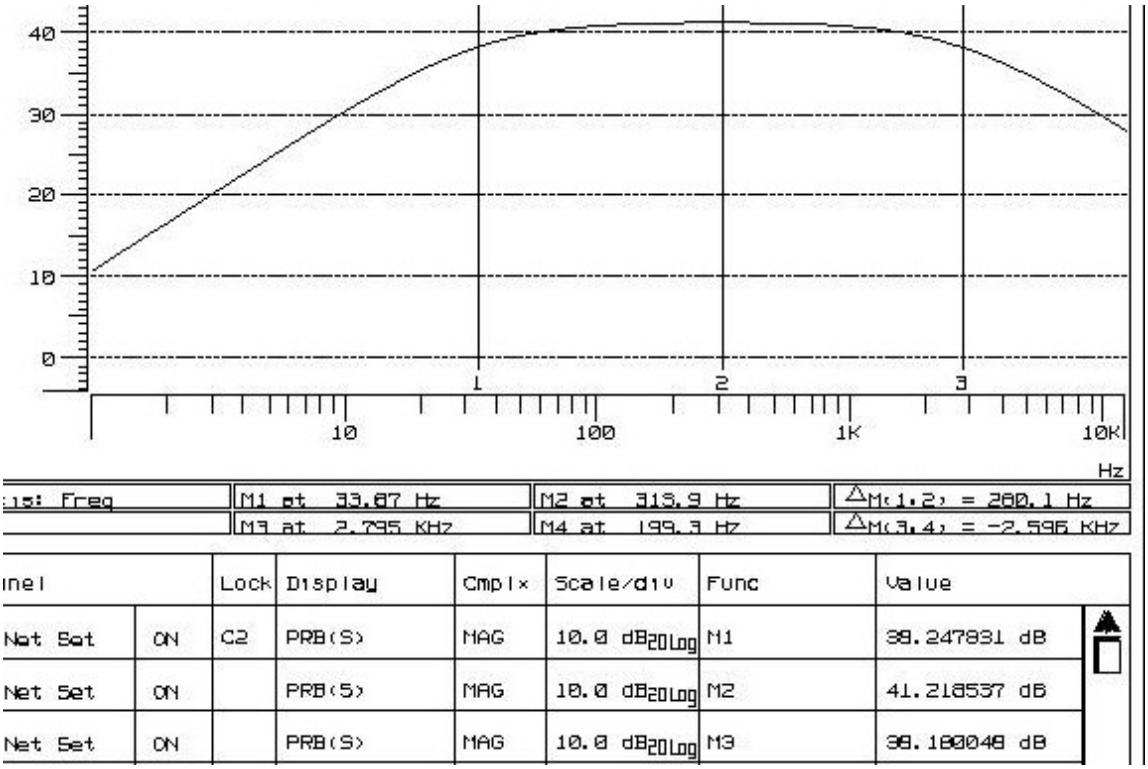
Picture 4-20 LIA Spectrometer Pre-amplifier BPF

The gain of this pre-amplifier is found by employing the following calculation: 2xR2/R1 = 2x15K/263 = 114.

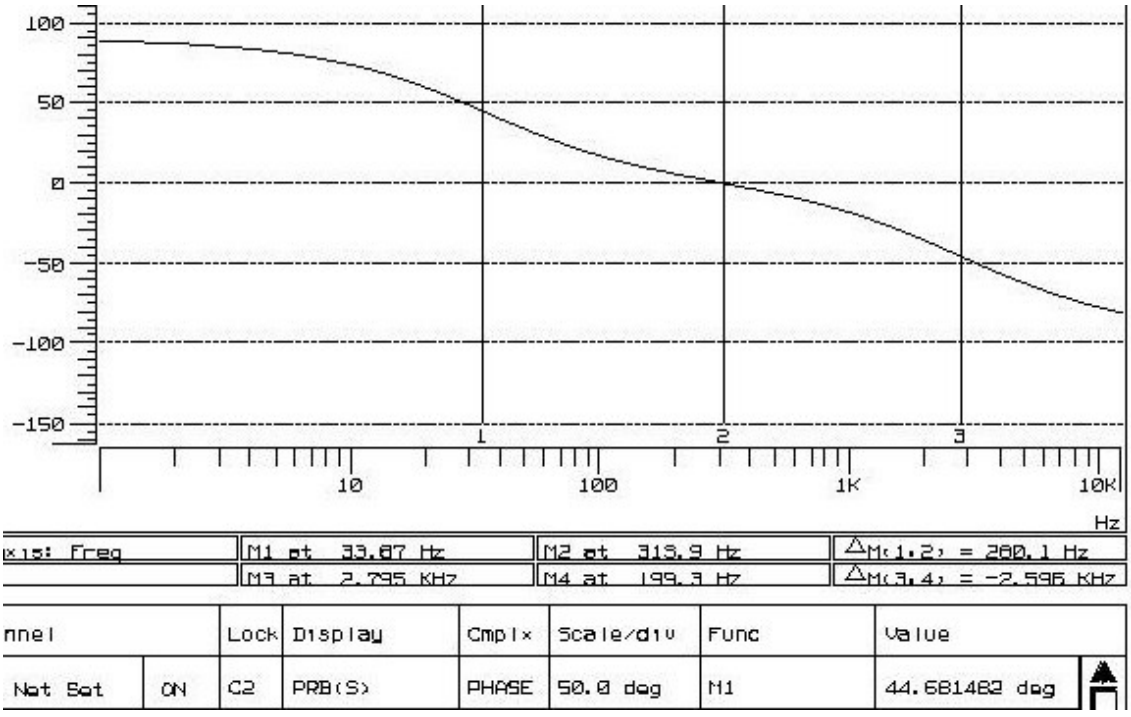
The BPF's low frequency cut-off is found by employing the following calculation:

$$F_{CL}=\frac{1}{2\pi.R_L.C_L}=\frac{1}{2\pi.100Kx47nF}=33,8Hz$$

The two following simulation results show respectively the magnitude and the phase transfer function of LIA Spectrometer Pre-amplifier BPF:

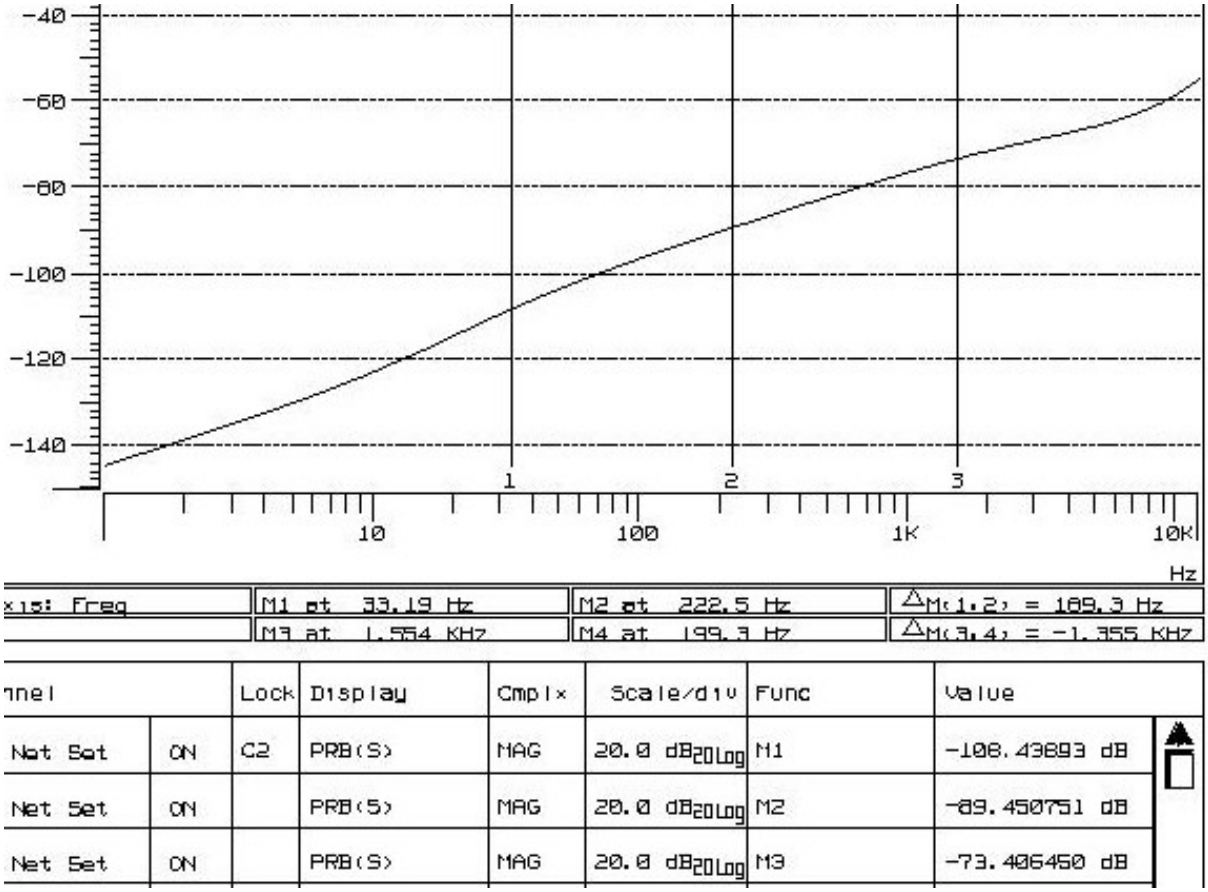


Picture 4-21 LIA Spectrometer Pre-amplifier BPF Magnitude Transfer Function



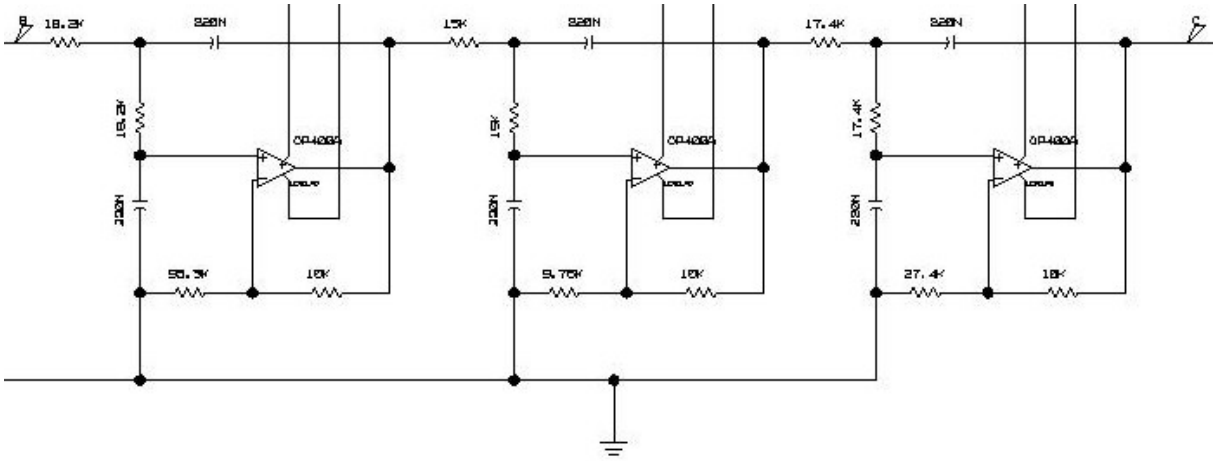
Picture 4-22 LIA Spectrometer Pre-amplifier BPF Phase Transfer Function

The following simulation result shows the common mode transfer function. It shows that we have at least –80dB common mode rejection between 50Hz and 300Hz.
In other words, there is some leeway with the –60dB requirement.



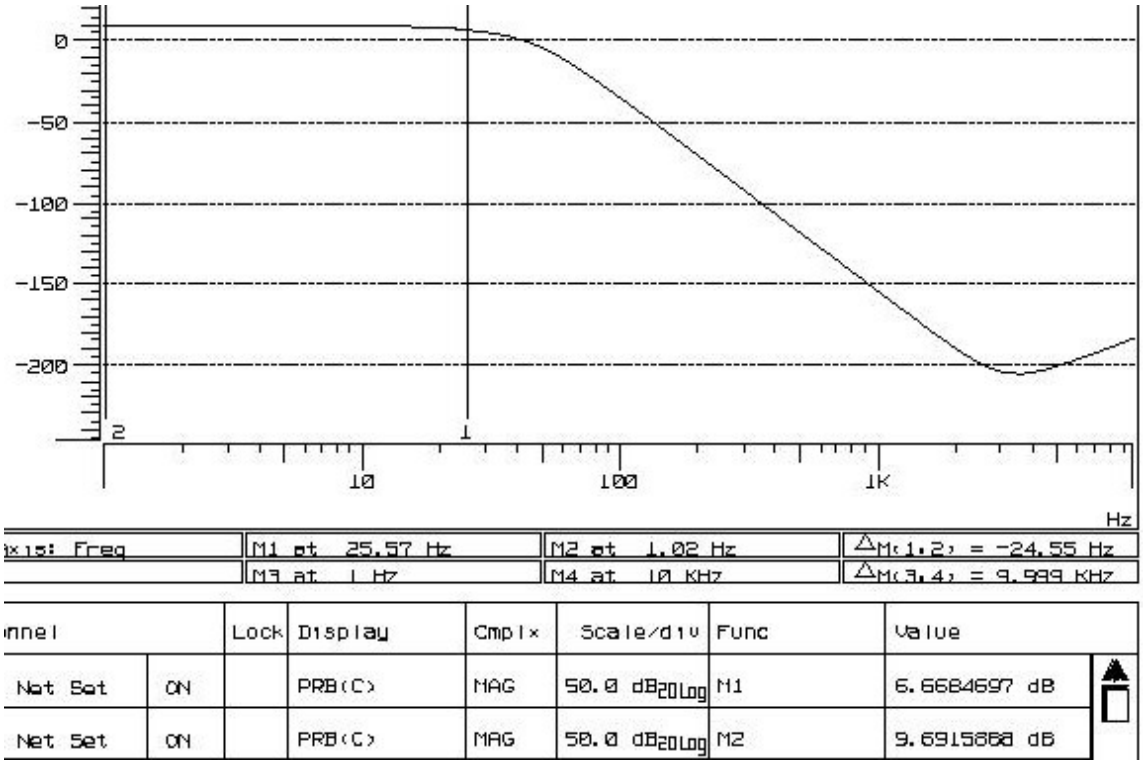
Picture 4-23 LIA Spectrometer Pre-amplifier BPF Common Mode Rejection

4.1.6.3 LIA Spectrometer Channel LPF

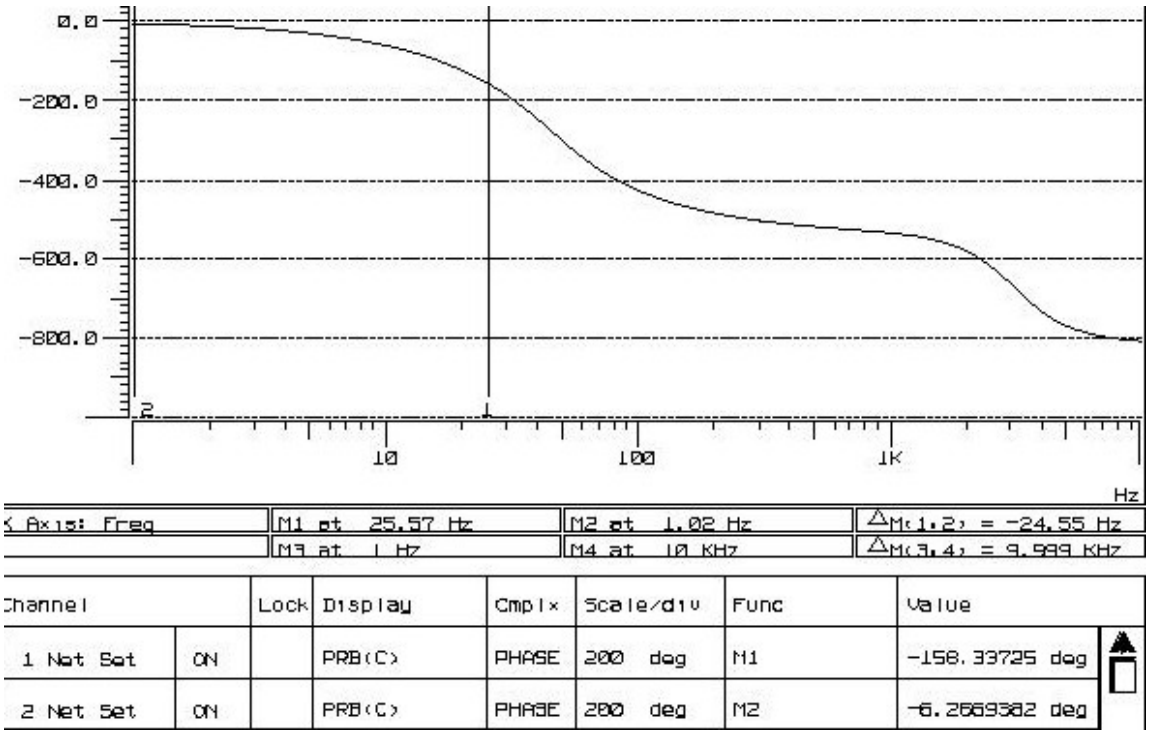


Picture 4-24 LIA Spectrometer Pre-amplifier BPF

The two following simulation results show respectively the magnitude and the phase transfer function of LIA Spectrometer six-pole Bessel LPF:



Picture 4-25 LIA Spectrometer LPF Magnitude Transfer Function



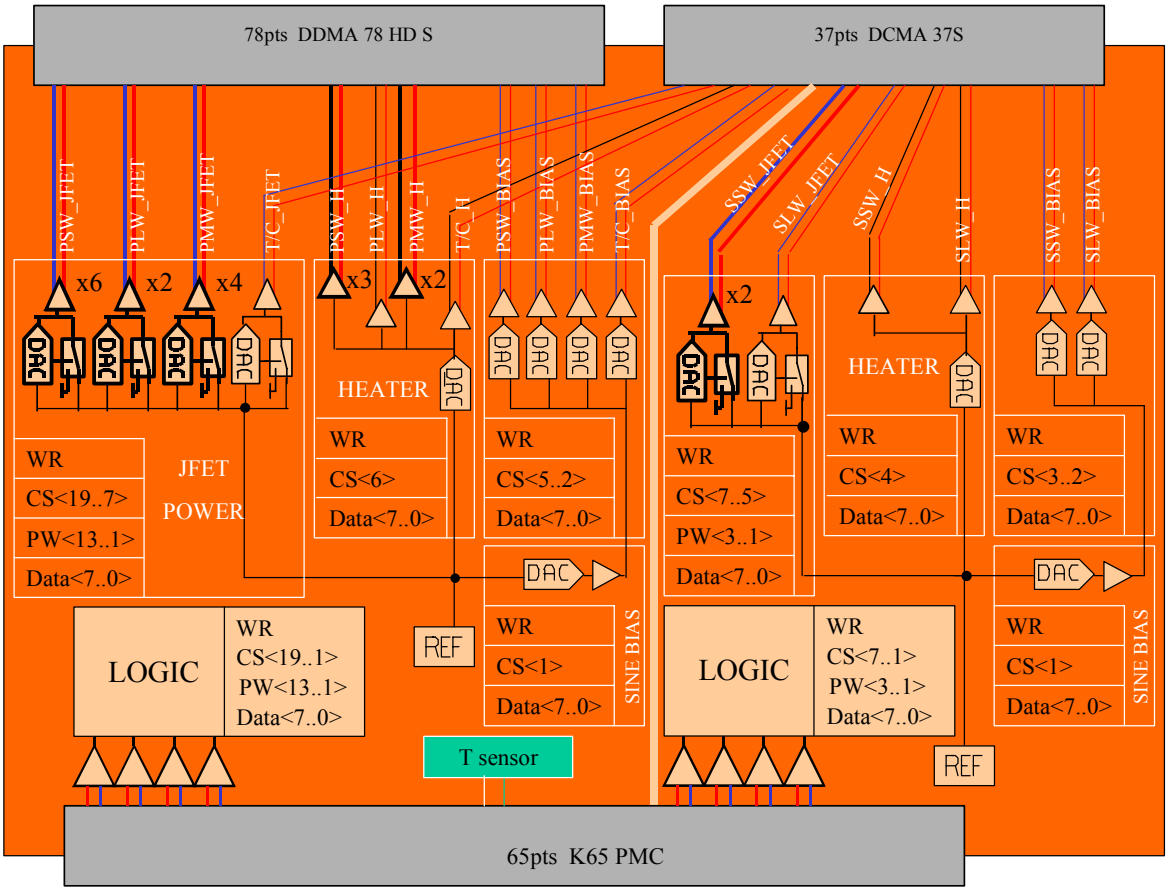
Picture 4-26 LIA Spectrometer LPF Phase Transfer Function

4.1.6.4 LIA Photometer Channel Input Noise

TBW

4.1.7 BIAS BOARDS

4.1.7.1 BIAS Board Overview



Picture 4-27 BIAS Board Overview

The BIAS boards generate sine biases for the bolometers and DC biases for JFETs and heaters.

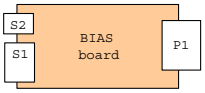
- •Adjustable sine biases:
  - –Photometer: 1sine generator/ 4 channels with independent amplitudes
  - –Spectrometer: 1sine generator/ 2 channels with independent amplitudes
  - –Voltage range: 0 to 200 mVrms for the bolometers 0 to 500 mVrms for the thermometers
  - –Accuracy: 256 levels
  - –Frequency range: 50 to 300Hz
- •Adjustable DC JFET biases:
  - –Photometer: 13 generators for JFET
  - –Spectrometer: 3 generators for JFET
  - –Voltage range: 0 to –5V for VSS with 256 levels and VDD is set between 0 and 4V by two resistors
  - –Output currents: 5mA max
- •Adjustable DC heater biases:
  - –Photometer: 1heater generator and 7 buffers
  - –Spectrometer: 1 heater generator and 3 buffers
  - –Voltage range: 0 to –5V with 256 levels
  - –Output currents: 5mA max for each buffer

Note: Each buffer biases at most 2 JFET module* heaters. (*JFETmodule = 24 channels)

4.1.7.2 BIAS Board Interface

connector	S1						
type				DDMA 78 HD S			
pin	signal name	pin	signal name	pin	signal name	pin	signal name
1	VDD_PSW1	21	GND_P	40	GND_P	60	VSS_PSW4
2	VSS_PSW1	22	GND_P	41	VDD_PSW4	61	VDD_PSW5
3	VDD_PSW2	23	VSS_PSW2	42	GND_P	62	VSS_PSW5
4	VDD_PSW3	24	GND_P	43	GND_P	63	VDD_PSW6
5	VSS_PSW3	25	GND_P	44	VSS_PSW6	64	NBIAS_PSW
6	PBIAS_PSW	26	NBIAS_PSW	45	GND_P	65	PBIAS_PSW
7	GND_P	27	GND_P	46	GND_P	66	NBIAS_PSW
8	Pheater_PSW1	28	GND_P	47	PBIAS_PSW	67	Nheater_PSW3
9	Nheater_PSW1	29	Pheater_PSW2	48	GND_P	68	Pheater_PSW3
10	VDD_PMW1	30	GND_P	49	Nheater_PSW2	69	VDD_PMW3
11	VSS_PMW1	31	VSS_PMW2	50	GND_P	70	VSS_PMW3
12	VDD_PMW2	32	GND_P	51	GND_P	71	VDD_PMW4
13	PBIAS_PMW	33	GND_P	52	VSS_PMW4	72	NBIAS_PMW
14	NBIAS_PMW	34	GND_P	53	GND_P	73	PBIAS_PMW
15	Nheater_PMW1	35	GND_P	54	Pheater_PMW2	74	Nheater_PMW2
16	Pheater_PMW1	36	VDD_PLW1	55	GND_P	75	PBIAS_PLW1
17	VSS_PLW1	37	GND_P	56	GND_P	76	NBIAS_PLW1
18	VDD_PLW2	38	GND_P	57	NBIAS_PLW2	77	PBIAS_PLW2
19	VSS_PLW2	39	Nheater_PLW1	58	GND_P	78	GND_P
20	Pheater_PLW1			59	GND_P		

connector	S2		
type	DCMA 37 S		
pin	signal name	pin	signal name
1	PBIAS_T/C		
2	GND_P	20	NBIAS_T/C
3	VDD_T/C	21	VSS_T/C
4	GND_P	22	Pheater_T/C
5	Nheater_T/C	23	GND_P
6	NBIAS_S-LW	24	PBIAS_S-LW
7	GND_S	25	VDD1_S-LW
8	VSS1_S-LW	26	GND_S
9	GND_S	27	GND_S
10	NBIAS_S-SW	28	PBIAS_S-SW
11	GND_S	29	NBIAS_S-SW
12	PBIAS_S-SW	30	GND_S
13	VSS1_S-LW	31	VDD1_S-LW
14	VDD2_S-SW	32	GND_S
15	GND_S	33	VSS2_S-SW
16	Nheater_SLW	34	Pheater_SLW
17	GND_S	35	GND_S
18	Nheater_SSW	36	Pheater_SSW
19	Nheater_SSW	37	Pheater_SSW



connector	P1		
type	KNB65		
pin	signal name	pin	signal name
1	T		
3	T_P9V	2	T_P9V
5	wr_data_p+	4	wr_data_p+
7	wr_data_p-	6	wr_data_p-
9	wr_address_p+	8	wr_address_p+
11	wr_address_p-	10	wr_address_p-
13	clk_p+	12	clk_p+
15	clk_p-	14	clk_p-
17	sdata_p+	16	sdata_p+
19	sdata_p-	18	sdata_p-
21	P9V_P	20	P9V_P
23	P9V_P	22	P9V_P
25	GND_P	24	GND_P
27	GND_P	26	GND_P
29	N9V_P	28	N9V_P
31	N9V_P	30	N9V_P
33	GND_P	32	GND_P
35	GND_S	34	GND_S
37	P9V_S	36	P9V_S
39	P9V_S	38	P9V_S
41	GND_S	40	GND_S
43	GND_S	42	GND_S
45	N9V_S	44	N9V_S
47	N9V_S	46	N9V_S
49	wr_data_s+	48	wr_data_s+
51	wr_data_s-	50	wr_data_s-
53	wr_address_s+	52	wr_address_s+
55	wr_address_s-	54	wr_address_s-
57	clk_s+	56	clk_s+
59	clk_s-	58	clk_s-
61	sdata_s+	60	sdata_s+
63	sdata_s-	62	sdata_s-
65	GND_S	64	GND_S

Picture 4-28 BIAS Board Interface

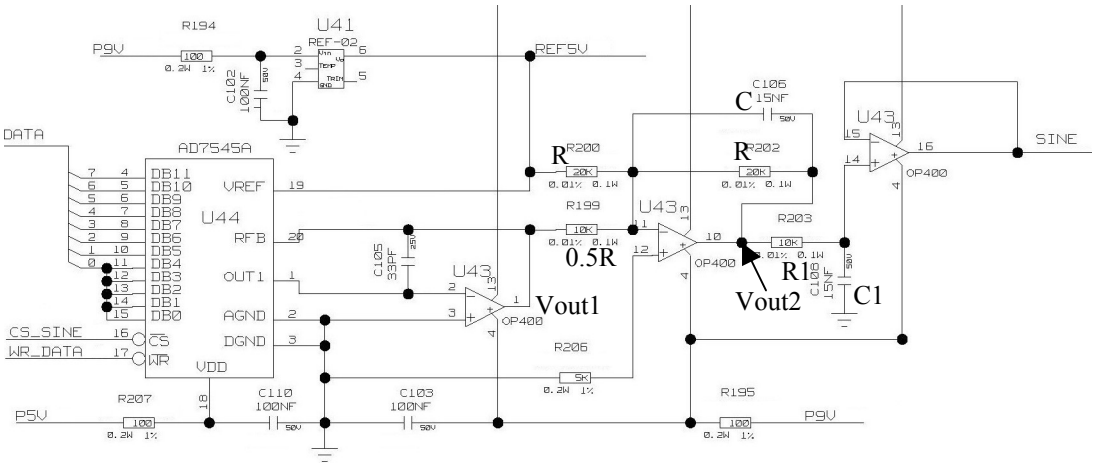
Name	Description	Type	Level	In/Out	Frequency

TBW

4.1.8 BIAS BOARD FUNCTIONS

4.1.8.1 Bolometer BIAS

The following circuit is used to generate a sinusoidal signal with amplitude of 5V and a 0Vcenter.
There are two identical sine generators on the BIAS board (1for the photometer and 1 for the spectrometer.)



Picture 4-29 Sine Generator

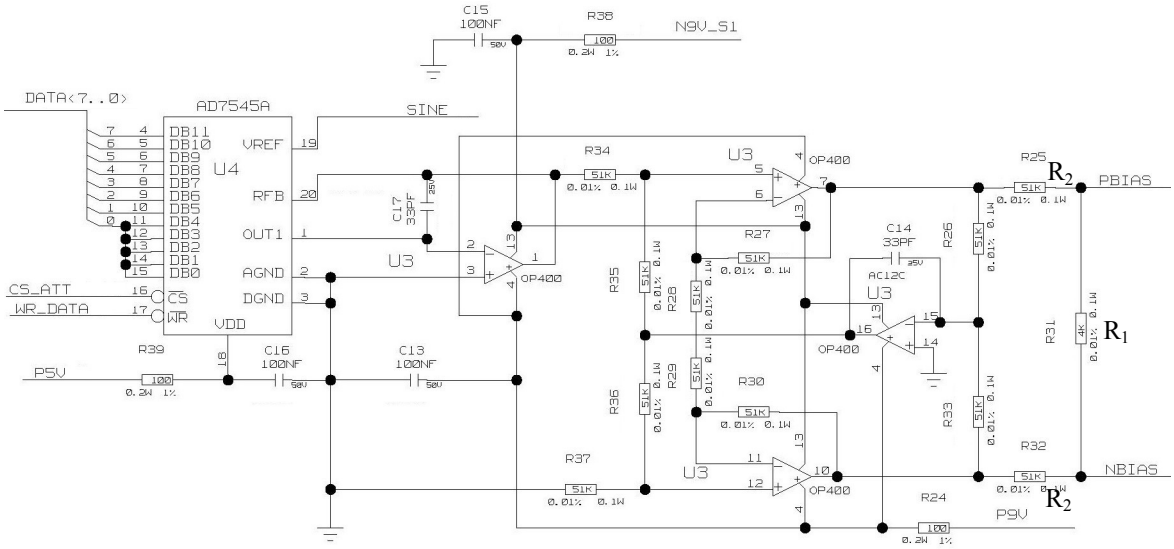
- From a +5V precision voltage reference, the DAC and the first OP generate a tension proportional to the numeric 8 bits signal DATA: ***Vout1 = -REF5V(DATA/256).***
- The second OP adds half the reference voltage to ***Vout1*** and multiplies the result by 2 as well as filters: ***Vout2=REF5V(1-DATA/128)/(1+jω/ ωc)*** with ω_c ***=1/RC => Fc=530Hz***
- Afterward the signal go through another low pass filter: ***SINE= Vout2/(1+jω/ωc1)*** with ***ωc1 =1/R1C1 => Fc1=1061Hz***

DATA is an integer between 0 and 255
To generate sinusoidal signal (SINE) with frequency **Fsine** the 256 integers, which describe a sine, should be wrote in the digital to analog converter with a frequency for **256.Fsine**.
The 256 values can be calculated by taken the nearest integer of [***127.SIN(2π(n+1/2)/256)+128***] with ***n*** between ***0*** and ***255***.

Each bolometer group has his own bias attenuator.

- The 4 bias attenuators of the photometer receive at their input the signal coming from the photometer sine generator.
- As well as The 2 bias attenuators of the spectrometer receive at their input the signal coming from the spectrometer sine generator.

The bias attenuator circuit is as follow:

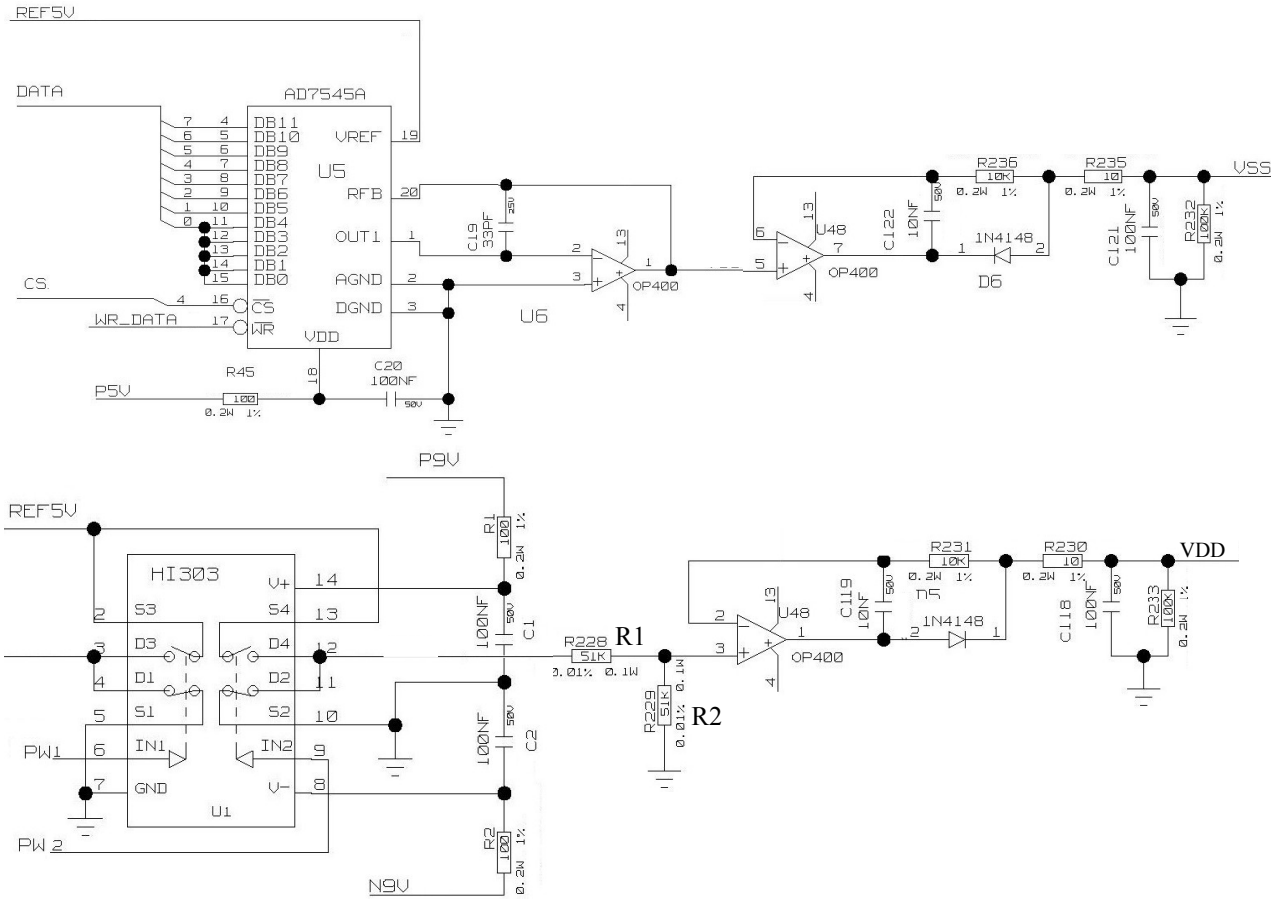


Picture 4-30 Bias Attenuator

- From the output of a sine generator (SINE) the DAC and the first OP generate a tension proportional to the numeric 8 bit signal DATA: ***Vout1 = -SINE(DATA/256).***
- The three others OP make the signal differential with a 0Vcenter by filtering the DC component.
- The 3 last resistors divide the differential signal by $\frac{R_1/2}{2.R_2+R_1/2}$ if the redundant and prime bias boards are connected together or by $\frac{R_1}{2.R_2+R_1}$ if they are not.

4.1.8.2 JFET BIAS

Each JFET module has its own bias generator. A JFET bias generator provide a negative DC tension VSS and a positive DC tension VDD



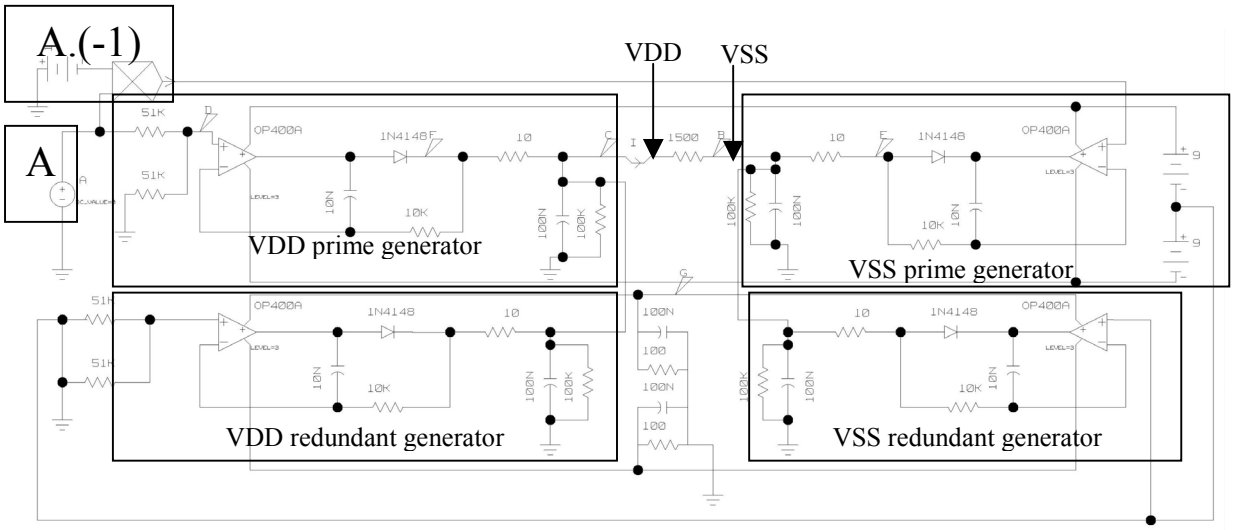
Picture 4-31 JFET Bias Generator

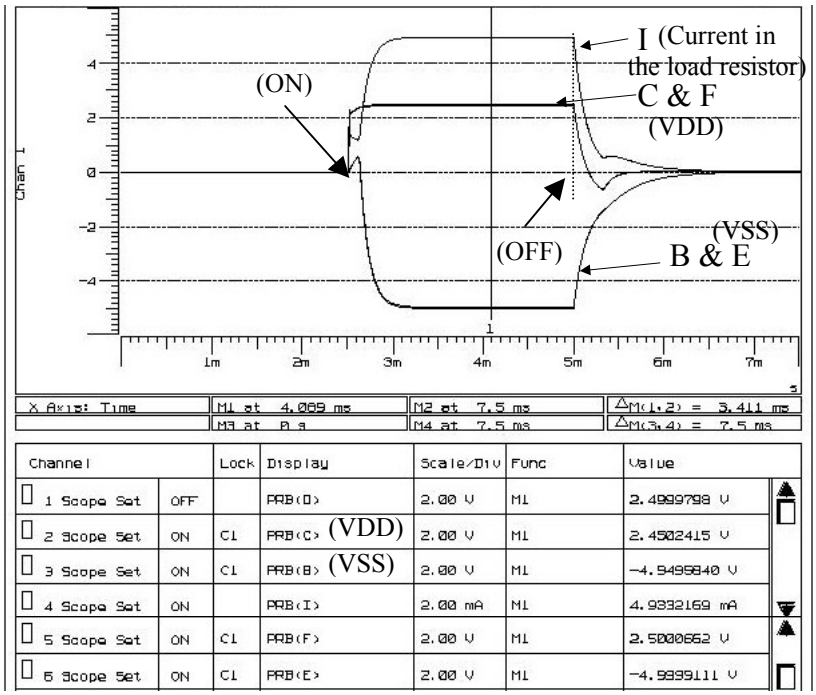
- VSS generator:
  - From a +5V precision voltage reference, the DAC and the first OP generate a tension proportional to the digital 8 bits DATA: ***VSS = -REF5V(DATA/256).***
  - The second OP and his following components are there to:
    - Avoid overshoot when VSS is set ON from OFF or the other way
    - Make the connection with the empowered redundant bias board safe and use full
    - Provide the 5mA required.
- VDD generator:
  - When the switch is **ON** a +5V precision voltage reference is applied on two resistors R1 and R2 so ***VDD = REF5V.R2/(R1+R2).***
  - When the switch is **OFF** the ground is applied on two resistors R1 and R2 so ***VDD= 0V.***
  - The second OP and his following components are there to:
    - Avoid overshoot when VDD is set ON from OFF or the other way
    - Make the connection with the empowered redundant bias board safe and use full
    - Provide the 5mA required.

The following simulation shows the switching ON and OFF of VSS, VDD.

- VSS switched ON 0V to –5V. (A=5V)
- VSS switched OFF -5V to 0V. (A=0V)
- VDD switched ON 0V to 2.5V. (A=5V)
- VDD switched OFF 2.5V to 0V. (A=0V)

The prime generators are powered, the redundant ones are not.
The load resistor is set for a nominal generator output current of 5mA.





Picture 4-32 JFET Bias Generator Simulation

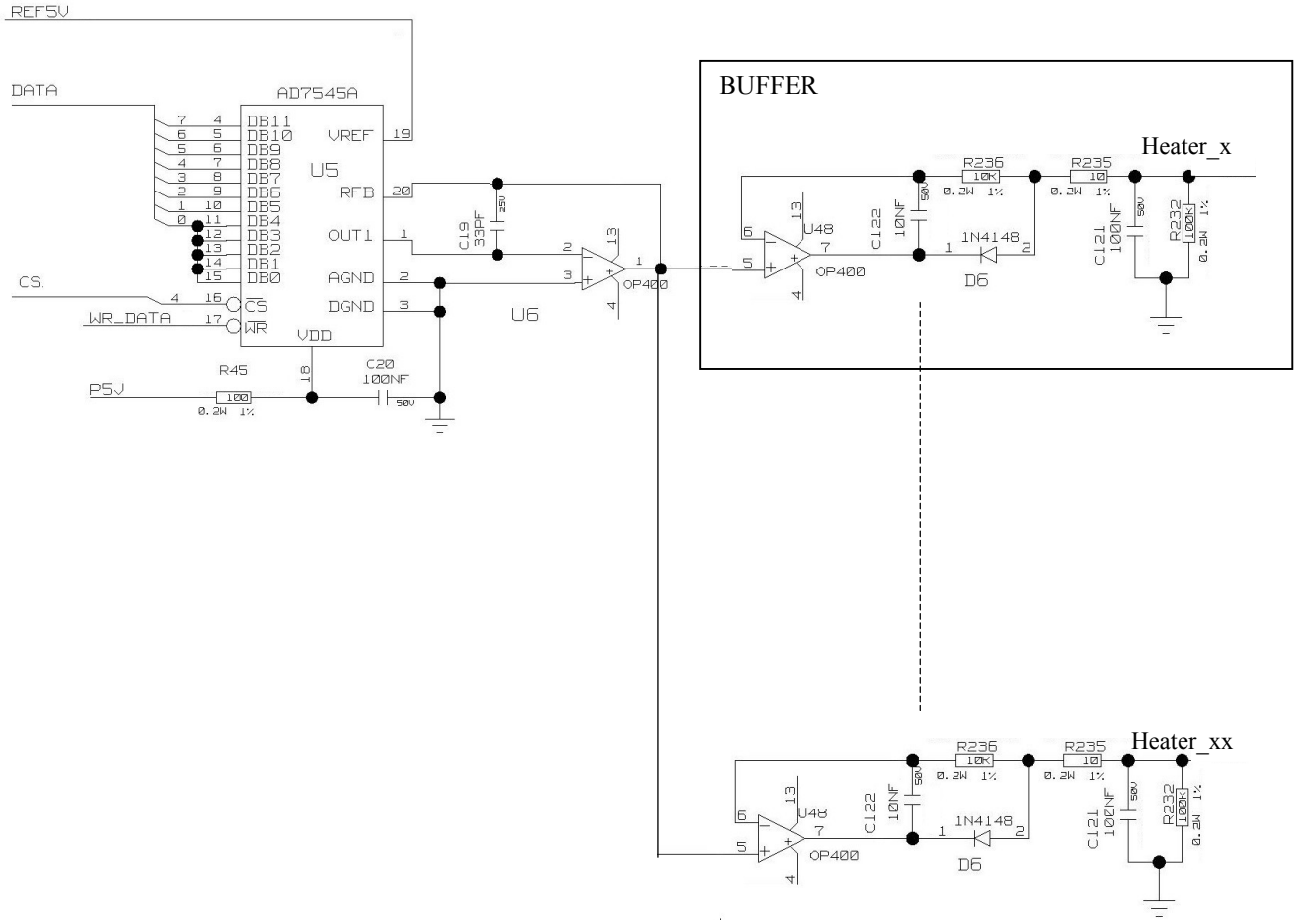
4.1.8.3 Heater

To bias the photometer heaters there are:

- A bias generator and 7 buffers (the buffer heater is similar to a VSS buffer) of which:
  - each 6 buffers bias each 2 JFET module heaters
  - 1 buffer biases only the T/C JFET module

To bias the spectrometer heaters there are:

- A bias generator and 2 buffers (the buffer heater is similar to a VSS buffer) of which:
  - 1 buffer biases 2 JFET module heaters
  - 1 buffer biases only 1 JFET module heater

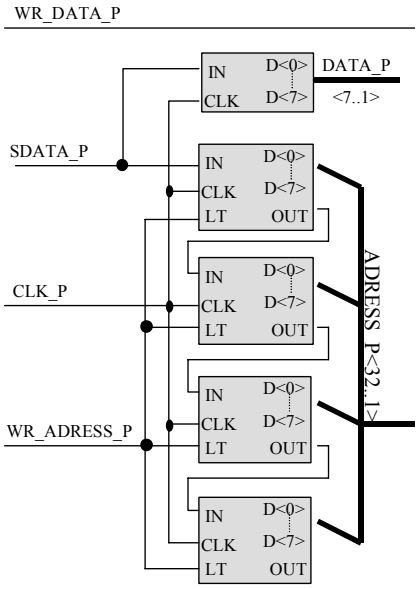


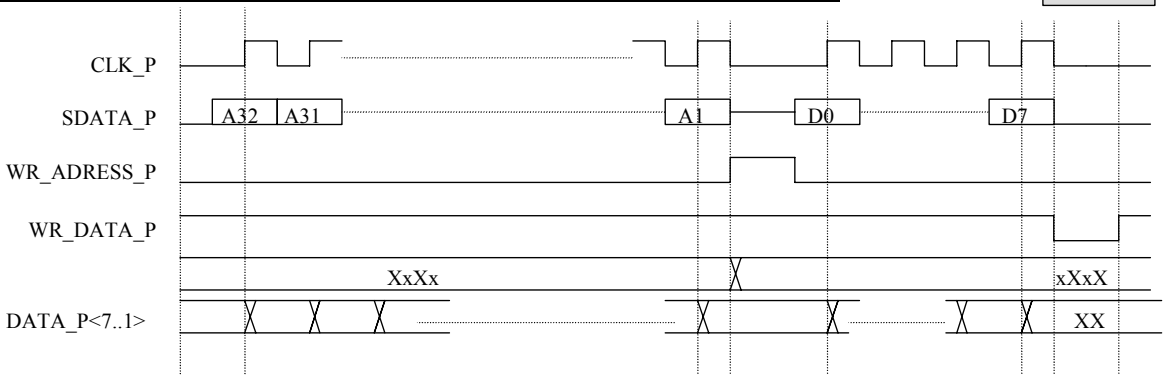
Picture 4-33 Heater Bias Generator

4.1.8.4 Commands

- All of the photometer ADCs CS (chips select) and ON/OFF switches are connected to four 8-bit latched SIPO (Serial Input to Parallel Output) shift registers.
- The 17 photometer ADCs are connected to the same write signal WR_DATA_P.
- The four 8-bit latch SIPO shift registers are connected to the same latch signal WR_ADRESS_P
- The photometer 8-bit parallel DATA_P bus is provided by one SIPO shift register.

BIT number	Command	BIT number	Command
A1	CS Sine bias generator	A17	CS VSS12_P
A2	CS PSW bias attenuator	A18	ON/OFF VDD1_P
A3	CS PLW bias attenuator	A19	ON/OFF VDD2_P
A4	CS T/C bias attenuator	A20	ON/OFF VDD3_P
A5	CS PMW bias attenuator	A21	ON/OFF VDD4_P
A6	CS VSS1_P	A22	ON/OFF VDD5_P
A7	CS VSS2_P	A23	ON/OFF VDD6_P
A8	CS VSS3_P	A24	ON/OFF VDD7_P
A9	CS VSS4_P	A25	ON/OFF VDD8_P
A10	CS VSS5_P	A26	ON/OFF VDD9_P
A11	CS VSS6_P	A27	ON/OFF VDD10_P
A12	CS VSS7_P	A28	ON/OFF VDD11_P
A13	CS VSS8_P	A29	ON/OFF VDD12_P
A14	CS VSS9_P	A30	CS HEATER_P
A15	CS VSS10_P	A31	ON/OFF VDD_TC
A16	CS VSS11_P	A32	CS VSS_TC

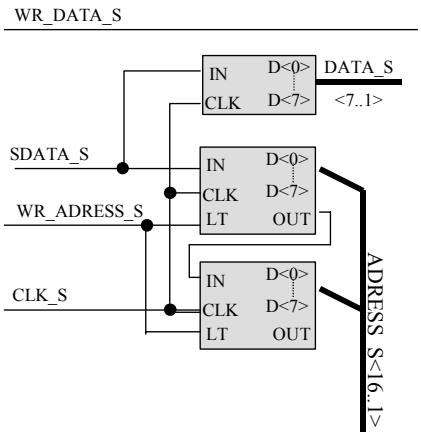


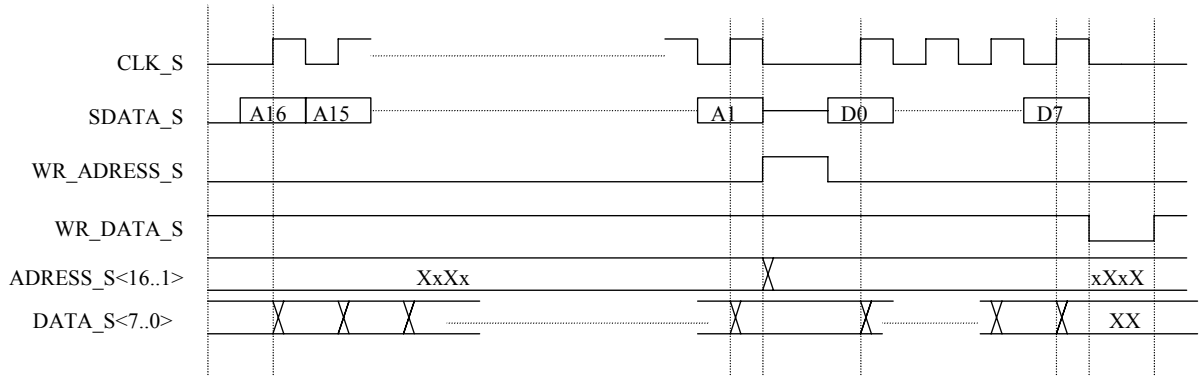


Picture 4-34 Photometer Bias Command

- All of the spectrometer ADCs chips select and ON/OFF switches are connected to two 8-bit latch SIPO (Serial Input to Parallel Output) shift registers.
- The 7 spectrometer ADCs are connected to the same write signal WR_DATA_S.
- The two 8-bit latch SIPO shift registers are connected to the same latch signal WR_ADRESS_S
- The spectrometer 8-bit parallel DATA_S bus is provided by SIPO shift register.

BIT number	Command	BIT number	Command
A1	CS Sine bias generator spectro	A9	ON/OFF VDD1_S
A2	CS SSW bias attenuator	A10	ON/OFF VDD2_S
A3	CS SLW bias attenuator	A11	ON/OFF VDD3_S
A4	CS VSS1_S	A12	-
A5	CS VSS2_S	A13	-
A6	CS VSS3_S	A14	-
A7	CS HEATER_S	A15	-
A8	-	A16	-





Picture 4-35 Spectrometer Bias Command

4.1.8.5 Bolometer Bias Noise

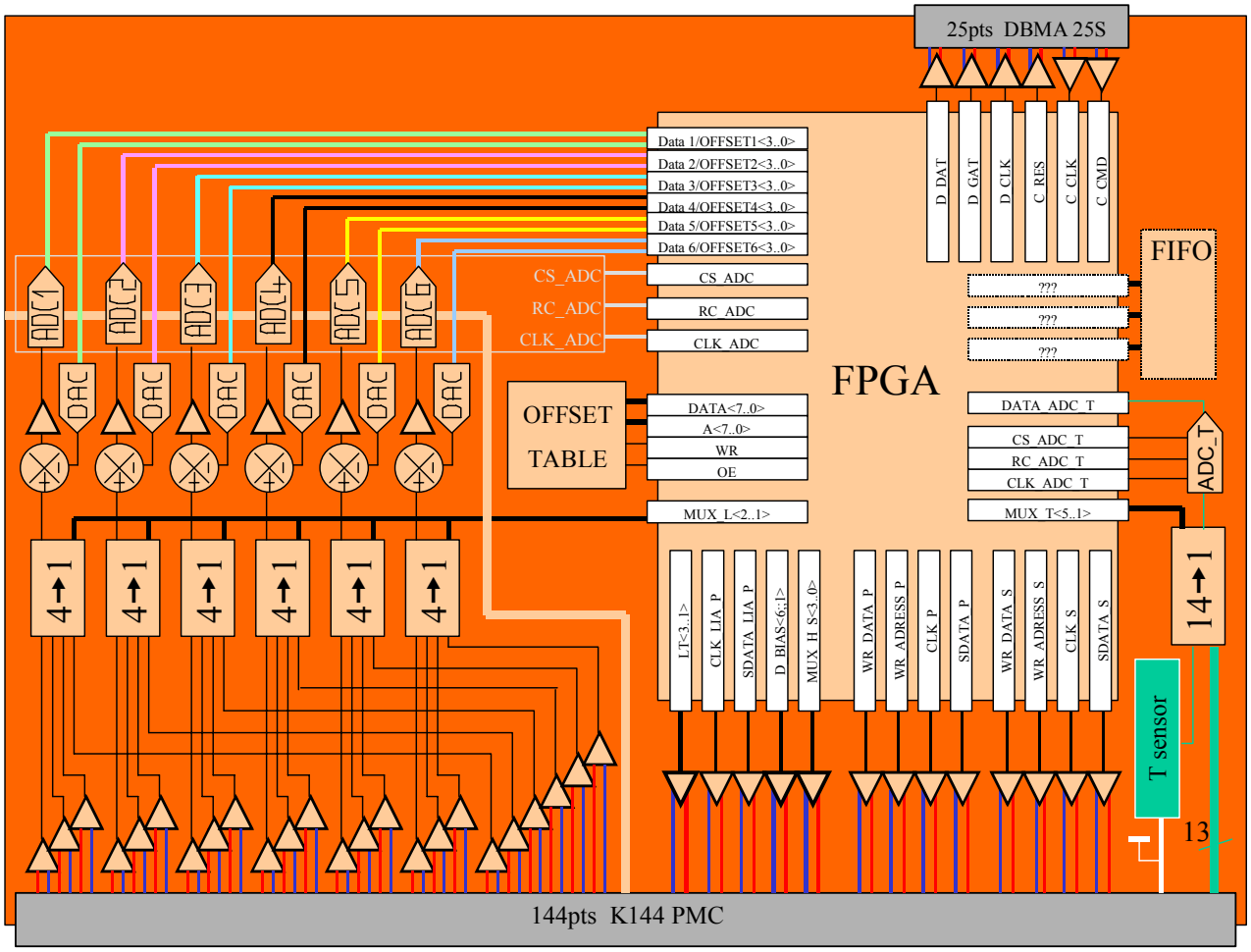
TBW

4.1.8.6 JFET BIAS Noise

TBW

4.1.9 DAQ+IF BOARD

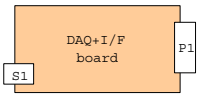
4.1.9.1 DAQ+IF Board Overview



Picture 4-36 DAQ+IF Board Overview

TBW

DAQ+IF Board Interface



connector	S1		
type	DBMA 25 S		
pin	signal name	pin	signal name
1	NC		
2	C_CLK_DCU_P+	14	C_SHD
3	C_CMD_DCU_P+	15	C_CLK_DCU_P-
4	C_RES_DCU_P+	16	C_CMD_DCU_P-
5	C_RES_SHD	17	C_RES_DCU_P-
6	NC	18	NC
7	NC	19	NC
8	D_CLK_DCU_P+	20	NC
9	D_CLK_SHD	21	D_CLK_DCU_P-
10	D_DAT_DCU_P+	22	D_DAT_DCU_P-
11	D_GAT_DCU_P+	23	D_GAT_DCU_P-
12	D_GAT_SHD	24	D_SHD
13	NC	25	NC

connector	P1				
type	KND144 1310 110				
pin	signal name	pin	signal name	pin	signal name
1	NOUTP250<1>	2	POUTP250<1>	3	gnd
4	NOUTP250<2>	5	POUTP250<2>	6	gnd
7	NOUTP250<3>	8	POUTP250<3>	9	gnd
10	NOUTP250<4>	11	POUTP250<4>	12	gnd
13	NOUTP250<5>	14	POUTP250<5>	15	gnd
16	NOUTP250<6>	17	POUTP250<6>	18	gnd
19	NOUTP250<7>	20	POUTP250<7>	21	gnd
22	NOUTP250<8>	23	POUTP250<8>	24	gnd
25	NOUTP250<9>	26	POUTP250<9>	27	gnd
28	NOUTP500<1>	29	POUTP500<1>	30	P5V
31	NOUTP500<2>	32	POUTP500<2>	33	T13
34	NOUTP500<3>	35	POUTP500<3>	36	T12
37	NOUTP350<1>	38	POUTP350<1>	39	T11
40	NOUTP350<2>	41	POUTP350<2>	42	T10
43	NOUTP350<3>	44	POUTP350<3>	45	T9
46	NOUTP350<4>	47	POUTP350<4>	48	T8
49	NOUTP350<5>	50	POUTP350<5>	51	T7
52	NOUTP350<6>	53	POUTP350<6>	54	T6
55	NOUTS-SW<1>	56	POUTS-SW<1>	57	T5
58	NOUTS-SW<2>	59	POUTS-SW<2>	60	T4
61	NOUTS-SW<3>	62	POUTS-SW<3>	63	T3
64	NOUTS-SW<4>	65	POUTS-SW<4>	66	T2
67	NOUTS-LW<1>	68	POUTS-LW<1>	69	T1
70	NOUTS-LW<2>	71	POUTS-LW<2>	72	P5V
73	gnd	74	gnd	75	gnd
76	N9V	77	N9V	78	N9V
79	N9V	80	N9V	81	N9V
82	P9V	83	P9V	84	P9V
85	P9V	86	P9V	87	P9V
88	gnd	89	gnd	90	gnd
91	P5V	92	P5V	93	P5V
94	P5V	95	P5V	96	P5V
97	gnd	98	gnd	99	wr_data_p+
100	NC_MUX_HS<0>	101	PC_MUX_HS<0>	102	wr_data_p-
103	NC_MUX_HS<1>	104	PC_MUX_HS<1>	105	wr_address_p+
106	NC_MUX_HS<2>	107	PC_MUX_HS<2>	108	wr_address_p-
109	NC_MUX_HS<3>	110	PC_MUX_HS<3>	111	clk_p+
112	CLK_LIA_P-	113	CLK_LIA_P+	114	clk_p-
115	LT1-	116	LT1+	117	sdata_p+
118	LT2-	119	LT2+	120	sdata_p-
121	LT3-	122	LT3+	123	wr_data_s+
124	SDATA_LIA_P-	125	SDATA_LIA_P+	126	wr_data_s-
127	N_D_BIAS<1>	128	P_D_BIAS<1>	129	wr_address_s+
130	N_D_BIAS<2>	131	P_D_BIAS<2>	132	wr_address_s-
133	N_D_BIAS<3>	134	P_D_BIAS<3>	135	clk_s+
136	N_D_BIAS<4>	137	P_D_BIAS<4>	138	clk_s-
139	N_D_BIAS<5>	140	P_D_BIAS<5>	141	sdata_s+
142	N_D_BIAS<6>	143	P_D_BIAS<6>	144	sdata_s-

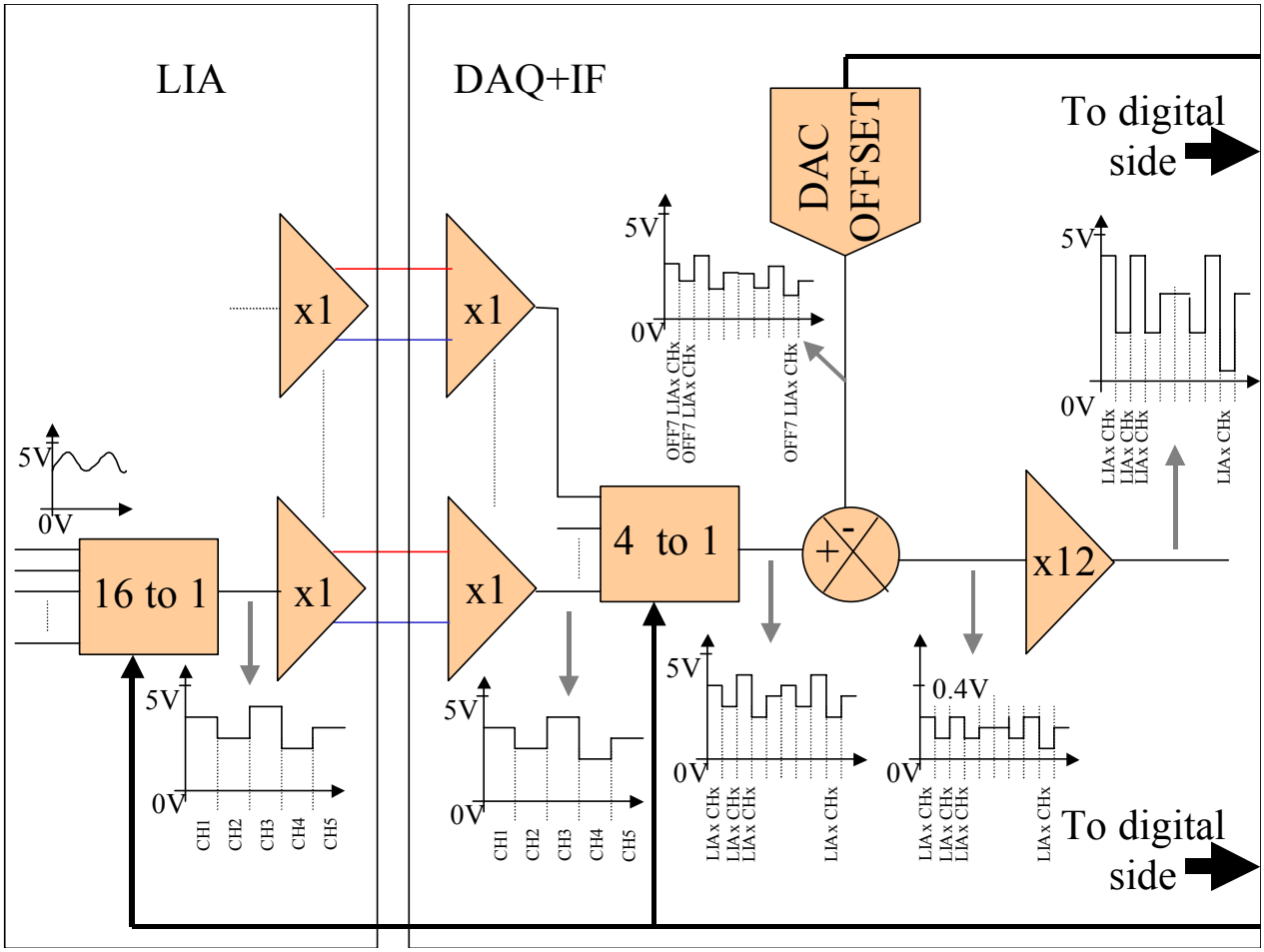
Picture 4-37 DAQ+IF Board Interface

Name	Description	Type	Level	In/Out	Frequency

TBW

4.1.10 DAQ+IF BOARD FUNCTIONS

4.1.10.1 LIA Channel Digitization Overview



Channel way to digitization:

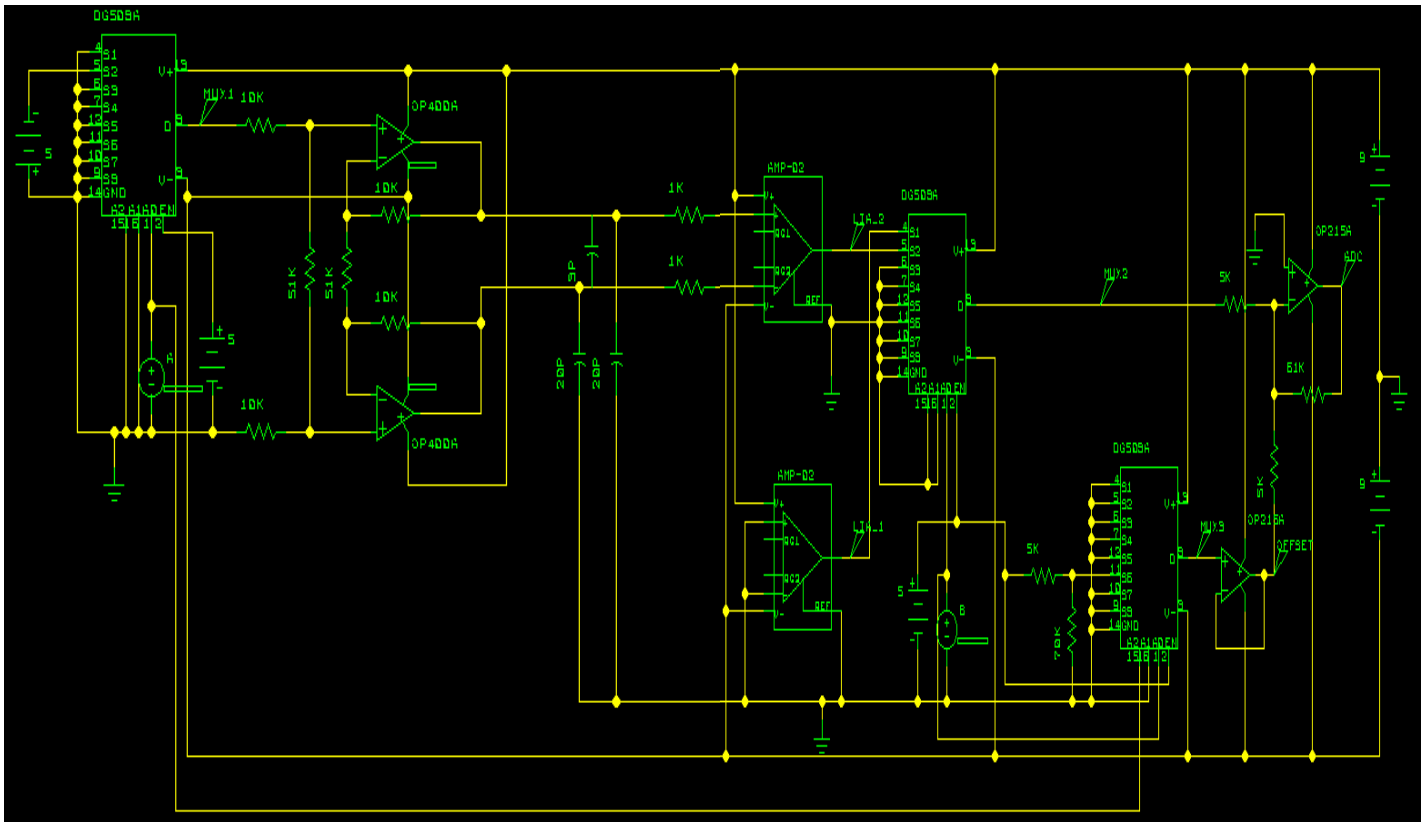
1. After the LIA_P (or LIA_S) channel processing, a bolometer signal is multiplexed with 15 (or 11) other bolometer signals on the same board.
2. Then the multiplexed signal goes out the LIA board through a differential amplifier with one unit gain.
3. The differential multiplexed signal goes into the DAQ+IF board through a differential receiver with one unit gain.
4. DAQ+IF board multiplexing stage:
   - If this multiplexed signal comes from the photometer it is then multiplexed with 2 other signals which come from 2 other LIA_P multiplexers. There are 48 photometer bolometer signals that are multiplexed.
   - If this multiplexed signal comes from the spectrometer then it goes straight through the multiplexer.
5. For each bolometer signal a predetermined offset signal is subtracted.
6. Afterwards, the signal is amplified by 12 and digitized.

4.1.10.2 Analog Receiver and Multiplexer

On a DAQ+IF board there are:

- 18 photometer analog receivers for the 18 LIA_P board output.
- 6 "Spectrometer" Analog receivers for the 6 LIA_S board output.
- 6 muxplexers
- Each multiplexer handles
  - 1 spectrometer analog receiver output.
  - 3 photometer analog receiver output.

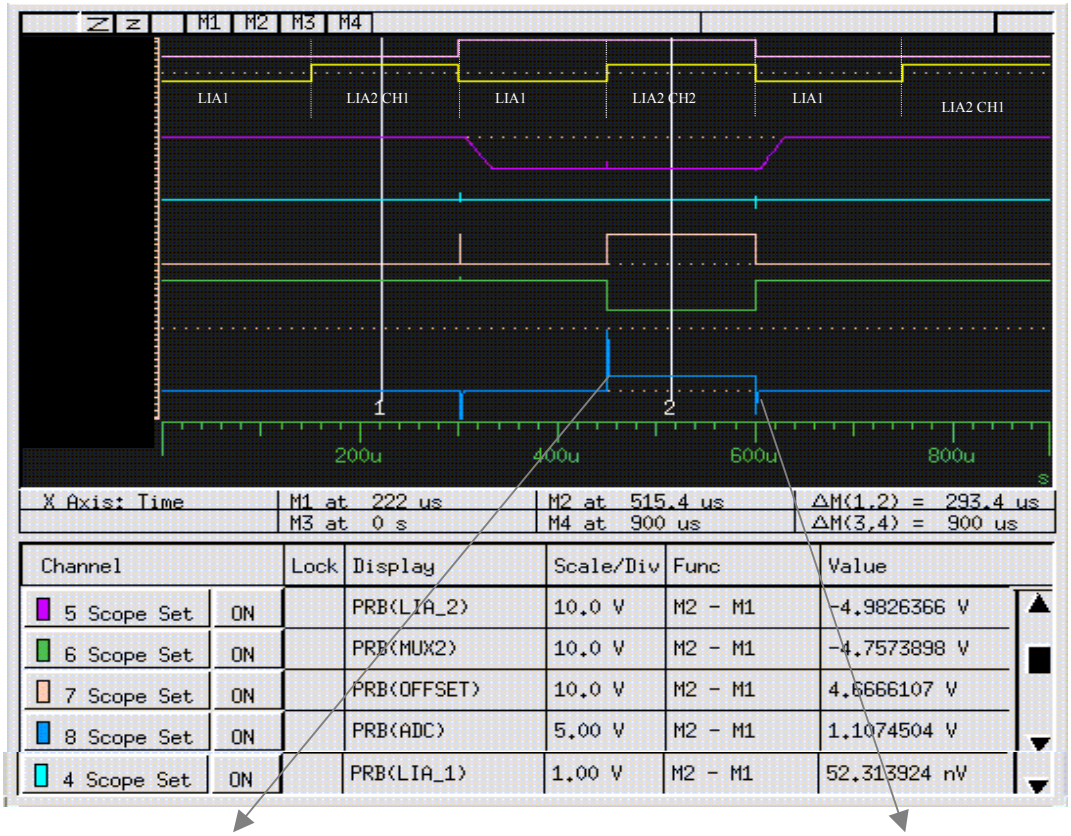
The following simulation circuit shows how to determine the maximum time that an input ADC signal needs to be stabilized after different kinds of multiplexer switching:



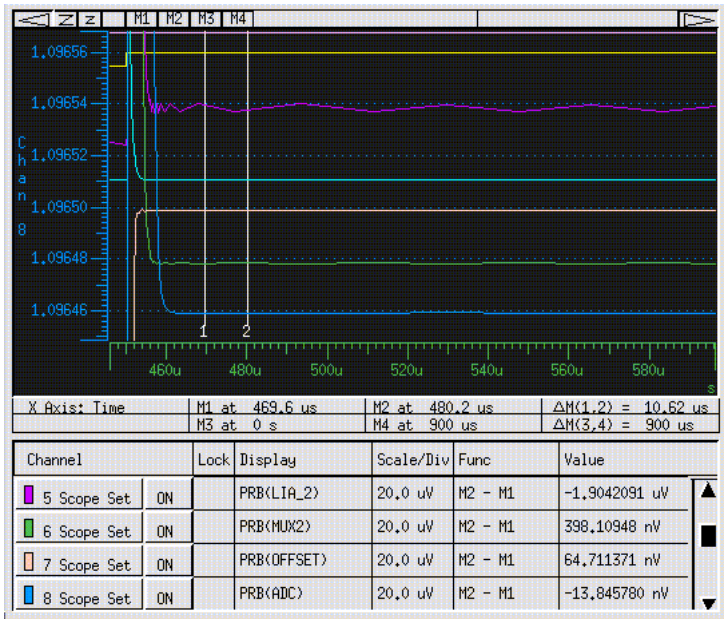
There is a small difference between the real design and the previous Channel Digitization Overview, however result is the same:

- In reality the output signal of a receiver is negative between 0v and –5V.
- After the DAQ Multiplexer, it is added to a positive offset between 0v and 5Vand multiplied by a negative gain of –12.

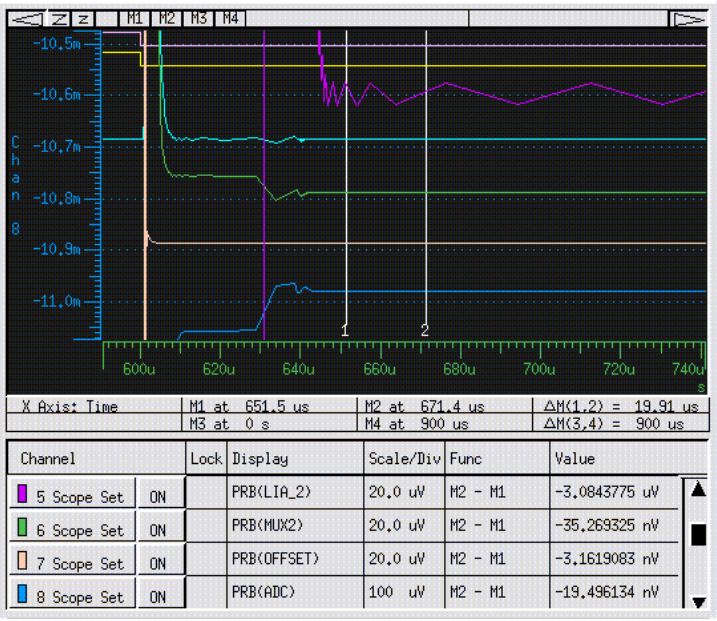
So we have (-channel +offset)x(-12) which it equivalent to (channel-offset)x(12).



DETAIL N°1



DETAIL N°2

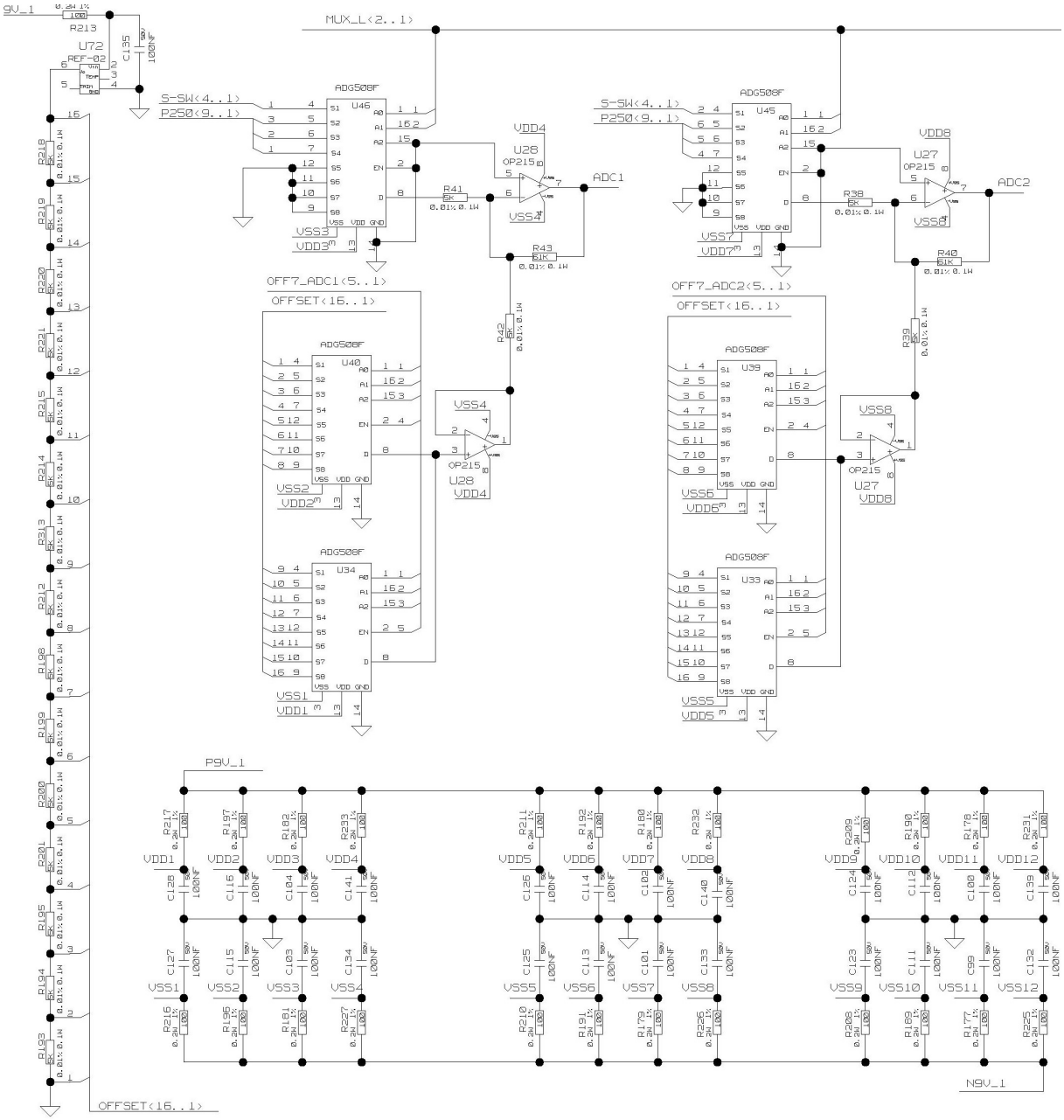


- When the LIA multiplexer and the DAQ multiplexer are switched at the same time, the ADC input signal is established and stabilized after 50 µs. (DETAIL N°2)
- When only the DAQ multiplexer is switched. The ADC input signal is established and stabilized after 20 µs. (DETAIL N°1)

4.1.10.3 Offset and Gain

After each mulptiplexer the channel signals that are going to be digitized are added with their 4-bit predetermined offset signal and the result is multiplied by -12 before to be digitized.
Each ADC is associated to one offset generator and gain amplifier.
2 multiplexers with an OP as follower build the 4-bit offset generators.

See the following circuit:



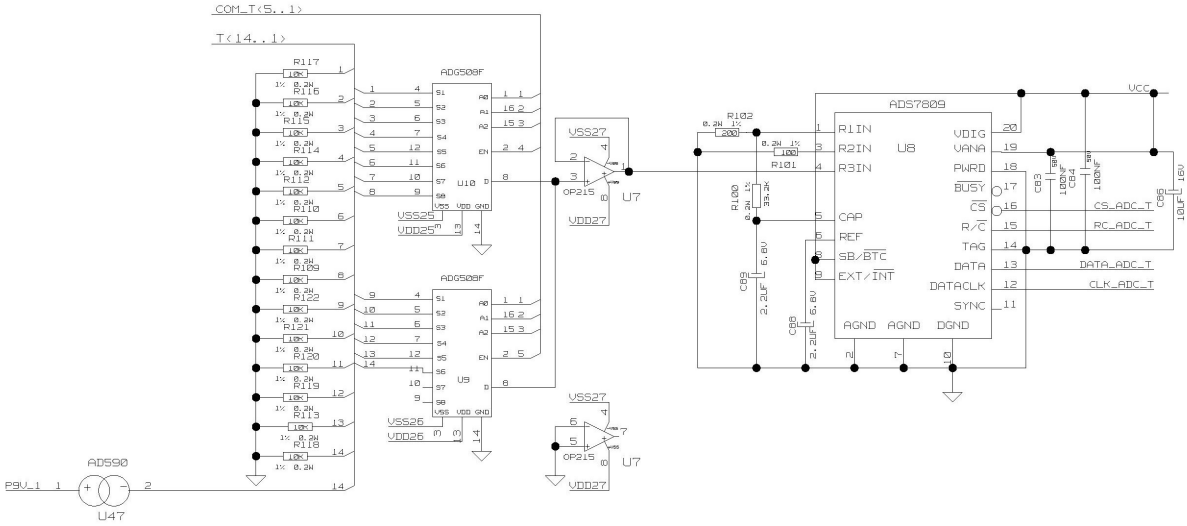
Picture 4-38 Offset and Gain Circuit

4.1.10.4 ADC

TBW

4.1.10.5 Boards Temperature Acquisition

See the following circuit:

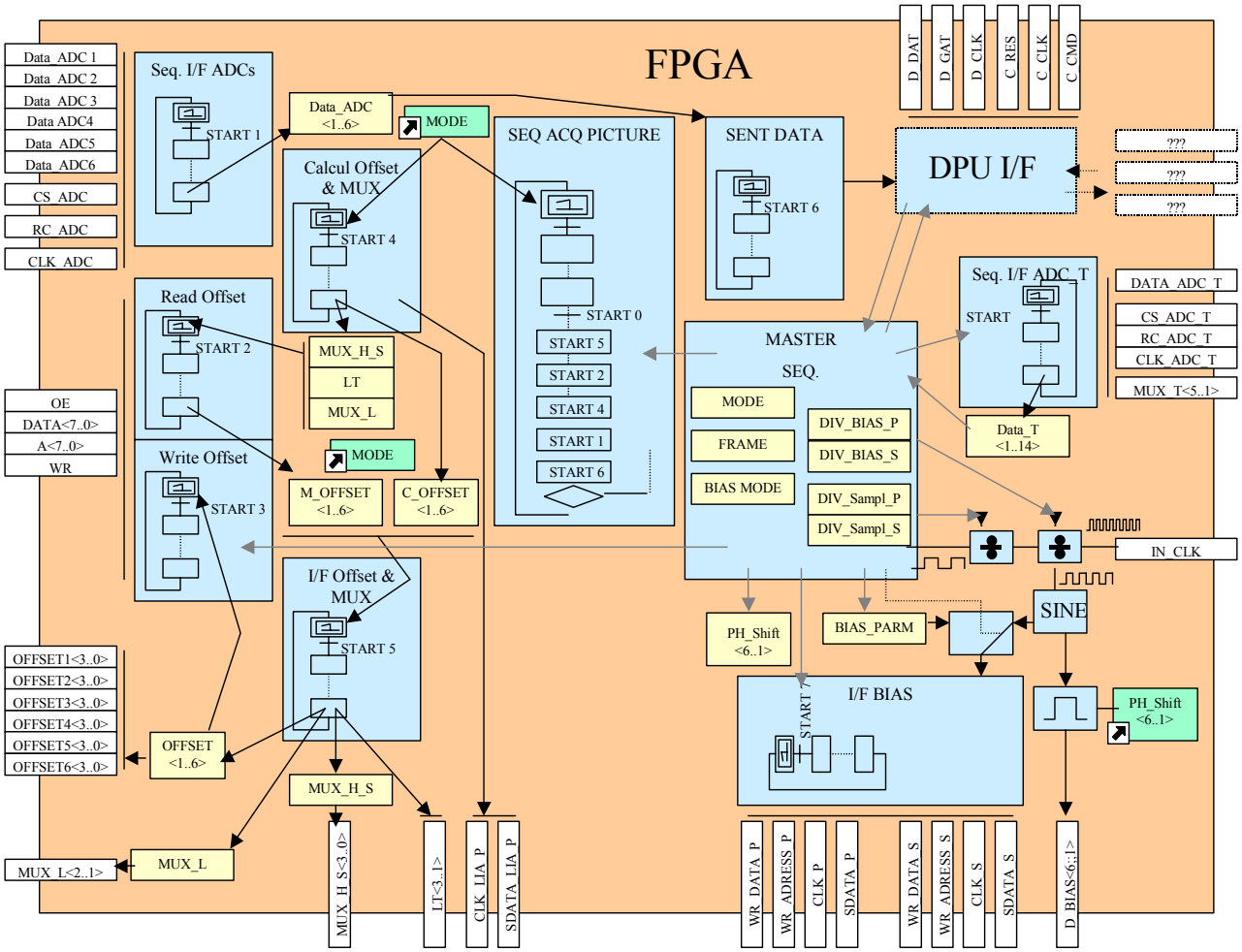


- COM_T selects the board temperature, that will to be digitized.
- The temperature range is –40°C to 80°C.
- The digitized signal voltage range is 2.33V to 3.61V.
- The ADC is 16-bit with a 0V to 5V input range.
- So, the voltage resolution is 76µV.
- And the temperature resolution is 0.008°C.
- The 10 most significant bits give a resolution of 0.48°C

COM_T<5..1>					Board temperature
5	4	3	2	1	
0	1	0	0	0	BIAS
0	1	0	0	1	LIA_S1
0	1	0	1	0	LIA_S2
0	1	0	1	1	LIA_S3
0	1	1	0	0	LIA_P9
0	1	1	0	1	LIA_P8
0	1	1	1	0	LIA_P7
0	1	1	1	1	LIA_P6
1	0	0	0	0	LIA_P5
1	0	0	0	1	LIA_P4
1	0	0	1	0	LIA_P3
1	0	0	1	1	LIA_P2
1	0	1	0	0	LIA_P1
1	0	1	0	1	DAQ+IF

4.1.11 DAQ+IF FPGA

4.1.11.1 DAQ+IF FPGA Overview



Picture 4-39 DAQ+IF FPGA Overview

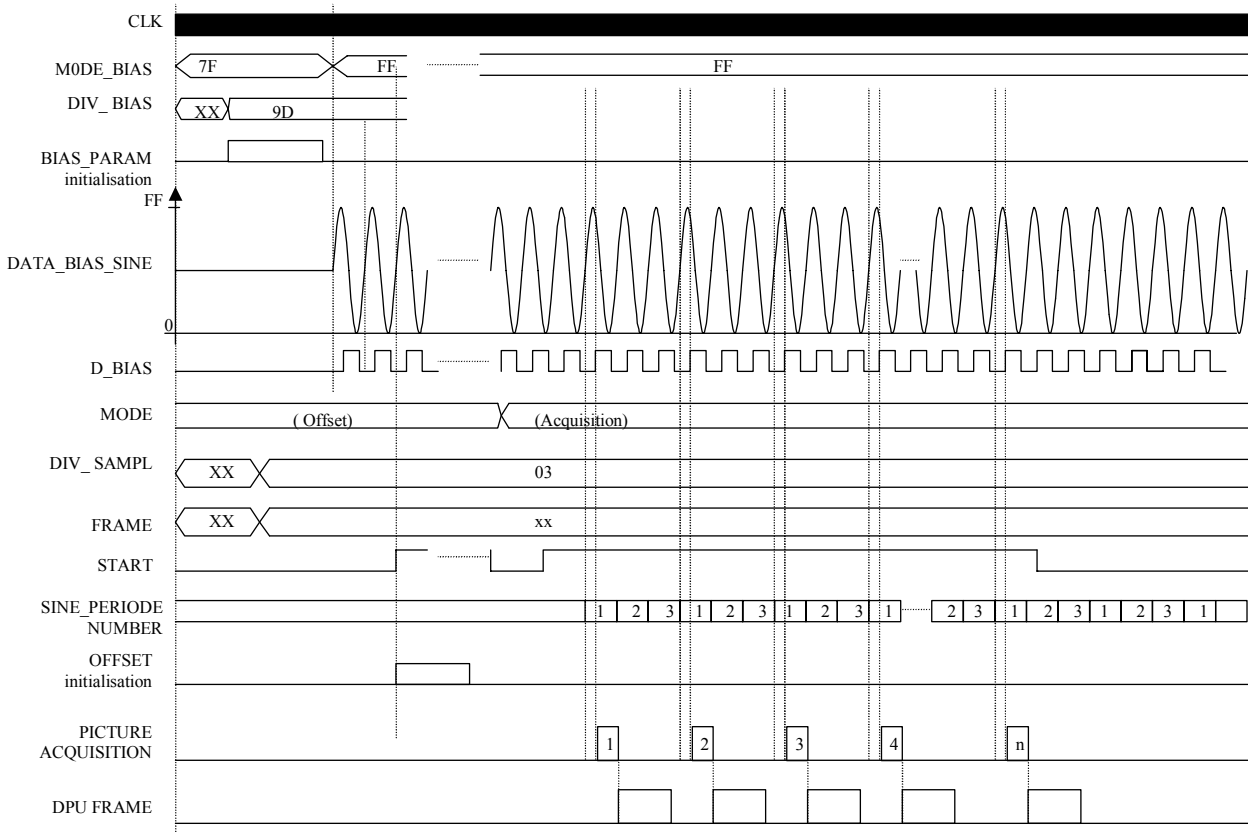
This FPGA is divided into 3 main parts:

- One handles the communication with the DPU (DPU I/F)
- One handles the command executions and the "high-level sequencer"(MATER SEQ)
  - Bias generator management (Frequency, amplitude, demodulation signals phase shift…
  - Mode management (picture acquisition Number and frequency, Spectrometer or photometer mode, offset set up…
  - Board Temperature acquisition.
- The last one handles the sequencing of picture acquisition and the offset set up (SEQ AQC PICTURE)

4.1.12 DAQ+IF FPGA FUNCTIONS

4.1.12.1 Mode Overview and Timing

This timing diagram shows how this instrument works:



1. Bias parameters are set (JFET power, heater, demodulation signal phase shift, bias frequency and Amplitude…) See detail in 4.1.12.4 Bias Control.
2. Then the sine bias signal starts.
3. The offsets are determined and memorized. See detail in 4.1.12.5 Offset.
4. After each x* bias period a picture is digitized (PICTURE ACQUISITION) and sent to the DPU (DPU FRAME.) For the picture acquisition detail see 4.1.12.2 Channel Multiplexing and 4.1.12.3 Channel Acquisition
5. The acquisition stops when the start signal become low or in photometer mode when the programmed number of FRAME (between 1and 255) has been acquired.

* x is determined by DIV_SAMPL

4.1.12.2 Channel Multiplexing

Spectrometer mode:

The following table shows the chronological sequence of the spectrometer's picture acquisition mode:

- The indicated times show when the digitization occurs. These times are given with reference to the beginning of the picture acquisition.
- The six ADCs work in parallel.
- The LIA_S MUX line specifies the LIA_S board's multiplexer positions at the digitization time.
- The DAQ+IF board multiplexer position is 0 during the spectrometer mode.
- The table shows for each ADC which board's channel is associated with each digitization time.

Time in ms		0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1.0	1.1	1.2
ADC1	channel	1	2	3	4	5	6	7	8	9	10	11	12
	Lia_s	1	1	1	1	1	1	1	1	1	1	1	1
ADC2	channel	13	14	15	16	17	18	19	20	21	22	23	24
	Lia_s	1	1	1	1	1	1	1	1	1	1	1	1
ADC3	channel	1	2	3	4	5	6	7	8	9	10	11	12
	Lia_s	2	2	2	2	2	2	2	2	2	2	2	2
ADC4	channel	13	14	15	16	17	18	19	20	21	22	23	24
	Lia_s	2	2	2	2	2	2	2	2	2	2	2	2
ADC5	channel	1	2	3	4	5	6	7	8	9	10	11	12
	Lia_s	3	3	3	3	3	3	3	3	3	3	3	3
ADC6	channel	13	14	15	16	17	18	19	20	21	22	23	24
	Lia_s	3	3	3	3	3	3	3	3	3	3	3	3
LIA_S	MUX	0	1	2	3	4	5	6	7	8	9	10	11
DAQ	MUX	0	0	0	0	0	0	0	0	0	0	0	0

Photometer mode:

The following tables show the chronological sequence of the photometer's picture acquisition mode:

- The times point out digitization times. These times are given with reference to the beginning of the picture acquisition.
- The six ADCs work in parallel.
- The LIA_P MUX specifies multiplexer positions at the digitization time
- The DAQ MUX specifies DAQ+IF board's multiplexer positions at the digitization time.
- The table shows for each ADC which board's channel of which is associated with each digitization time.

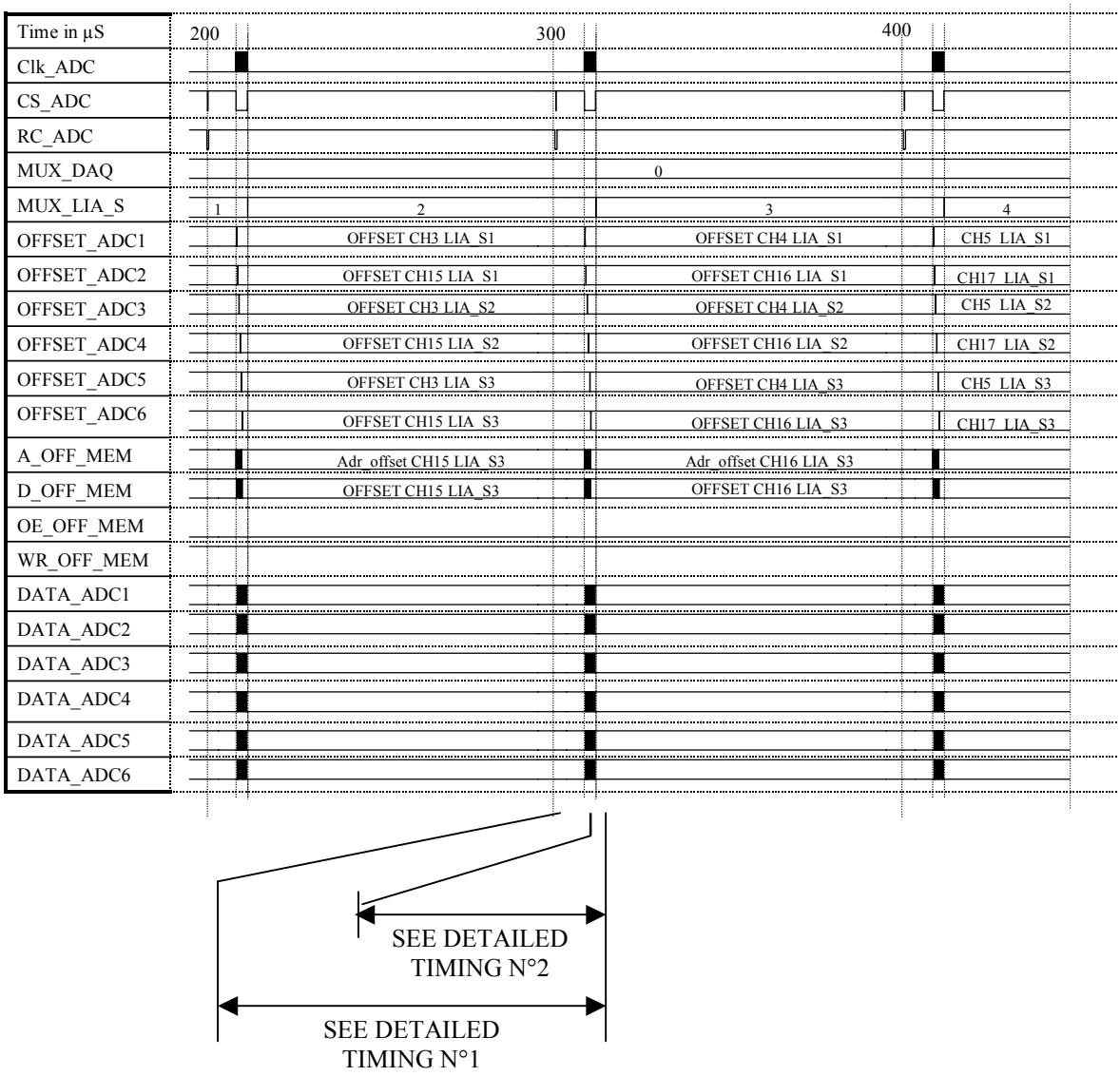
Time in ms		0.15	0.25	0.35	0.5	0.6	0.7	0.85	0.95	1.05	1.3	1.4	1.5	1.65	1.75	1.85	2
ADC1	channel	1	17	1	2	18	2	3	19	3	4	20	4	5	21	5	6
	Lia_p	1	1	2	1	1	2	1	1	2	1	1	2	1	1	2	1
ADC2	channel	17	1	17	18	2	18	19	3	19	20	4	20	21	5	21	22
	Lia_p	2	3	3	2	3	3	2	3	3	2	3	3	2	3	3	2
ADC3	channel	1	17	1	2	18	2	3	19	3	4	20	4	5	21	5	6
	Lia_p	4	4	5	4	4	5	4	4	5	4	4	5	4	4	5	4
ADC4	channel	17	1	17	18	2	18	19	3	19	20	4	20	21	5	21	22
	Lia_p	5	6	6	5	6	6	5	6	6	5	6	6	5	6	6	5
ADC5	channel	1	17	1	2	18	2	3	19	3	4	20	4	5	21	5	6
	Lia_p	7	7	8	7	7	8	7	7	8	7	7	8	7	7	8	7
ADC6	channel	17	1	17	18	2	18	19	3	19	20	4	20	21	5	21	22
	Lia_p	8	9	9	8	9	9	8	9	9	8	9	9	8	9	9	8
LIA_P	MUX	0	0	0	1	1	1	2	2	2	3	3	3	4	4	4	5
DAQ	MUX	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1

Time in ms		2.1	2.2	2.35	2.45	2.55	2.7	2.8	2.9	3.05	3.15	3.25	3.4	3.5	3.6	3.75	3.85
ADC1	channel	22	6	7	23	7	8	24	8	9	25	9	10	26	10	11	27
	Lia_p	1	2	1	1	2	1	1	2	1	1	2	1	1	2	1	1
ADC2	channel	6	22	23	7	23	24	8	24	25	9	25	26	10	26	27	11
	Lia_p	3	3	2	3	3	2	3	3	2	3	3	2	3	3	2	3
ADC3	channel	22	6	7	23	7	8	24	8	9	25	9	10	26	10	11	27
	Lia_p	4	5	4	4	5	4	4	5	4	4	5	4	4	5	4	4
ADC4	channel	6	22	23	7	23	24	8	24	25	9	25	26	10	26	27	11
	Lia_p	6	6	5	6	6	5	6	6	5	6	6	5	6	6	5	6
ADC5	channel	22	6	7	23	7	8	24	8	9	25	9	10	26	10	11	27
	Lia_p	7	8	7	7	8	7	7	8	7	7	8	7	7	8	7	7
ADC6	channel	6	22	23	7	23	24	8	24	25	9	25	26	10	26	27	11
	Lia_p	9	9	8	9	9	8	9	9	8	9	9	8	9	9	8	9
LIA_P	MUX	5	5	6	6	6	7	7	7	8	8	8	9	9	9	10	10
DAQ	MUX	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2

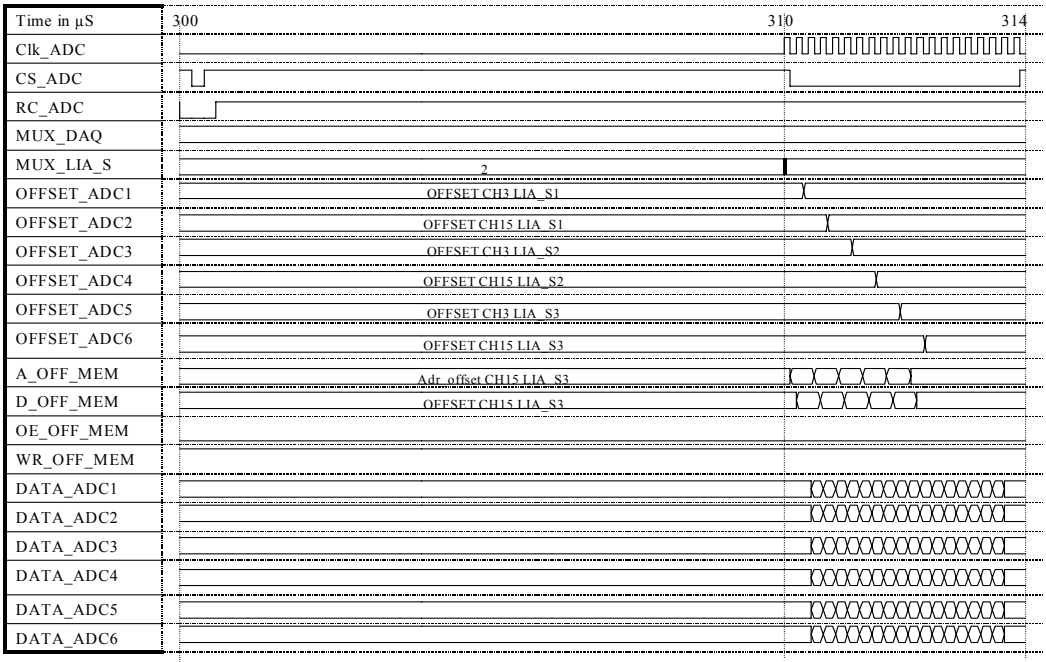
Time in ms		3.95	4.1	4.2	4.3	4.45	4.55	4.65	4.8	4.9	5	5.15	5.25	5.35	5.5	5.6	5.7
ADC1	channel	11	12	28	12	13	29	13	14	30	14	15	31	15	16	32	16
	Lia_p	2	1	1	2	1	1	2	1	1	2	1	1	2	1	1	2
ADC2	channel	27	28	12	28	29	13	29	30	14	30	31	15	31	32	16	32
	Lia_p	3	2	3	3	2	3	3	2	3	3	2	3	3	2	3	3
ADC3	channel	11	12	28	12	13	29	13	14	30	14	15	31	15	16	32	16
	Lia_p	5	4	4	5	4	4	5	4	4	5	4	4	5	4	4	5
ADC4	channel	27	28	12	28	29	13	29	30	14	30	31	15	31	32	16	32
	Lia_p	6	5	6	6	5	6	6	5	6	6	5	6	6	5	6	6
ADC5	channel	11	12	28	12	13	29	13	14	30	14	15	31	15	16	32	16
	Lia_p	8	7	7	8	7	7	8	7	7	8	7	7	8	7	7	8
ADC6	channel	27	28	12	28	29	13	29	30	14	30	31	15	31	32	16	32
	Lia_p	9	8	9	9	8	9	9	8	9	9	8	9	9	8	9	9
LIA_P	MUX 3	10	11	11	11	12	12	12	13	13	13	14	14	14	15	15	15
DAQ	MUX	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3

4.1.12.3 Channel Acquisition

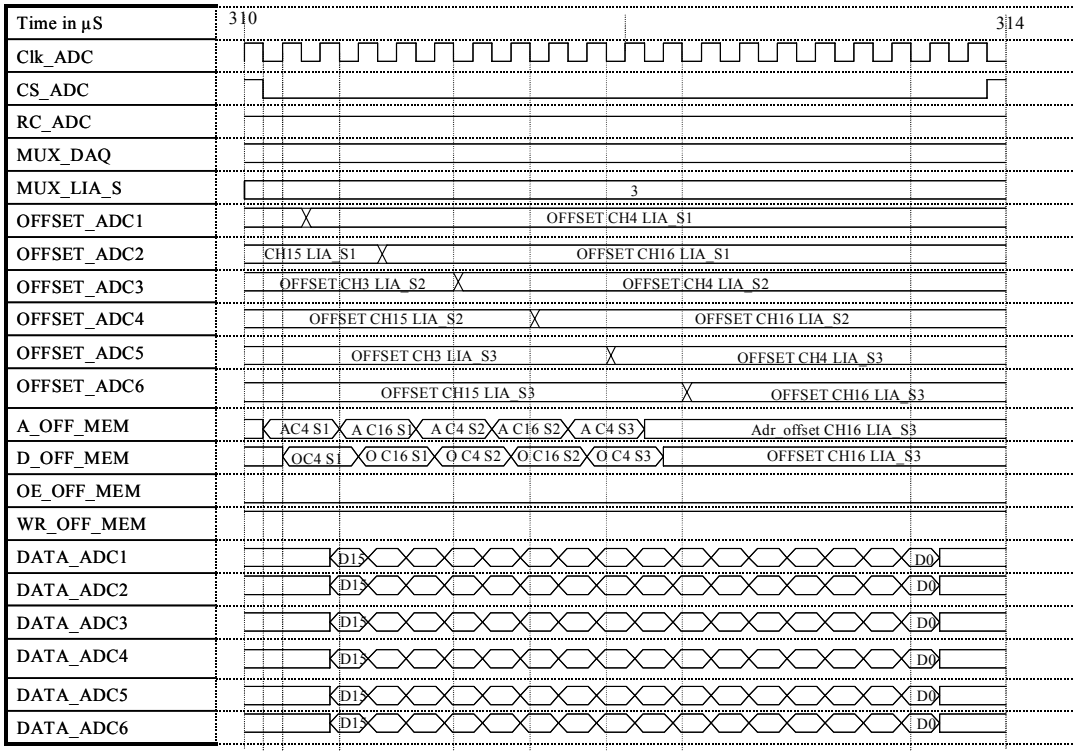
Spectrometer Mode Digitization Timing Diagram:



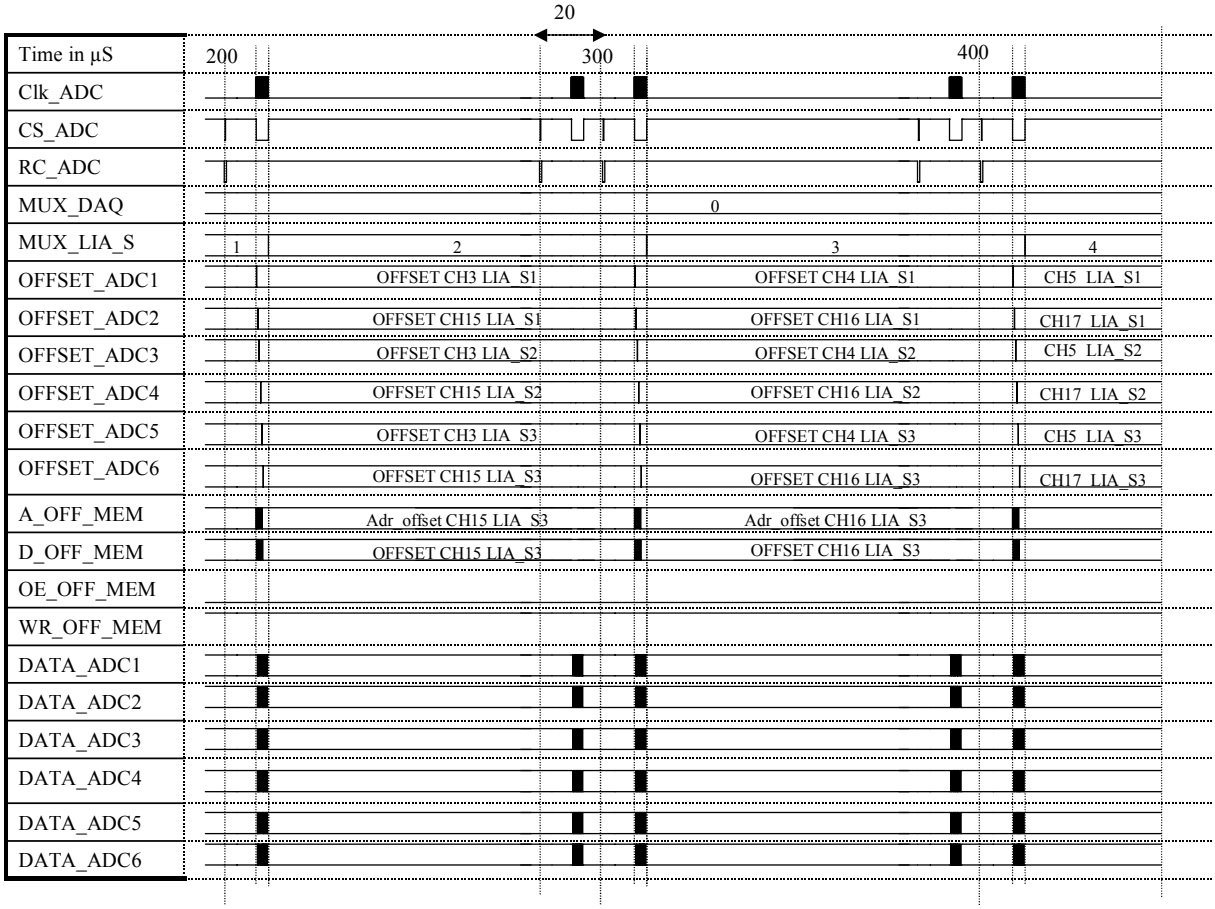
DETAILED TIMING N°1



DETAILED TIMING N°2



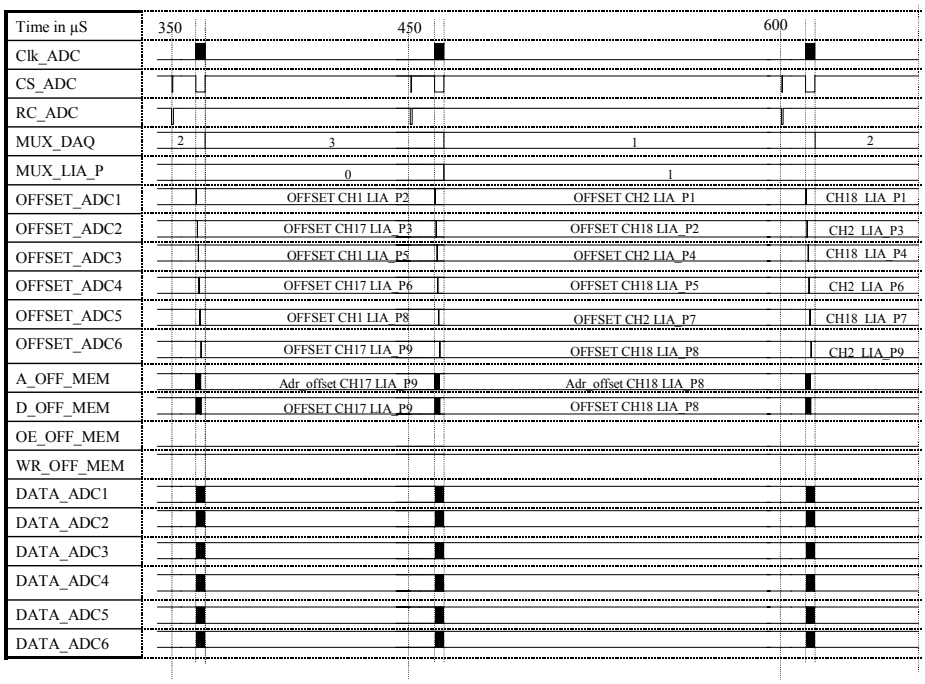
Spectrometer Mode Digitization Timing Diagram for the over sampling option:



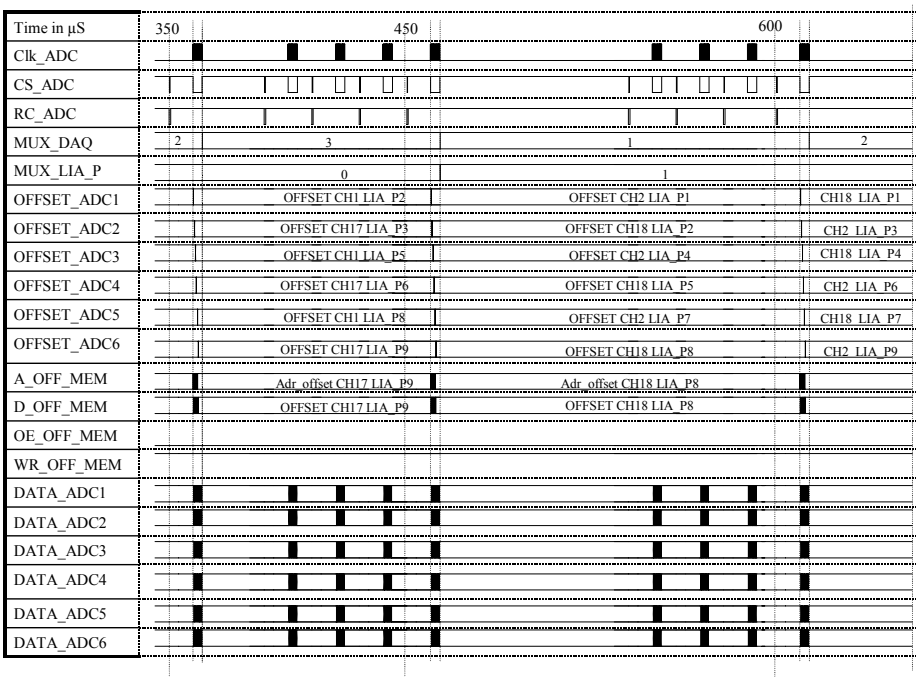
For each channel it is possible have 2 samples. A channel values of a will be the average of its 2 samples.

We will choose whether or not to implement this option after the QM1 test. At that point, the number of samples will be set and won't be able to be changed!!!

Photometer Mode Digitization Timing Diagram:



Photometer mode Digitization Timing Diagram for over sampling option:



For each channel, it is possible have 4 (or 2) samples. A channel values of a will be the average of its 4 (or 2) samples.

We will choose whether or not to implement this option after the QM1 test. At that point, the number of samples will be set and won't be able to be changed!!!

4.1.12.4 Bias Control

SINE BIAS generator:

The CLK_BIAS is the sine bias clock. This clock is determined by dividing the master clock's CLK_IN frequency by the parameter DIV_BIAS_PHOTO (or DIV_BIAS_SPECTRO.)

- 256 of this clock periods equal one sine period.

To write the Sine bias data on one of the BIAS board sine bias generator:

- All 32 (or 16) CS and ON/OFF positions are sent through a serial link (see BIAS § 4.1.8.4 Commands)
- For each the clock 256 periods a sine data is written in a sine bias generator.

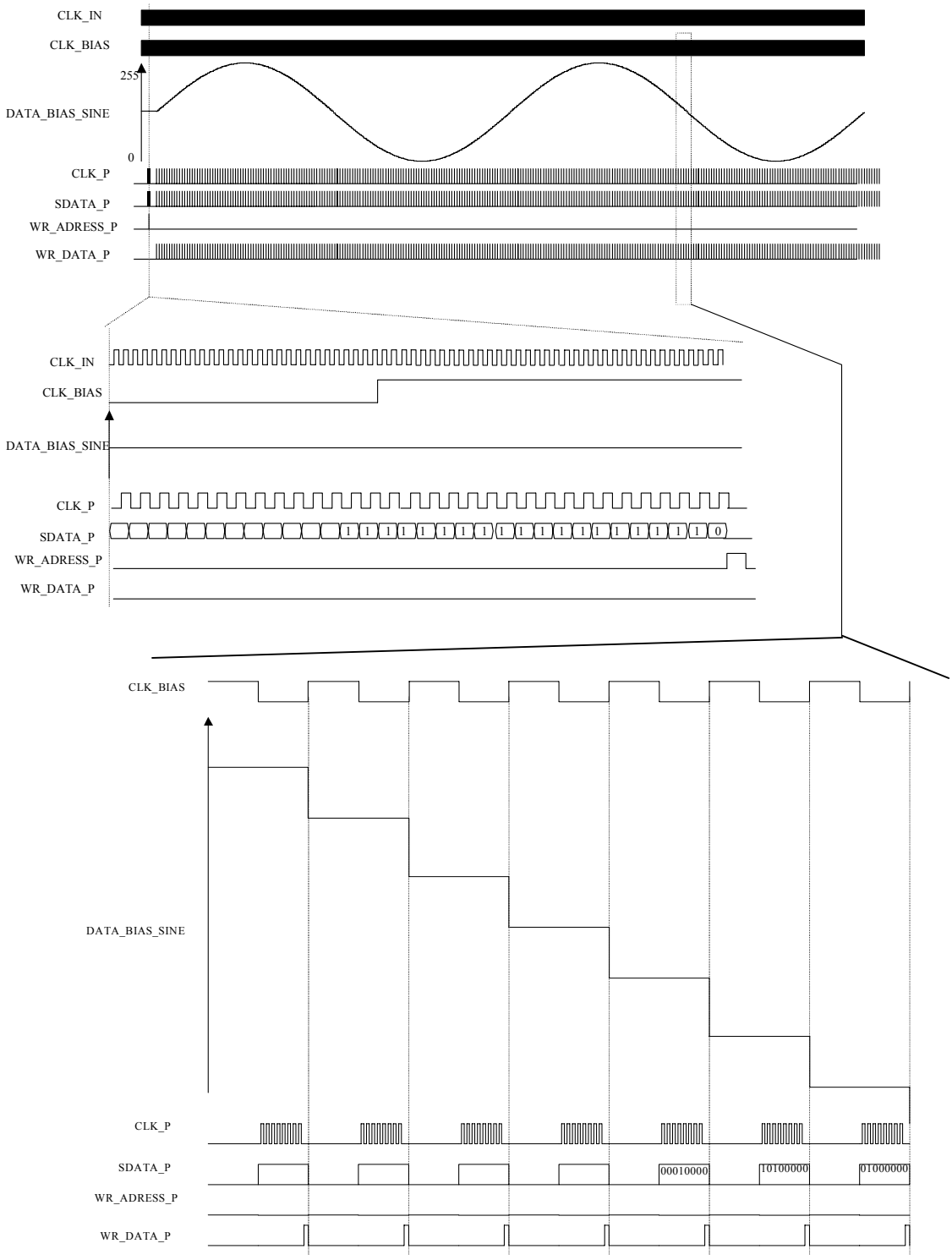
See next timing diagram

Demodulation signals:

TBW

BIAS parameter:

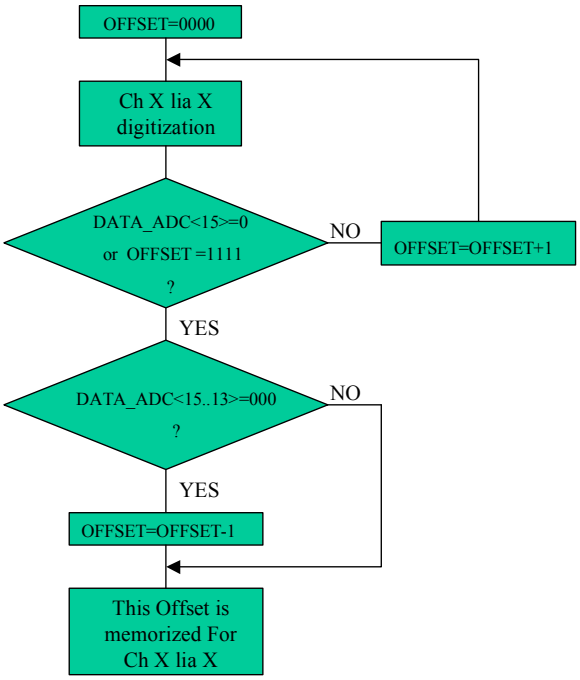
TBW

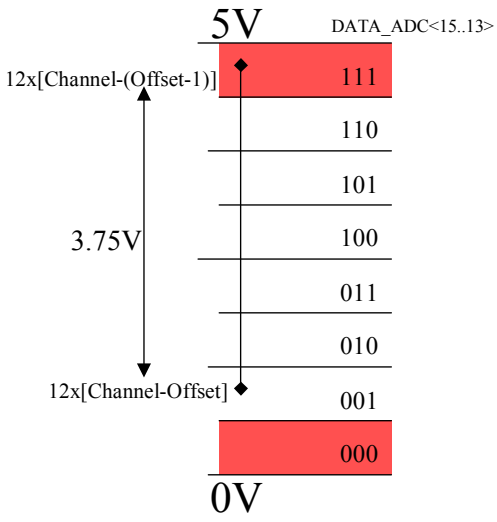

CLK_IN
CLK_BIAS
255
DATA_BIAS_SINE
0
CLK_P
SDATA_P
WR_ADRESS_P
WR_DATA_P
CLK_IN
CLK_BIAS
DATA_BIAS_SINE
CLK_P
SDATA_P
WR_ADRESS_P
WR_DATA_P
CLK_BIAS
DATA_BIAS_SINE
CLK_P
SDATA_P
WR_ADRESS_P
WR_DATA_P
00010000
10100000
01000000

4.1.12.5 Offset

For each channel, the following algorithm determines its offset:

Offset Calculation for Ch X lia X





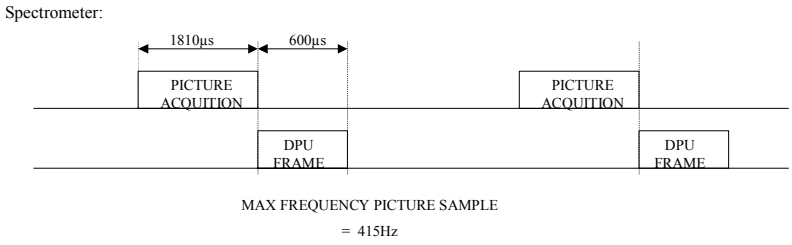
4.1.12.6 Command

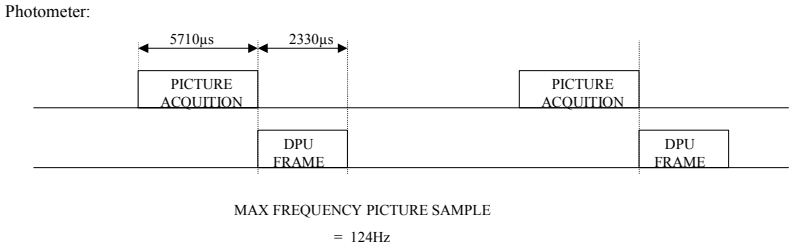
See DCU/DRCU ICD

TBW

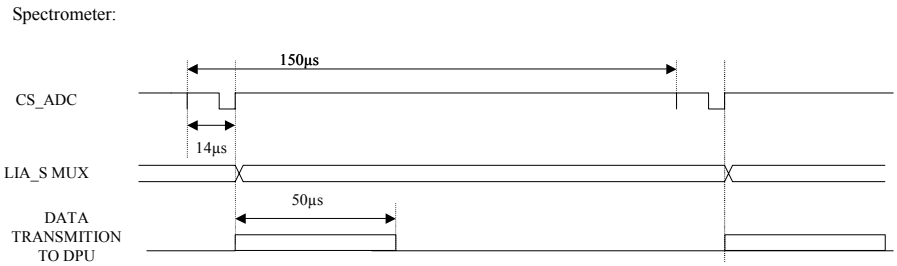
4.1.12.7 Data Transmission

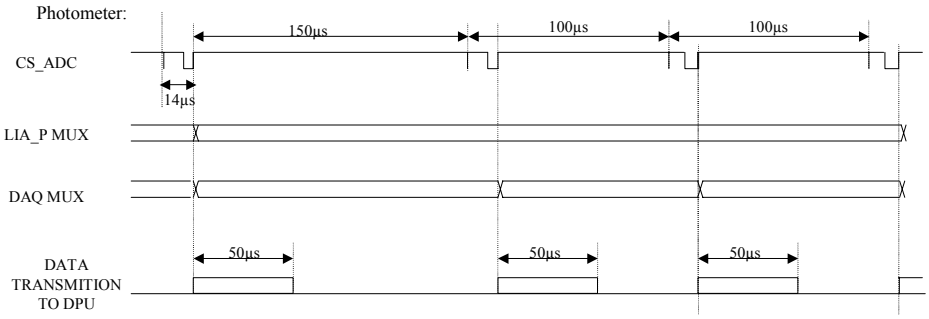
1. With a FIFO the data are transmitted to the DPU through a serial link at 2Mb/s after a complete PICTURE AQUISITION





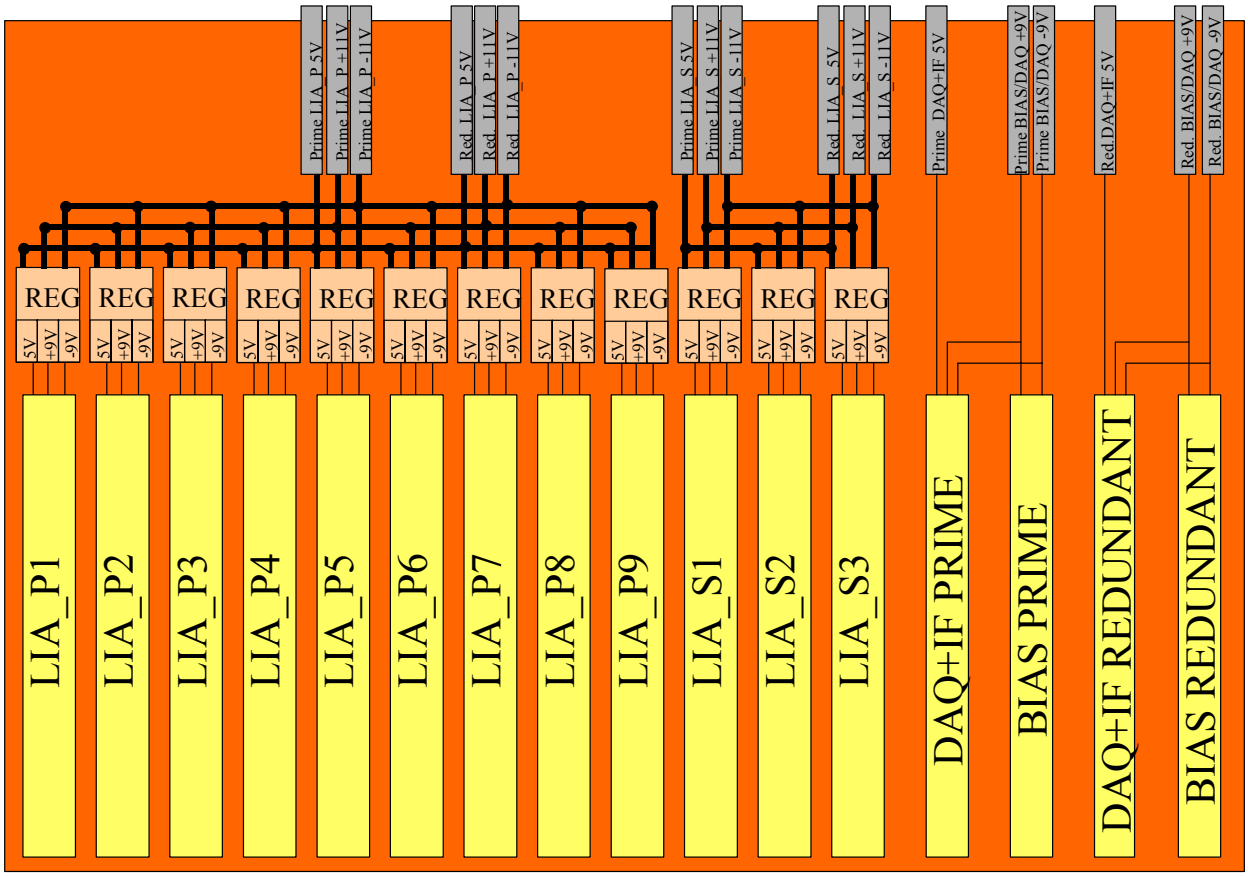
2. Without a FIFO data are transmitted to the DPU through a serial link at 2Mb/s after ADC digitization; this case, the over sample option is not possible.





4.2 DCU Power Supply

4.2.1 DCU POWER SUPPLY OVERVIEW

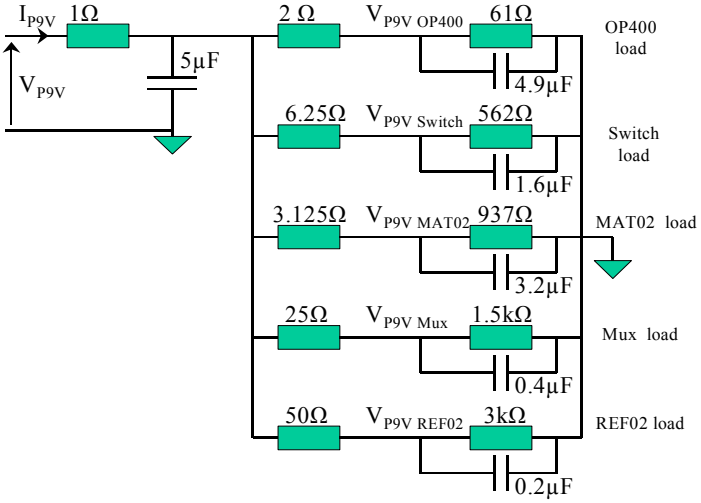


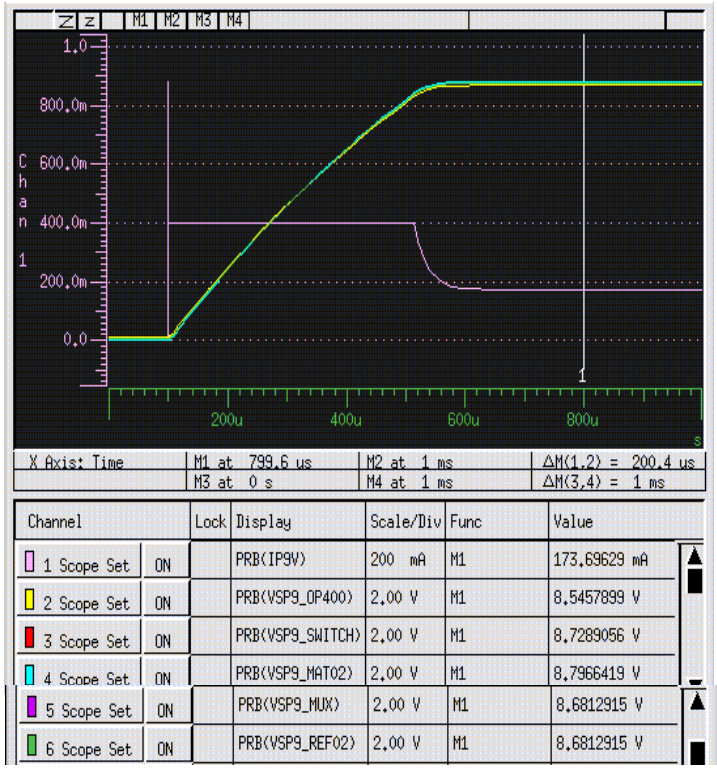
4.2.2 LIA PHOTOMETER POWER SUPPLY

4.2.2.1 LIA Photometer Board Power Supply

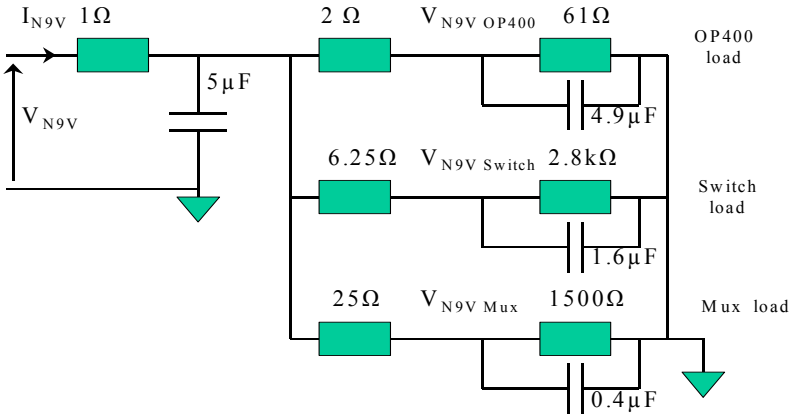
A LIA board receives 3 different power supply line 5V,-9V and +9V. All regulators used to supply LIA boards have a limited electric current of 400mA.

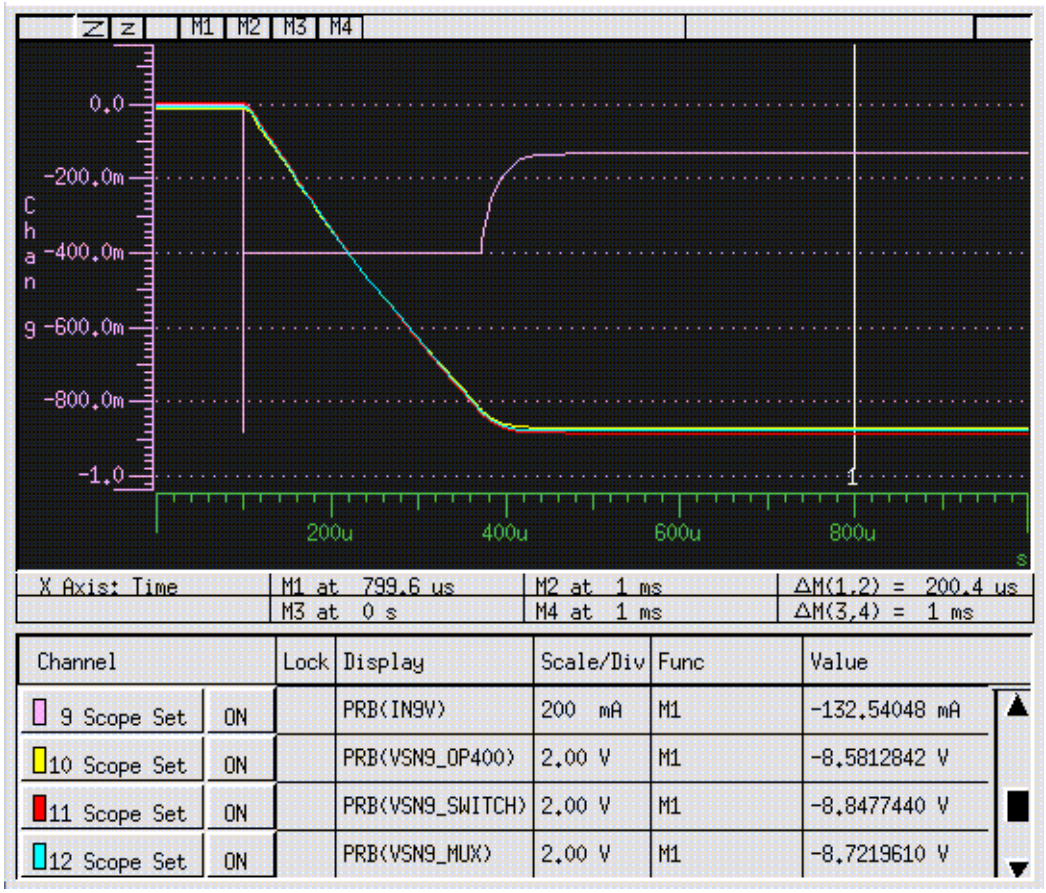
The following circuit is a simplified model of the LIA Photometer board seen from the +9V power supply line. The current is nominal around 175mA less than 1ms. See the following simulation result.



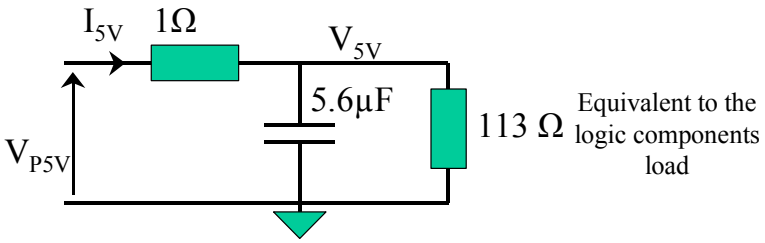


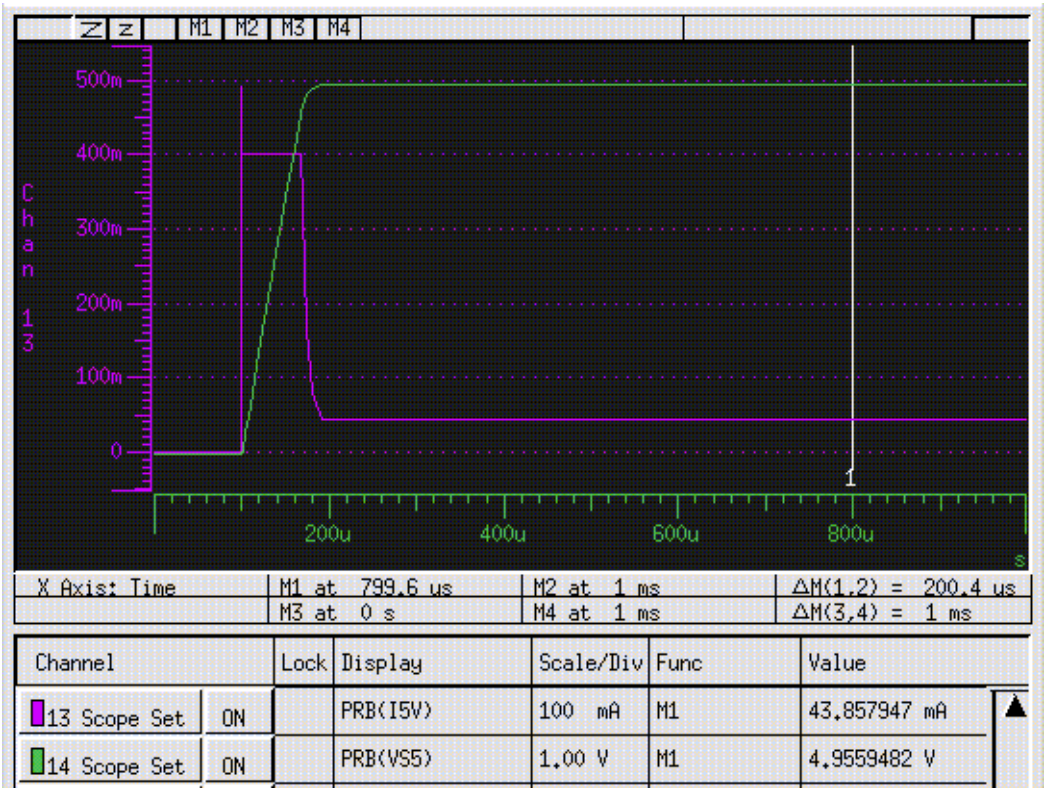
The following circuit is a simplified model of the LIA Photometer board seen from the -9V power supply line. The current is nominal around -150mA after less than 1ms. See the following simulation result.



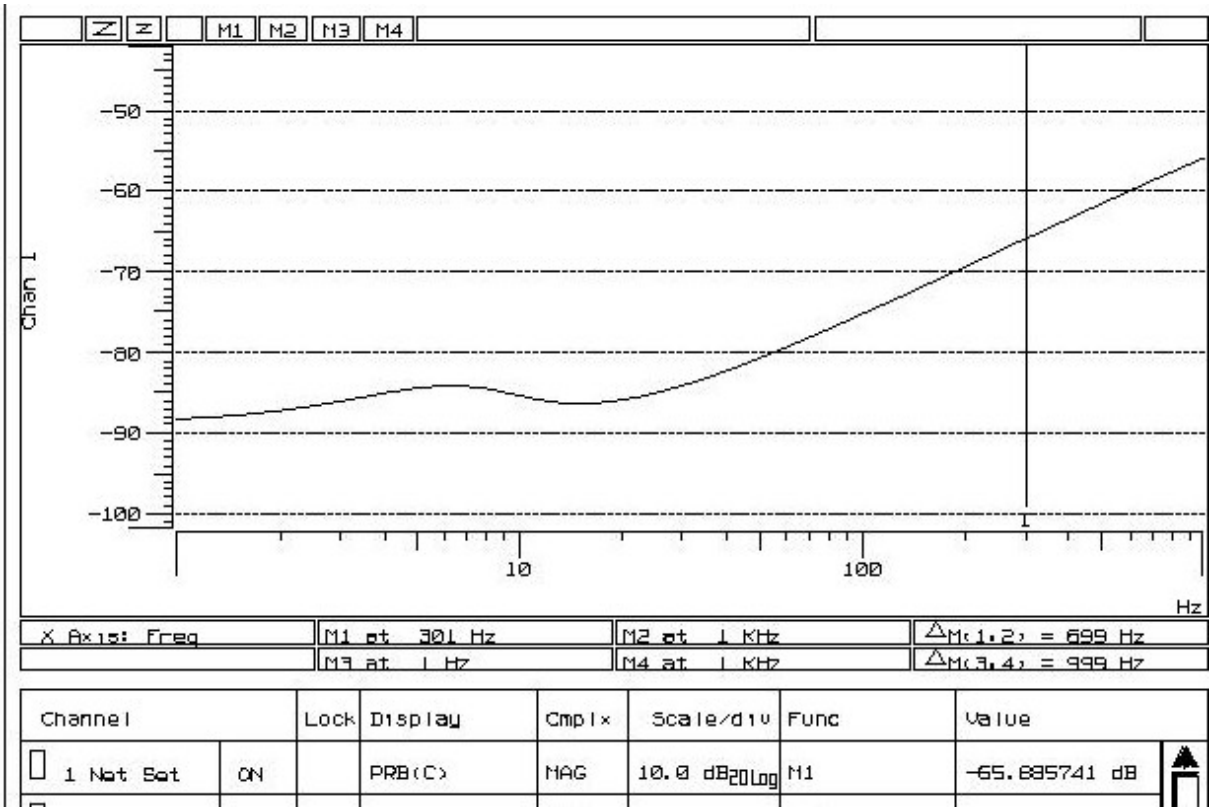


The following circuit is a simplified model of the LIA Photometer board seen from the 5V power supply line. The current is nominal around 45mA after less than 1ms. See the following simulation result.





Power Supply Rejection Ratio:

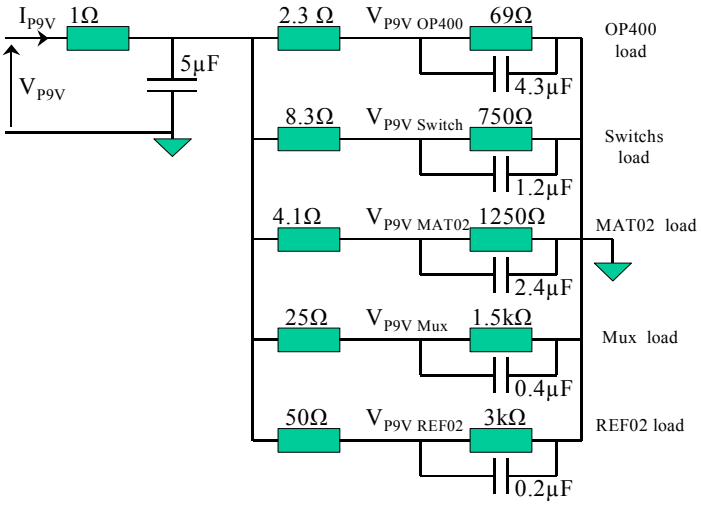


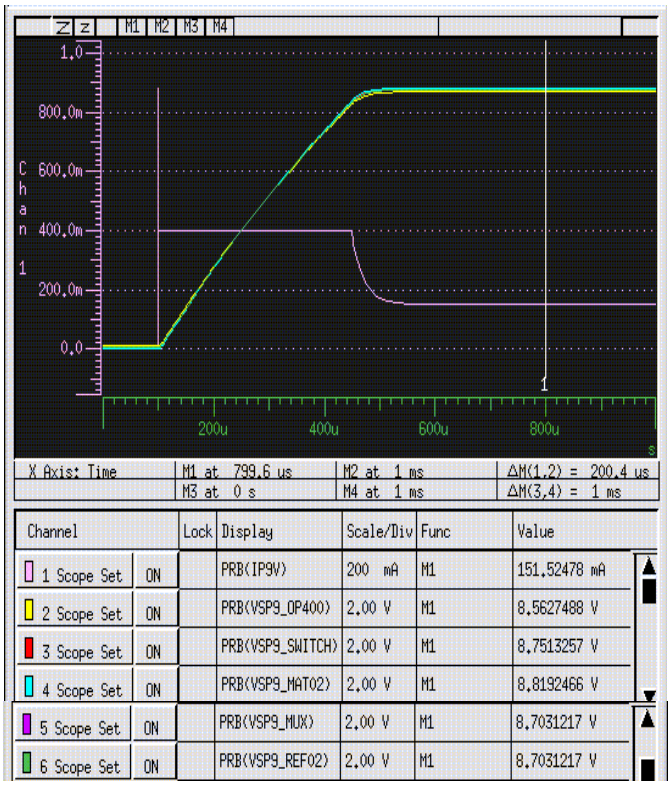
TBW

4.2.2.2 LIA Spectrometer Board Power Supply

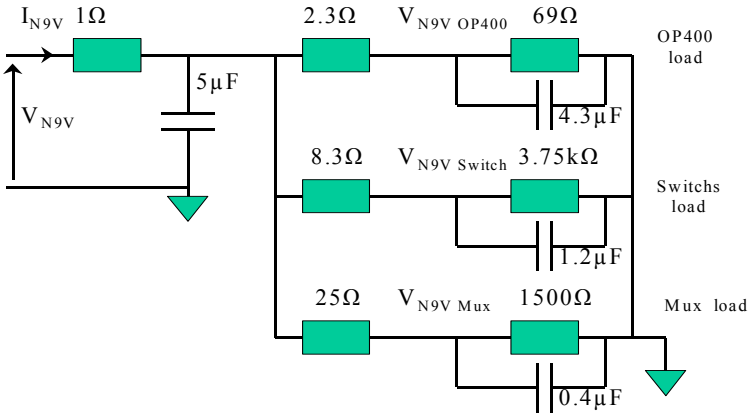
A LIA board receives 3 different power supply line 5V,-9V and +9V. All regulators used to supply LIA boards have a limited electric current of 400mA.

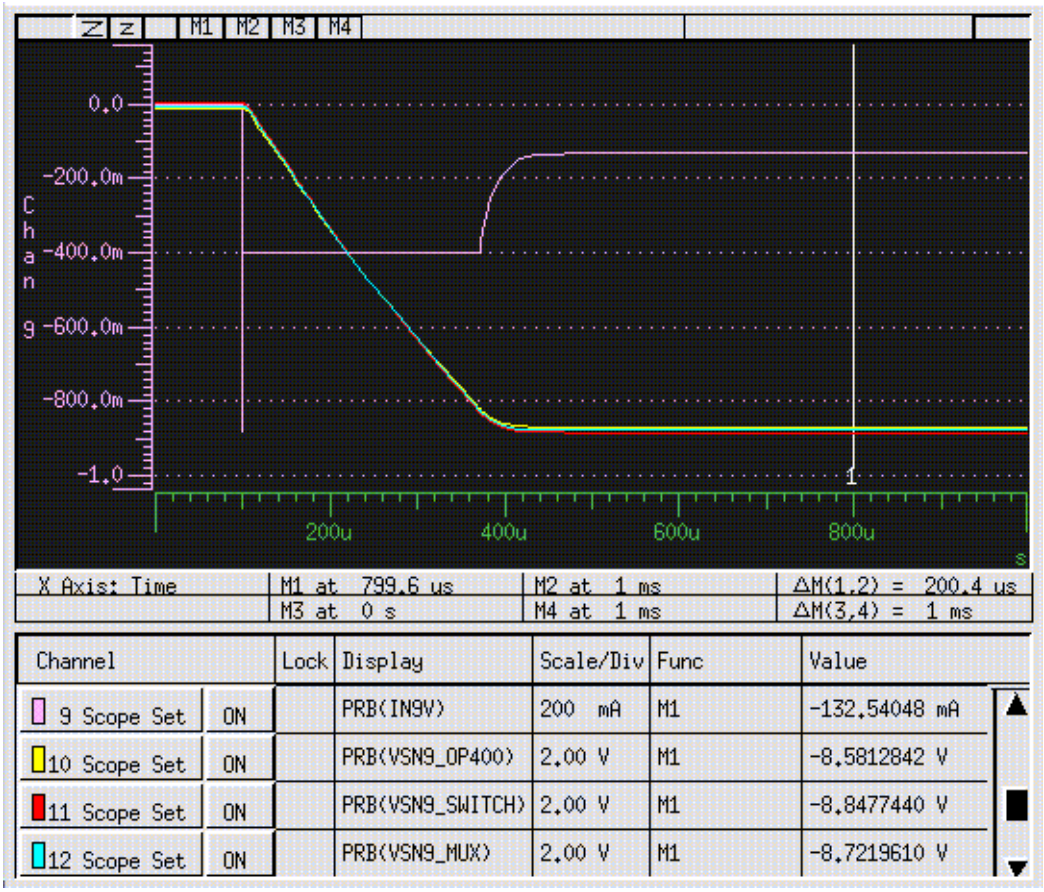
The following circuit is a simplified model of the LIA Spectrometer board seen from the +9V power supply line. The current is nominal around 155mA less than 1ms. See the following simulation result.



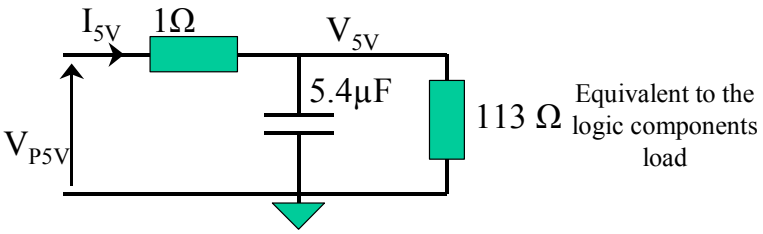


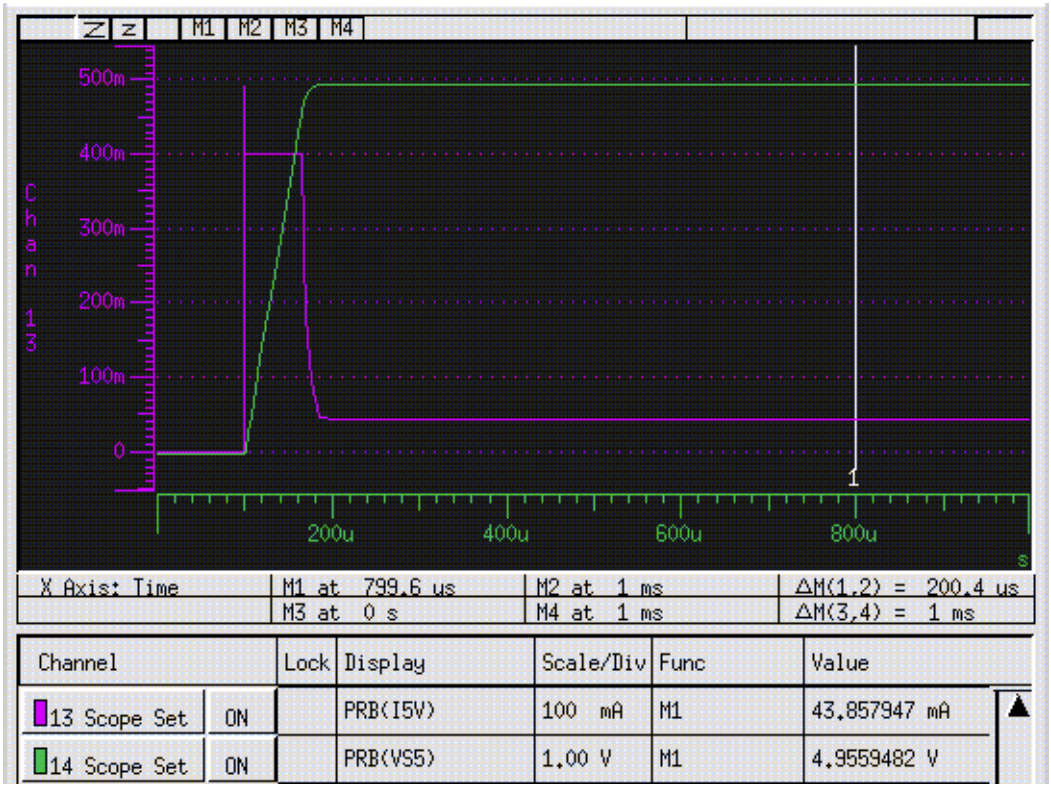
The following circuit is a simplified model of the LIA Spectrometer board seen from the -9V power supply line. The current is nominal around 135mA less than 1ms. See the following simulation result.



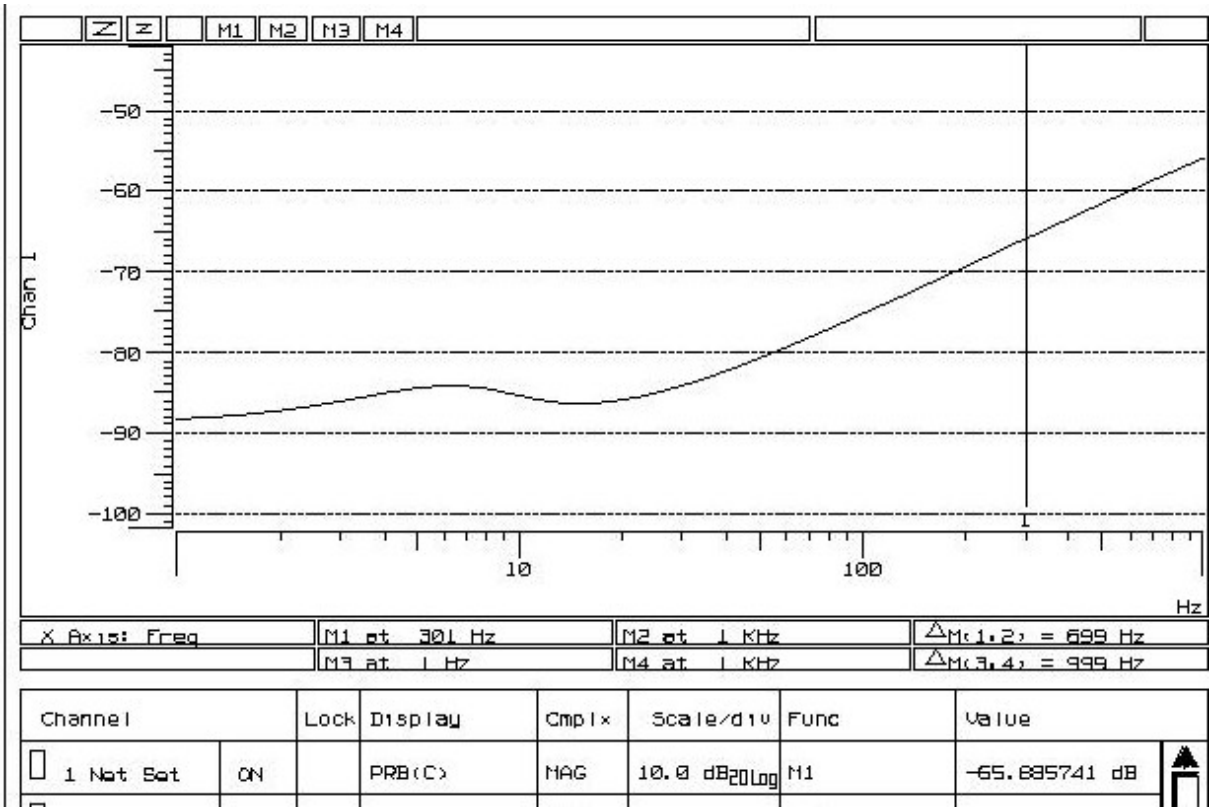


The following circuit is a simplified model of the LIA Spectrometer board seen from the 5V power supply line. The current is nominal around 45mA less than 1ms. See the following simulation result.





Power Supply Rejection Ratio:



TBW

4.2.3 BIAS AND DAQ power SUPPLY

The PRIME (redundant) BIAS board and the PRIME(redundant) DAQ+IF board receive the same -9V and +9V power supply line.
A DAQ+IF board receives also a 5V power supply line.

The following circuit is a simplified model of one BIAS board with one DAQ+IF board seen from the 9V power supply line. The current is nominal around xx mA less than 1ms. See the following simulation result.

TBW

The following circuit is a simplified model of one BIAS board with one DAQ+IF seen from the -9V power supply line. The current is nominal around xx mA less than 1ms. See the following simulation result.

TBW

The following circuit is a simplified model of DAQ+IF board seen from the 5V power supply line. The current is nominal around xx mA less than 1ms. See the following simulation result.

TBW

4.2.4 Grounding Network

TBW

Picture 4-40 Grounding Network

5 INTERFACES

5.1 INTERFACE WITH FPU

5.1.1 Harness

- The DCU will be connected to the FPU with four different types of harnesses.

- TYPE I will connect the LIA_P board with the FPU. Six TYPE I harnesses will connect the nine LIA_Ps.
- TYPE II will connect the photometer section of both the PRIME and REDUNDANT BIAS boards with the FPU.
- TYPE III will connect the spectrometer section of both the PRIME and REDUNDANT BIAS boards as well as a LIA_S board with the FPU.
- TYPE IV will connect the last two LIA_S boards with the FPU.

ANNEX A shows the composition of the TYPE I, TYPE II, TYPE III and TYPE IV harnesses.

ANNEX A shows how the nine harnesses are connected between the FPU and the DCU.

	Harness NAME	Harness type
Harness 1	H_FPU_BOLO_P1	TYPE I
Harness 2	H_FPU_BOLO_P2	TYPE I
Harness 3	H_FPU_BOLO_P3	TYPE I
Harness 4	H_FPU_BOLO_P4	TYPE I
Harness 5	H_FPU_BOLO_P5	TYPE I
Harness 6	H_FPU_BOLO_P6	TYPE I
Harness 7	H_FPU_BOLO_S	TYPE IV
Harness 8	H_FPU_BIAS_S	TYPE III
Harness 9	H_FPU_BIAS_P	TYPE II

5.2 INTERFACE WITH THE DPU

5.2.1 Harness

TBW

5.3 INTERFACE WITH THE FCU

5.3.1 Harness

TBW

5.4 INTERFACE WITH THE TEST EQUIPEMENT

5.4.1 Harness

TBW

6 TRACEABILITY MATRIX

DRCU Subsystem Specification	Detector Subsystem Specification	DCU Design Document	Description	Check by		
				Design	Simulation	Measurement
DRCU REQ-36	BDA-DRCU-01 BDA-DRCU-18	4.1.3.4 4.1.6.4	Noise<7nV/rt(Hz)			X
	BDA-DRCU-03		Input capa< 100pF			X
	BDA-DRCU-04		Input impedance>1MΩ			X
	BDA-DRCU-11	4.1.3.2 4.1.6.2	CMR<-60dB		X	
	BDA-DRCU-13	4.1.3.3	Bandwidth photo		X	X
	BDA-DRCU-14	4.1.6.3	Bandwidth spectro		X	X
	BDA-DRCU-22	4.1.3.1 4.1.6.1	Channel saturation	X		
	BDA-DRCU-25		Cross talk<0.05%			X
	-	4.1.3.3 4.1.6.3	LPF (HR-SP-RAL-ERC-001)	X		
	-	4.1.1.1 4.1.4.1	Channel number	X		
	-	4.1.2.2 4.1.5.2	LIA Interface Balanced signal + Shield	X		
DRCU REQ-37	BDA-DRCU-19	4.1.3.4 4.1.6.4	NOISE with thermal drift			X
DRCU REQ-38	BDA-DRCU-05	4.1.7 4.1.12.4	BIAS	X		
DRCU REQ-39		4.1.8.1 4.1.8.4	Amplitude command	X		
DRCU REQ-40		4.1.12.4	Bias frequency	X		
-		4.1.8.5	Noise<20nV/rt(Hz)			X
DRCU REQ-41	BDA-DRCU-06 BDA-DRCU-07	4.1.7 4.1.8.2	JFET BIAS	X		
	BDA-DRCU-08	4.1.8.6	VSS and VDD Noise			X
DRCU REQ-42	BDA-DRCU-09	4.1.8.4 4.1.12.6	VSS and VDD ON/OFF command	X		
DRCU REQ-43		4.1.8.2	VSS and VDD overshoot		X	
	BDA-DRCU-21	4.1.8.6	JFET power NOISE with thermal drift			X
DRCU REQ-44	BDA-DRCU-10	4.1.8.3	heater	X		
DRCU REQ-45		4.1.8.4 4.1.12.6	heater command	X		
DRCU REQ-46	-	4.1.12.6	DCU data	X		
DRCU REQ-47	-	3.1.1.1	DAQ PRIME/ REDUNDANT	X		
DRCU REQ-48	BDA-DRCU-12	4.1.10.4	ADC resolution	X		
	-	4.1.12.2	TOTAL Acquisition time	X		
DRCU REQ-49	BDA-DRCU-15 BDA-DRCU-16	4.1.12.1 4.1.12.6	Sample clock	X		
DRCU REQ-50	-	4.1.12.1 4.1.12.6	Frame number	X		
DRCU REQ-51	-	4.1.12.6	Mode data frame	X		

DRCU Subsystem Specification	Detector Subsystem Specification	DCU Design Document	Description	Check by		
				Design	Simulation	Measurement
DRCU REQ-52	-	4.1.10.5	Temperature probe Location	X		
DRCU REQ-53	-	4.1.10.5	Temperature acquisition	X		
DRCU REQ-54	-	4.1.10.5	Temperature range	X		
DRCU REQ-55	-	4.1.12.6	Housekeeping parameter	X		
DRCU REQ-56	-	4.2	DCU power suply	X		
DRCU REQ-57	-					
DRCU REQ-58	-					
DRCU REQ-59	-					