FCU & DCU units

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Unit Design (1)

- **FCU Unit Design**
  - **Electrical / MCU sub-unit**
    - **4 board types:**
      - *MAC (Multi Axis Controller) - 1 M + 1 R*
      - *SMEC (Spectro. Analog Electronics) - 1 M + 1 R*
      - *BSM (Mirror Analog Electronics) - 1 M / R*
      - *MCU_BP (passive Backplane) - 1 M / R*
  - **Mechanical / MCU sub-unit**
    - *Electronics boards are mounted on stiffeners*
    - *Modules (electronics boards+stiffeners) - x5 - are plugged and locked into an enclosure which also supports the backplane*

Unit Design (2)

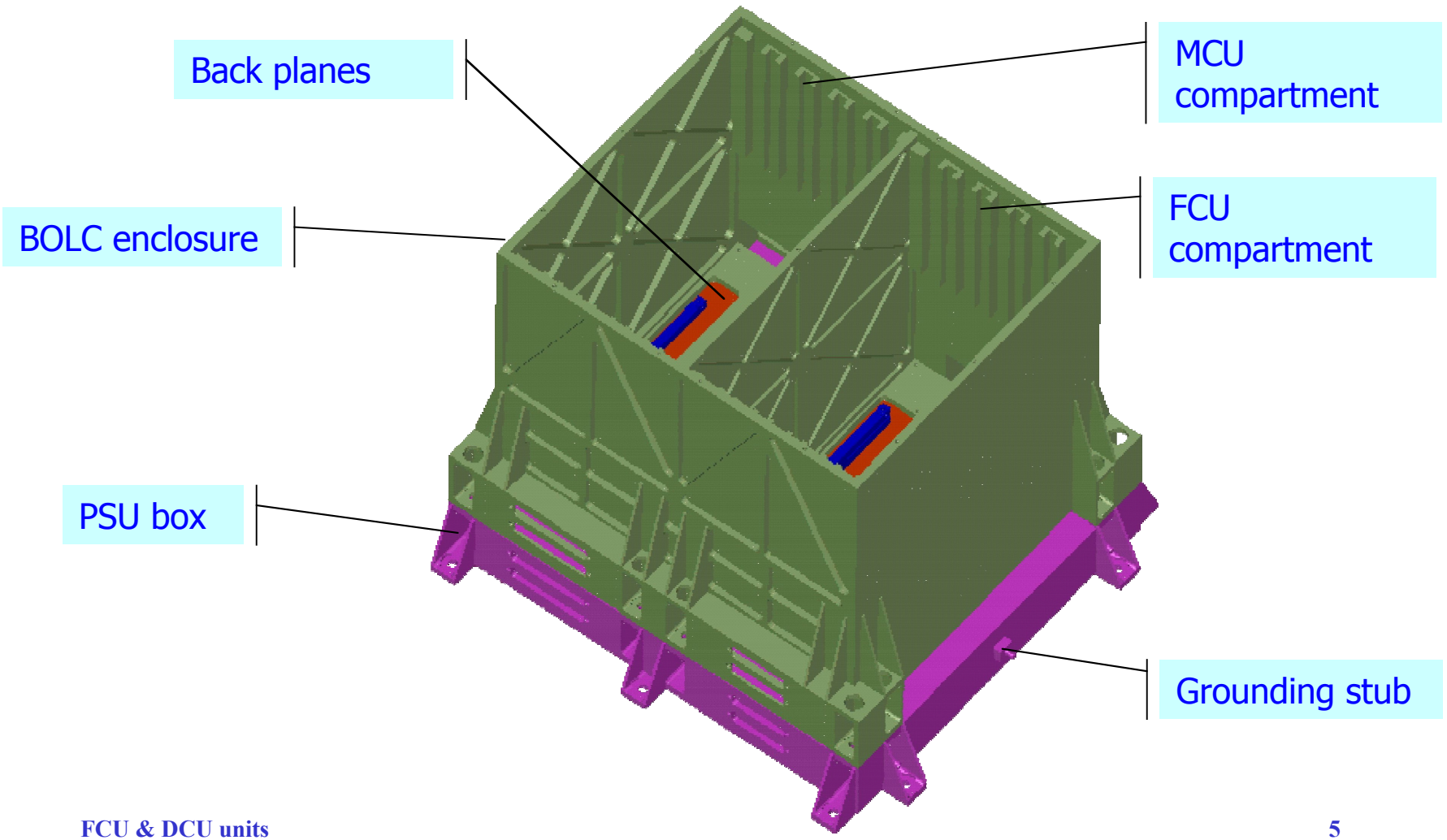
- **FCU Unit Design …**
  - **Electrical / SCU sub-unit**
    - **3 board types:**
      - ***CCHK_IF (DPU IF + Cool/Cal/HK ctrl) - 1 M + 1 R***
      - ***TEMP (Spectro. Analog Electronics) - 1 M + 1 R***
      - ***SCU_BP (passive Backplane) - 1 M / R***
  - **Mechanical / SCU sub-unit**
    - **Similar to MCU:**
      - ***Electronics boards are mounted on stiffeners***
      - ***Modules (electronics boards+stiffeners) - x4 - are plugged and locked into an enclosure which also supports the SCU backplane***

Unit Design (3)

- **FCU Unit Design …**
  - **Mechanical / FCU unit**
    - ***Box is divided into two compartments: MCU & SCU are fully independent (no cross talk inside FCU)***
    - ***Total of 9 modules***
  - ***In addition:***
    - ***PSU mounted on the bottom of the box***
    - ***"Internal" (DRCU sub-unit to sub-unit) Harnesses for secondary power routing between PSU and S/S (MCU-SCU-DCU) and DCU on/off power remote commanding.***

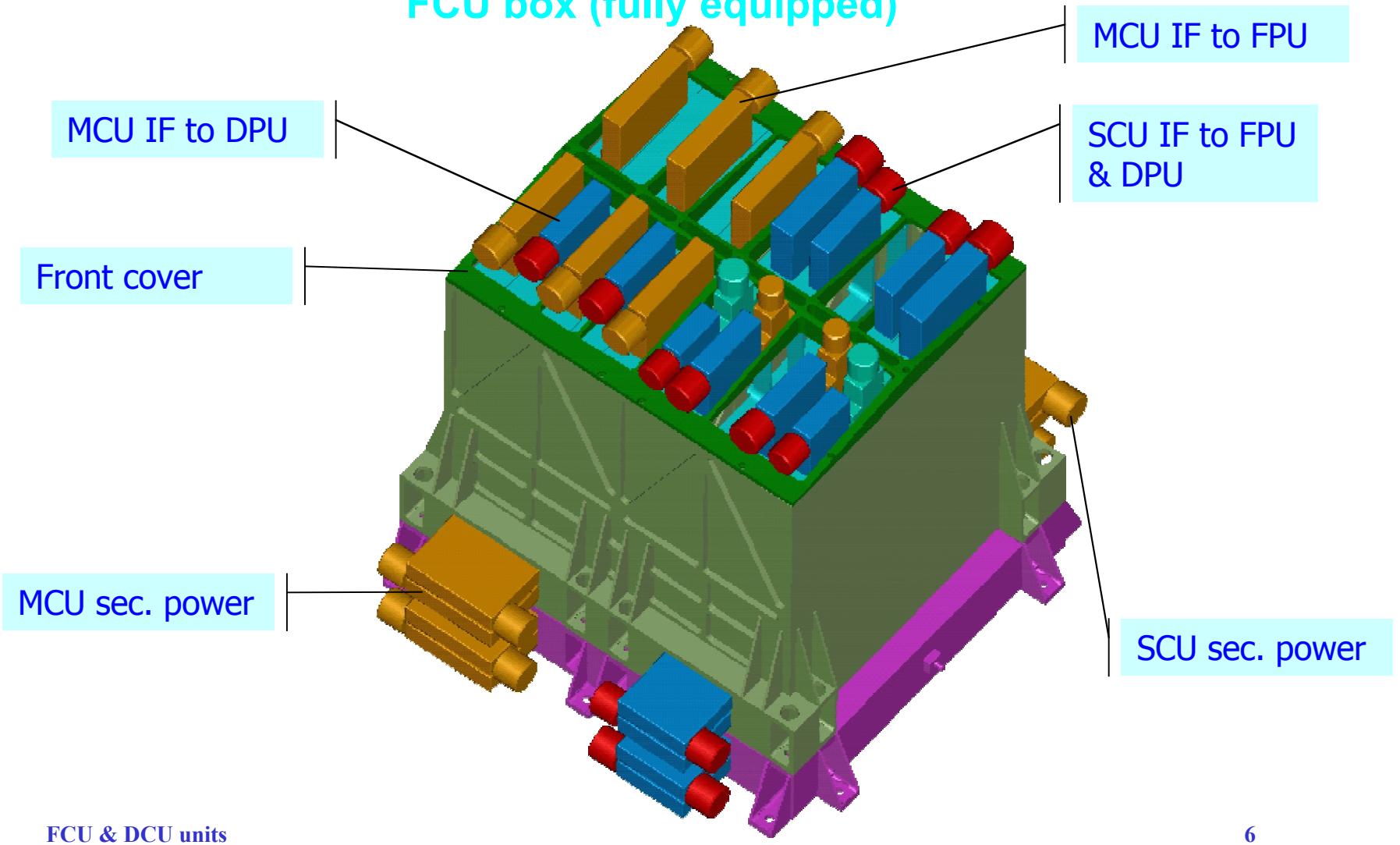
Unit Design (4)

FCU box



Unit Design (5)

FCU box (fully equipped)



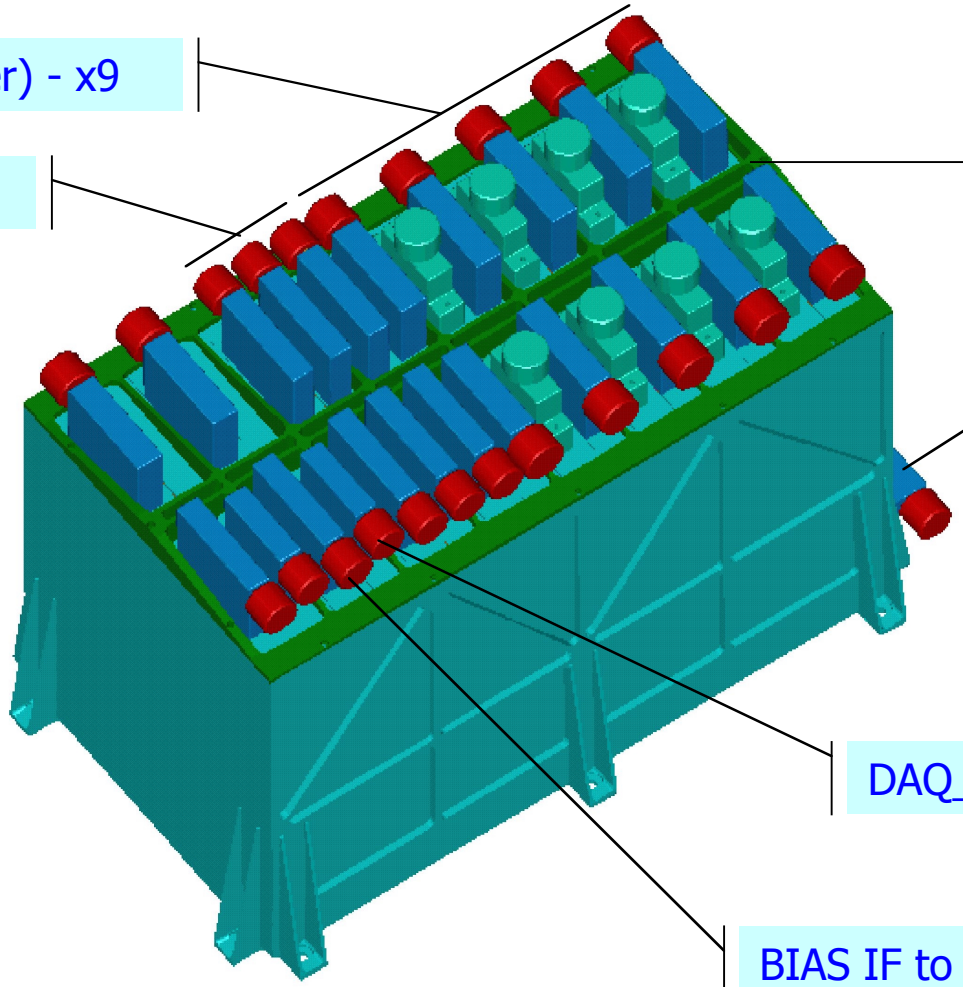
Unit Design (6)

- DCU Unit Design
  - Electrical
    - 5 board types:
      - *LIA_P (Photometer Lock-In Amplifier) - 9 x 32 analog channels*
      - *LIA_S (Spectrometer Lock-In Amplifier) - 3 x 24 analog channels*
      - *BIAS (Bolometer/JFET Bias) - 1 M + 1 R*
      - *DAQ_IF (Data Acquisition & DPU IF) - 1 M + 1R*
      - *DCU_BP (backplane & sps* regulators) - 1 M/R*
  - Mechanical
    - Similar to MCU & SCU
    - Same board geometry & stiffeners
    - Total of 16 modules

*: secondary power supply

Unit Design (7)

DCU box



Unit Status - H/W design(1)

- **DCU unit**
  - ***Readout:***
    - ***Breadboard tested (2 analog channels+1 bias channel)***
    - ***LIA_P QM1 ready for manufacturing: design transferred to JPL subcontractor***
    - ***LIA_S QM1 board design in progress (➔ 4/04)***
  - ***Control:***
    - ***Breadboard tested***
    - ***DAQ_IF QM1 board ready for manufacturing: design transferred to JPL subcontractor***
    - ***DAQ_IF control FPGA VHDL: 50% completion***
    - ***BIAS QM1 board ready for manufacturing: design transferred to JPL subcontractor***

Unit Status - H/W design (2)

- *Mechanics:*
  - *Overall Design (Stiffener+box) are ready*
  - *Detailed Design started (13/02)*

- **MCU S/S**

  ➔See dedicated presentation …

- **SCU S/S**
  - *DAQ_IF VHDL code CmdIF: version 2 distributed*
  - *DAQ_IF VHDL DataIF: version 2 distributed*
  - *DCU specific FIFO control to be designed*
  - *DAQ_IF master sequencer is designed*
  - *DAQ_IF acquisition sequencer to be designed*
  - *300mK temperature channel design is validated (jan. 02)*
  - *«>1K» temperature channel, Heater control design tests in progress (→ end of march)*
  - *TEMP board design starts after previous design validation*

Unit Status - H/W design (3)

- **FCU unit**
  - **Mechanics**
    - *Overall Design (Stiffener+box) are ready*
    - *Detailed Design started (13/02)*
    - *Thermal Modeling done (mainly for MCU boards)*
    - *Dynamic Modeling in progress:*
      - » *For S/S interface definition*
        - ✉ ***Last minute info:*** **box frequency ≥ 260 Hz**

Unit Status - S/W design (3)

- **The MCU is the only S/S which is concerned**

→ see dedicated presentation…

Unit Status (4)

- Test Equipments:
  - LTU
    - Preliminary specification available
    - Full specification in progress
    - Software specification is started
  - FPU simulator
    - Specification available
    - Electronics boards in fabrication
    - Software implementation in progress
- Documentation:
  - DRCU specifications - SAp-SPIRE-CCa-25-00 - 0.91
  - DRCU ICD - SAp-SPIRE-CCa-24-00 - 0.6
    - Electrical interface description is almost complete
    - Data and Command format is defined
    - Sub-system command list is preliminary (for MCU and SCU)
  - DCU design document - SAp-SPIRE-FP-xx-02 - draft
  - MCU design description - LAM/ELE/SPI/000619 - 3.0
  - FPU simulator specification - SIG-SPIRE-PDa-30-01 - 1.0
  - PSU specification
  - SCU design document redaction ongoing (→ end of march: draft)

Budgets

FCU

- *Outer envelope:*
  - 334 x 329 x 330.5
  (L x D x H - mm)
- *Mass:*
  - 18.26 kg (initial)
  - 14.28 kg (optimized)

DCU

- Outer envelope:
  - 494 x 289 x 305
  (L x D x H - mm)
- *Mass:*
  - 17.74 kg (initial)
  - 15.41 kg (optimized)

Allocation (IID-B): 23 kg

(IIDR: 25.35 kg)

- *Power consumption:*

Max. average: 79.9 W (photometer)

56.8 W (spectrometer)

Average (2/3 photo + 1/3 spectro): 71.5 W

Allocation (IID-B): 71.3 W

Models Definition

- **From the "Development Plan" document:**
  - **Breadboards:** to validate electronics designs (in particular: detector readout & drive electronics) [1]
  - **STMs:** to validate (vibration & thermal) DCU, PSU mechanical structure [1-2]
  - **EMs:** to perform electrical compatibility tests PSU-DRCU - PSU only [1]
  - **QMs:**
    - QM1: to validate design & electrical IF with FPU
    - QM2: fully qualified model [1]
  - **FM:** full model …
  - **FS:** spare boards only

[1]: not for delivery

[2]: FCU mechanical structure validated by BOLC unit STM(PACS) by similarity

Model summary

Systems	S/S L1	S/S L2	S/S L3	STM	EM	QM1	QM2	FM	FS
DRCU	DCU	DAQ_IF			1	1	2	2	1
		BIAS			1	1	2	2	1
		LIA_TC			0	0	1	1	1
		LIA_S			3	3	3	3	1
		LIA_P			2	2	8	8	2
		DCU_BP			1	1	1	1	1
		Box		1		“light”	1	1	-
	FCU	SCU	CCHK_IF			1	2	2	
			TEMP			1	2	2	
			SCU_BP			1	1	1	
	MCU					“light”	1	1	
		PSU			Lab	Power bench	STM EM	1	
Harness	DRCU/DPU					1	2	2	
	PSU/DCU-MCU/SCU					1 of each	2 of each	2 of each	

PA / QA Activities

- **Documentation available:**
  - Standard Product Assurance Plan
    - *SAp-GERES-FLo-436-00 issue 1.0 of 09/11/2000*
  - DRCU DCL
    - *SAp-SPIRE-VM-0058-01 issue 10 of 01/2002*
  - MCU EEE Part List
    - *LAM/SPIR/QUA/000201 issue 0.8*
  - DRCU DML
    - *SAp-SPIRE-NC-0060-02*
    - *LMA/ELE/FTS/011008.01*
  - DRCU DPL
    - *SAp-SPIRE-NC-0061-02*
    - *LAM/ELE/FTS/011009.01*
  - DRCU FMECA report
    - *SAp-SPIRE-FLo-0039_01 Issue 1.0 of 25/10/01*
  - MCU FMECA report
    - *LAM/ELE/SPI/010920 draft 1*

AIV Plan & Activities

- **AIV activities diagram is available for**
  - ***QM1***
  - ***QM2***
  - ***FM***

- *Test configurations document is available in draft form*

- *Test equipments required are identified & defined*
  - ***Factory Support Equipment (FSE) for post-fabrication testing (1 per electronics board)***
  - ***Local Test Unit (LTU) for DMC interface simulation***
  - ***FPU simulator for PhFPU simulation***

Problem Areas

- ***DCU/FCU mechanical interface with S/C***
  - *Problem: Need for formal agreement to proceed with mechanical manufacturing*
  - *Solution(s): depends on boxes configuration on panel*
    - *H/W is frozen: mechanical design modification would generate additional delay and cost*
    - *Connector back-shell modification might be still possible*
- ***Power Budget***
  - *Problem: Power Budget has increased since IIDR - close to SPIRE allocation*
- ***DCU QM1 PCB manufacturing:***
  - *Problem: manufacturing file transfer to US manufacturer extra delay in QM1 development*
  - *Solution(s):* Big effort at SACLAY to understand/correct potential problems

Problem Areas

- ***High accuracy capacitor (for LPF)***
  - *Problem: Procurement is difficult (due to manufacturer problem with specific dielectric)*
  - *Solution(s): find replacement*
    confirm requirement
- ***Component cost***
  - *Problem: current estimation exceed initial estimation*
  - *Solution(s):*
    - *…*

Schedule / Milestones

Milestones	
DCU QM1 delivery at CEA	08/11/2002
LTU need date	19/11/2002
SPIRE FPU simulator #1 need date	19/11/2002
Detector test cryostat delivered by JPL to CEA	26/11/2002
DRCU QM1 ready for delivery to RAL	03/03/2003
SPIRE FPU simulator #2 need date	28/07/2003
SCU QM2 ready	27/08/2003
MCU QM2 need date	27/08/2003
DRCU QM2 delivery to RAL	05/01/2004
MCU FM need date	26/04/2004
SCU FM need date	05/05/2004
DRCU FM ready for delivery to RAL	30/07/2004

MCU

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MCU

- The MCU controls the SMEC and the BSM mechanisms.
- The MCU is designed and developed at LAM with the cooperation of UKATC for the BSM part and of CEA-Sap for the DRCU part.

- No design change since DDR
- QM1 under progress
- Interfaces to be fixed with CEA for the QM2 and FPM to be subcontracted
- Planning shifted due to preceding point not achieved on time

MCU : QM1

dedicated to CQM tests

- Not form & fit
- Delivered in a separate box with power supplies
- Electrical and command interface Ok
- Flight functions Ok

Status

- MAC boards and BSM boards at LAM, being tested
- SMEC board to be at LAM end of May 2002
- QM1 finished end of June 2002, ready to operate the mechanisms
- QM1 used with SMECm CQM in Sep-Nov 2002
- To be delivered to CEA in Dec 2002

MCU : QM2 (1/2)

Used to qualify the electronics

- Subcontracted to the industry : call for tender beginning Apr 2002, for the QM2 and the PFM
- To be delivered to CEA in June 2003
- Apr-Jul 2002 = 4 months for industry answer
- Sep 2002 = T0 with the selected industrial
- Sep 2002-Mar 2003 = 7 months for manufacture(to be assessed with the selected industrial)
- *Oct-Nov 2002 = Technologica components received*
- Apr-May 2003 = electronic tests at LAM
- June 2003 = qualification tests at LAM

MCU : QM2 (2/2)

Point durs planning :

- Administrative delays for the contract
- Mech/Therm/Elec Interfaces MCU/DRCU (geometry, vibrations levels, thermal interfaces, location of some components, etc…) to be fixed in March 2002 between CEA and LAM

  Mechanical IF meeting: planned mid-march

  Electrical IF meeting: planned end of march
- FPGA Interface VHDL to be provided by CEA to be implemented on the QM1 and verified before Sep 2002

  Note: Version 2 VHDL distributed last week for validation

Open Point :

Mech/Therm behaviour of the MAC board. To close this point, the mech/therm interfaces must be fixed for LAM to evaluate the problem to specify correctly to the industry in Apr 2002.

SPIRE: DRCU & WIH Overall Development schedule

22/01/02

Nº	Nom de la tâche
1	
2	**SPIRE IBDR**
3	**Test means**
4	DRCU Simulator #1 development
5	DRCU Simulator #1 available
6	DRCU Simulator #2 available
7	LTU Development
8	LTU #1 available
9	**DRCU QM1**
10	DCU QM1 Development
11	SCU QM1 Development
12	MCU EM Available (from LAM)
13	DRCU QM1 Power bench development
14	BSM & FTS mec. Simulator #1 available (from LAM)
15	DRCU QM1 I&T
16	DRCU QM1 & WIH available
17	DRCU & WIH QM1 required at RAL
18	**DRCU QM2**
19	DCU QM2 Development
20	SCU QM2 Development
21	MCU QM Available (from LAM)
22	DRCU PSU SM available (from industry)
23	DRCU PSU EM available (from industry)
24	DRCU QM2 Power bench development
25	BSM & FTS mec. Simulator #2 available (from LAM)
26	FCU QM2 I&T
27	DRCU QM2 I&T
28	DRCU & WIH QM2 available
29	DRCU & WIH QM2 required at RAL
30	**DRCU FM**
31	DCU FM Development
32	SCU FM Development
33	MCU FM Available (from LAM)
34	DRCU PSU FM available (from industry)
35	BSM & FTS mec. Simulator #2 available (from LAM)
36	FCU FM I&T
37	DRCU FM I&T
38	DRCU & WIH FM available
39	DRCU & WIH QM2 required at RAL