DRCU FREQUENCY PLAN - 4/02/02   SPIRE-SAP-NOT-001175

P. Levacher / C. Cara

SPIRE Unit / subsystem	Frequency Source	Frequency Range Lower	Upper	W-form	Signal Level		Comment
DCU	Cmd IF Clock	312 kHz		Rect.	0	5 V	Differential RS422 – Continuous
	Data IF Clock	1MHz	2.5 MHz	Rect	0	5 V	Differential RS422
	Master Clock	10 MHz		Rect		5 V	Crystal Oscillator – Internal to unit
	Bolometer Bias	50 Hz	300 Hz	Sine	0	100 mV	Differential – Highly sensitive signal
	T/C Bias	50 Hz	300 Hz	Sine	0	500 mV	Differential – Highly sensitive signal
MCU	Cmd IF Clock	312 kHz		Rect.	0	5 V	Differential RS422-Continuous
	Data IF Clock	1MHz	2.5 MHz	Rect	0	5 V	Differential RS422
	Master Clock	40 MHz		Rect		5 V	Crystal Oscillator – Internal to unit
	DSP Clock	20 MHz		Rect		5 V	Master clock / 2 Internal to unit
	LVDT excitation	2.5 kHz		Sine		3 V	Differential +/- 20 %
	DAC change	3.0 kHz	10 kHz	Random		10 V	Internal to unit
	Position encoder	0	2.5 kHz	Sine		3 mV	Differential 250 Hz at nominal speed
SCU	Cmd IF Clock	312 kHz		Rect.	0	5 V	Differential RS422-Continuous
	Data IF Clock	1MHz	2.5 MHz	Rect	0	5 V	Differential RS422
	Master Clock	10 MHz		Rect		5 V	Crystal Oscillator – Internal to unit
	300 mK TS Bias	20 Hz		Rect		6 mV	Tr/Tf = 1ms Highly sensitive signal
	Photo Stimulus	0	5 Hz	Rect			
PSU	DC/DC switching frequency	131 kHz TBC					Free runing - ± 10% - internal to unit