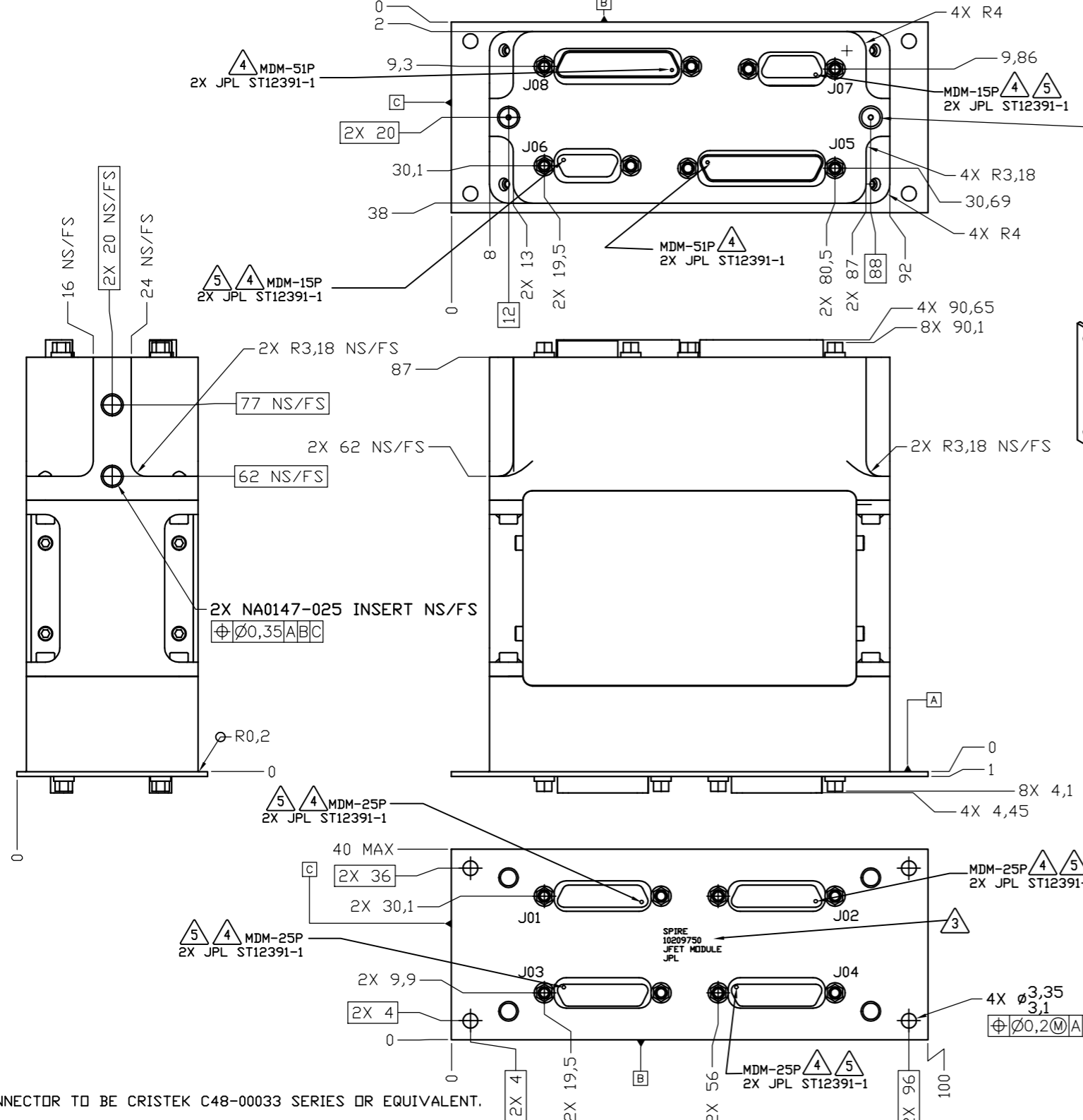
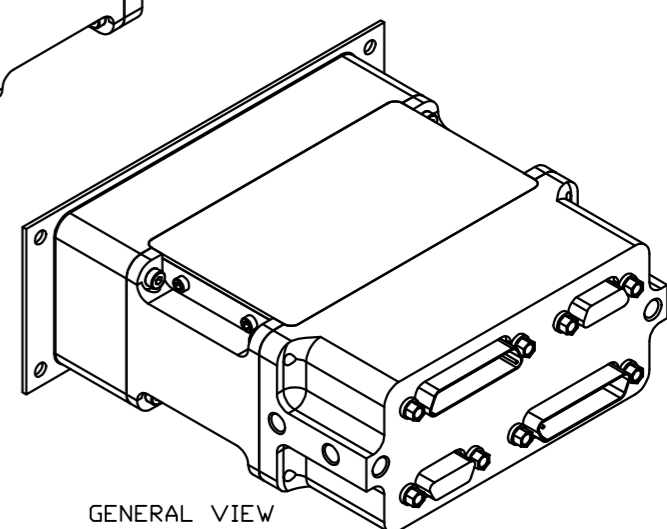
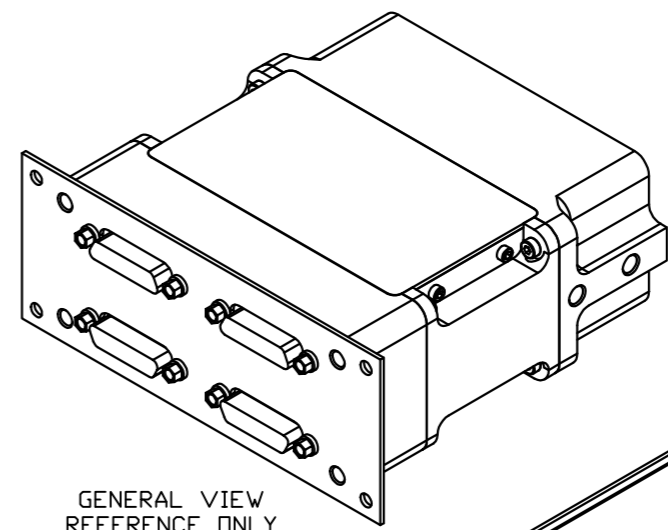


LTR		ZONE		REVISIONS										
DESCRIPTION				DWN	CHK	STRUCT	MATL	THRU	CONT	ENGR	DSGN	DATA	RELEASE	DATE
INITIAL RELEASE														
				SEE TITLE BLOCK										



2X NA0147-025 INSERT
 $\varnothing 0,35$ ABC



- 5 CONNECTOR TO BE CRISTEK C48-00033 SERIES OR EQUIVALENT.
- 4 CONNECTOR CUT OUTS SIZED TO ALLOW PROPER MATING OF SOCKET CONNECTORS.
- 3 ASSEMBLY NUMBER, NAME, TITLE, DASH NUMBER, AND REV LETTER TO APPEAR AS SHOWN IN THIS AREA.

2. THIS IS THE INTERFACE CONTROL DRAWING FOR THE JFET MODULE ASSEMBLY, JPL PART NUMBER 10209750, REFERENCE DESIGNATION TBD. JPL DRAWING NUMBER 10209750 SHALL CONTAIN THE FOLLOWING NOTE: THIS ASSEMBLY MEETS THE INTERFACE REQUIREMENTS OF JPL INTERFACE CONTROL DRAWING 10209722.

1. THIS TECHNICAL DATA IS EXPORT CONTROLLED UNDER U.S. LAW AND IS BEING TRANSFERRED BY JPL TO PPARC PURSUANT TO THE NASA / PPARC LETTER OF AGREEMENT WHICH ENTERED INTO FORCE ON DECEMBER 2, 1999. THIS TECHNICAL DATA IS TRANSFERRED TO PPARC FOR USE EXCLUSIVELY ON THE NASA/PPARC SPIRE ON FIRST COOPERATIVE PROJECT, MAY NOT BE USED FOR ANY OTHER PURPOSE, AND SHALL NOT BE RE-TRANSFERRED OR DISCLOSED TO ANY OTHER PARTY WITHOUT THE PRIOR WRITTEN APPROVAL OF NASA.

NOTES: UNLESS OTHERWISE SPECIFIED

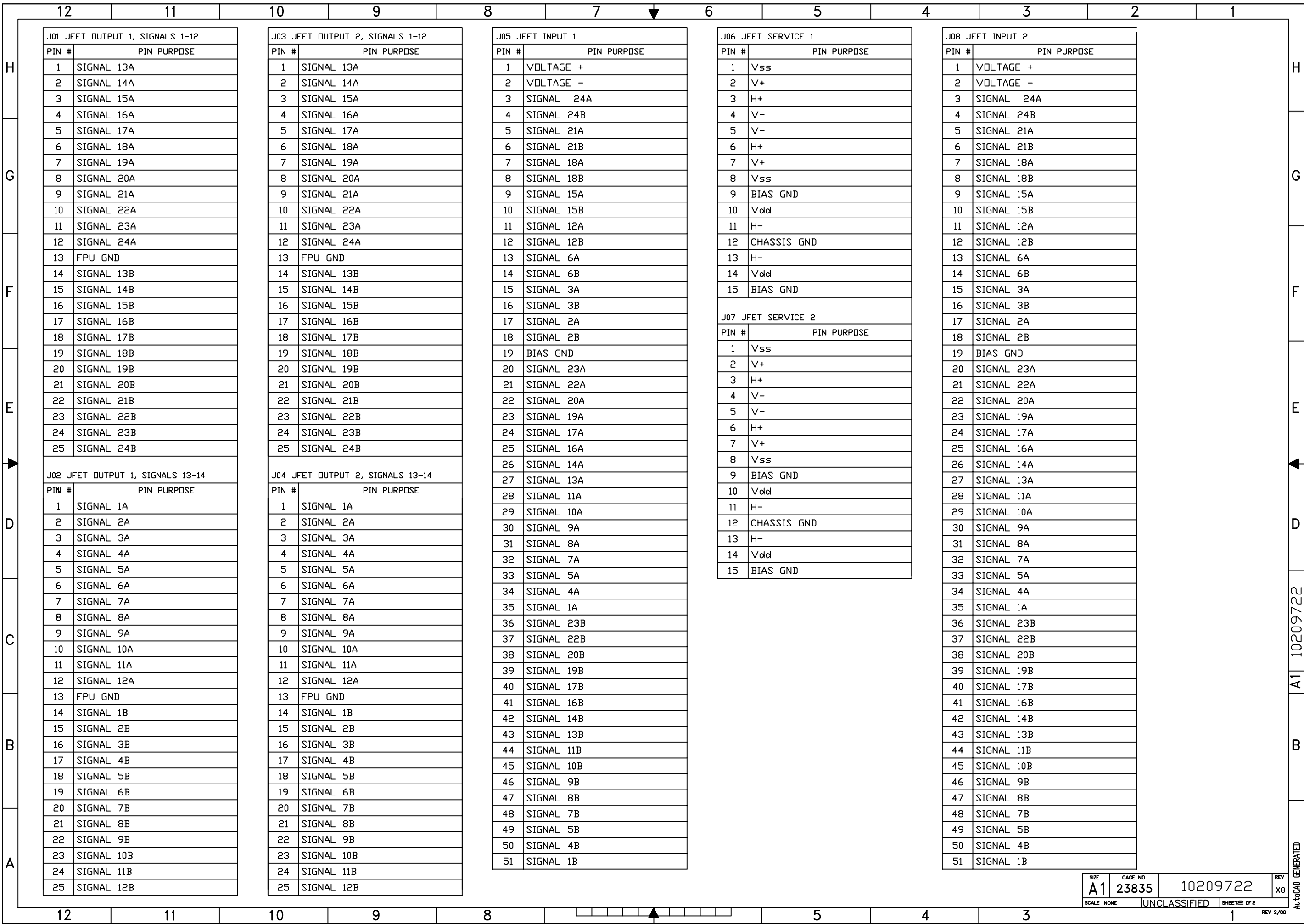
INTERFACE CONTROL DRAWING

QTY REQD	ITEM NO	REF DES	CAGE NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	MATERIAL OR NOTE	ZONE
PARTS LIST								
				CONTRACT NO	960939			
				APPD	DATE			
				DWN	01/09/02			
				CHK	01/10/02			
				STRUCT				
				MATL				
				THRU				
				CONT				
				ENGR				
				DSGN				
				SUPV				
				APPLICATION				
				UNLESS OTHERWISE SPECIFIED	DIMENSIONS ARE IN MILLIMETERS			
				LINEAR TOLERANCES:				
				0-6	± 0.1			
				OVER 6-30	± 0.2			
				OVER 30-120	± 0.3			
				OVER 120-315	± 0.5			
				OVER 315-1000	± 0.8			
				OVER 1000	± 1.2			
				ANGULAR TOLERANCES:				
				± 0.5°				
				MACHINE FINISH (MICROMETERS)				
				32/				
				DO NOT SCALE DRAWING				
				INTERPRET DWG PER ANSI Y14.100M				
				NEXT ASSEMBLY				
				SPIRE USED ON				
				APPLICATION				
				SCALE 2:1				
				UNCLASSIFIED				
				SHEET 1 OF 2				
				REV 2/00				

JET PROPULSION LABORATORY
 CALIFORNIA INSTITUTE OF TECHNOLOGY
 PASADENA, CA 91109
 RELEASED THROUGH EDMG
**JFET MODULE,
 INTERFACE CONTROL
 DRAWING**

SIZE **A1** CAGE NO **23835** **10209722** REV **X8**
 SCALE 2:1 UNCLASSIFIED SHEET 1 OF 2

A1 10209722 AutoCAD GENERATED



J01 JFET OUTPUT 1, SIGNALS 1-12

PIN #	PIN PURPOSE
1	SIGNAL 13A
2	SIGNAL 14A
3	SIGNAL 15A
4	SIGNAL 16A
5	SIGNAL 17A
6	SIGNAL 18A
7	SIGNAL 19A
8	SIGNAL 20A
9	SIGNAL 21A
10	SIGNAL 22A
11	SIGNAL 23A
12	SIGNAL 24A
13	FPU GND
14	SIGNAL 13B
15	SIGNAL 14B
16	SIGNAL 15B
17	SIGNAL 16B
18	SIGNAL 17B
19	SIGNAL 18B
20	SIGNAL 19B
21	SIGNAL 20B
22	SIGNAL 21B
23	SIGNAL 22B
24	SIGNAL 23B
25	SIGNAL 24B

J03 JFET OUTPUT 2, SIGNALS 1-12

PIN #	PIN PURPOSE
1	SIGNAL 13A
2	SIGNAL 14A
3	SIGNAL 15A
4	SIGNAL 16A
5	SIGNAL 17A
6	SIGNAL 18A
7	SIGNAL 19A
8	SIGNAL 20A
9	SIGNAL 21A
10	SIGNAL 22A
11	SIGNAL 23A
12	SIGNAL 24A
13	FPU GND
14	SIGNAL 13B
15	SIGNAL 14B
16	SIGNAL 15B
17	SIGNAL 16B
18	SIGNAL 17B
19	SIGNAL 18B
20	SIGNAL 19B
21	SIGNAL 20B
22	SIGNAL 21B
23	SIGNAL 22B
24	SIGNAL 23B
25	SIGNAL 24B

J05 JFET INPUT 1

PIN #	PIN PURPOSE
1	VOLTAGE +
2	VOLTAGE -
3	SIGNAL 24A
4	SIGNAL 24B
5	SIGNAL 21A
6	SIGNAL 21B
7	SIGNAL 18A
8	SIGNAL 18B
9	SIGNAL 15A
10	SIGNAL 15B
11	SIGNAL 12A
12	SIGNAL 12B
13	SIGNAL 6A
14	SIGNAL 6B
15	SIGNAL 3A
16	SIGNAL 3B
17	SIGNAL 2A
18	SIGNAL 2B
19	BIAS GND
20	SIGNAL 23A
21	SIGNAL 22A
22	SIGNAL 20A
23	SIGNAL 19A
24	SIGNAL 17A
25	SIGNAL 16A
26	SIGNAL 14A
27	SIGNAL 13A
28	SIGNAL 11A
29	SIGNAL 10A
30	SIGNAL 9A
31	SIGNAL 8A
32	SIGNAL 7A
33	SIGNAL 5A
34	SIGNAL 4A
35	SIGNAL 1A
36	SIGNAL 23B
37	SIGNAL 22B
38	SIGNAL 20B
39	SIGNAL 19B
40	SIGNAL 17B
41	SIGNAL 16B
42	SIGNAL 14B
43	SIGNAL 13B
44	SIGNAL 11B
45	SIGNAL 10B
46	SIGNAL 9B
47	SIGNAL 8B
48	SIGNAL 7B
49	SIGNAL 5B
50	SIGNAL 4B
51	SIGNAL 1B

J06 JFET SERVICE 1

PIN #	PIN PURPOSE
1	V _{ss}
2	V+
3	H+
4	V-
5	V-
6	H+
7	V+
8	V _{ss}
9	BIAS GND
10	V _{dd}
11	H-
12	CHASSIS GND
13	H-
14	V _{dd}
15	BIAS GND

J07 JFET SERVICE 2

PIN #	PIN PURPOSE
1	V _{ss}
2	V+
3	H+
4	V-
5	V-
6	H+
7	V+
8	V _{ss}
9	BIAS GND
10	V _{dd}
11	H-
12	CHASSIS GND
13	H-
14	V _{dd}
15	BIAS GND

J08 JFET INPUT 2

PIN #	PIN PURPOSE
1	VOLTAGE +
2	VOLTAGE -
3	SIGNAL 24A
4	SIGNAL 24B
5	SIGNAL 21A
6	SIGNAL 21B
7	SIGNAL 18A
8	SIGNAL 18B
9	SIGNAL 15A
10	SIGNAL 15B
11	SIGNAL 12A
12	SIGNAL 12B
13	SIGNAL 6A
14	SIGNAL 6B
15	SIGNAL 3A
16	SIGNAL 3B
17	SIGNAL 2A
18	SIGNAL 2B
19	BIAS GND
20	SIGNAL 23A
21	SIGNAL 22A
22	SIGNAL 20A
23	SIGNAL 19A
24	SIGNAL 17A
25	SIGNAL 16A
26	SIGNAL 14A
27	SIGNAL 13A
28	SIGNAL 11A
29	SIGNAL 10A
30	SIGNAL 9A
31	SIGNAL 8A
32	SIGNAL 7A
33	SIGNAL 5A
34	SIGNAL 4A
35	SIGNAL 1A
36	SIGNAL 23B
37	SIGNAL 22B
38	SIGNAL 20B
39	SIGNAL 19B
40	SIGNAL 17B
41	SIGNAL 16B
42	SIGNAL 14B
43	SIGNAL 13B
44	SIGNAL 11B
45	SIGNAL 10B
46	SIGNAL 9B
47	SIGNAL 8B
48	SIGNAL 7B
49	SIGNAL 5B
50	SIGNAL 4B
51	SIGNAL 1B

J02 JFET OUTPUT 1, SIGNALS 13-14

PIN #	PIN PURPOSE
1	SIGNAL 1A
2	SIGNAL 2A
3	SIGNAL 3A
4	SIGNAL 4A
5	SIGNAL 5A
6	SIGNAL 6A
7	SIGNAL 7A
8	SIGNAL 8A
9	SIGNAL 9A
10	SIGNAL 10A
11	SIGNAL 11A
12	SIGNAL 12A
13	FPU GND
14	SIGNAL 1B
15	SIGNAL 2B
16	SIGNAL 3B
17	SIGNAL 4B
18	SIGNAL 5B
19	SIGNAL 6B
20	SIGNAL 7B
21	SIGNAL 8B
22	SIGNAL 9B
23	SIGNAL 10B
24	SIGNAL 11B
25	SIGNAL 12B

J04 JFET OUTPUT 2, SIGNALS 13-14

PIN #	PIN PURPOSE
1	SIGNAL 1A
2	SIGNAL 2A
3	SIGNAL 3A
4	SIGNAL 4A
5	SIGNAL 5A
6	SIGNAL 6A
7	SIGNAL 7A
8	SIGNAL 8A
9	SIGNAL 9A
10	SIGNAL 10A
11	SIGNAL 11A
12	SIGNAL 12A
13	FPU GND
14	SIGNAL 1B
15	SIGNAL 2B
16	SIGNAL 3B
17	SIGNAL 4B
18	SIGNAL 5B
19	SIGNAL 6B
20	SIGNAL 7B
21	SIGNAL 8B
22	SIGNAL 9B
23	SIGNAL 10B
24	SIGNAL 11B
25	SIGNAL 12B