DPU/ICU

Derating and Worst Case Analysis

Document Ref: CNR.IFSI.2002TR06

Issue 1.4

Distribution List :

K. King		
O. Bauer		
K. Wafelbakker		
R. Cerulli		
S. Molinari		
S. Pezzuto		
A. Di Giorgio		

Prepared by: Renato Orfei Date: 24 September 2003

Document Status Sheet

Issue	Revision	Date	Reason for Change
Issue 1		31-01-2002	
	1	15-05-2002	Updating
	2	28-02-2003	Updating
	3	17-03-2003	Updating
	4	24-09-2003	Updating

Document Change Record

Document Title: DPU/ICU Derating and Worst Case Analysis	
Document Reference Number: CNR.IFSI.2002TR6	
Document Issue/Revision Number: Issue 1.4	
Section	**Reason For Change**
All	Issue 1
	Issue 1.1
All	Full revision
	Issue 1.2
3.1.3	Added with 3 sub-sections
3.2.3	Added with 4 subsections
3.3.4	Added

	Issue 1.3
2.1	Added documents 9, 10 and 11
2.2	Updated reference documents list
3.3.4	Changed the maximum working temperature
	Issue 1.4
3.4	Updated after SPIRE IHDR

Acronyms

AD	Architectural Design
ASI	Italian Space Agency
ATP	Acceptance Test Plan
AVM	Avionic Model
BSW	Basic SW
CDR	Critical Design Review
CGS	Carlo Gavazzi Space
CIDL	Configuration Item Data List
CSL	Configuration Status List
CNR	Consiglio Nazionale delle Ricerche
CPP	Co-ordinated Parts Procurement Board
CPU	Control Processing Unit
CDMS	Central Data Management System
CDMU	Central Data Management Unit
CQM	Cryogenic Qualification Model
DCU	Detector Control Unit
DDD	Detailed Design Document
DPU	Digital Processing Unit
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electro Magnetic Compatibility

EMI	Electro Magnetic Interference
ESA	European Space Agency
FIRST	Far InfraRed and Submillimeter Telescope
HK	HouseKeeping
HW	HardWare
IBDR	Instrument Baseline Design Review
ICD	Interface Control Document
ICDR	Instrument Critical Design Review
ICU	Instrument Control Unit
IHDR	Instrument Hardware Design Review
IFSI	Istituto di Fisica dello Spazio Interplanetario
ISVR	Instrument Science Verification Review
LCU	Local oscillator Control Unit
LVDS	Low Voltage Differential Signal
MCU	Mechanism Control Unit
NA	Not Applicable
OBS	On-Board Software
OBSM	On Board Software Management
PA	Product Assurance
PDU	Power Distribution Unit
PROM	Programmable Read Only Memory
PUS	Packet Utilisation Standard
S/C	SpaceCraft

SCC	SpaceCraft Components
SEU	Single Event Upset
SPIRE	Spectral and Photometric Imaging Receiver
S/S	SubSystem
SPR	Software Problem Report
SSD	Software Specification Document
SVM	Service Module
SW	Software
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TV	Thermal Vacuum
WBS	Work Breakdown Structure
WCA	Worst Case Analysis
WRT	With Respect To

1 SCOPE

The Istituto di Fisica per lo Spazio Interplanetario (IFSI) of the Italian Consiglio Nazionale delle Ricerche (CNR) is responsible for the design and manufacturing of the three Digital Processing Units/Instrument Control Unit for the three instruments to be flown on board of the ESA satellite Herschel (ex FIRST): HIFI, PACS and SPIRE.

The design, manufacturing, electrical and functional tests of the DPU/ICU boards and the Basic Software in PROM, are implemented by Carlo Gavazzi Space (CGS) under a contract with ASI. IFSI is responsible of the mechanical box, the box connectors, the electrical-mechanical integration, the environmental tests and the On Board Software.

The purpose of this document is to assess the derating concepts and the Worst Case Analysis used during the design of the DPU/ICU.

It has to be noted that all DPU/ICU electronic components will be purchased through the Co-ordinated Parts Procurement Agency set up by ESA and contracted to Tecnologica (Sevilla, Spain) and TOP-REL (Rome, Italy).

2 DOCUMENTS

2.1 APPLICABLE DOCUMENTS

AD	Name
01	Herschel/Planck Instrument Interface Document, part A
02	Herschel/Planck Instrument Interface Document, part B, Instrument PACS
03	Herschel/Planck Instrument Interface Document, part B Instrument HIFI
04	Herschel/Planck Instrument Interface Document, part B Instrument SPIRE
05	DPU/ICU PA Plan
06	PACS PA Plan
07	HIFI PA Plan
08	SPIRE PA Plan
09	PACS AVM Design Description
10	HIFI AVM Design Description
11	SPIRE AVM Design Description

2.2 Reference documents

Reference Document	Name
01	Derating Requirements Applicable to Electronic, Electrical and Electro-mechanical Components for ESA Space Systems (ESA PSS-01-301)
02	Declared Components Lists: IFSI/ICU/LI/2001-004
03	Declared Components, Materials and Processes Lists: PACS-CR-GS-012
04	Declared Components, Materials and Processes Lists: SPIRE-IFS-DOC-001031
05	PACS FMECA
06	HIFI FMECA
07	SPIRE FMECA
08	PAD for CGS made inductors
09	PAD for CGS made transformers
10	RFA for CGS made inductors
11	RFA for CGS made transformers
12	CPU Board Design
13	CPU Board Piggy-Back Design

14	Interface Board Design
15	DC/DC Converter Board Design
16	Mother-Board Design
17	HLP-6000 Series Beta Transformer Technology Corporation data Sheet

3 Analysis of the "internal" electronics

For "internal electronics" it is meant all the electronics of the following boards, excluding the electrical interfaces with the spacecraft that will be dealt with in the following section:

- CPU board
- I/F board
- DC/DC Converter Board
- Motherboard.

According to a general statement in the contract ASI-CGS, all design activities are in agreement with the ESA applicable directives, e.g. as per REF 01.

3.1 CPU Board Derating and Worst Case Analysis

The whole CPU Board is powered with 5 V, the core of the FPGA RT54SX32S is powered with 2.5 V. The differences between the CPU boards for HIFI and SPIRE with respect to the PACS one is the presence on the PACS mezzanine board of the ATMEL chip TSS901ESBMV implementing 3 STD 1355 links and the relevant LVDS drivers/receivers. Hence from the point of view of the following analysis there is no difference in the CPU boards for the 3 instruments.

3.1.1 Capacitors Derating and WCA

As can be seen from REF 02-03-04 the capacitors of the CPU board are of the following types:

-chip ceramic capacitors: 50 V 10%
-Tantalum capacitors: 30 V 10% or 60V 10%

The required derating is 50% for chip ceramic capacitors: actual derating is 10 times.
The required derating is 60% for tantalum capacitors: actual derating is 6 or 12 times, respectively, with respect to 30 V or 60 V tantalum capacitors.

WCA: the delta C variations, a 50% drop in initial minimum insulation resistance, a 100% increase of the initial maximum leakage current are well within the selected capacitors rated values.

3.1.2 Resistors derating and WCA

As can be seen from REF 02-03-04 the resistors of the CPU board are of the following types:

-chip resistors: 0.1 W , 1%, 50 V, 200 ppm/C°
-network resistors: 0.325 W 5%

The required derating is 80% for voltage, 50% for power for chip resistors.
The actual voltage derating is 10 times.
The power derating is such that the minimum allowed resistor directly connected between 5V and GND is 500 OHM. By checking REF 12 and REF 13 it is clear that this is not the case.

WCA: the worst case for all chip resistors is during thermal vacuum at about 70 C°, in this condition, by allowing a 2% reduction in resistance and taking into account the delta °C variations, a minimum resistance of 517 OHM directly connected between 5V and GND is allowed. By checking the schematics shown in REF 12 and REF 13 it is clear that this is not the case.

3.1.3 Other Components

As can be seen from REF 02-03-04 the remaining CPU board components are :

- digital integrated circuits
- 20 MHz clock oscillator
- 1 diode 1N6642US20

3.1.3.1 Digital Integrated Circuits

The digital integrated circuits are:
-powered with 5 V (greater than the minimum (4.5 V) recommended voltage and less than the 75% of the maximum specified rated value (7V)); maximum recommended voltage is 5.5 V.
(The FPGA power supply is 2.5 V, within the recommended 2,25 V ÷ 2.75 V)
-connected to other CMOS circuits via buffers to increase the fan-out.

WCA: no degradation beyond the minimum specified input and output voltage range is to be considered

3.1.3.2 20 MHz clock oscillator

For the digital integrated circuit what is above applies; for the quartz temperature the operating temperature is well higher than 10 °C WRT the minimum specified value (-55 °C) and 10 °C less than the maximum specified value (125 °C).

WCA: there is no DPU-ICU specification of the clock frequency stability, the quartz stability of a maximum of 65 ppm over the full temperature range – 55°C to + 125 °C is more than sufficient.

3.1.3.3 Diode 1N6642US

The diode is used for further protection of a CMOS input of the switch-on circuitry (RD12) . It is in 5 V circuit as far as the reverse voltage is concerned (rated 75 V) and its direct current is limited by a 100 OHM resistor in series with a 5V generator, plus CMOS internal resistance, well below the 65% of the rated 0.3 A.

WCA: leakage current (NA) , breakdown voltage (reduced by 5%) and forward voltage (NA) are well below the rated values.

3.2 I/F Board Derating and Worst Case Analysis

The I/F Board is powered with 5 V, the core of the FPGA RT54SX32S is powered with 2.5 V; the analogue electronics and the DDC chip BU-61582F1 implementing the STD 1553B are powered with +15 V and – 15 V (the DDC chip also with +5 V). The differences between the I/F boards for HIFI and SPIRE with respect to the PACS one is the absence on the PACS I/F board of the FIFOs and the balanced line drivers and receivers as the internal I/F to/from subsystems is made in PACS, as already written, via the ATMEL chip TSS901ESBMV implementing 3 STD 1355 links and the relevant LVDS drivers/receivers. Hence from the point of view of the following analysis there is no difference in the I/F boards for the 3 instruments.

3.2.1 Capacitors Derating and WCA

As can be seen from REF 02-03-04 the capacitors of the CPU board are of the following types:

-chip ceramic capacitors: 50 V 10%
-chip ceramic capacitors: 100 V 10%

-Tantalum capacitors: 50 V 10%

The required derating is 50% for chip ceramic capacitors: actual derating is 10 times for capacitors connected to + 5 V, and it is more than 3 times for those connected to + - 15 V.

The required derating is 60% for tantalum capacitors: actual derating is 10 times for capacitors connected to + 5 V, and it is more than 3 times for those connected to + - 15 V.

WCA: the delta C variations, a 50% drop in initial minimum insulation resistance, a 100% increase of the initial maximum leakage current are well within the selected capacitors rated values.

3.2.2 Resistors derating and WCA

As can be seen from REF 02-03-04 the resistors of the I/F board are of the following types:

-chip resistors: 0.1 W , 1%, 50 V, 200 ppm/C°
-metal film resistors 0.125 W 0.1% 200 V 5ppm
-network resistors: 0.325 W 5%.

The required derating is 80% for voltage, 50% for power for chip resistors.
The actual voltage derating:

- for chip resistors is 10 times at +5 V, more than 3 times at +-15 V;
- for metal film resistors is 40 times at +5 V, more than 10 times at +-15 V.

The power derating is such that the minimum allowed resistor directly connected between 5V and GND is 500 OHM and from +-15 V and GND is 4500 OHM. By checking the schematics shown in REF 14 it is clear that this is not the case.

WCA: the worst case for all resistors is during thermal vacuum at about 70 C°, in this condition, by allowing a 2% reduction in resistance and taking into account the delta °C variations, a minimum resistance of 517 OHM directly connected between 5V and GND and of 4650 OHM between +-15 V and GND are allowed. By checking the schematics shown in REF 14 it is clear that this is not the case.

3.2.3 Other Components

As can be seen from RF 02-03-04 the remaining I/F board components are :

- digital integrated circuits
- 16 MHz clock oscillator for the DDC chip implementing the STD-1553

- 1 diode 1N5811US
- 2 transformers HLP6002 for the "long stub" implementation of the STD-1553

3.2.3.1 Digital Integrated Circuits

The digital integrated circuits are:
powered with 5 V (greater than the minimum (4.5 V) recommended voltage and less than the 75% of the maximum specified rated value (7V)); maximum recommended voltage is 5.5 V.
(The FPGA power supply is 2.5 V, within the recommended 2,25 V ÷ 2.75 V)

WCA: no degradation beyond the minimum specified input and output voltage range is to be considered

3.2.3.2 16 MHz clock oscillator

For the digital integrated circuit what is above applies; for the quartz temperature the operating temperature is well higher than 10 °C WRT the minimum specified value (-55 °C) and 10 °C less than the maximum specified value (125 °C).

WCA: the STD-1553 specifies a clock frequency stability better than 1%: i.e. 1 MHz ±10 kHz, which, referred to the 16 MHz clock means 16 MHz ± 160 kHz. The quartz stability of a maximum of 65 ppm over the full temperature range – 55°C to + 125 °C is far better (1040 Hz).

3.2.3.3 Diode 1N5811US

The diode is used for further protection of a CMOS input of the switch-on circuitry (RD14) . It is in 5 V circuit as far as the reverse voltage is concerned (rated 150 V) and its direct current is limited by the CMOS internal resistance well below the 65% of the rated 3 A.

WCA: leakage current (NA) , breakdown voltage (reduced by 5%) and forward voltage (NA) are well below the rated values.

3.2.3.4 HLP6002 STD-1553 transformers

The HLP6002 transformer is manufactured by Beta Transformer Technology Corporation (RD17), a subsidiary of DDC (Data Device Corporation, the firm which produces the chip that implements the

STD-1553). The transformer is guaranteed to be built and tested for the STD-1553A and B, MIL-PRF-21038, designed to meet ESDS Test, MIL-STD-883, Method 3015.3 Category B, operating temperature range – 55°C ÷ 130 °C.
WCA: no degradation is foreseen for the Worst Case Analysis for transformers, chokes, coils, motor windings components characteristics (section 3.3, page 8 of REF 01).

3.3 DC/DC Converter Board Derating and Worst Case Analysis

The circuits of the DC/DC Board powered with 28 V are:

- the soft start circuitry,
- the Under Voltage Protection,
- the "power" switching section.

The switching control section is powered with 15 V.

The differences between the DC/DC boards for PACS and SPIRE with respect to the HIFI one is the absence on the PACS and SPIRE board of 3 regulated and 3 unregulated additional voltages used to power the HIFI subsystem FCU. The general concept of the different output voltages is always the same and so we can consider that there are no relevant differences among the three DC/DC converters, two of them (i.e. PACS and SPIRE) actually identical in design and implementation.

3.3.1 Capacitors Derating and WCA

As can be seen from REF 02-03-04 the capacitors of the DC/DC board are of the following types:

- chip ceramic capacitors: 50 V 10%
- chip ceramic capacitors: 100 V 10%
- Tantalum capacitors: 50 V 10%
- Tantalum capacitors: 60 V 10%

Looking at the schematics in REF15, page 2 of 6, one can see that capacitor C6 in series with C16, and capacitor C19 in series with C21 are connected to the input lines. The capacitors are identical and of 3.3 nF, 50 V 10%, so the nominal derating is greater than 3 times.

The capacitors directly connected to Power GND and to + 28 V are C10, C11, C12 and C13, all tantalum 8.2 uF 60 V: derating greater than 2 times; the capacitors C14 and C15 are also connected to Power GND and to 28 V: they are .1uF 100 V and their derating is larger than 3 times; capacitors C4 in series with C17 and the like C5 in series with C18 are .47uF and 50 V, their derating is larger than 3 times.

Looking at the schematics in REF15, page 3 of 6, one can see the remaining capacitors directly connected to Power GND and to 28 V in the switching transformer: C134, C136, C137, and C144 all tantalum 8.2 uF 60 V: derating greater than 2 times; the capacitors C129 and C147 are .1uF 100 V and their derating is larger than 3 times.

The required derating is 50% for chip ceramic capacitors: actual derating is 10 times for capacitors connected to + 5 V, and it is more than 3 times for those connected to + - 15 V.

The required derating is 60% for tantalum capacitors: actual derating is 10 times for capacitors connected to + 5 V, and it is more than 3 times for those connected to + - 15 V.

WCA: the delta C variations, a 50% drop in initial minimum insulation resistance, a 100% increase of the initial maximum leakage current are well within the selected capacitors rated values.

3.3.2 Resistors derating and WCA

As can be seen from REF 02-03-04 the resistors of the DC/DC board are of the following types:

-chip resistors: 0.25 W , 1%, 50 V, 200 ppm/C°
-metal film resistors 0.125 W, 0.1%, 200 V 5ppm
-low valued resistors: 1 W 1%

The required derating is 80% for voltage, 50% for power for chip resistors.
The actual voltage derating:

- for chip resistors is 10 times at +5 V, more than 3 times at +-15 V;
- for metal film resistors is 40 times at +5 V, more than 10 times at +-15 V.
- at least 2 chip resistors are in series if connected to Power GND and to + 28 V, so their derating is larger than 3 times.

The power derating is such that the minimum allowed resistor directly connected between 5V and GND is 500 OHM and from +-15 V and GND is 4500 OHM. By checking REF 15 it is clear that this is not the case.

WCA: the worst case for all chip resistors is during thermal vacuum at about 70 C°, in this condition, by allowing a 2% reduction in resistance and taking into account the delta °C variations, a minimum resistance of 517 OHM directly connected between 5V and GND and of 4650 OHM between +-15 V and GND are allowed. By checking REF 15 it is clear that this is not the case.

3.3.3 Transformers and inductances

All transformers and inductances are designed in agreement with REF 01 with respect to:

- the voltage applied, to be considered for insulation properties (REF 08 and 10);
- the current flowing, to be considered for the transformer/inductance core selection and wire gauge selection (REF 08 and 10).

WCA: no degradation is foreseen for the Worst Case Analysis for transformers, chokes, coils, motor windings components characteristics (section 3.3, page 8 of REF 01).

3.3.4 Transistors and diodes of the Power Converter Section

The Part Stress Analysis and the Worst Case Analysis for diodes and transistors follows. The DC/DC schematics (REF15) shows the components types, the thermal worst case analysis is shown in AD 9-10-11.

UNIT: DPU-ICU	Date: 28/02/2003
Schematic drawing: DPU-EM-310.02-0	Analysed by: Renato Orfei
Parts List: IFSI/ICU/LI/2001-004 (HIFI)	Parts List :PACS-CR-GS-012
Parts List :SPIRE-IFS-DOC-001031	
Ambient Temperature : Typ. 25 °C S/C max: 40 °C max 72 °C	

Ref Des.	Type Value	Para.	RatedValue	Derat. value	Oper. value	C	Remark
Q1	2N7236	Id	18 A @ 25 °C	11 A	2A	Y	Used for soft start

	(IRFM9140)	BVdss Tj	11 A @100 °C 100 Vmin 150 °C	6.6 A 95V 110 °C	35V 72 °C		
Q3,	2N2905A	Ic P VCEsat Tj	600 mA@25°C 600mW@25°C 0.71V@240mA 200 °C	450 mA 360mW 0.78V 110 °C	240mA 324mW 1.35V 72 °C	Y	HIFI-FCU +5V stabilised CN : SRON-U/HIFI/CN/2002-003 pending
Q5,	2N2905A	Ic P VCEsat Tj	600 mA@25°C 600mW@25°C 0.71V@240mA 200 °C	450 mA 360mW 0.78V 110 °C	190mA 256mW 1.35V 72 °C	Y	HIFI-FCU +15V stabilised CN : SRON-U/HIFI/CN/2002-003 pending
Q6	2N2905A	Ic P VCEsat Tj	600 mA@25°C 600mW@25°C 0.71V@240mA 200 °C	450 mA 360mW 0.78V 110 °C	150mA 150mW 1.35 V 72 °C	Y	HIFI-FCU -15V stabilised CN : SRON-U/HIFI/CN/2002-003 pending
Q4	2N5154	Ic Ic P Tj	10A <8,3 ms 2A continuous 1W @25 °C 200 °C	7,5 A 1,4 A 600mW 110 °C	- - - 40 °C	Y	HIFI-FCU +5 V stabilized craw-bar protection
Q7, Q8	2N7224	Id BVdss Tj	34 A @ 25 °C 21 A @ 100 °C 100 Vmin 150 °C	20 A 12 A 95V 110 °C	1A 58V 72 °C	Y	Used in the push-pull for HIFI-FCU
Q9, Q10	2N7224	Id BVdss Tj	34 A @ 25 °C 21 A @ 100 °C 100 Vmin 150 °C	20 A 12 A 95V 110 °C	1A 58V 72 °C	Y	Used in the push-pull for DPU-ICU
Q11, Q12, Q13	2N2222 SMD	Ic P Tj	500 mA 500mW 200 °C	375 mA 300mW 110 °C	<10mA <10mW 40 °C	Y	Used at signal levels
D2	1N4467 12V/0.12A Zener	I P Tj	120 mA 1,5W 175 °C	60mA 0.75W 110 °C	< 2mA <25 mW 40 °C	Y	

D3	1N5811US	Vr	150V	112V	35V	Y	Inversion protection
D6	1N4465 10V/0.14A Zener	I P Tj	143 mA 1,5W 175 °C	70mA 0.75W 110 °C	< 3mA <30 mW 40 °C	Y	
D7, D10	1N5811US	Vr I Tj	150V 3A@55°C 175°C	112V 1.5A 110°C	15V < 5 mA 40 °C	Y	Used at signal level
D9, D17	1N5811US	Vr I Tj	150V 3A@55°C 175°C	112V 1.5A 110°C	70V < 40 mA 40 °C	Y	Snubber circuit for HIFI-FCU
D8, D11	1N5822US	Vr I Tj	40V 3A@55°C 175°C	30V 1.5A 110°C	15V < 300 mA 40 °C	Y	5V Rectifier for 5 V stabilized for HIFI-FCU
D12, D14, D18, D19	1N5811US	Vr I Tj	150V 3A@55°C 175°C	112V 1.5A 110°C	36V <1 A 40 °C	Y	±15V Rectifier for ±16 V Stabilized for FCU
D13, D15	1N5811US	Vr I Tj	150V 3A@55°C 175°C	112V 1.5A 110°C	15V < 500 mA 40 °C	Y	PWM feed-back control for FCU
D18	1N6642US	Vr I Tj	100V 300mA@25°C 175°C	75V 150mA 110°C	15V < 5 mA 40 °C	Y	Used at signal level
D20, D22	1N5822US	Vr I Tj	40V 3A@55°C 175°C	30V 1.5° 110°C	20V < 50 mA 40 °C	Y	8V Rectifier for 8 V unregulated for FCU
D21, D23, D25, D26	1N5811US	Vr I Tj	150V 3A@55°C 175°C	112V 1.5A 110°C	40V < 80 mA 40 °C	Y	±18V Rectifier for ± 18V unregulated for FCU
D24, D27	1N5811US	Vr I Tj	150V 3A@55°C 175°C	112V 1.5A 110°C	15V < 5 mA 40 °C	Y	Used at signal level
D54	1N4465 10V/0.14A Zener	I P Tj	143 mA 1,5W 175 °C	70mA 0.75W 110 °C	< 10mA <100 mW 40 °C	Y	
D28,	1N5811US	Vr	150V	112V	70V	Y	Snubber circuit for

D31		I Tj	3A@55°C 175°C	1.5A 110°C	< 40 mA 40 °C		DPU-ICU
D29, D30	1N5811US	Vr I Tj	150V 3A@55°C 175°C	112V 1.5A 110°C	15V < 500 mA 40 °C	Y	PWM feed-back control for DPU-ICU
D40, D42, D44, D47	1N5811US	Vr I Tj	150V 3A@55°C 175°C	112V 1.5A 110°C	32V < 300 mA 40 °C	Y	±15V Rectifier for DPU-ICU
D32, D33, D34, D35, D36, D37, D38, D39, D41, D49	1N6642US	Vr I Tj	100V 300mA@25°C 175°C	75V 150mA 110°C	15V < 5 mA 40 °C	Y	Used at signal level
D43, D48	1N6642US	Vr I Tj	100V 300mA@25°C 175°C	75V 150mA 110°C	30V < 45 mA 40 °C	Y	Rectifier for PWM control
D53	1N6660	Vr I Tj	45V 15A@25°C 150°C	33V 7.5A 110°C	12V < 2 A 40 °C	Y	5V Rectifier for DPU-ICU

WCA: the breakdown decrease of 5%, the 10% increase in the forward voltages and the increase of 5 times of the leakage currents do not affect the performances of the above diodes and transistors.

3.4 Motherboard Derating

The Motherboard is purely passive and contains only 12 DIN 41612 Eurocard connectors. The PCB itself, as all Printed Circuit Boards, will be designed and manufactured according to ESA approved Flight quality rules both for the materials and for the technology design rules. The DIN 41612 connectors are designed to withstand 2A per pin/socket. With reference to RD16 we can see what shown in the following table for the Nominal (or Prime) DPU:

Connector	Pins	Current expected (A)	Maximum allowed Current (A)	Note
P6	1,33,65; 3,35,67	< 2A	6A	+28 Bus
	22-31,54-63,86-95	<1A	6A	5,±15,8V, ±18V only HIFI FCU
P5	1,33,65,2,3,35,36,66, 17,81,30,32,62,64,94,96	<2A	16A	5V DPU
	34	<100mA	2A	2.5V FPGA
	29,61,93; 31,63,95	<0,5A	6A	±15 V DPU

The same applies for DPU Redundant on the same pins for connectors P11 and P12.

4 Analysis of the electrical interfaces with the spacecraft

The interfaces of the DPU/ICU with the spacecraft are:
- mechanical,
- thermal
- electrical.

Only the electrical interfaces will be dealt with in the following and these can be splinted in two:
- Power interface
- Telemetry and Telecommand interface.

4.1 Power interface derating and Worst Case Analysis

The DPU/ICU power interface with the spacecraft is shown in the following figure.
It is to be recalled that in a single DPU/ICU box there will be two completely separated units with one ON while the other is OFF in cold redundancy state. The spacecraft decides which unit is ON by powering it via the 28 V lines.
The interfaces with the S/C power system are:

a) the wires from the spacecraft PDU to DPU/ICU connector(s);
b) the power connector pins;
c) the common mode transformer located in the DC/DC converter board.

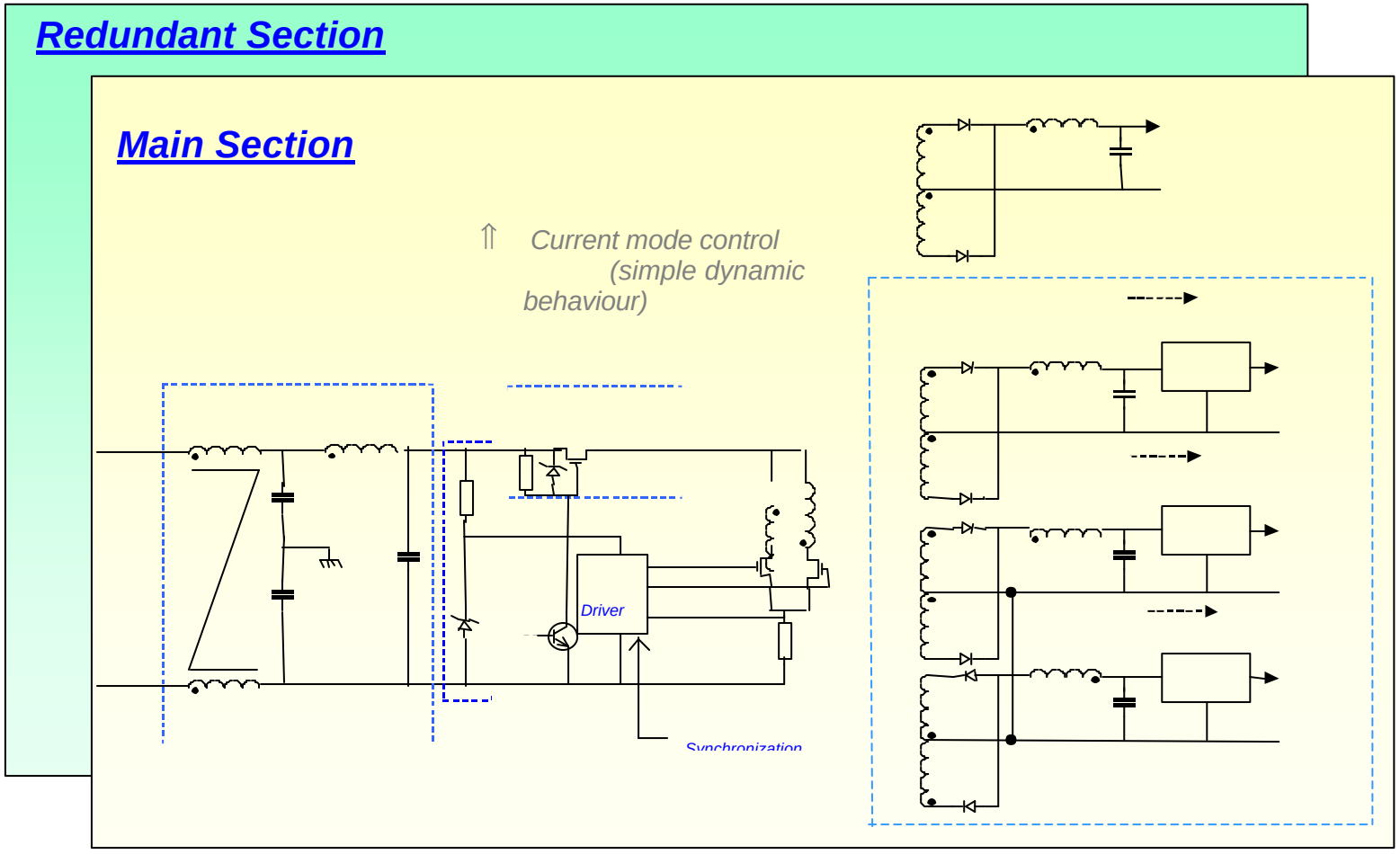
a) The wires from the PDU to DPU/ICU are not considered here as they are S/C provided.

b) There are 2 power connector pins for +28 V and 2 power connector pins for 28 V return. The maximum steady current is less than 1 A for PACS and SPIRE and less than 2 A for HIFI, when HIFI is fully operational. The 2 pins are well beyond the 50% required derating as each connector pin is rated 5 A.

WCA: no degradation is foreseen for the Worst Case Analysis for the connectors components characteristics (section 3.6, page 11 of REF 01).

c) The common mode transformer is designed in agreement with REF 01 with respect to:
- the voltage applied, to be considered for insulation properties (REF 08 and 10);
- the current flowing, to be considered for the transformer core selection and wire gauge selection (REF 08 and 10).

WCA: : no degradation is foreseen for the Worst Case Analysis for transformers, chokes, coils, motor windings components characteristics (section 3.3, page 8 of REF 01).


Redundant Section
Main Section
⇑ Current mode control (simple dynamic behaviour)
Driver
Synchronization

4.2 Spacecraft Interface Derating and Worst Case Analysis

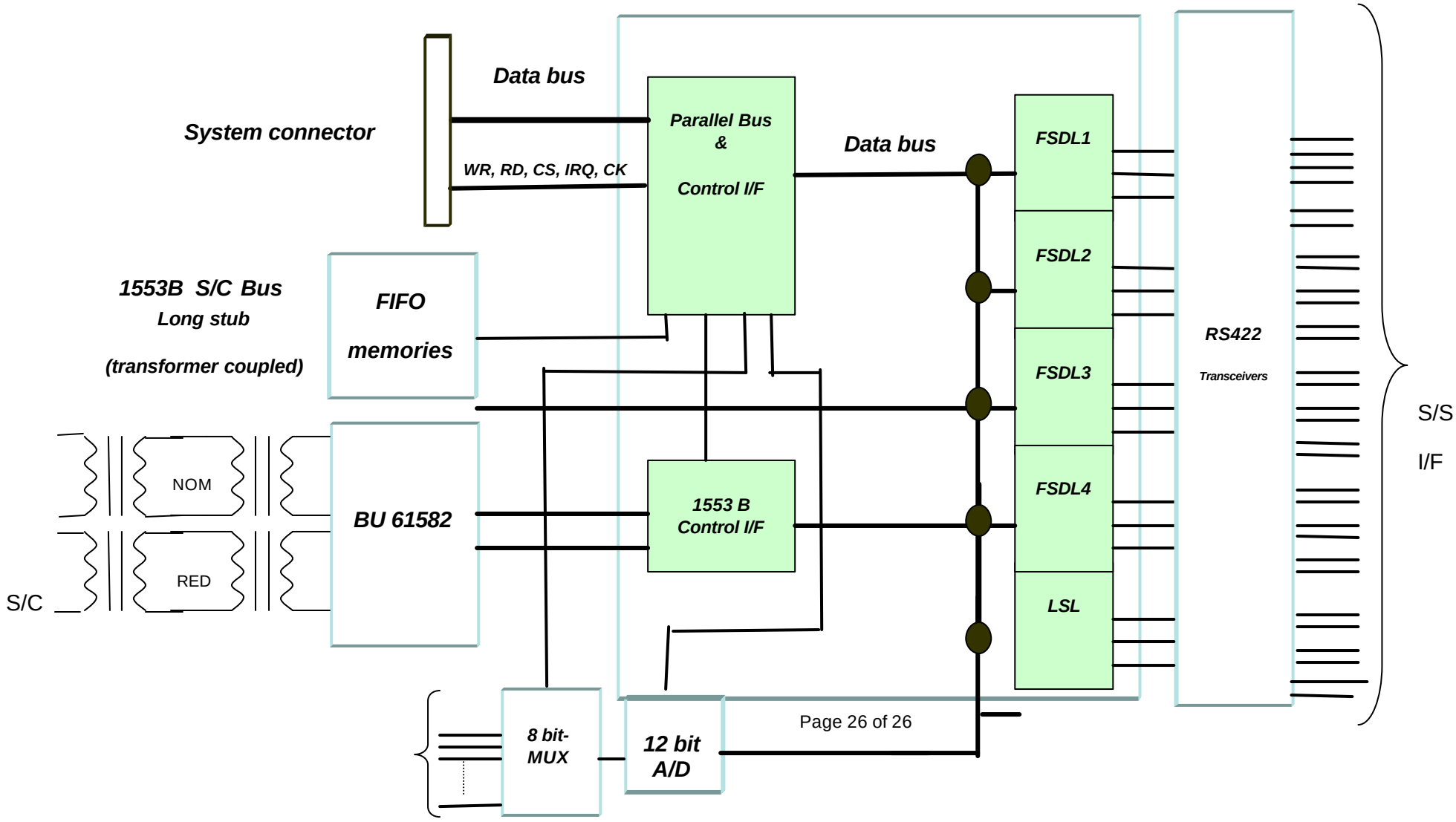
In the following figure the spacecraft interface circuitry is shown as part of the interface board. The interface is based on the MIL STD 1553B, that is on the spacecraft side (acting as Bus Controller) there is a bus on which are serially transmitted telecommands and serially received the telemetry from the instruments (acting as Remote Terminals).

The chosen configuration is "long stub" and the electrical interface is implemented via a suitable transformer. It is to be noted that there are a Prime ("A") and Redundant (B") connections to the Prime CDMS, and the same applies for the Redundant CDMS and the Redundant DPU/ICU.

There are no derating and/or WCA rules to be followed in the cabling from CDMU (S/C responsibility) and the pertinent DPU/ICU box connectors, as the current flowing via the sockets is well below the rated 5 A (28 Vpp on 75 OHM).

The transformer used to interface with the spacecraft 1553B bus in the "long stub" configuration is just designed by BTC (a subsidiary of DDC) to this purpose and recommended by DDC (the manufacturer of the special hybrid device that implements the 1553B standard). The transformer characteristics (type HLP6002) are then such as to be selected and be put in the Co-ordinated Parts Procurement Agency. No further analysis is then carried out about this component and thus this has to be considered "passed" as far as the derating criteria are concerned (see also section 3.2.3.4).

WCA: this interface has to be considered compliant not only because the transformers are purchased via the Co-ordinated Parts Procurement Agency, but also because no degradation is foreseen for the Worst Case Analysis for transformers, chokes, coils, motor windings components characteristics (section 3.3, page 8 of REF 01).


Data bus
System connector
WR, RD, CS, IRQ, CK
Parallel Bus
&
Control I/F
Data bus
FSDL1
FSDL2
FSDL3
FSDL4
LSL
RS422
Transceivers
S/S
I/F
1553B S/C Bus
Long stub
(transformer coupled)
FIFO
memories
NOM
RED
S/C
BU 61582
1553 B
Control I/F
8 bit-
MUX
12 bit
A/D