HERSCHEL/SPIRE

Breadboard test report

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	Function	Name	Date	Visa
Prepared by		**PINSARD**	**3/7/2001**	
Verified by				
Approved by				

DOCUMENT STATUS and CHANGE RECORD

Date	Issue	Affected pages
3/7/2001	1	Creation

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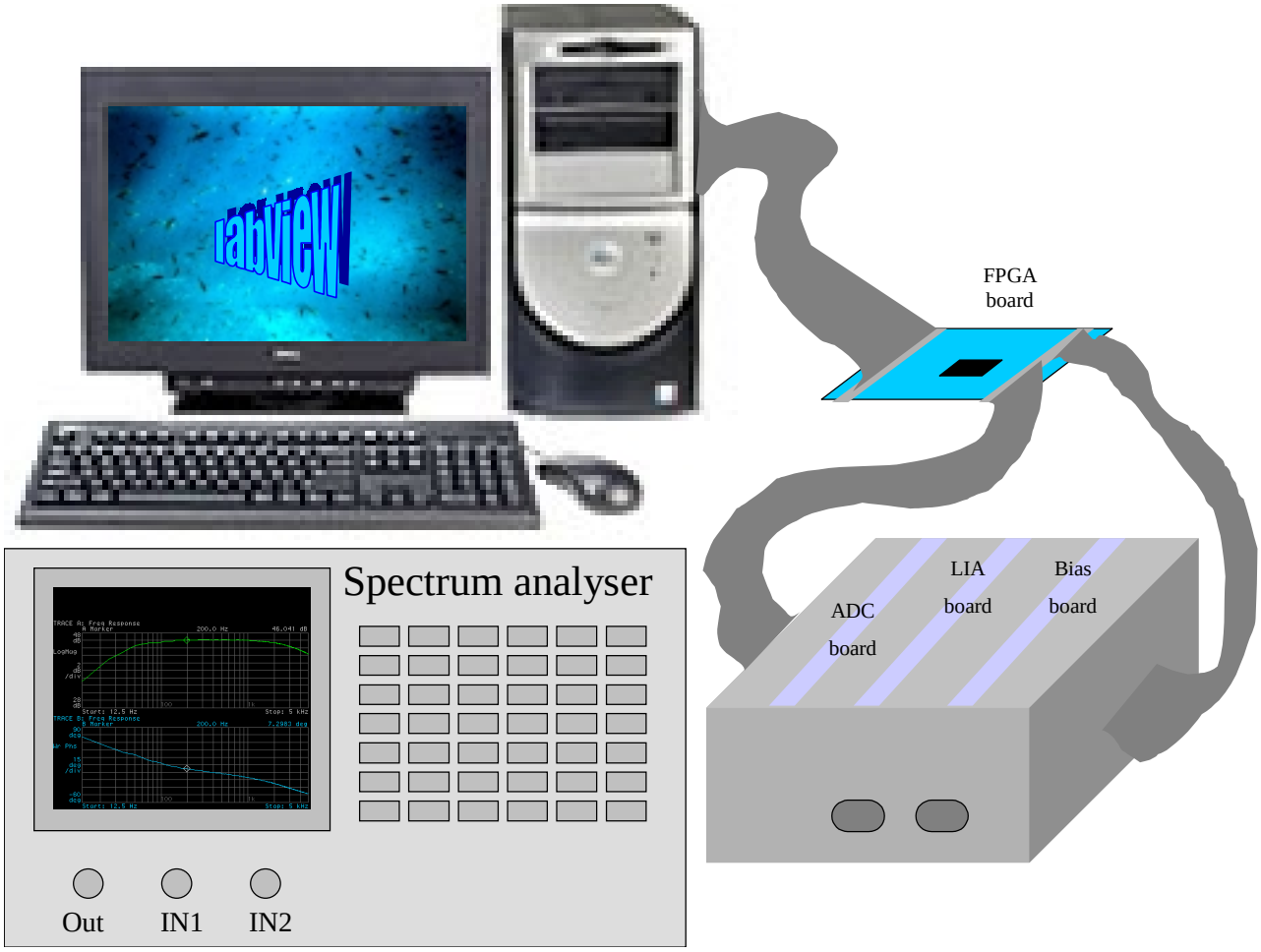
1 GENERAL DESCRIPTION

3 boards constitute the prototype. A back plane insure internal connection

The boards are:

-1 LIA board with 2 photometer channels
-1 BIAS board with 1 bias generator
-1 ADC board with 2 channels input and 1 ADC

A FPGA board and a PC with Labview control the prototype.



2 REFERENCE DOCUMENT

Detector Subsystem Specification Document: FIRS-SPI-PRJ-000103

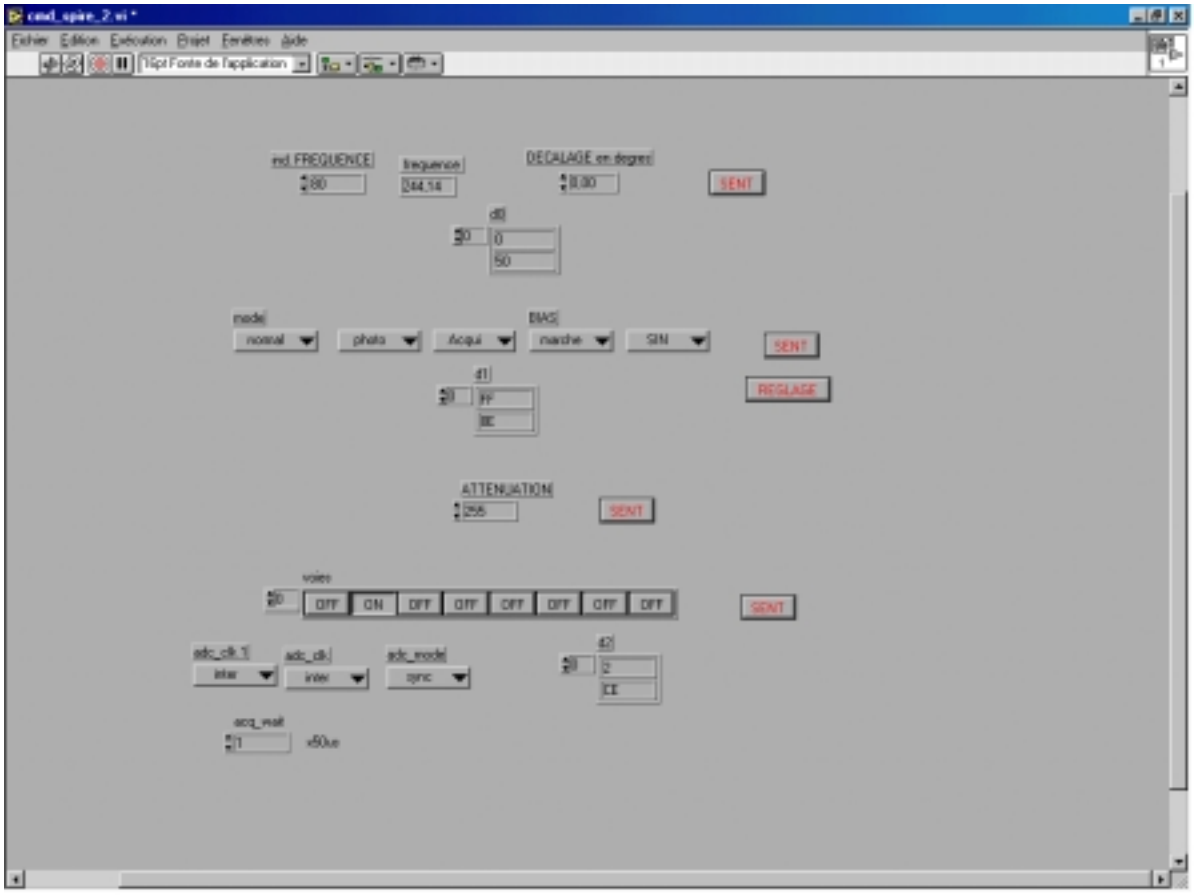
3 PC configuration

Labview + acquisition board PCI DIO 32 HS

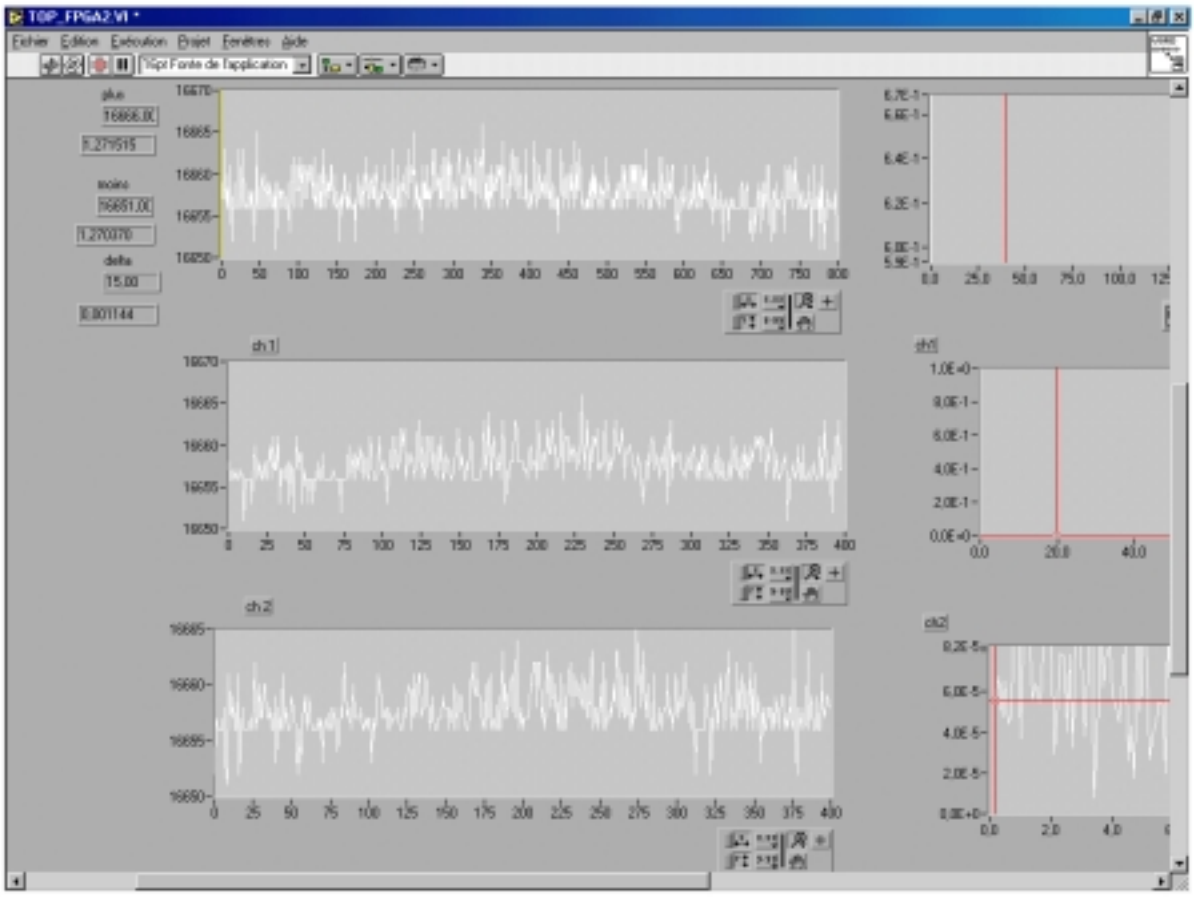
We have different VI (Virtual Instrument) to command the prototype and log the data

With The command VI (cmd_spire_2.vi), we can choose:

- The bias Frequency and the phase between the sine bias and the square demodulation signal.
- The bias amplitude
- The FPGA mode (normal/test, photometer/spectrometer, bias ON/OFF…)
- Start the offset setup
- From which channels we want to take the data.



With The acquisition VI (top_FPGA_2.vi) we can see the data from different channels.

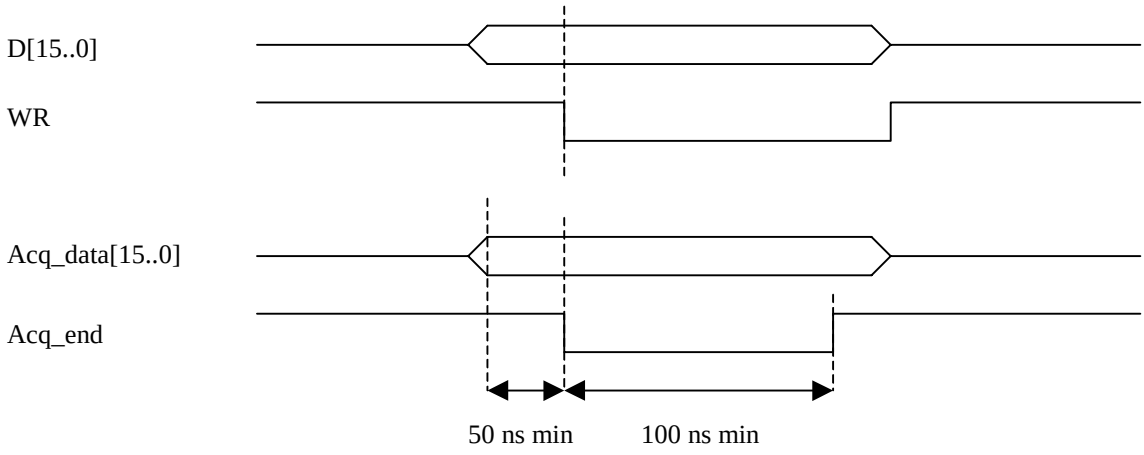


4 Interface between the PCI board and FPGA board

4.1 Interface description

We use a 16 bits parallel bus to transmit the commands word to the FPGA.
And an other one to catch the data from the FPGA.

Carte FPGA	Carte CPI DIO		Carte FPGA	Carte CPI DIO
Acq_data (15)	DIOD7		D(15)	DIOB7
Acq_data (14)	DIOD6		D(14)	DIOB6
Acq_data (13)	DIOD5		D(13)	DIOB5
Acq_data (12)	DIOD4		D(12)	DIOB4
Acq_data (11)	DIOD3		D(11)	DIOB3
Acq_data (10)	DIOD2		D(10)	DIOB2
Acq_data (9)	DIOD1		D(9)	DIOB1
Acq_data (8)	DIOD0		D(8)	DIOB0
Acq_data (7)	DIOC7		D(7)	DIOA7
Acq_data (6)	DIOC6		D(6)	DIOA6
Acq_data (5)	DIOC5		D(5)	DIOA5
Acq_data (4)	DIOC4		D(4)	DIOA4
Acq_data (3)	DIOC3		D(3)	DIOA3
Acq_data (2)	DIOC2		D(2)	DIOA2
Acq_data (1)	DIOC1		D(1)	DIOA1
Acq_data (0)	DIOC0		D(0)	DIOA0
Acq_end	REQ2		WR	ACK1

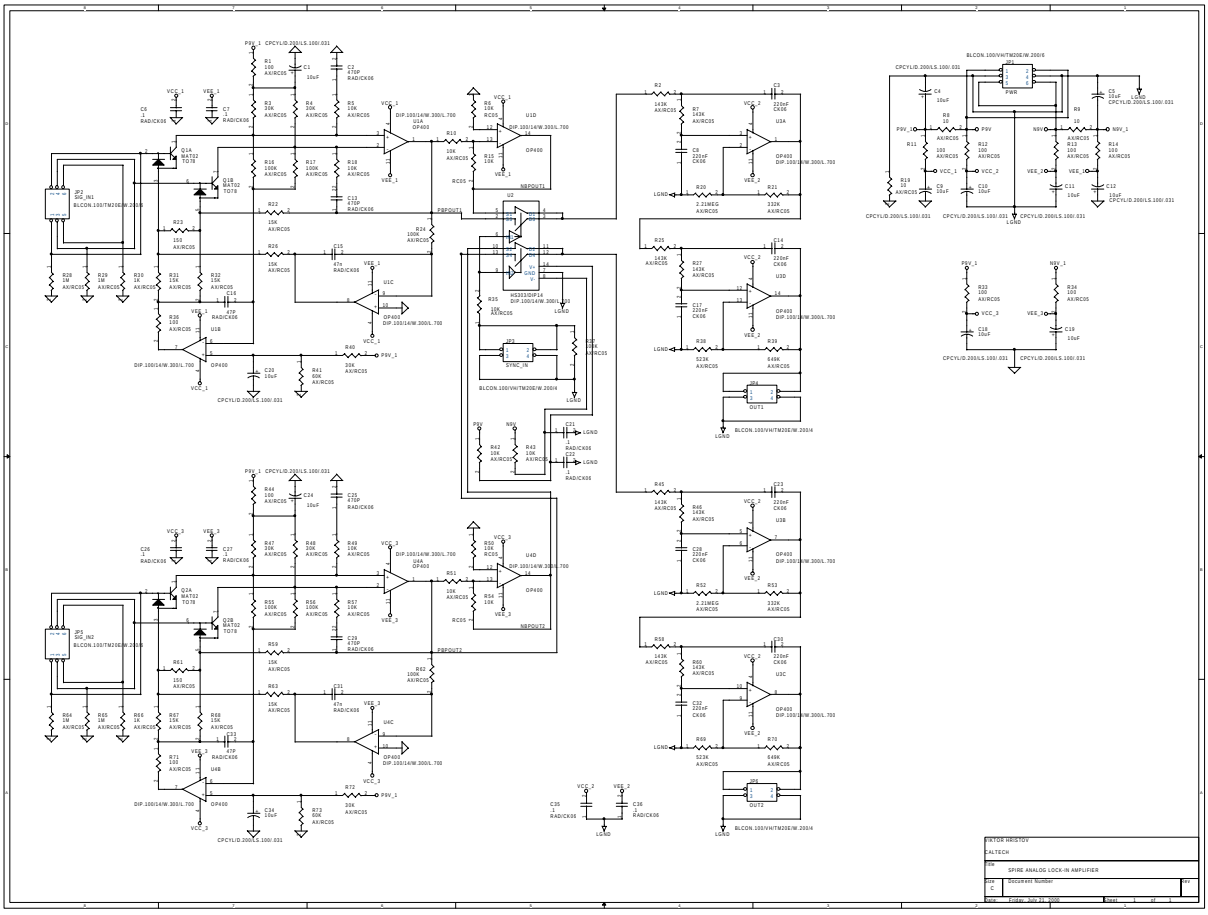


5 LIA board tests

For LIA function, we tested two drawings

5.1 LIA schematic 1

Scheme with MAT02

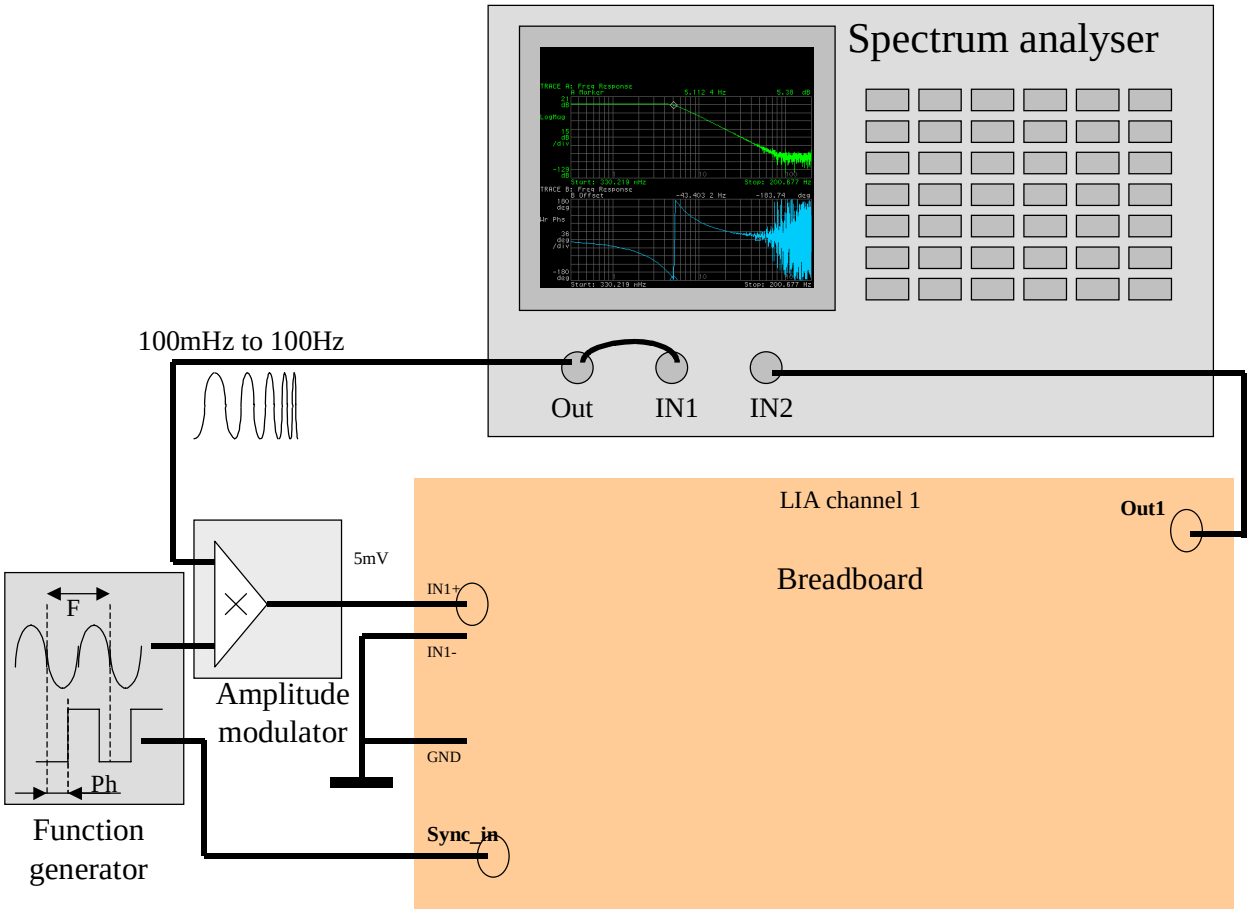


We found a problem due to the high resistor values we have implemented in the Low Pass Filter.
To solve the problem, we choose to replace:

- R20 and R52 =2,21 MΩ by 65kΩ
- R21 and R53 =332 kΩ by 10kΩ
- R38 and R69 =523 kΩ by 8kΩ
- R39 and R70 =649 kΩ by 10kΩ

5.1.1 Transfer function

5.1.1.1 Measurement configuration



For this measurement the modulation frequency F was put at 200Hz

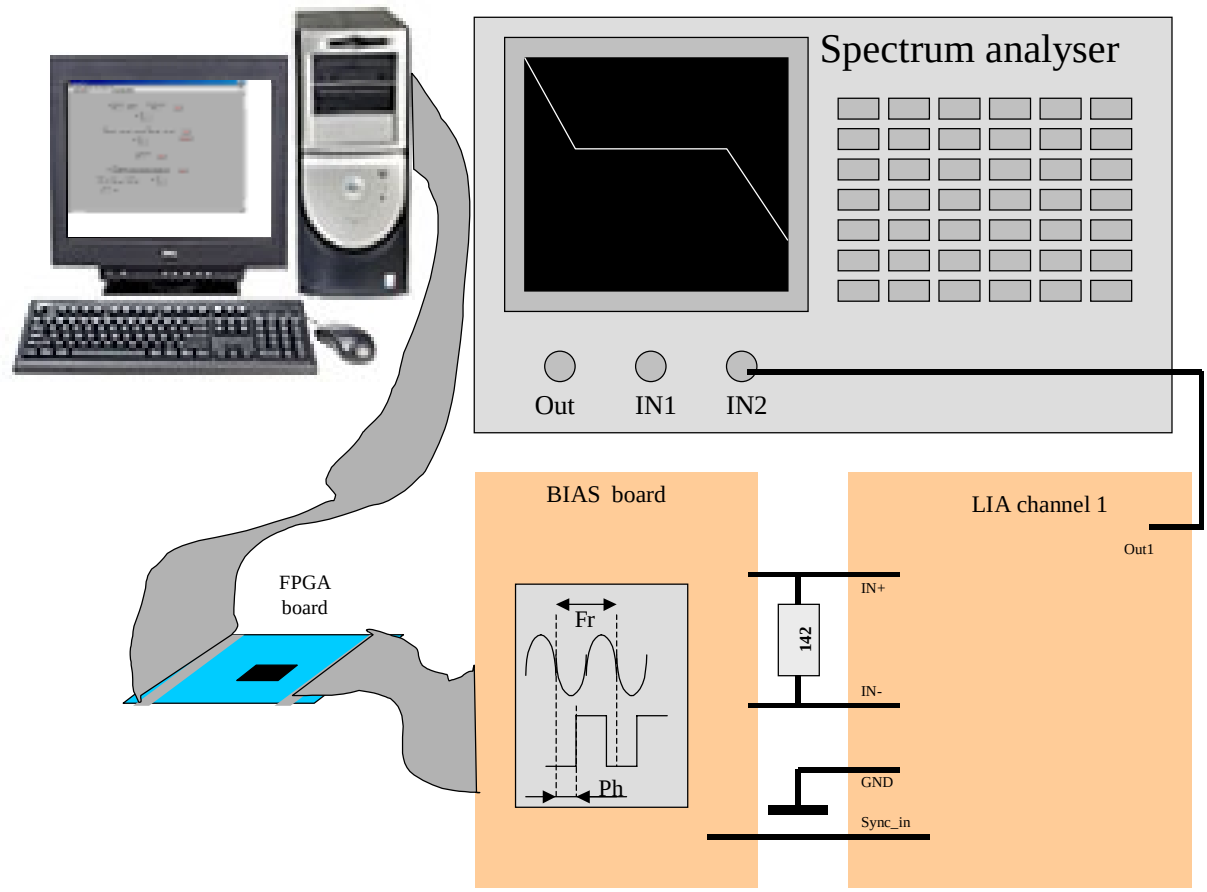
5.1.1.2 Result

Aim was the BDA-DRCU13 requirement: The signal bandwidth of photometer channels shall be 0.03 to 5Hz.

We have measured a gain of 500 and a –3dB cut off of 5Hz with –80dB slope.

5.1.2 Input noise

5.1.2.1 Measurement configuration

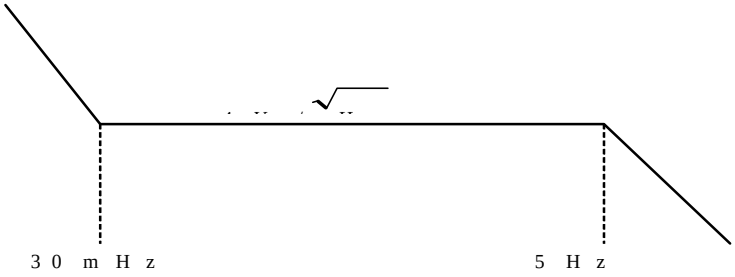


Noise Measurements was done at Fr = 200Hz and 240 Hz and with three different amplitudes of Bias for each frequency (max bias, max bias/2 and max bias/4)

5.1.2.2 Result

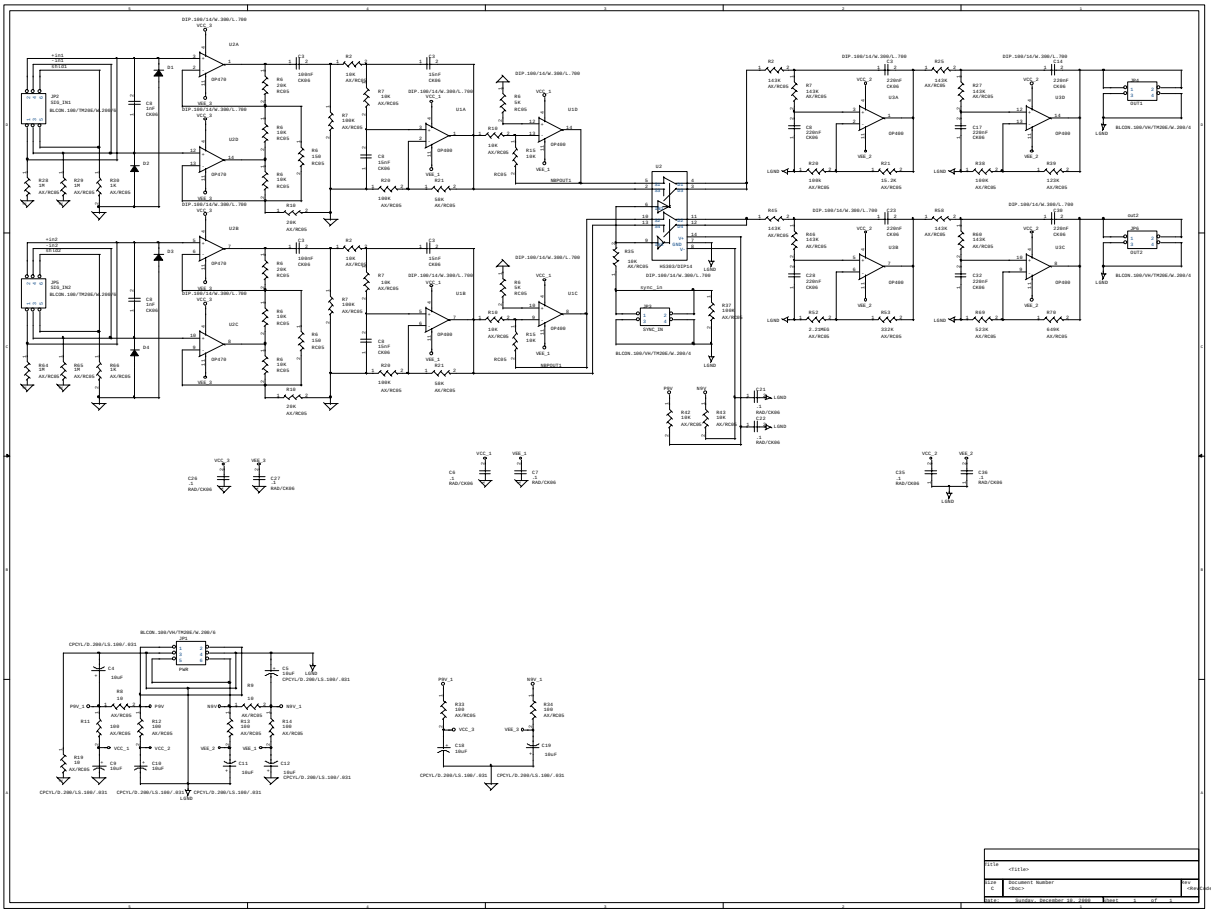
Aim was the BDA-DRCU-01 requirement: The input noise shall have less than $7nV/\sqrt{Hz}$.

We observed in each case a white noise between 30mHz and 5Hz under $4nV/\sqrt{Hz}$ as shown on the following drawing:



5.2 LIA schematic 2

Scheme with OP470

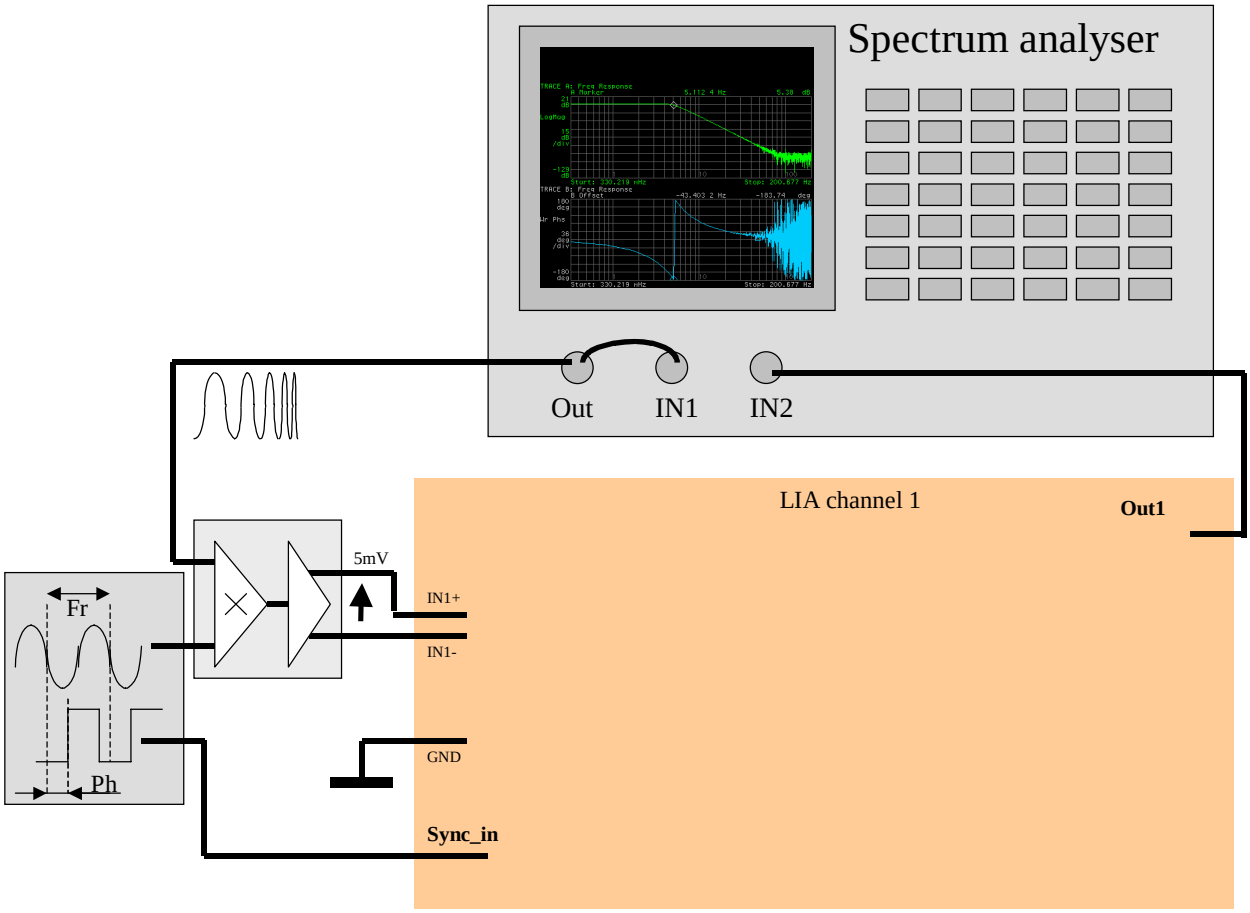


we put same values than in the first drawing for :

- R20 and R52 = 65kΩ
- R21 and R53 = 10kΩ
- R38 and R69 = 8kΩ
- R39 and R70 = 10kΩ

5.2.1 Transfer function

5.2.1.1 Measurement configuration



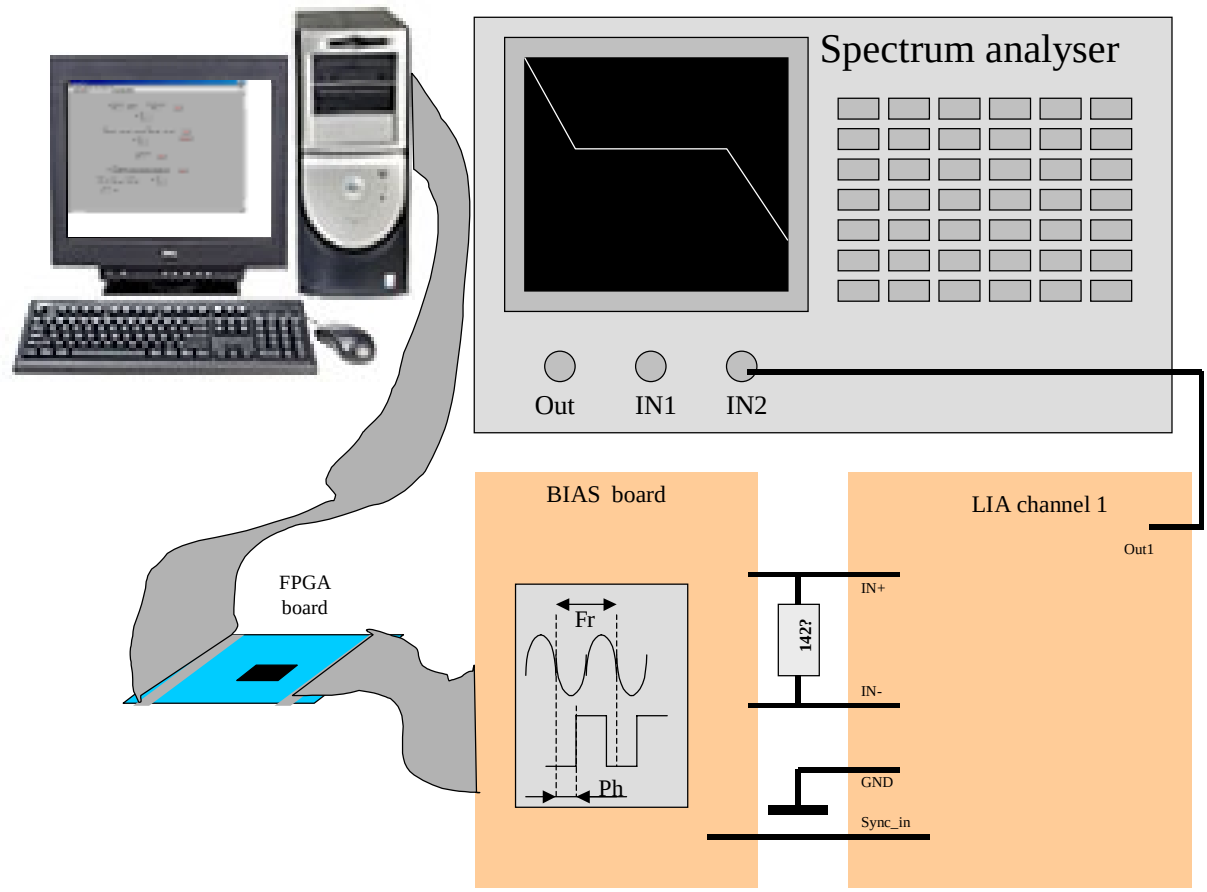
5.2.1.2 Result

Aim was the BDA-DRCU-13 requirement: The signal bandwidth of photometer channels shall be 0.03 to 5Hz.

We have measured a gain of 500 and a –3dB cut off at 5Hz with –80dB slope.

5.2.2 Input noise

5.2.2.1 Measurement configuration

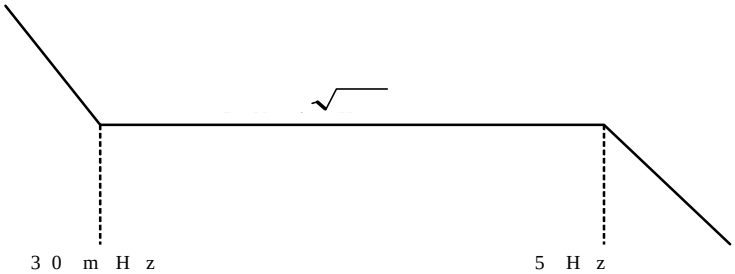


Noise Measurements was done at Fr = 200Hz and 240 Hz and with three different amplitudes of Bias for each frequency (max bias, max bias/2 and max bias/4)

5.2.2.2 Result

Aim was the BDA-DRCU-01 requirement: The input noise shall have less than $7nV/\sqrt{Hz}$.

We observed in each case a flat noise between 30mhz and 5Hz under $7nV/\sqrt{Hz}$ like show on the following drawing:



5.3 Choice between the two solutions

Solution 2 will be less complicated to implement than the first one but .
- It requires twice the solution 1 power and its noise performance is just on the requirement limit.

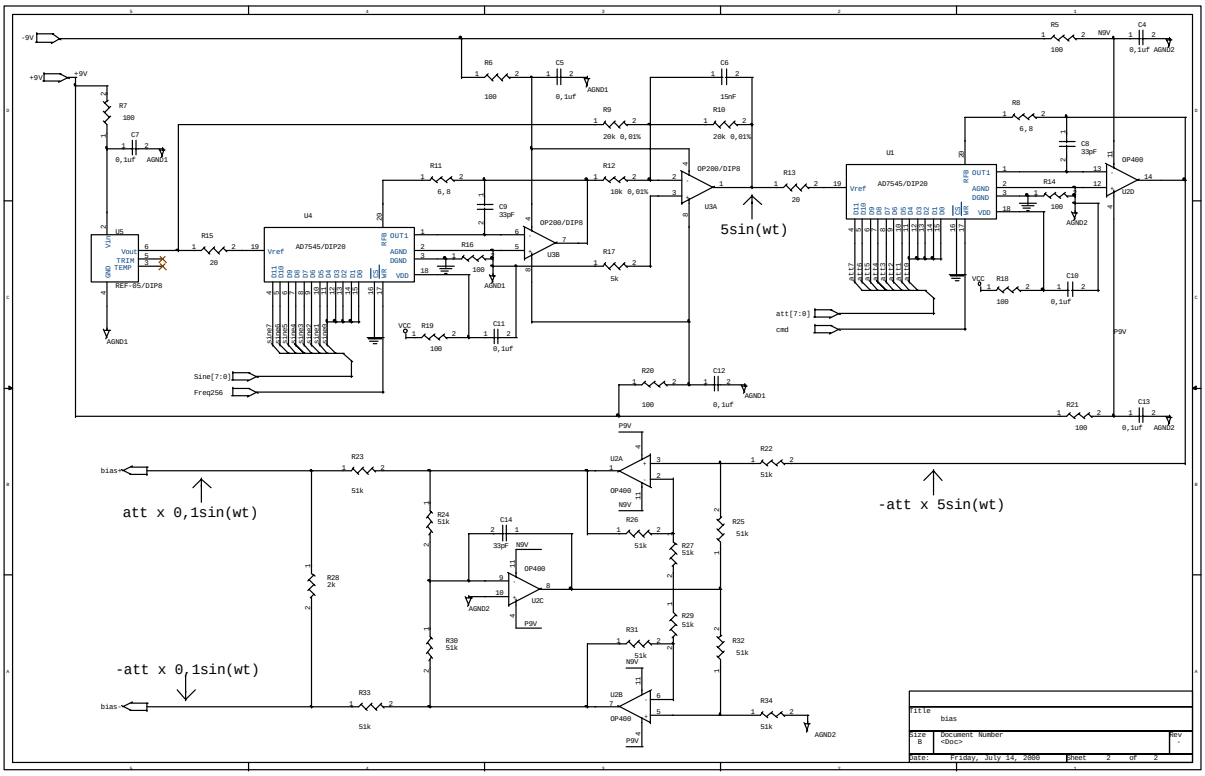
The first solution has been preferred for EM, QM and FM.

5.4 Conclusion

The chosen solution answers to the photometer noise and bandwidth requirements. For the spectrometer, the Low Pass Filter will have to be adjusted.

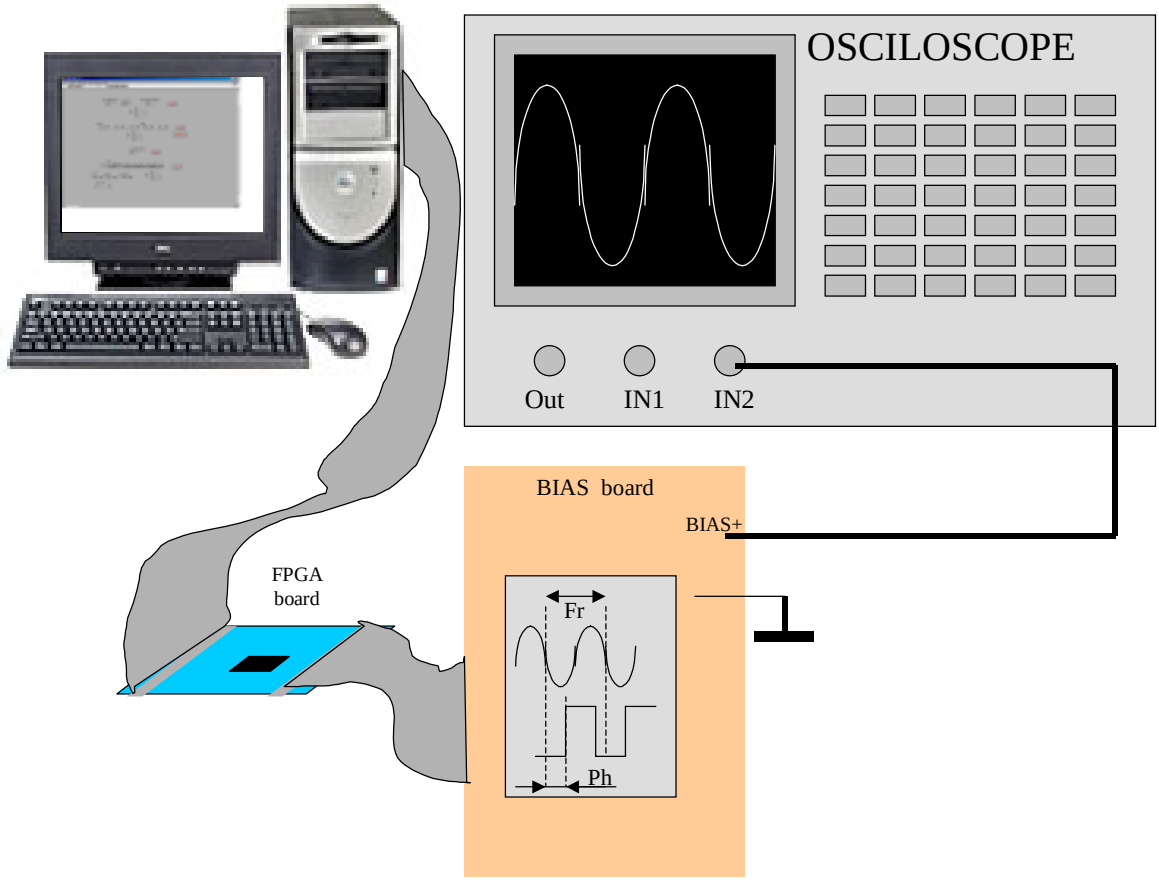
6 BIAS board functional test

6.1 BIAS schematic



6.2 Frequency and Amplitude range test

6.2.1.1 Measurement configuration



Aim was the BDA-DRCU-05 requirements:

- Bias shall be adjustable between 50 and 300Hz with a precision of 5Hz.
- Bias amplitude shall be adjustable with 8bits precision.

We tested that we can change the bias frequency and that we have a sine wave form.

We have checked that we had on the oscilloscope a sine signal with the same frequency and amplitude we had sent through the command VI.

We can choose a frequency in the following list by the appropriate code.

code	frequency	code	frequency	code	frequen
64	300	100	192	39	123
65	295	101	190	40	120
66	291	102	188	41	117
67	287	103	186	42	114
68	282	104	185	43	112
69	278	105	183	44	109
70	274	106	181	45	107
71	270	107	179	46	104
72	267	108	178	47	102
73	263	109	176	48	100
74	259	110	175	49	98
75	256	111	173	50	96
76	253	112	171	51	94
77	249	113	170	52	92
78	246	114	168	53	91
79	243	115	167	54	89
80	240	116	166	55	87
81	237	117	164	56	86
82	234	118	163	57	84
83	231	119	161	58	83
84	229	120	160	59	81
85	226	121	159	60	80
86	223	122	157	61	79
87	221	123	156	62	77
88	218	124	155	63	76
89	216	125	154	16	75
90	213	126	152	17	71
91	211	127	151	18	67
92	209	32	150	19	63
93	206	33	145	20	60
94	204	34	141	21	57
95	202	35	137	22	55
96	200	36	133	23	52
97	198	37	130	24	50
98	196	38	126		
99	194				

The test was done for frequency of 50Hz, 200Hz, 240hz and 300Hz

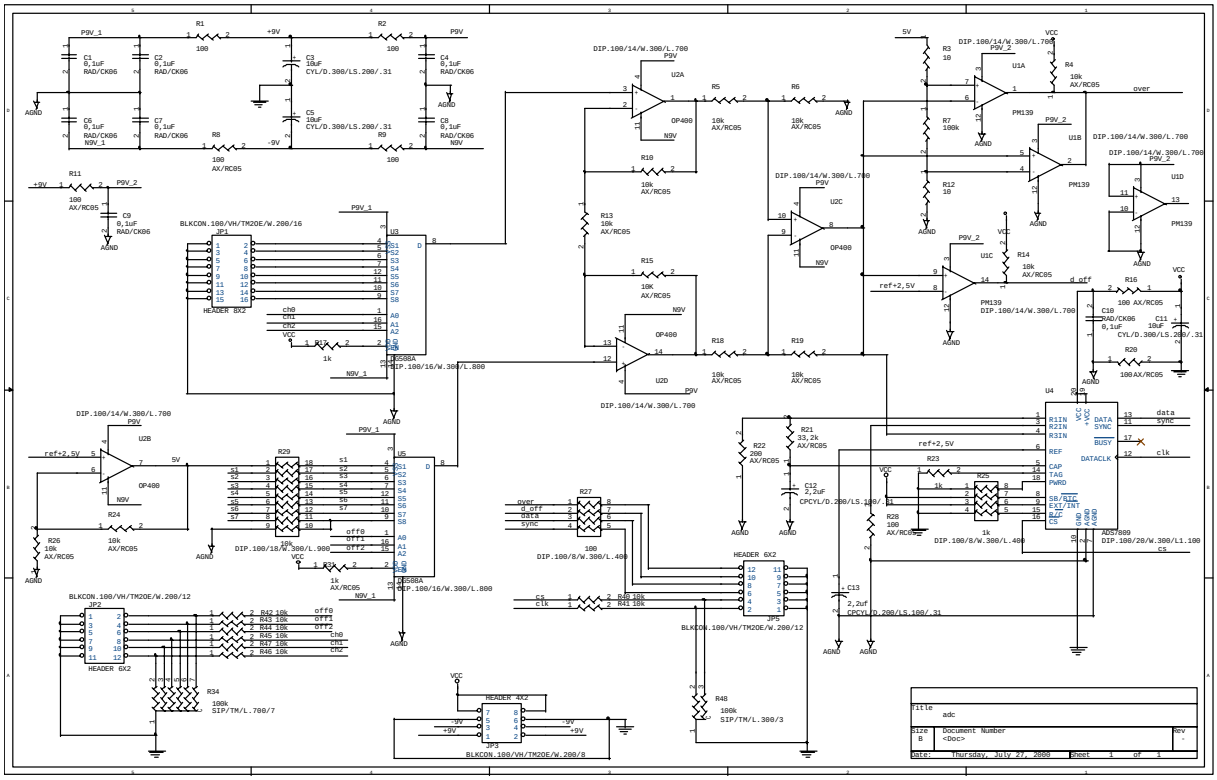
We can choose the bias Amplitude between $Vbias_{max}$ and 0. Vbias= $n.Vbias_{max}/255$ with $255 \geq n \geq 0$
The amplitude test was done for n equal 255, 100 and 40.

6.3 Conclusion

This design is compliant with the bias requirements on the frequency and amplitude range and precision.

7 ADC board test

7.1 ADC schematic



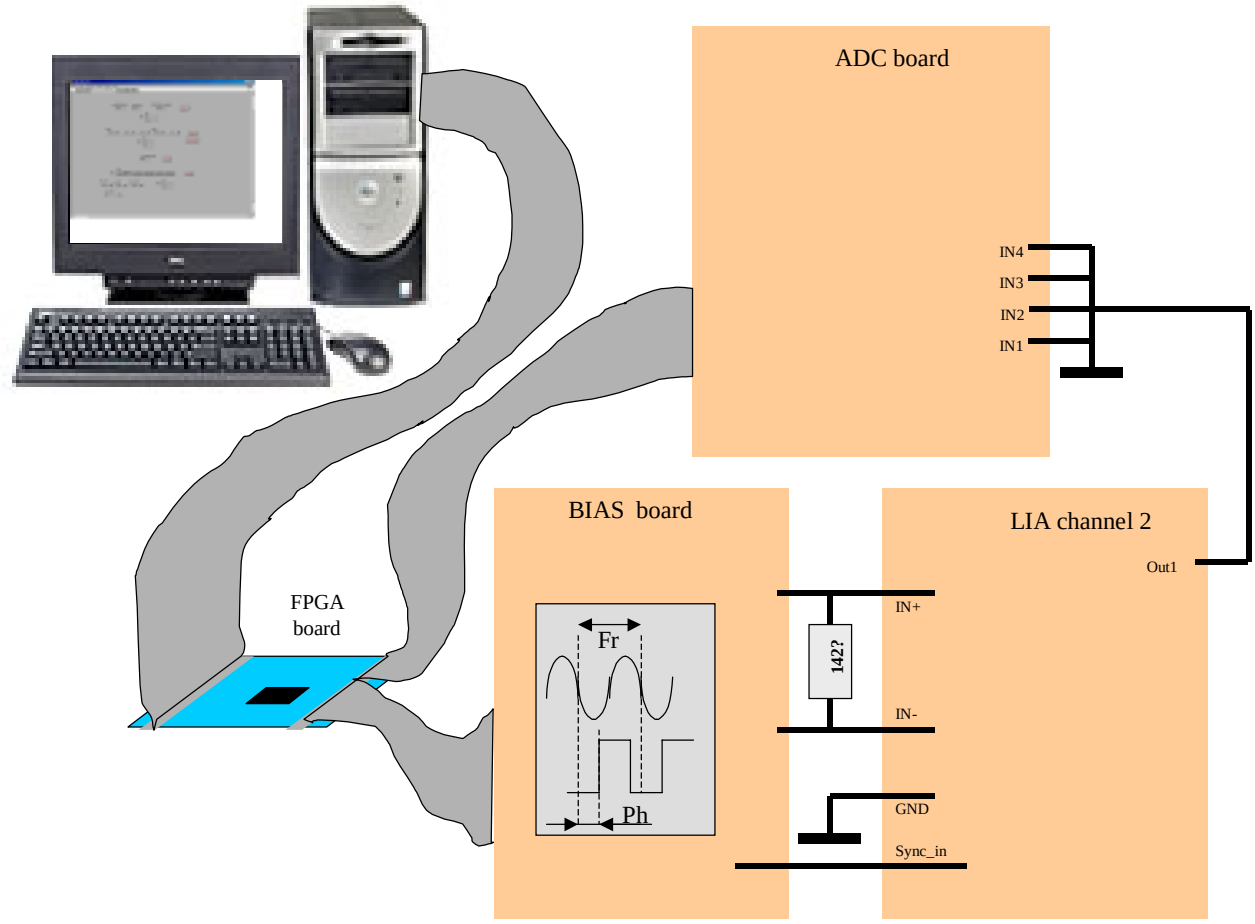
Schematic problems

The power supply of the U3 and U5 are inverted

On R29 we had to bypass the resistor between pin 1 and 18 and the resistor between pin 9 and 10

We had to replace the “sync” signal by the “RC” signal on the ADC signals connector.

7.1.1.1 Measurement configuration



7.2 Offset control

The offset control is done by the FPGA. It choose the offset value that set the signal nearest to the ADC middle scale.

How it works:

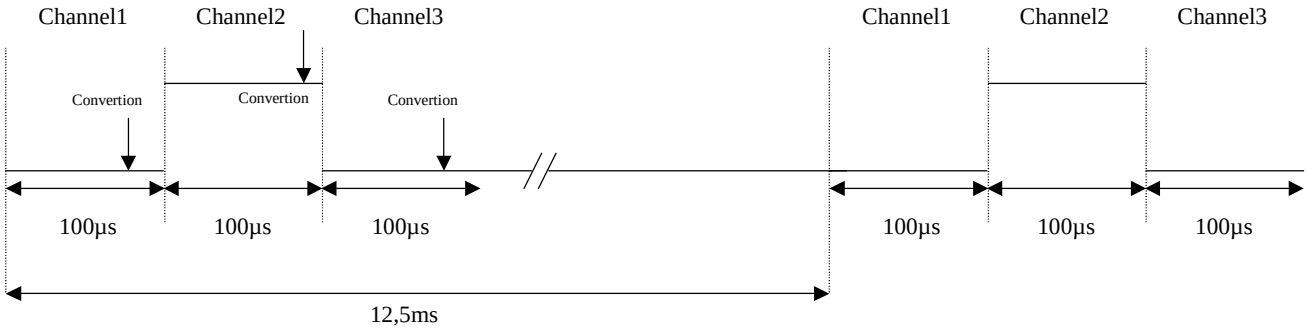
- A bias level is applied on the LIA input
- The offset set up is stared with the command VI
- The FPGA go through an algorithm to find the best value for the offset and it stores this value
- The offset will stay the same as long as a new set up is started.

We have checked that the FPGA has always chosen the right offset value for different bias amplitudes.
And everything was OK

7.3 Channel switching test

Channel 1 was connected to gnd
Channel 2 received the signal from the LIA
Channel 3 was connected to gnd

Measurement Timing :



We found the same results with and without channel commutation.
So everything is OK

Input :

Bias Amplitude = BIASmax
Bias frequency = 240Hz

Number of Measurements = 1000

Average Value =38461 Lsb ; Value max – Value min =30 Lsb

7.4 ADC Noise

When we have checked the noise at the input of the ADC with the spectrum analyzer, we have found LIA input equivalent white noise between 30mHz and 5Hz under $4nV/\sqrt{Hz}$.

But we haven't managed to find the equivalent noise on the data taken by the ADC.
This extra noise can come from different point:

- the OP400 isn't enough strong to drive correctly the ADC input
- We have some coupling between the numeric bias signals and the input of the ADC.
- And maybe we had a problem with the ADC power supply because we had a 100Ω between the 5V(VCC) and the power pin of the ADC.

All these points will be checked on the EM.

7.5 Conclusion

This design must be improved to solve the ADC noise problem.

Requirement ID	Description	Test result	Comment
BDA-DRCU-01	The DRCU signal processing electronics shall have less than 7 nV/rtHz as seen post demodulation, after digitzation. Noise is referred to the input over the frequency range 0.05 to 25 Hz. This performance must be accomplished with a bias input signal to the DRCU of 10 mVrms AC, 5 mV DC, 1 V DC common-mode offset, with an input load of 7 kOhms.	4nV/rtHz as seen post demodulation, before digitization tested and validate on the breadboard	
BDA-DRCU-03	Input capacitance to be less than 100 pF, measured from the DRCU DxMA connector pins without the harness.	OK	
BDA-DRCU-04	Input impedance to be larger than 1 MΩ from 50 – 300 Hz.	OK	
BDA-DRCU-05	The DRCU is to provide 5 BDA bias signals, adjustable from 0 to 200 mV_{rms}, and 1 bias signal for temperature readout, adjustable from 0 to 500 mV_{rms}. The temperature readout biases are to be divided from a common oscillator. Each bias shall be adjustable with 8-bit precision. The frequency of each bias shall be adjustable between 50 and 300 Hz, with a precision of 5 Hz.	One bias tested an validated on the breadboard	
BDA-DRCU-06	The DRCU will provide 15 commandable JFET source voltages with 256 levels. The range of Vss is from 0 V to –5 V.	will be tested with the EM	
BDA-DRCU-07	Vdd is to be adjustable from 1.5 to 4 V.	will be tested with the EM	
BDA-DRCU-08	Vdd and Vss lines individually must source 1 mA to 5 mA. Noise on Vss < 1 μV/√Hz, and noise on Vdd < 0.3 μV/√Hz within modulated band (50 – 300 Hz), measured at the DRCU DxMA connector.	will be tested with the EM	
BDA-DRCU-09	Each of the 15 Vdd and Vss supplies must be commandable ON/OFF for spectrometer and photometer independently, without overshoot. Each Vdd and Vss pair are turned on and off together.	will be tested with the EM	
BDA-DRCU-10	The DRCU will provide 2 double-wired JFET heater lines with adjustable amplitude and duration. The supplies must be able to provide 5 V and 25 mA (photometer), 3 V and 10 mA (spectrometer). Each heater line is commandable ON/OFF, with a minimum duration of 10 s.	will be tested with the EM	
BDA-DRCU-11	The common-mode rejection is –60 dB (50 – 300 Hz).	will be tested with the EM	
BDA-DRCU-12	The DRCU shall provide a dynamic range at the ADC sufficient to maintain the noise performance of the detectors under maximal signal conditions. This is estimated to be 16 ADC telemetry bits (TBC).	tested and valid on the breadboard	

BDA-DRCU-13	The signal bandwidth of the photometer channels shall be 0.03 Hz to 5 Hz. The 5 Hz cutoff should have a precision of 1 %.	tested and valided on the breadboard	
BDA-DRCU-14	The signal bandwidth of the spectrometer channels shall be 0.03 Hz to 25 Hz. The 25 Hz cutoff should have a precision of 1 %.	will be tested with the EM	
BDA-DRCU-15	The sampling of the photometer channels shall be synchronised with the bias, at a rate selectable between $\nu_{bias}/2$ to $\nu_{bias}/256$.	will be tested with the EM	New requirement
BDA-DRCU-16	The sampling of the spectrometer channels shall be synchronised with the bias, at a rate selectable between $\nu_{bias}/2$ to $\nu_{bias}/256$.	will be tested with the EM	New requirement
BDA-DRCU-17	THE DRCU SHALL PROVIDE 2 ADJUSTABLE POWER SUPPLIES FOR TEMPERATURE CONTROL USING A HEATER LOCATED AT THE 300 MK STAGE. THIS SUPPLY MUST PROVIDE AT LEAST 300 MV AND 50 UA.	will be tested with the EM	New requirement
BDA-DRCU-18	NOISE PERFORMANCE BDA-DRCU-01 SHALL BE MAINTAINED UNDER BIAS RANGE 50 – 300 HZ.	will be tested with the EM	New requirement
BDA-DRCU-19	DRCU noise performance (BDA-DRCU-01) to be maintained under a warm electronics thermal drift of 1 K / hour (TBC).	will be tested with the EM	New requirement
BDA-DRCU-20	Thermal requirements on bias stability are implicit in BDA-DRCU-01.	will be tested with the EM	New requirement
BDA-DRCU-21	Thermal requirement on JFET power is dV/V < 500 ppm / K for Vdd and Vss.	will be tested with the EM	New requirement
BDA-DRCU-22	The DRCU shall not saturate at an input voltage as large as 11 (TBC) mV_{rms} at input (photometer), 17 (TBC) mV_{rms} at input (spectrometer). DRCU channels shall remain functional if one input signal goes to Vbias.	will be tested with the EM	New requirement
BDA-DRCU-23	Specification on isolation of power supplies, ripple, noise, EMC TBD. Specifications to flow from keeping the electrical interference and dissipation at the bolometer below fundamental noise as in Table 3-3-3.	TBD	New requirement
BDA-DRCU-24	Bias, JFET power, and readout electronics for the spectrometer and photometer arrays are to run from separate dedicated power supplies, with independent, isolated grounds.	TBD	New requirement
BDA-DRCU-25	The electrical cross-talk between channels in the DRCU shall be less than 0.05 % (TBC). The electrical cross-talk shall be verified by varying the input signal on one channel and measuring the response in other channels. The input signal level to each channel must be representative.	will be tested with the EM	New requirement
BDA-DRCU-26	Each signal input to the LIA module must be connected to ground by a diode. This provides both protection and allows the JFETs to turn on without the JFET heater.	OK	New requirement