SUBJECT: SPIRE JFET Enclosure
Thermal Design Trade-Off

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CHANGE RECORD

ISSUE	DATE	SECTION	CHANGE
D1	26-Sept-01	-	New Document
I1	05-Nov-01	All	Updated cases. Add additional strap cases.

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1. SCOPE

This document describes a study of potential improvements to the JFET enclosure thermal design, given various harness routing options, enclosure mount designs and thermal straps.

2. APPLICABLE DOCUMENTS

ID	TITLE	NUMBER
AD2.1.1	SPIRE Thermal Configuration Control Document	SPIRE-RAL-PRJ-000560 D8 18-04-01 S.Heys
AD 2.1.2	FIRST Simplified Optical Bench Thermal Model	Fax Ref: SCI-PT/FIN-08132 24-08-00
AD2.1.3	SPIRE Harness Definition Document	Issue 0.5 22-8-01
AD2.1.4	Herschel/Planck IID-A	SCI-PT-IIDA-04624 2/0 31-07-01
AD2.1.5	EM Membrane Thermal.xls	22-09-01 T.Cafferty

Table 2.1: Applicable Documents

3. INTRODUCTION

The SPIRE JFET enclosures are mounted adjacent to the FPU on the Level 2 (~10K) HOB. The individual JFET chips require heating to 110K (TBC) during operation of their respective detector. In some cases all chips relating to the mode of operation (photometer or spectrometer) require heating simultaneously. In other cases only a proportion of the chips will be heated. This heating is achieved by mounting sets of 24 pairs of JFETs together on low conductance, silicon nitride membranes. The JFETs then self-heat to a temperature dependant upon the input power, the base temperature of the membrane support and the location of the JFET on the membrane.

Membrane modules are stacked within aluminium enclosures, one housing the 3-off spectrometer membranes, and a second the 12-off photometer membranes. In the baseline enclosure design the enclosures are hard mounted to the HOB, and therefore follow the Level 2 temperature closely. The harnesses from the DCU are sunk to the Herschel Shield 1 at approximately 35K, and to the HOB, prior to connection to the JFET enclosures. The harnesses from the JFET enclosures to the FPU are not sunk to the HOB, however a minimum thermal path of 100mm is specified for this harness, to reduce heat leaks to the Level 1 FPU.

In Photometer Mode the power required to heat the JFET chips to an acceptable operating temperature is high compared to the Herschel Cryostat Level 2 budget. The actual power will depend upon a system performance analysis, relating JFET temperature to science performance. However, in the absence of this analysis it is necessary to investigate options for reducing the SPIRE Level 2 loads. Various methods are under investigation to reduce this power, including:

1) Thermal isolation of the JFET enclosures from the HOB using low conductance stand-offs, thus allowing the enclosure temperature to increase (due to dissipated power) and hence reducing the input power required to achieve operating temperature.
2) Route DCU-JFET harness such that it passes directly from the Herschel Shield 1 to the JFET enclosures, rather then being sunk to the HOB. In this way, whilst the total cryostat level 2 loads remains effectively unchanged, the enclosures receive some heating effect due to conduction down the harness.
3) Incorporate a thermal strap between Shield 1 and the JFET enclosures, in order to heat the enclosures due to conduction down the straps.

Several issues are raised by the above design options. In particular, by running the enclosures warm, the loads on the FPU due to the harness from the JFET enclosures will increase. Therefore it is likely that the JFET-FPU

harness will require heat sinking to the HOB. Other issues relate to harness lengths, which have an impact on the analysis results and are not defined in all cases. There is also concern about stray light from components within the cryostat Level 2 enclosure running at temperature significantly above the specified 10-15K stage temperature.
The heating effect of routing the harness from the shield direct to the JFETs will be significantly less for the spectrometer enclosure than the photometer, due to the smaller harness for this enclosure. However, the power dissipation within the spectrometer enclosure is low compared to the Level 2 budget, therefore a reduction in dissipated power is not necessary in spectrometer mode.

4. ANALYSIS

4.1. Thermal Mathematical Model

The SPIRE ESATAN DTMM 'SPIRE15.d' has been used for this analysis. This model is as that defined in AD1, with some modifications to Herschel boundary conditions, material properties functions and power dissipations. Updates to the harness have been made according to AD2.1.3 and AD2.1.4.

4.2. Herschel Interface Temperatures

The Herschel boundary temperatures are calculated for each case using the Herschel cryostat ITMM defined in AD2.1.2.
The heat loads on Level 2 due to the DCU-HOB harness are believed to be included in the Herschel ITMM. However, the actual contribution this harness makes on the total load is not explicitly defined. Therefore, in order to allow a fair trade-off between a DCU-JFET harness sunk to the HOB and one routed direct to the JFETs, it is necessary to include this load independently into the model, and accept that it is therefore accounted for twice. The result is that the absolute temperature and heat load predictions are higher than anticipated, but can be used to assess of the relative impact of design changes.
The Herschel Shield 1 temperature is held at 38K in all cases. The impact of any proposed design changes on this shield temperature will require investigation by the Herschel Cryostat team.

4.3. Analysis Cases

Table 4.3.1 describes the various analysis cases examined. Case 1 is the current baseline design. The effect of isolating the JFET enclosures on low conductance stand-offs of CFRP and Vespel SP1 is shown in Cases 2a and 2b respectively (4-off washers 20mm OD, 5mm ID, 15mm high). Case 2c uses Vespel stand-offs, with the JFET-FPU harness sunk to the HOB in order to minimise the heat load to Level 1. In this case the harness is assumed to be sunk at its mid-point.
Cases 3 examines the effects of routing the DCU-JFET harness direct from the Herschel Shield 1 to the JFETs without stand-offs.
Case 4a examines the effect of both isolating the enclosure on stand-offs and routing the harness direct from Shield 1. Case 4b examines sensitivity to the length of this harness. In Case 4c the JFET power is reduced by 4%, to reflect the reduced power required to heat the JFETs to their operating temperature from a warmer base temperature. The 4% reduction is estimated from AD2.1.5 as the power reduction for a base temperature increase from 14K to 24K, given an original power of 49.5mW.
Case 5b is as Case 4a, but with the inclusion of a strap from the Photometer JFET enclosure to the Herschel Shield 1. The strap conductance is sized to give a maximum increase in enclosure temperature without exceeding the 50mW Level 2 cryostat budget. Case 5c is as 5b, except that Shield 1 temperature is increased from 38K to 48K to check sensitivity to an increase in this boundary temperature. Finally in Case 5d the JFET power is reduced by 8% due to the increase in enclosure temperature from 14K to 28.5K.

Case No.	JFET Power (mW)	JFET Enclosure Mounting	DCU-JFET Harness route/length	JFET-FPU Harness route/length
1	49.5	Hard Mounted to HOB	Sunk to HOB 300mm	Direct 100mm
2a	49.5	Isolated CFRP stand-offs	Sunk to HOB 300mm	Direct 100mm
2b	49.5	Isolated SP1 stand-offs	Sunk to HOB 300mm	Direct 100mm
2c	49.5	Isolated SP1 stand-offs	Sunk to HOB 300mm	Sunk to HOB 50mm + 50mm
3	49.5	Hard Mounted to HOB	Direct from Shield 1 300mm	Direct 100mm
4a	49.5	Isolated SP1 stand-offs	Direct from Shield 1 300mm	Sunk to HOB 50mm + 50mm
4b	49.5	Isolated SP1 stand-offs	Direct from Shield 1 500mm	Sunk to HOB 50mm + 50mm
4c	47.2	Isolated SP1 stand-offs	Direct from Shield 1 300mm	Sunk to HOB 50mm + 50mm
5b	49.5	Isolated SP1 stand-offs Brass Strap Phot JFET to Shield 1 12.5mm*2mm/300mm	Direct from Shield 1 300mm	Sunk to HOB 50mm + 50mm
5c	49.5	Isolated SP1 stand-offs Brass Strap Phot JFET to Shield 12.5mm*2mm/300mm	Direct from Shield 1 300mm Shield T increased from 38K to 48K	Sunk to HOB 50mm + 50mm
5d	45.5	Isolated SP1 stand-offs Brass Strap Phot JFET to Shield 1 12.5mm*2mm/300mm	Direct from Shield 1 300mm	Sunk to HOB 50mm + 50mm

Table 4.3.1: Analysis Cases

5. RESULTS

Table 5.1 shows an overview of the results obtained by analysis of the various design cases. Further details of heat load breakdowns are provided in Appendix A.

Case	Temperature (K)								Heat Load			
	HOB L2	Herschel L1	Herschel L0	JFET Phot	JFET Spec	FPU L1	FPU L0	FPU Det	L2	L1	L0	Cooler
									(mW)	(mW)	(mW)	(microW)
1	13.938	5.377	1.7	14.441	13.927	6.5759	2.15922	0.3365	39.9	21.13	7.421	33.4
2a	13.882	5.441	1.7	16.549	13.819	6.6744	2.1785	0.3377	38.63	22.24	7.675	34.1
2b	13.681	5.692	1.7	22.761	13.429	7.052	2.25365	0.3423	32.32	26.53	8.69	37
2c	13.836	5.51	1.7	22.043	13.836	6.779	2.19888	0.3389	37.16	23.395	7.948	34.9
3	13.925	5.376	1.7	14.542	13.945	6.576	2.15955	0.337	39.73	21.16	7.425	33.4
4a	13.591	5.413	1.7	23.745	14.328	6.664	2.18156	0.338	34.79	22.57	7.693	34.1
4b	13.307	5.303	1.7	23.074	13.771	6.531	2.16193	0.3367	32.1	21.64	7.406	33.3
4c	13.449	5.357	1.7	23.399	14.197	6.597	2.17166	0.3372	33.31	22.11	7.548	33.7
5b	15.161	6.051	1.7	28.52	15.81	7.419	2.299	0.3453	50.28	28.116	9.463	39.3
5c	16.722	6.723	1.7	33.04	17.34	8.335	2.456	0.3563	67	35.304	11.931	46.9
5d	15.015	5.989	1.7	28.01	15.67	7.347	2.2877	0.3446	48.43	27.571	9.284	38.8

NOTE: This analysis calculates the heat load on Level 2 due to the DCU-JFET harnesses. The resulting loads are included in the Herschel ITMM calculation of boundary temperatures at Level 0,1 and 2. However, the ITMM already includes this load and it is therefore accounted for twice. This is unavoidable, since a load breakdown is not provided within the ITMM. The result is that the temperatures and loads shown in this document are above those achieved in reality and should be used only as a guide to the relative merits of each design option.

Table 5.1: Summary of Results

6. DISCUSSION

The aim of this analysis was to investigate options available for reducing SPIRE heat loads to the Herschel Level 2 cryostat stage. By increasing the JFET enclosure temperature, it is possible to reduce the internal power dissipation required to achieve the JFET chip operating temperature. A number of options have been investigated as follows:

a) Incorporating isolating stand-offs between the JFET enclosures and the HOB,
b) Routing the DCU-JFET harness direct from the Herschel Shield 1 to the JFET enclosures,
c) Incorporating a thermal strap from the Photometer JFET Enclosure to the Herschel Shield 1,
d) Combinations of the above.

The main conclusions of the analysis are as follows:

1) Case 2a shows that CRP or GRP stand-offs alone have little impact on JFET enclosure temp. Case 2b shows that Vespel SP1 stand-offs could have significant impact on enclosure temperature, for example a 8.4K temperature rise compared to the baseline design, using 4-off stand-offs OD20mm, ID5mm, length 15mm.
2) Comparison of Cases 2b and 2c demonstrates the advantages of sinking the FPU-JFET harness to the HOB at its mid-point, to prevent increases in L1 harness loads caused by high JFET enclosure temperatures.
3) Case 3 shows that routing the DCU-JFET harness direct from Shield 1 with a hard mounted JFET enclosure causes no significant increase in bulk enclosure temperature, due to the good conductance across the bolted interface.
4) Comparison of cases 2c and 4a shows an additional 1.7K increase in enclosure temperature results from routing the DCU-JFET harness direct from Shield 1, in addition to Vespel standoffs. However, harness loads to L2 are significantly less in Case 4a, since the temperature difference from Shield 1 to the Photometer Enclosure is significantly less than that from Shield 1 to the HOB. This reduction in Level 2 loads results in a lower HOB temperature and correspondingly lower L1 and L0 loads and temperatures.
5) Comparison of cases 4a and 4b show that a 500mm Shield 1-JFET harness length, rather than the 300mm assumed, would reduce the enclosure temperature by 0.7K, together with a small reduction in loads at all stages.
6) The increase in enclosure temperature from 14K to 24K (Case 1 to Case 4a) is predicted (AD2.1.5) to reduce the input power to the JFETs by approximately 4%. Case 4c shows that the net effect of Vespel stand-offs, rerouting the DCU-JFET harness and reducing the JFET dissipation is a 6.6mW (17%) reduction in Level 2 cryostat load and a small increase in Level 1 and Level 0 SPIRE loads (due to higher harness loads caused by a halving of the harness thermal length between Level 2 and Level 1).
7) Case 5b shows the impact of including a thermal strap between the Photometer JFET enclosure and Shield 1. Unlike the DCU-JFET harness re-routing, inclusion of such straps results in a net increase in Level 2 cryostat load. Since no increase in spectrometer enclosure temperature is necessary, the spectrometer enclosure is not strapped to the Shield. The photometer strap is sized to give the maximum enclosure temperature, whilst preventing Level 2 net loads exceeding the 50mW cryostat budget.
8) Case 5c shows that with a strap from Shield 1, the Shield temperature has a significant impact on JFET temperature (and L2 load). Therefore the strap conductance would have to be defined with good knowledge of Shield temperatures. This issue would require assessment by the Cryostat design team.
9) A comparison of Cases 4c and 5d shows that the reduction in JFET dissipated power, made possible by the increase in enclosure temperature due to the strap, is insufficient to compensate for the extra strap heat load at Level 2. A strap load of 26mW causes an increase in JFET enclosure temperature of 4.6K, allowing a further reduction in JFET dissipation of 1.7mW (4%). However the net cryostat Level 2 load increases by 15.1mW (45%). In addition this higher Level 2 load results in a HOB temperature rise of 1.6K, causing an increase in SPIRE Level 1 and Level 0 loads of 5.5mW (25%) and 1.7mW (23%) respectively.

The analysis demonstrates that the optimum JFET enclosure thermal design for SPIRE includes the following features:

-Support of the JFET enclosures off the HOB on low conductance mounts, for example Vespel SP1 washers with a xsection/length ratio of approximately 0.02m.
-Routing of the DCU-JFET harness from Shield 1 direct to the JFET enclosures with an effective thermal length of between 300mm and 500mm.
-Sinking of the JFET-FPU harnesses to the HOB at their mid-points.
-No thermal straps incorporated from either enclosure to Shield 1, since this results in a significant increase in Level 2 loads.

7. SUMMARY

The analysis demonstrates that Level 2 Cryostat loads can be significantly reduced by the incorporation of isolating stand-offs between the enclosure and the HOB and routing the DCU-JFET harness direct from the Herschel Cryostat Shield 1 to the JFET enclosures. A temperature increase from 14.4K to 23.7K is predicted for a simple Vespel SP1 stand-off design and JFET harness routing direct from Shield 1 to JFET enclosures (harness length 300mm). This design results in a net reduction in Cryostat Level 2 loads of 6.6mW or 17%, due to the lower temperature difference from Shield 1 to JFET enclosure, compared to Shield 1 to HOB. Further increases in temperature and reduction in loads may be possible, given an improvement in the isolation of the supports.
The addition of a thermal strap from Shield 1 to the Photometer enclosure results in a net increase in Level 2 loads, which is not compensated for by the small reduction in JFET dissipated power made possible by the higher enclosure temperature. Therefore the inclusion of such a strap is not recommended.
The impact of changes in Herschel Shield1 temperature (due to changes in loads on the various cryostat stages) are not accounted for in this analysis, due to the lack of information on this parameter at the current time. However sensitivity analysis shows that increases in this temperature would have a significant effect on the JFET enclosure temperatures.
Other issues to be addressed prior to implementation of any design changes:

-SPIRE calibration test facility requirement for 38K (TBC) stage in order that JFET thermal behavior is realistically represented during testing.
-Structural implications and analysis of JFET enclosure stand-offs.
-Feasibility of routing the DCU-JFET harness from Shield 1 direct to the JFETs, with minimal thermal couplings to Level 2 shield or HOB. The harness will require isolating supports between the Herschel Shield and the JFETs, and an isolating feedthrough at the Level 2 shield.
-Implications of sinking the JFET-FPU harness to HOB at approximately its mid-point.
- Investigations are required into the acceptability (stray light/thermal) of housing an enclosure at up to 30K within the Herschel Level 2 enclosure.

APPENDIX A: Heat Flow Ladder Diagrams

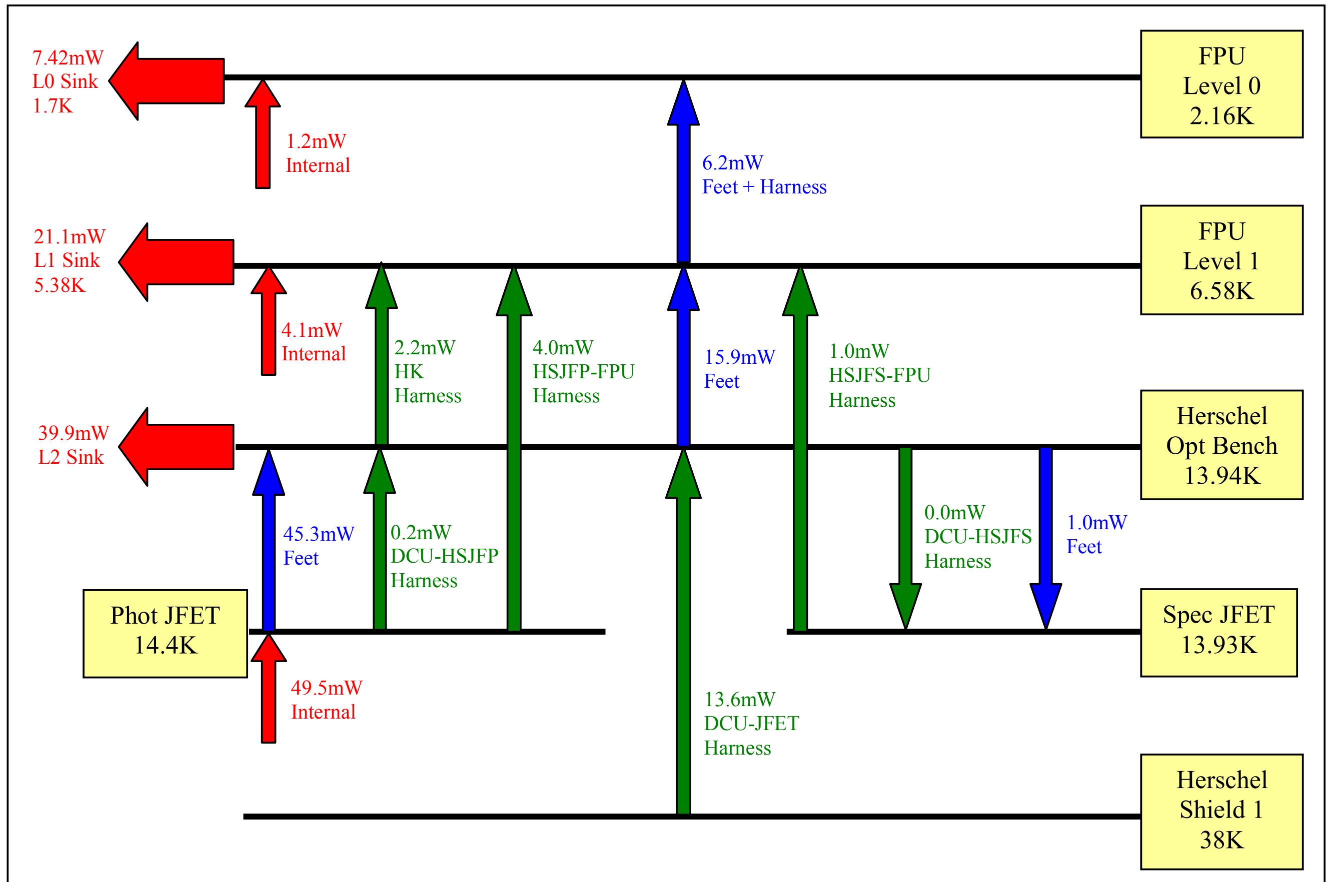

Figure 5.1: Case 1 Results

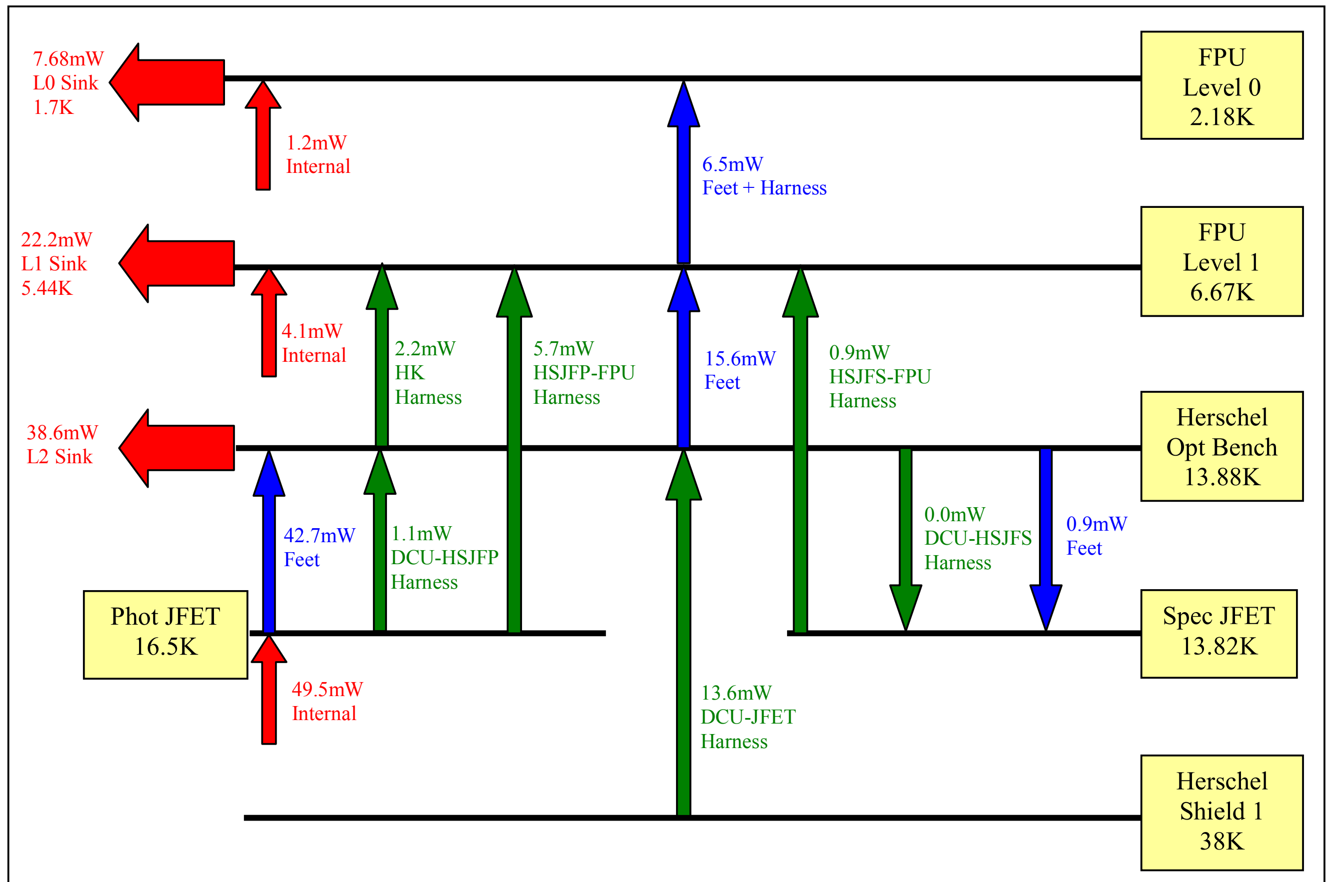

Figure 5.2: Case 2a Results

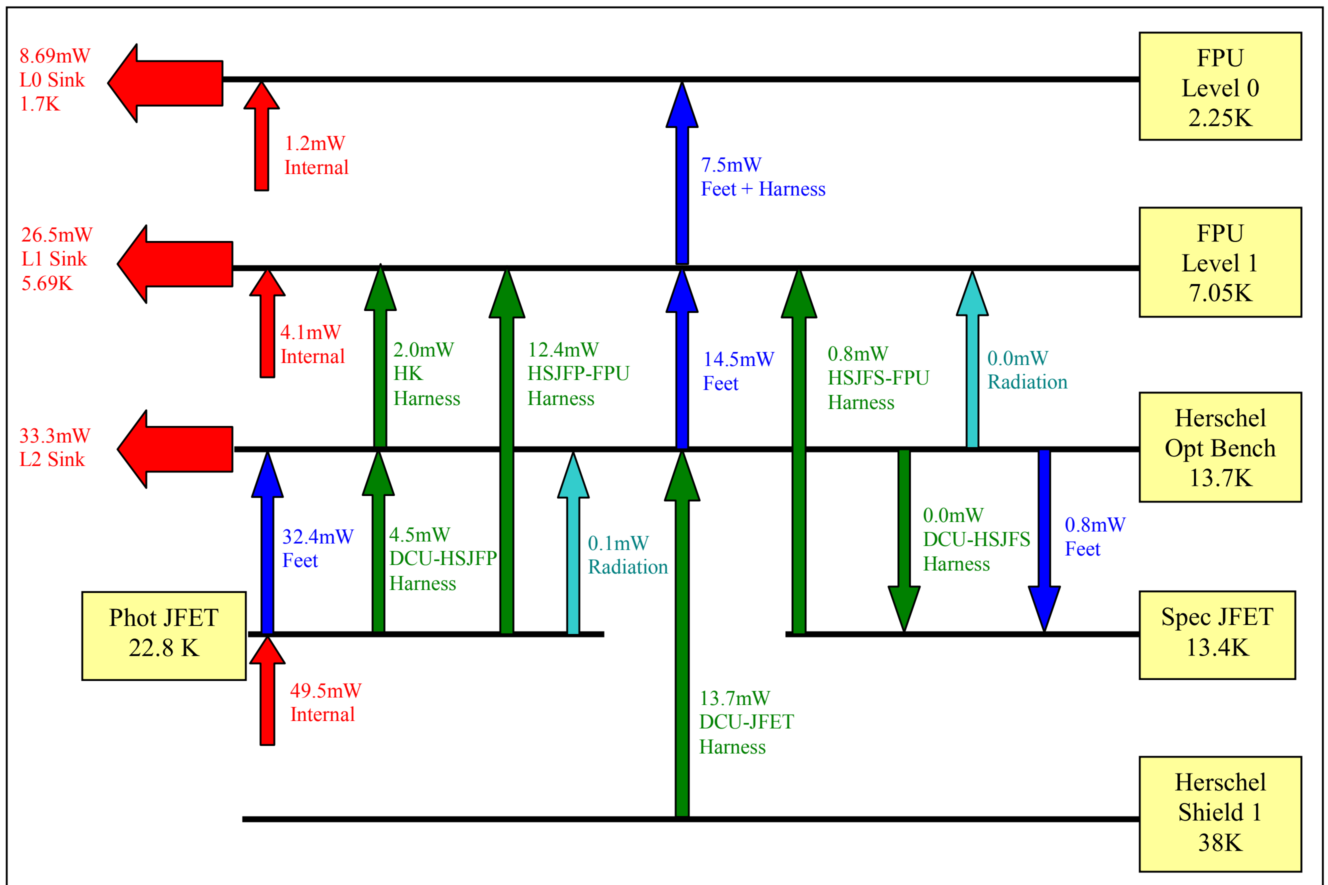

Figure 5.3: Case 2b Results

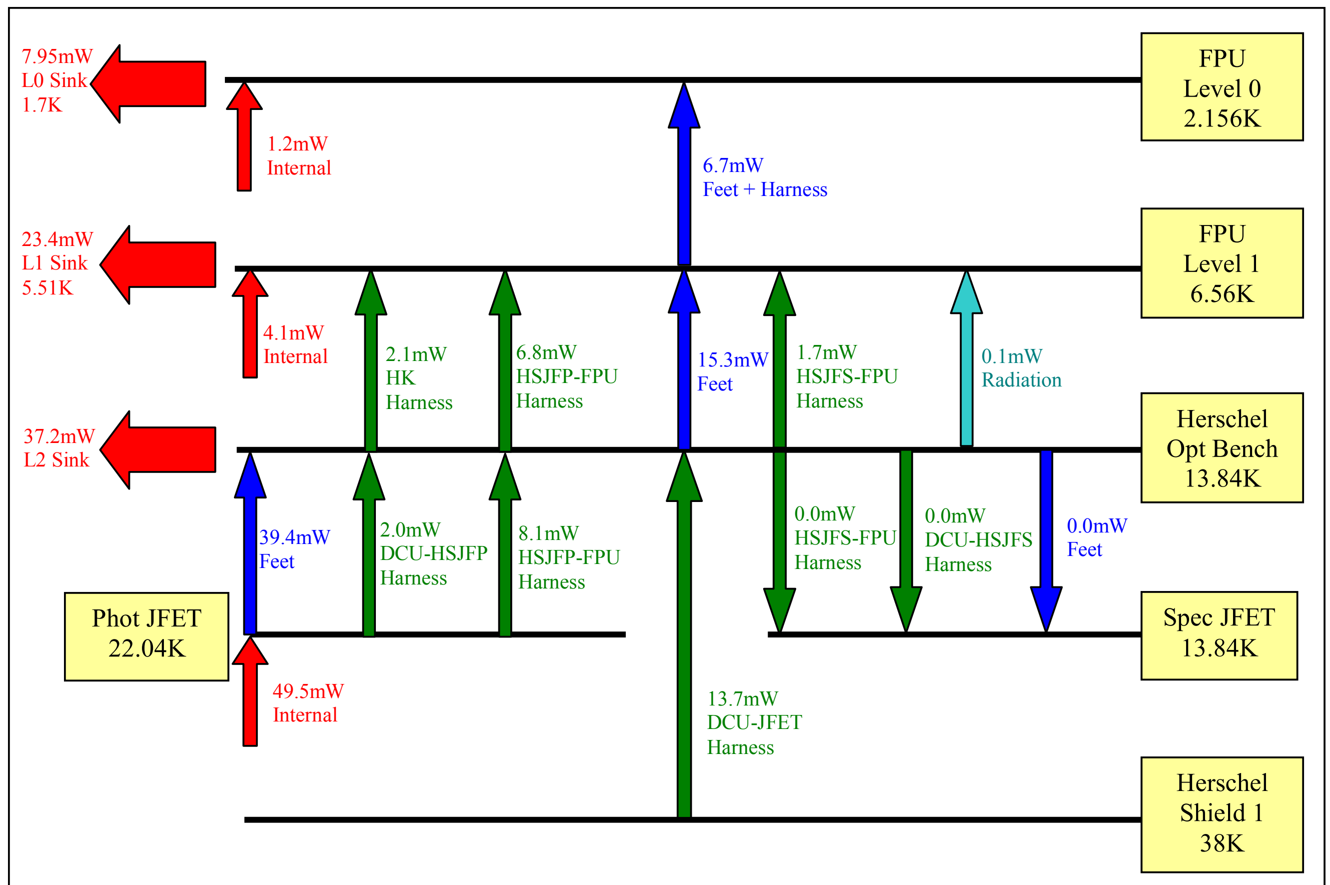

Figure 5.4: Case 2c Results

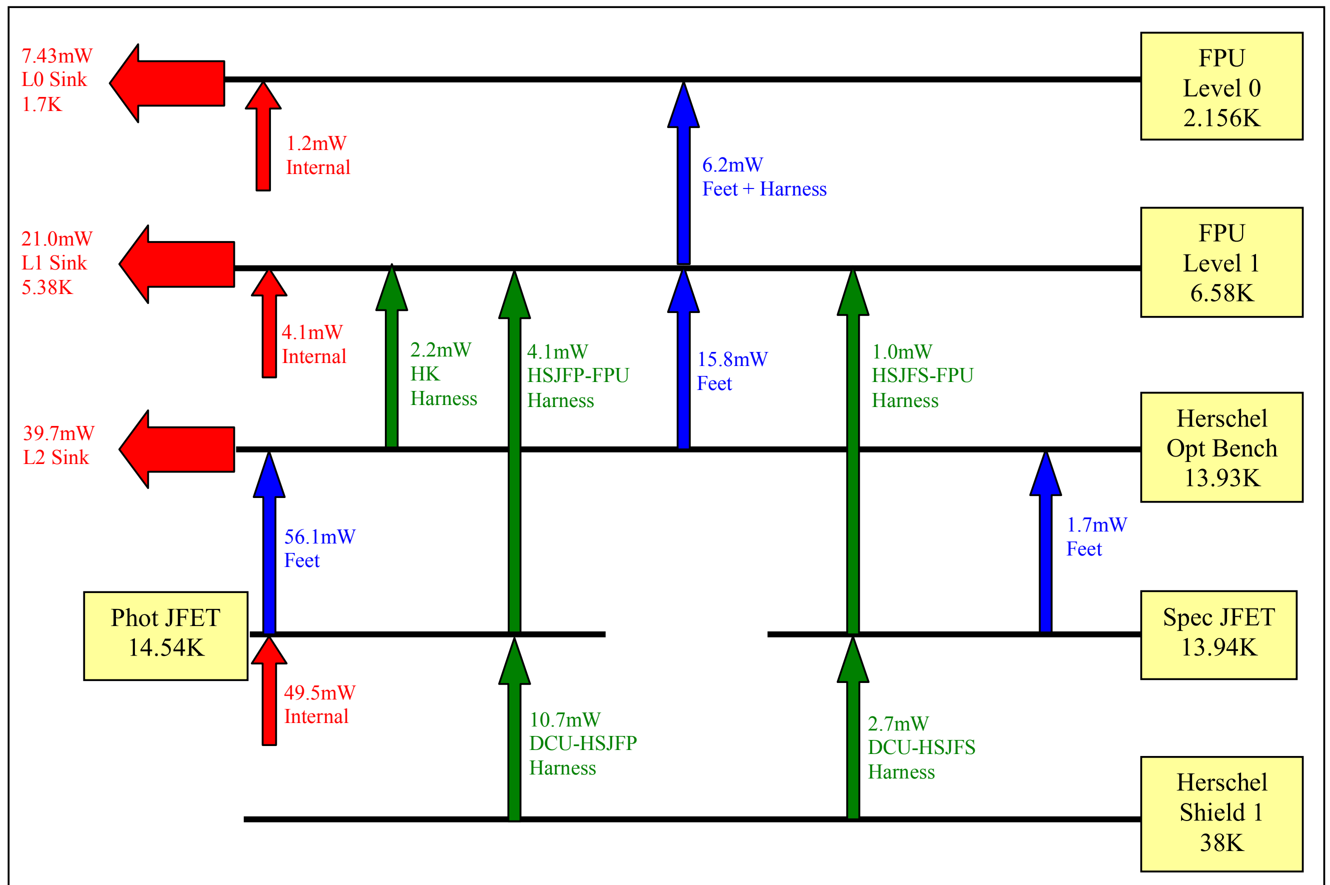

Figure 5.5: Case 3 Results

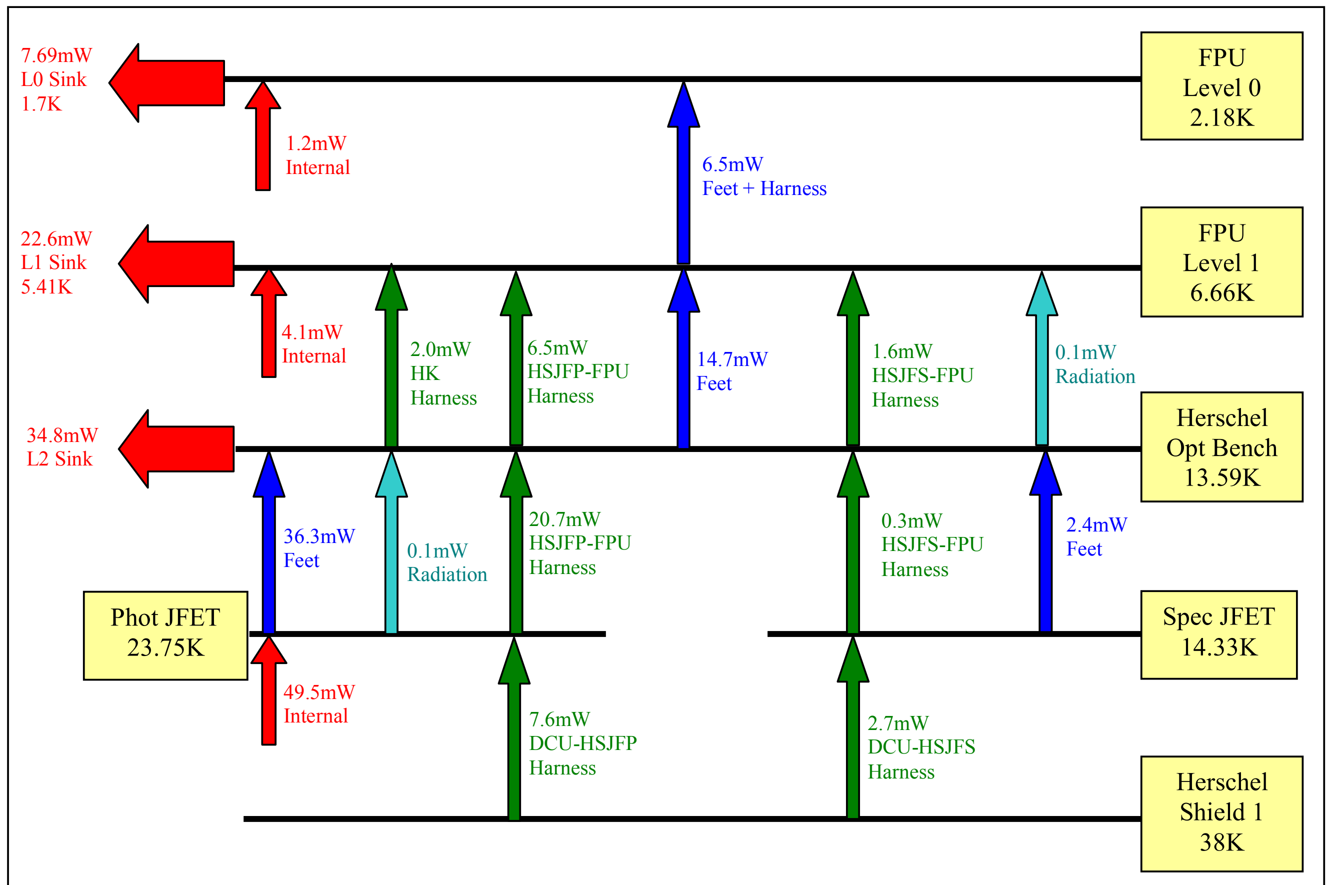

Figure 5.6: Case 4a Results

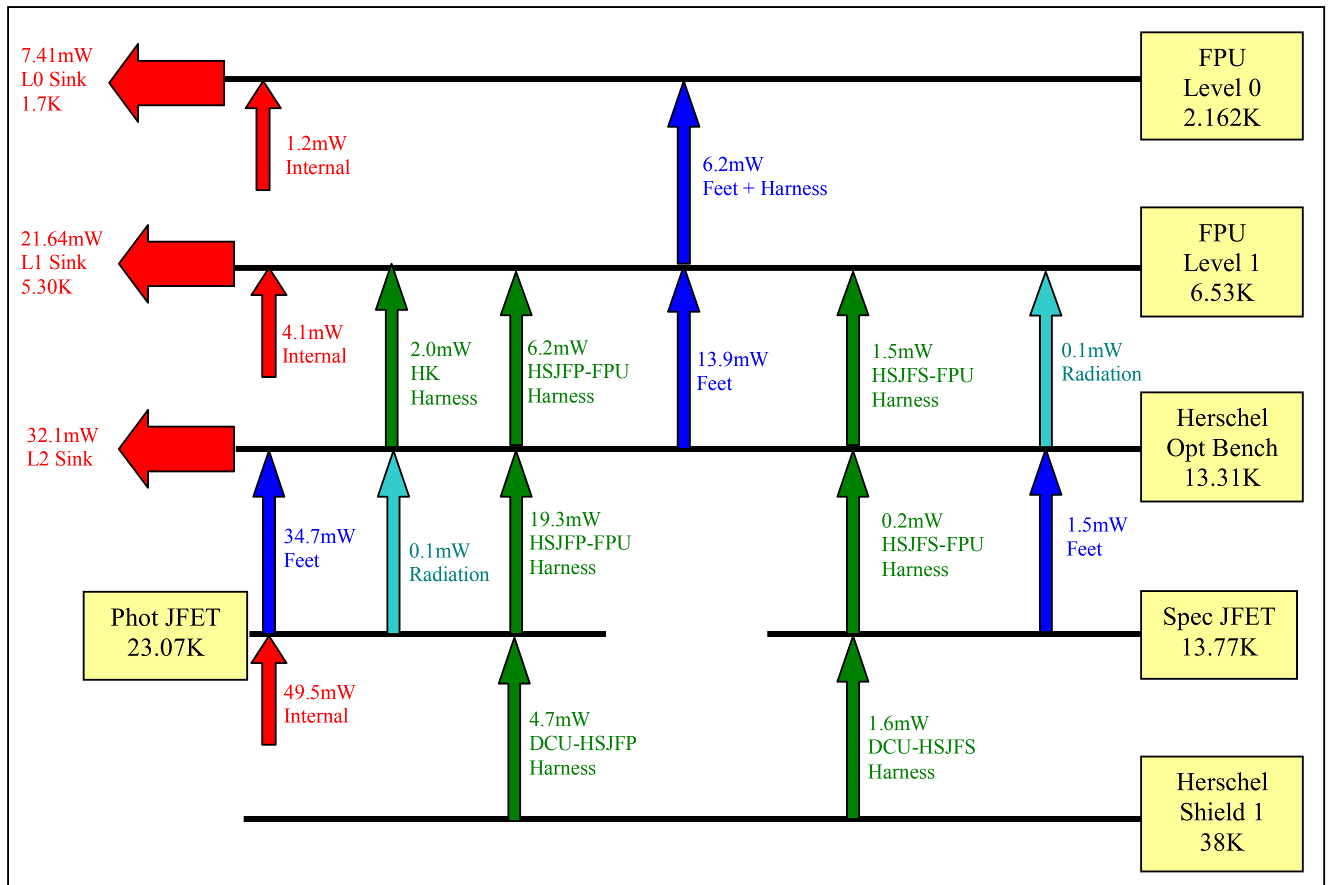

Figure 5.7: Case 4b Results

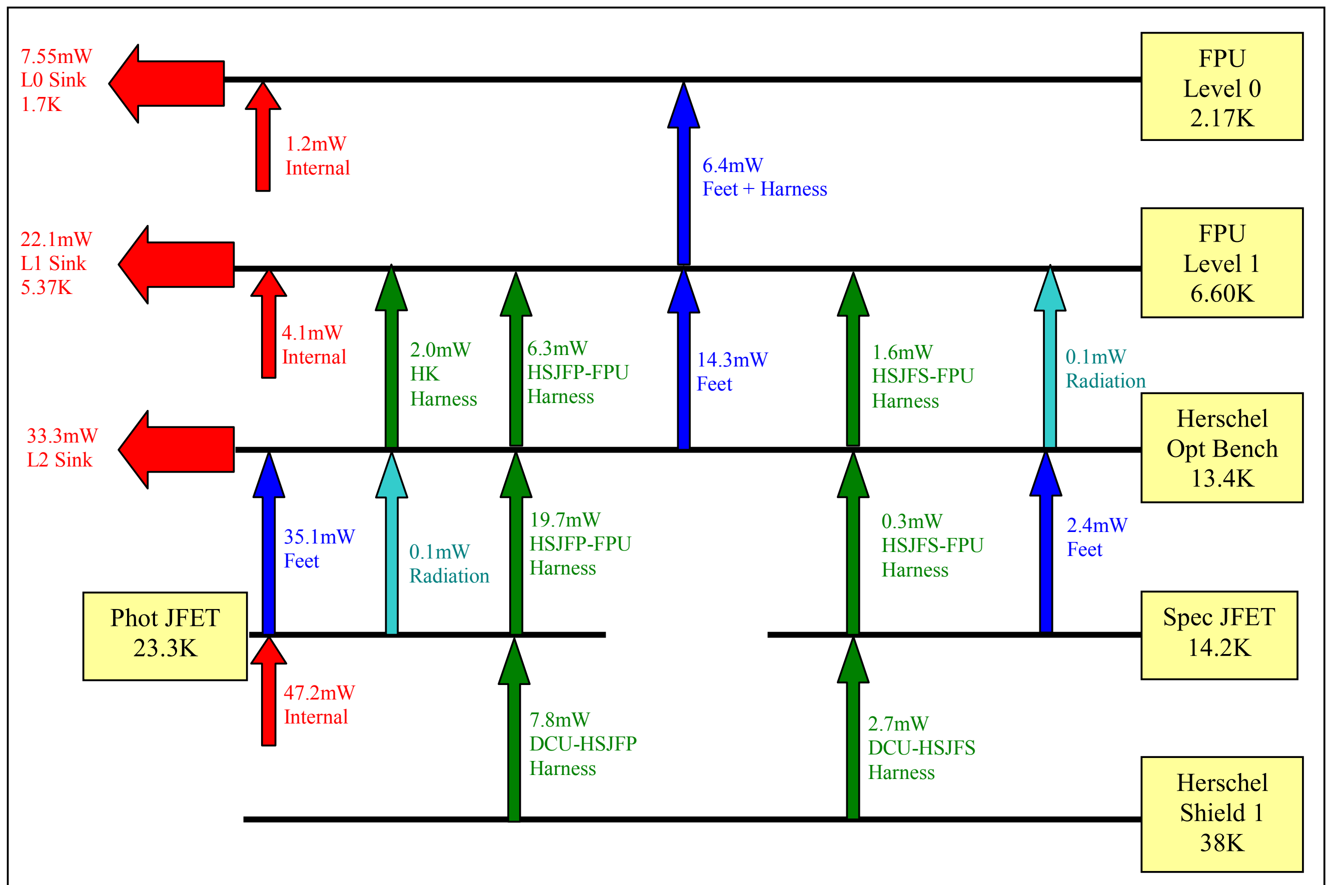

Figure 5.8: Case 4c Results

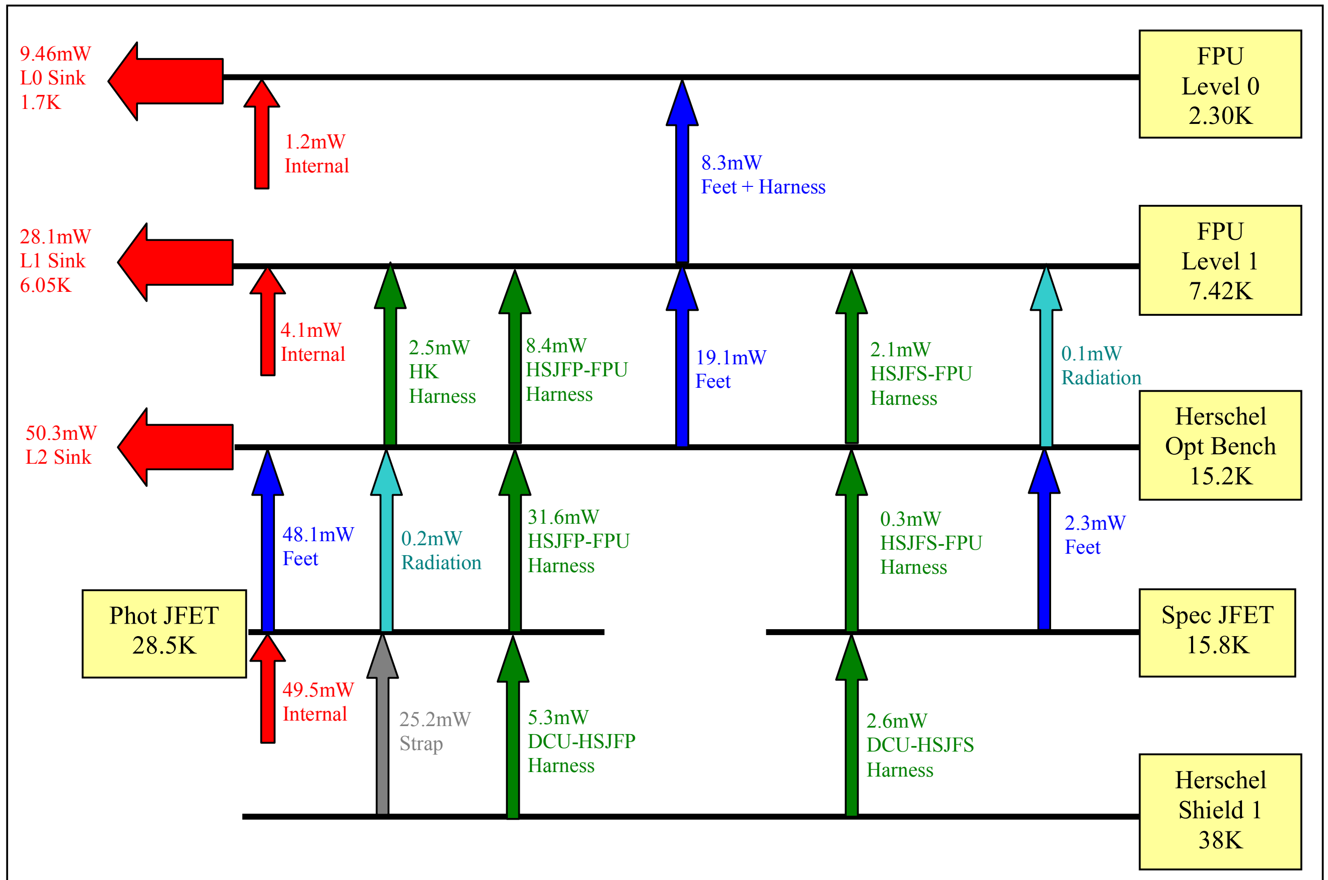

Figure 5.9: Case 5b Results

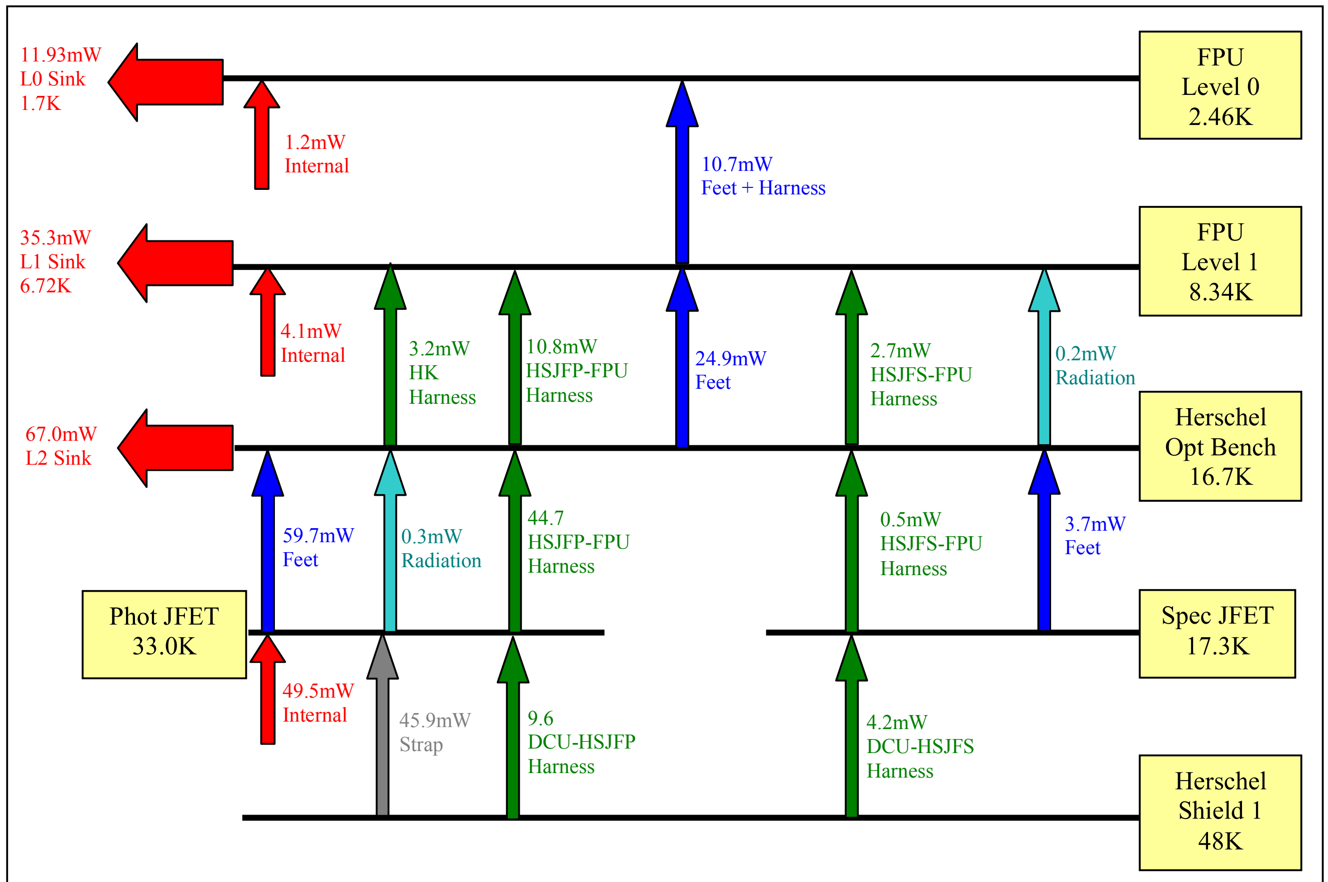

Figure 5.10: Case 5c Results

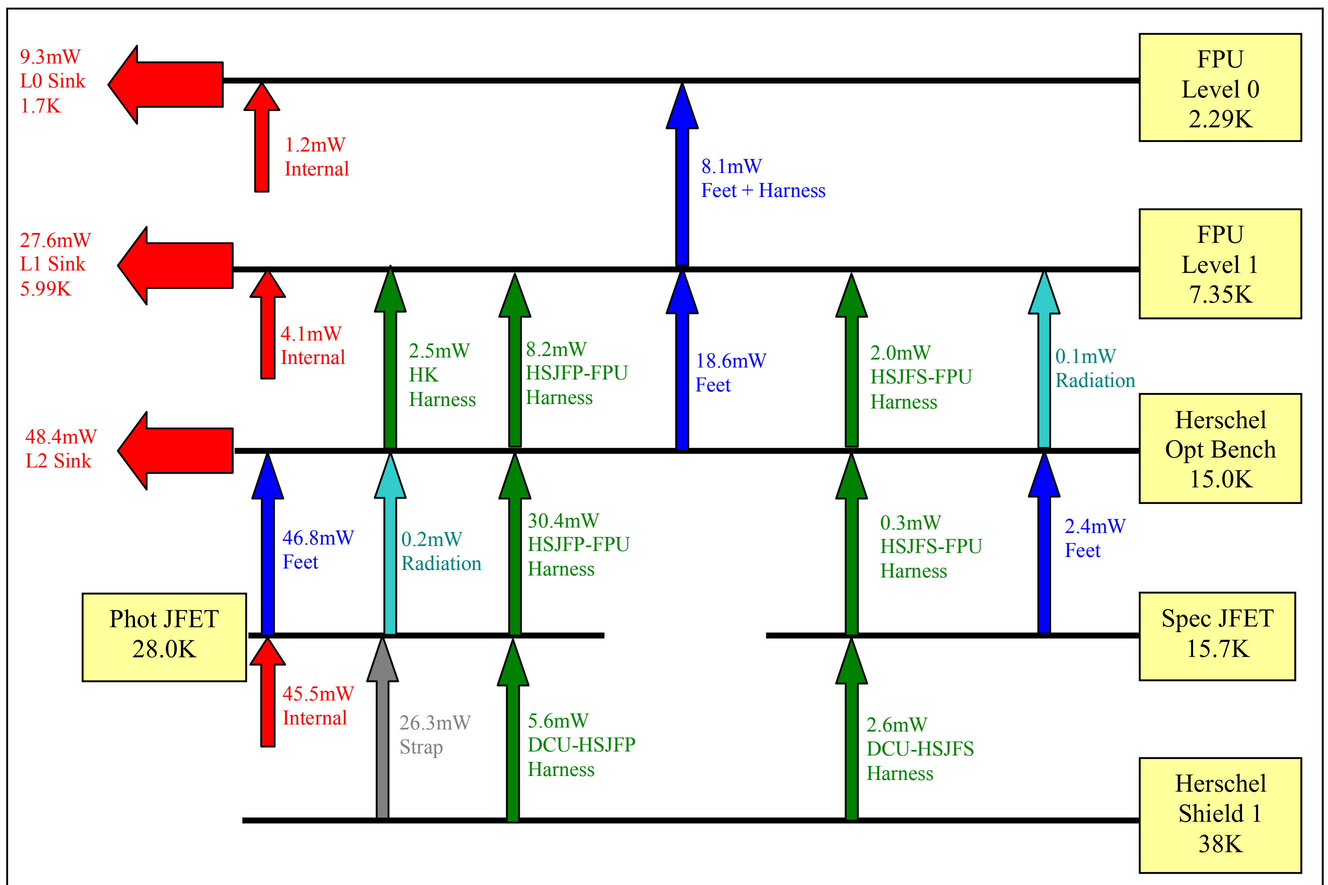

Figure 5.11: Case 5d Results