SPIRE warm electronics integration Plan

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Document Change Record

Date	Index	Affected Pages	Changes
10-Jan-2002	0.1	All	First Draft

Contents

1 Scope of Document

This document describes how the integration and test of the SPIRE warm electronics units will be implemented. It covers all models.

The term 'Warm Electronics' covers the following units:

- DPU Digital processor unit
- DRCU Detector Readout and Control Unit (consists of two units DCU and FCU)
- WIH Warm Interconnect Harness

2 Documents

2.1 Applicable Documents

	Title	Author	Reference	Date
AD 1	SPIRE Instrument Qualification Requirements	B. Swinyard	SPIRE-RAL-PRJ-000592 Issue 1.1	29-Mar-2001
AD 2	Instrument AIV Plan	B. Swinyard	SPIRE-RAL-PRJ-000410 Issue 2.1	29-Mar-2001
AD 3	DPU requirements specification		SPIRE-IFS-PRJ-000462 Issue 1.2	26-Nov 2001
AD 4	OBS URD		SPIRE-IFS-PRJ-000444 Issue 1.0	28-Sept-2000
AD 5	SPIRE Product Assurance Plan	D. Kelsh	SPIRE-RAL-PRJ-000017 Issue 1.0	11-Apr-2001
AD 6				
AD 7				

3 Model philosophy

For the warm electronics the following model philosophy will be adopted.

AVM	Avionics model
QM	Qualification Model
PFM	Proto-Flight Model
FS	Flight Spare (parts only)

AVM – Avionics Model.
This is an electrical model of the SPIRE instrument and will consist of the AVM DPU and a DRCU simulator. It will allow the electrical and software interfaces between the SPIRE instrument and the spacecraft to be validated. This will include the capability of testing the SPIRE autonomy functions and any exchange of information required between the spacecraft and SPIRE for any SPIRE operational mode. This model is delivered to ESA.

QM – Qualification Model
The DPU and DRCU follow different QM model philosophies.
There is a requirement to support the CQM test programme at instrument level.
The warm electronics for the CQM consists of the AVM together with a QM DRCU (designated QM1) and a warm integration harness. This model is delivered to ESA.

Qualification Models of the DPU (designated QM) and DRCU (designated QM2) will be built to qualify the design.
These qualification models will also be used to support instrument level testing of the PFM in advance of the warm electronics FMs being available.

PFM – Proto-Flight Model. The SPIRE warm electronics units will have full qualification models built and tested, therefore the PFM warm electronics units will only undergo acceptance testing.
This model is delivered to ESA.

3.1 Overall development programme

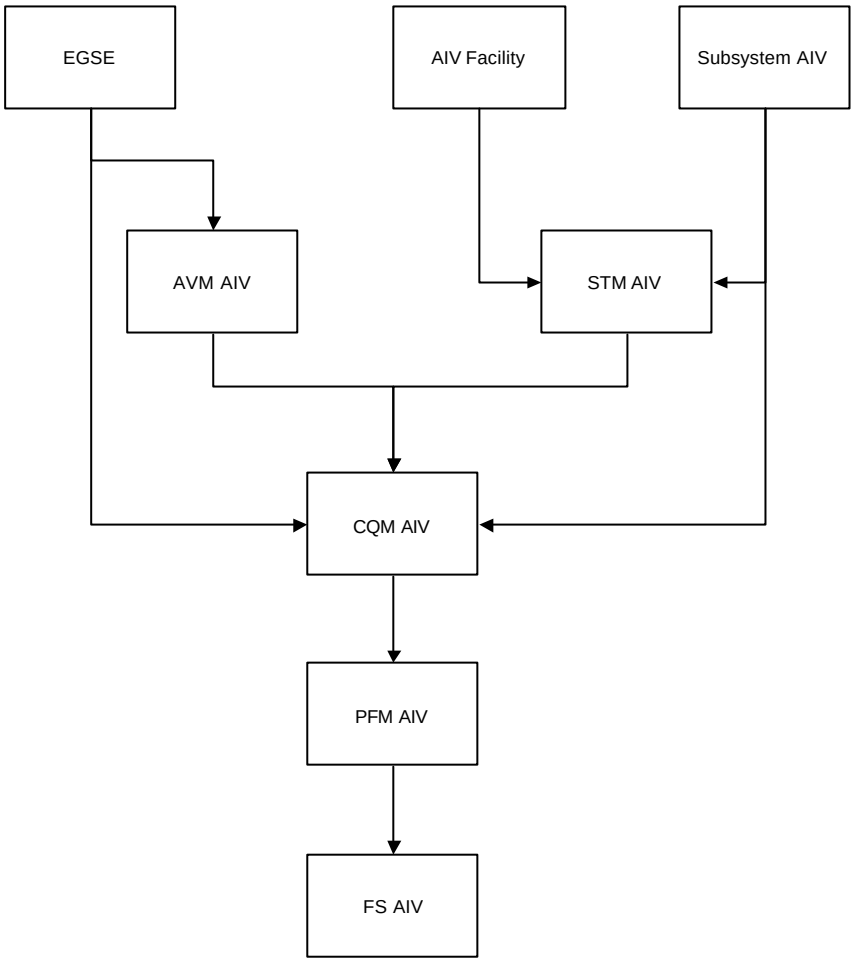

Figure 3.1: Flow chart showing the logical association of the various SPIRE models within the SPIRE development programme.

4 Warm Electronics AIV

4.1 Overview

Production of the warm electronics units for SPIRE is phased differently to the cold FPU and JFET Box production. This is dictated by the resources available and complex nature of the interfaces between the sub-systems and the warm electronics. In this section we describe the assembly and integration of the units that go to make up the warm electronics used to test each instrument model and those which will be delivered to ESA.

Each step of the AIV sequence is numbered and the tests are named in bold throughout the section. Whilst an indication of the types of tests that will be carried is given, the detailed procedures for each test are the subject of documents covering each test. The correspondence between each test named here and the instrument requirements that are verified in each test is given in AD2. The correspondence between sub-system specifications and tests is dealt with in the subsystem AIV plans.

5 AVM

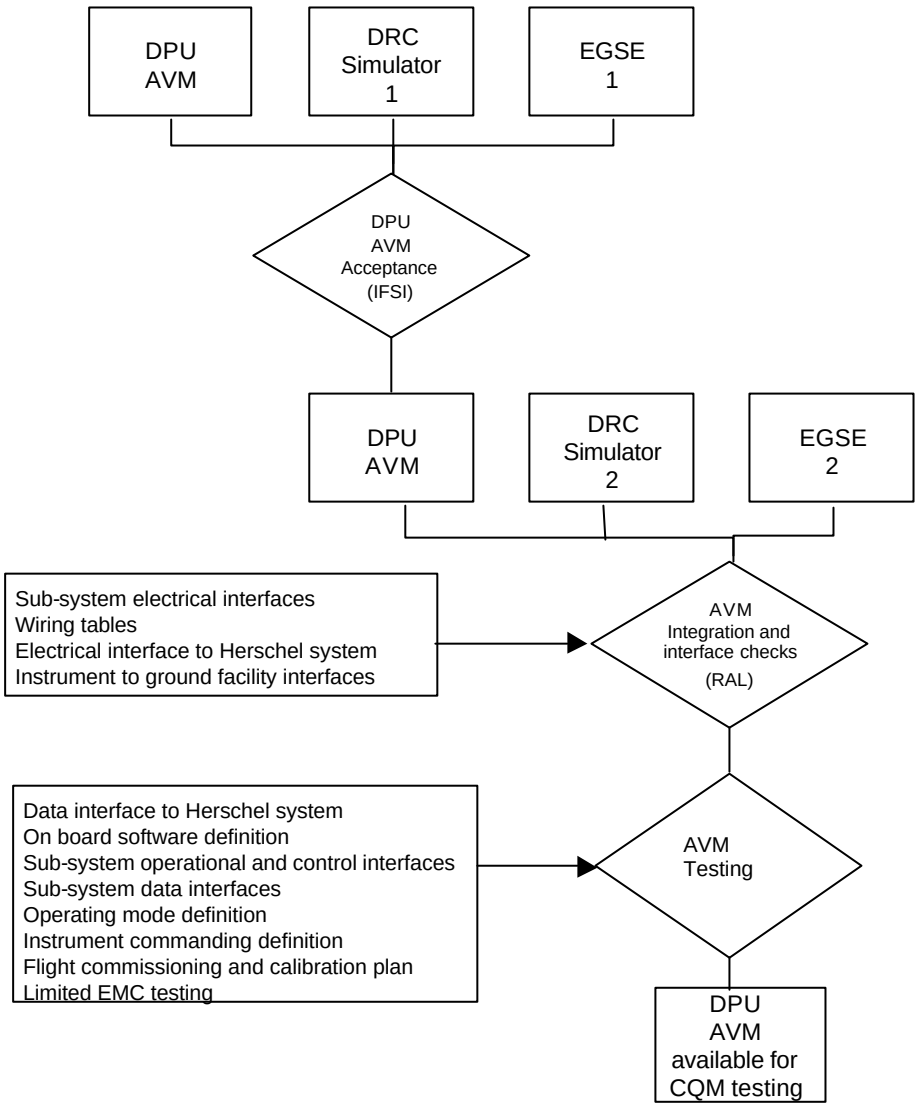

Figure 5-1

5.1 AVM Warm Electronics

5.1.1 Capabilities

The AVM warm electronics consists of the AVM model of the DPU and a simulator of the DRCU and cold FPU. It is intended that these will be delivered to ESA.

The DPU will have the full functionality of the flight version but it will be built with commercial grade parts and will not have redundant systems fitted. It will be identical in external form and fit to the flight unit. This unit will also be used for the testing of the CQM cold FPU and JFET box.

The DRCU simulator will be a computer with interface cards to the DPU that is capable of receiving commands from the DPU and returning realistic data to mimic the operation of the DRCU; cold FPU and JFET box. Several DRCU simulators will be required at different institutes.

5.1.2 Outline Integration and Verification

Figure 5-1 shows the indicative order of assembly, integration and verification of the instrument AVM and associated EGSE. More detail on the tests to be carried out is given here.

5.1.2.1 DPU Acceptance Tests at IFSI

These will be designed to test the specifications given in the DPU Specification Document (AD3) and the OBS URD (AD4). Some of the specifications reflect higher level requirements in the Instrument Requirements Document and, therefore, these tests form part of the instrument level verification. In outline the tests are:

Test low-level interface between the DPU and the CDMS conforms to the appropriate interface definition
Test high-level interface protocol to S/C (Packet protocols etc)
Test high and low speed interfaces between DPU and DRCU – again both hardware and protocols as given in ICD
Static OBS Functionality – acceptance of commands; TM generation; OBS performance requirements
OBS Management functions as given in the DPU specification document.

We wish to discover from these tests whether the DPU/OBS can "run" the instrument in all its operating modes with the correct data collection; extraction of real time parameters (if necessary); algorithm execution and real time commanding and execution of a command queue from the S/C to simulate instrument operation – again with correct data collection; TM formatting and transmission to CDMS.

We also need to test the response of the OBS/DPU to various failure conditions both in the DRCU (failure to initialise; PSU failure; interface failure etc) and within one of the sub-systems (loss of SMEC position sensor; loss of drive coils etc). We will also test the autonomy functions of the OBS – that is switching to SAFE mode in the event of DRCU/sub-system failure of OFF in the event of DPU failure.

In summary the AIV sequence at IFSI will be as follows -:

HS_WE_AIV_1. AVM DPU and OBS acceptance testing at IFSI

1.1. The DPU is assembled and integrated at IFSI
1.2. The DRCU simulator #1 is delivered to IFSI from Stockholm
1.3. The EGSE #1 is delivered to IFSI from RAL
1.4. The units are connected and basic interface checks are carried out to ensure compatibility between the DPU; DRCU simulator and the EGSE
1.5. The DPU acceptance procedure is carried out to ensure the compatibility of the unit as delivered from the manufacturer with the SPIRE instrument requirements and interface specification (this is the AVM **DPU_ACCEPT** test)
1.6. The On board Software acceptance procedure is carries out to ensure the compliance of the DPU and OBS with the OBS user requirements (this is the AVM **OBS_ACCEPT** test)
1.7. Following the acceptance of the DPU and OBS the DPU is prepared and shipped to RAL. The DRCU simulator #1 and the EGSE #1 remain at IFSI

5.1.2.2 DPU Integration at RAL

At RAL the AVM integration and functional test will be a repeat of a subset of the acceptance tests carried out at IFSI plus a test of running simulated instrument operations .

In summary the AIV sequence at RAL will be:

HS_WE_AIV_2. DPU integration at RAL

2.1. The DRCU simulator #2 is delivered to RAL from Stockholm
2.2. EGSE#2 is already at RAL
2.3. The DPU is received from IFSI
2.4. The DPU is integrated with the EGSE and DRCU simulator and basic interface checks are carried out.
2.5. The AVM functional test procedure is carried out. (this is the **AVM_FUNC** test)
2.6. The DPU AVM is now available for use with the warm electronics to be used with the instrument CQM.

5.1.2.3 AVM verification following CQM programme

This AVM DPU will be delivered to ESA together with the DRCU simulator #3 and the EGSE#3 to form the Instrument AVM. This delivery will occur at the end of the instrument CQM programme. Before the Instrument AVM can be delivered it has to be integrated and the AVM verification procedures carried out to ensure that any changes to the OBS; the DRCU simulator and/or the EGSE do not affect the performance of the integrated unit.

In summary the AIV sequence at RAL will be:

HS_AVM_AIV_1. DPU integration at RAL

1.1. The DRCU simulator #3 is delivered to RAL from Stockholm
1.2. EGSE#3 is already at RAL
1.3. The DPU is integrated with the EGSE and DRCU simulator and basic interface checks are carried out.
1.4. The AVM verification test procedure is carried out. (this is the **AVM_VER** test)

6 CQM

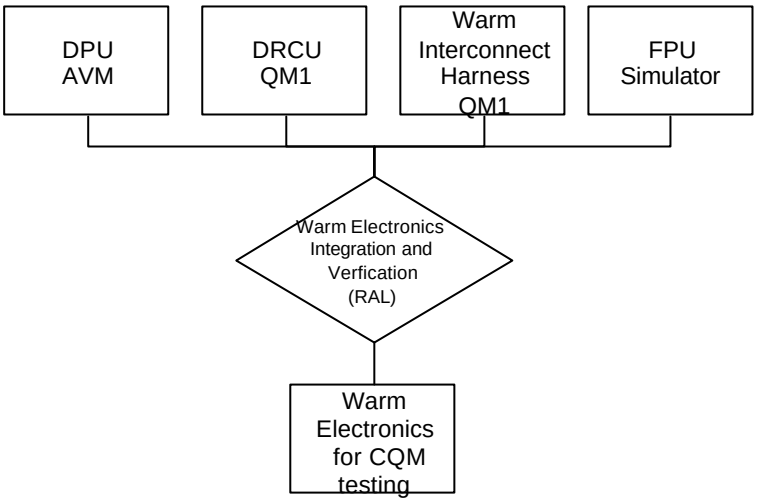

Figure 6-1

6.1 CQM Warm Electronics

6.1.1 Capabilities

The warm electronics for the CQM testing consist of the DPU AVM and a qualification model of the DRCU (QM1) that has full flight functionality but will be built with commercial grade parts and will not have any redundancy. The QM1 DRCU will not be identical in external form and fit to the flight unit. An engineering model of the warm interconnect harness will also be used. This will have external form and fit identical to the flight unit but will be built with commercial grade parts. In order to verify the function of the warm electronics for the CQM testing a simulator of the cold FPU and JFET box is required to give realistic responses to the DRCU in the absence of the real sub-systems. This FPU simulator is intended to be as passive as possible, i.e. resistors in place of JFETs; coils; thermistors etc. Only the output from the SMEC position encoder may have to provide some active return in the form of a sinusoidal signal.

6.1.2 Outline Integration

Figure 6-1 shows the indicative order of assembly and integration tests for the AVM DPU; the QM1 DRCU; the QM1 warm interconnect harness and the associated EGSE and FPU simulator. More detail on the steps to be followed is given here.

HS_WE_AIV_3. CQM Warm electronics integration at RAL

3.1. The FPU simulator; the DRCU and the warm interconnect harness will be delivered to RAL from CEA
3.2. The FPU simulator; the DRCU and the warm interconnect harness will be integrated with the DPU AVM and EGSE#2 and basic interface checks carried out
3.3. The warm electronics integration procedures will be carried out (this is the CQM **WE_INTG** test)
3.4. The warm electronics is now available for integration with the cold FPU and JFET box.

3.5. This set of electronics, including the FPU simulator, will be delivered to ESA as part of the instrument CQM.

7 QM

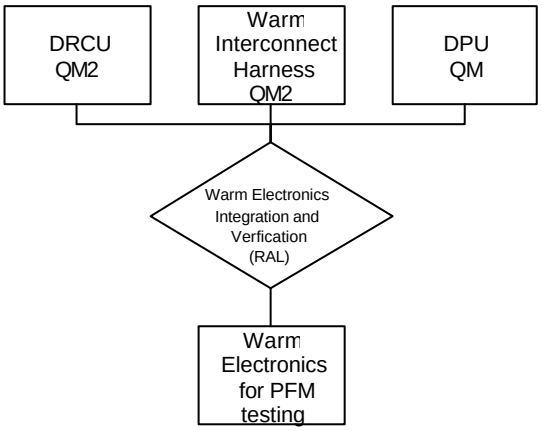

Figure 7-1

7.1 QM Warm Electronics

7.1.1 Capabilities

The QM electronics consists of the qualification model DPU; the second qualification model DRCU (QM2)and the second qualification model warm interconnect harness (QM2). These are identical in function; form and fit to the flight units. They will be built to flight standards but with some parts in both the DPU and DRCU being “extended range” or commercial grade rather than flight grade. The DPU QM will undergo full environmental and EMC (TBC) testing at IFSI before delivery. The DRCU QM2 will undergo full environmental and EMC testing at CEA before delivery. As the QM FPU simulator has been delivered to ESA as part of the instrument CQM, another one is required for testing this set of electronics. This set of electronics will be used to carry out the majority of instrument PFM tests, however they are not intended for flight and will not be delivered to ESA.

7.1.2 Outline Integration

Figure 7-1 shows the indicative order of assembly and integration for the QM DPU; the QM2 DRCU and the QM2 warm interconnect harness and the associated EGSE and FPU simulator. More detail on the steps to be followed is given here.

HS_WE_AIV_4. QM Warm electronics integration at RAL

4.1. The FPU simulator; the DRCU and the warm interconnect harness will be delivered to RAL from CEA
4.2. The DPU will be delivered to RAL from IFSI
4.3. The FPU simulator; the DRCU and the warm interconnect harness will be integrated with the DPU and EGSE#2 and basic interface checks carried out
4.4. The warm electronics integration procedures will be carried out (this is the QM **WE_INTG** test)
4.5. The warm electronics is now available for integration with the cold FPU and JFET box.

8 PFM

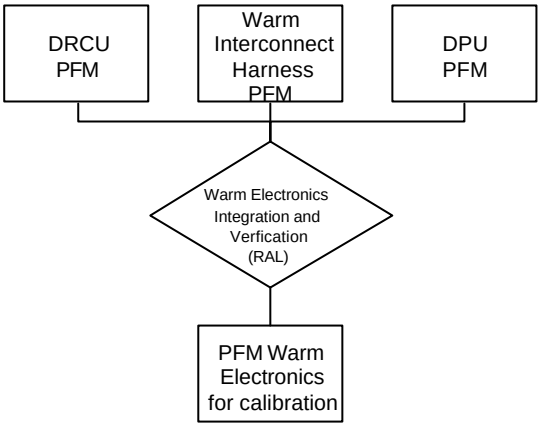

Figure 8-1

8.1 PFM Warm Electronics

8.1.1 Capabilities

The PFM electronics consist of the flight models of the DRCU; the warm interconnect harness and the DPU. These are the units intended for flight and have, naturally all the functions required including redundancy and are fully compliant with the satellite interface requirements. The DRCU; warm interconnect harness and the DPU will have been through environmental acceptance testing before delivery to RAL.

8.1.2 Outline Integration

Figure 8-1 shows the indicative order of assembly and integration for the FM DPU; the FM DRCU and the FM warm interconnect harness and the associated EGSE and FPU simulator. More detail on the steps to be followed is given here. This set of electronics will be used to carry out the calibration and functional performance tests on the PFM instrument. They will be delivered to ESA as part of the PFM instrument.

HS_WE_AIV_5. PFM Warm electronics integration at RAL

5.1. The DRCU and the warm interconnect harness will be delivered to RAL from CEA
5.2. The DPU will be delivered to RAL from IFSI
5.3. The FPU simulator; the DRCU and the warm interconnect harness will be integrated with the DPU and EGSE#2 and basic interface checks carried out
5.4. The warm electronics integration procedures will be carried out (this is the PFM **WE_INTG** test)
5.5. The warm electronics is now available for integration with the cold FPU and JFET box.

9 FS

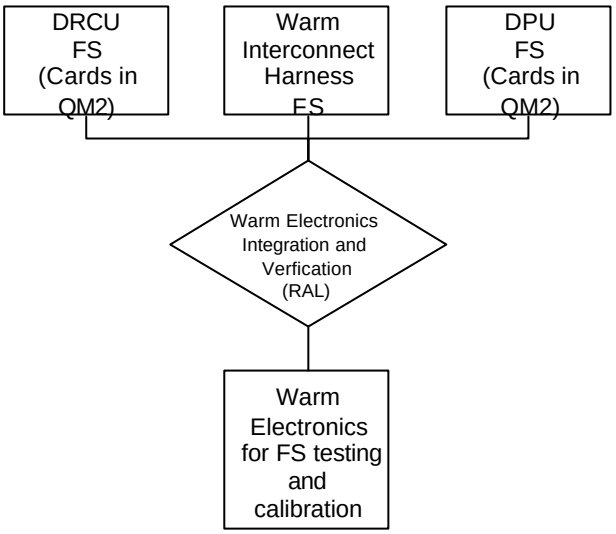

Figure 9-1

9.1 FS Warm Electronics

9.1.1 Capabilities

It is intended to provide flight spare electronics at board level only. In order to test the electronics the boards will be assembled into the qualification model DRCU and QM DPU frames (QM2 and QM respectively). Once assembled into the appropriate frames that FS boards will have fully flight like function and external form and fit. The QM2 warm interconnect harness will be used for flight spare testing and there will be no FS warm interconnect harness. The boards will undergo environmental acceptance testing in the qualification model boxes. It is assumed that the QM2 harness remains at RAL. This set of electronics will be used to carry out the calibration and functional performance tests on the FS instrument. The boards within the electronics will be available to replace PFM boards in the PFM instrument in the event of failures during system level AIV.

9.1.2 Outline Integration

Figure 9-1 shows the indicative order of assembly, integration and verification for the QM DPU; the QM2 DRCU and the QM2 warm interconnect harness and the associated EGSE and FPU simulator. More detail on the steps to be followed is given here.

HS_WE_AIV_6. FS Warm electronics integration at RAL

6.1. The DRCU boards assembled into the QM2 frame will be delivered to RAL from CEA
6.2. The DPU boards assembled into the QM frame will be delivered to RAL from IFSI
6.3. The FPU simulator; the DRCU and the warm interconnect harness will be integrated with the DPU and EGSE#2 and basic interface checks carried out
6.4. The warm electronics integration procedures will be carried out (this is the FS **WE_INTG** test)
6.5. The warm electronics is now available for integration with the cold FPU and JFET box.