CARLO GAVAZZI SPACE SpA

HSO/FIRST-DPU

DOCUMENT TYPE : TEST PROCEDURE **DRD :** -

TITLE: EM MOTHERBOARD TEST PROCEDURE

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THIS DOCUMENT IS SUBJECT TO THE APPROVAL OF:

	YES	NO	Approval Signature	Date
Product Assurance	X			
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Project Control		X		
Engineering	X			
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Higher Level Contractor				
Customer				

Data Management		
	Signature	Date

DOCUMENT CHANGE RECORD

ISSUE N°	DATE	CHANGE AUTHORITY	PAGES AFFECTED	REMARKS
1	18/10/2001			

LIST OF VALID PAGES

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LIST OF ACRONYMS

DPU	Data Processing Unit
EDAC	Error Detector And Corrector
DPR	Dual Port Ram
EEPROM	Electrically Erasable Programmable Read Only Memory
EM	Engineering Model
EPROM	Erasable Programmable Read Only Memory
EQM	Engineering Qualification Model
FIRST	Far Infra-Red and Sub-millimeter Telescope
FM	Flight Model
FPGA	Field Programmable Gate Array
FS	Flight Spare
HIFI	Heterodyne Instrument for First
HSO	Herschel Space Observatory
IF	Interface
ISR	Interrupt Service Routine
LSA	Logic State Analyzer
PACS	Photoconductor Array Camera and Spectrometer
PCB	Printed Circuit Board
PROM	Programmable Read Only Memory
PL	Payload
RAM	Random Access Memory
SC	Spacecraft
SPIRE	Spectral and Photometric Imaging Receiver

1 SCOPE

The aim of the present document is to define a procedure to test the EM version of Motherboard to be used in the Data Processing Units, developed in the framework of the HSO/FIRST program.

Scope of the test is verify the correct signal transfer between the connectors and the absence of shortcircuits on the board.

2 APPLICABLE DOCUMENTS

The current issue of the following documents are applicable:

[AD1]: DPU-SP-CGS-001, “First CPU Board Specification”

[AD2]: DPU-SP-CGS-003, “Payload & Spacecraft Interface Board Specification”

[AD3]: DPU-SP-CGS-004, “DC/DC Board Specification”

[AD4]: DPU-SP-CGS-005, “HSO/FIRST-DPU Motherboard Specification”

[AD5]: DPU-PL-CGS-001, “Product Assurance Plan for FIRST-DPU”

3 PARTICIPANTS REQUIRED

3.1 General

All tests shall be performed under QA surveillance in accordance with and following detailed procedure of CGS PA Plan [AD5].

The test shall be notified to the Customer as applicable.

3.2 Responsibility

The technical responsibilities for testing and test results is of the Engineering department.
Project and test managers are responsible for the test program. The test engineer is responsible for the correct execution of the test program and for the fulfilment of the requirements, for measurement and recording and for the preparation of the test report.

QA is responsible for ensuring that all the agreed procedures are carefully observed, that test equipment and instrumentation used during testing are calibrated and within validity date, that the test results are recorded in the relative Test Report and signed by the operators and QA witness, that all non conforming condition and test results are properly documented and notified to the customer and that all requirements of applicable PA Plan, Specification and Statement Of Work pertaining to the acceptance tests, are fully satisfied.

3.3 QA witness of Tests and Sign-off

QA inspector shall witness all tests described in this procedure and shall sign the test data sheet.

3.4 Non-conformance and failures

Any malfunction occurred during the tests shall be processed according to the Non-Conformance Procedure.

3.5 Calibration Requirements

All instruments used for testing shall be calibrated. Evidence of certification shall be provided by a label attached to the instruments itself, showing the calibration date, the expire date and the signature of the operator.

4 TEST CONDITIONS

- The Unit shall be tested in its defined configuration: it shall be properly mounted, all the electrical loads (if any) shall be present and the unit interface function(s) shall be simulated.
- Unless otherwise specified, all the measurements are to be performed at the following ambient conditions:

  - Temperature : 22°C ±3°C
  - Relative humidity: 55% ±10% RH
  - Pressure : Ambient
  - Cleanliness : NA

- All tests, unless otherwise specified, shall be performed internally to CGS laboratories in a proper area.
  General disposition shall be applied to maximise personnel safety from potential hazards.

- Connectors savers shall be used to protect the Unit Under Test (UUT) interface connectors.

- Skilled personnel shall be employed.

- All used instruments shall meet the necessary accuracy and shall not degrade the UUT performance.

5 EXECUTING TEST

Insulation and electrical tests are performed by manufacturer of PCB. Test engineer is responsible to verify the absence of shortcircuits on the board after assembly.

TITLE: MOTHERBOARD TEST PROCEDURE		UNIT UNDER TEST:	S/N:	
STEP N°	TEST SEQUENCE	EXPECTED VALUE	MEASURED VALUE	REMARKS
1	Visual inspection	OK		

DATE	TEST CONDUCTOR	PRODUCT ASSURANCE	CUSTOMER

6 DEVIATION

In case that for any reason the test procedure has to be changed, the change shall be described in a Procedure Variation Sheet (PVS) attached to this document in Table 1.

The PVS shall contain:

- Reference to the procedure to be changed
- Reference to the relevant test, procedure page and paragraph
- Description of the change
- Reason for change
- Engineering and QA signature
- Customer signature (when required).

6.1 Procedure variation sheet

The Procedure Variation Sheet is shown in Table 1.

PROCEDURE VARIATION SHEET

Test procedure Ref.:	Page revised	Para. revised
Description of changes:		
Reason for changes:		

CONCURRENCE			
TEST COND	P.A.	ENG.	CUSTOMER

Table 1