CARLO GAVAZZI SPACE SpA

HSO/FIRST-DPU

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Titolo : *Title :*	EM/QM/FM DC/DC CONVERTER BOARD ELECTRICAL AND FUNCTIONAL TEST PROCEDURE				

	Nome & Funzione *Name & Function*	Firma *Signature*	Data *Date*
Preparato da: *Prepared by:*	FIRST-DPU TEAM		
Approvato da: *Approved by:*	Francini E. (PA/QA) Di Gioia L. (PC/CC) Sciortino A. (DT/EE)		
Applicazione autorizzata da: *Application authorized by:*	Longoni A. (DP/PL)		
Customer / Higher Level Contractor			
Accettato da: *Accepted by:*			
Approvato da: *Approved by:*			

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REGISTRAZIONE DELLE MODIFICHE / *CHANGE RECORD*

EDIZIONE *ISSUE*	DATA *DATE*	AUTORIZZAZIONE *CHANGE AUTHORITY*	OGGETTO DELLA MODIFICA E SEZIONI AFFETTE *REASON FOR CHANGE AND AFFECTED SECTIONS*
1	04/02/2002		

LISTA DELLE PAGINE VALIDE / *LIST OF VALID PAGES*

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1. SCOPE

This document describe the test procedure applicable to the electrical and functional tests of the:

Engineering, Qualification and Flight Models of the DC/DC board which shall be used to supply the Data Processing Unit (DPU) of the Payload Instruments HIFI, PACS and SPIRE to be developed in the framework of the FIRST program.
For the payload experiment HIFI only, the DC/DC board, besides the supply of the DPU, shall provide supplying voltages for the HIFI instrument itself. In this case the DC/DC board shall be called “DPU+PL version”.
The DC/DC board devoted to supply the DPU unit only, shall be called as “DPU version”.

The test to be performed according to this procedure are to demonstrate the compliance of the above item(s) to the requirements specified in the applicable document as part of the overall verification program. The test results shall be collected in a Test Report.

For the “DPU version” of the DC/DC converter board, only test procedures applicable to “DPU version” must be considered.

2. DOCUMENTS

2.1 APPLICABLE DOCUMENTS

[AD1]: CNR.IFSI.2000TR01 "Documento di Specifiche Tecniche per il Contratto delle Data Processing Units del Satellite First dell'ESA" IFSI (Issue: 1 - 15/09/2000)
[AD2]: Technical proposal CGS (Ref. S9-030 November 99)
[AD3]: "Allegato Tecnico al Contratto ASI"
[AD4]: Product Assurance Plan for the FIRST DPU (DPU-PL-CGS-001 Issue 1 Jan. 2001)
[AD5]: DC/DC Board Specification DPU-SP-CGS-004-Iussue 1 dated May 21st 2001

2.2 REFERENCE DOCUMENTS

[RD1] - FIRST/Planck Instrument Interface Document Part A. (Ref. SCI-PT-IIDA-04624 Issue-Rev. No. : 1/1)
[RD2] - FIRST/Planck Instrument Interface Document Part B - Instrument "HIFI" (Ref. SCI-PT-IIDB/HIFI-02125 Issue-Rev No. : 1/0)

3. ACRONYMS

AD	Applicable Document Number
BB	Broadband
CE	Conducted Emission
C.I.	Configuration Item. Also called Part Number (P/N)
CGS	Carlo Gavazzi Space
CS	Conducted Susceptibility
DPU	Data Processing Unit
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
FIRST	Far Infra-Red and Sub-millimeter Telescope
FPU	Focal Plane Unit
FCU	Focal Control Unit
GND	Ground
HIFI	Heterodyne Instrument for First
HK	House Keeping
ICD	Interface Control Document
ICU	Instrument Control Unit
IID	Instrument Interface Document
I/F	Interface
LCL	Latching Current Limiter
NA	Not Applicable
NB	Narrowband
OCP	Over-Current Protection
OVP	Over-Voltage Protection
P/N	Part Number. Also called Configuration Item C.I.
PA	Product Assurance
PACS	Photoconductor Array Camera and Spectrometer
PDU	Power Distribution Unit
PL	Payload
PVS	Procedure Variation Sheet
QA	Quality Assurance
RD#	Reference Document Number
RE	Radiated Emission
RS	Radiated Susceptibility
RTN	Return Line
S/C	Spacecraft
S/N	Serial Number
SPIRE	Spectral and Photometric Imaging receiver
TBC	To Be Confirmed
TBD	To Be Determined
TM/TC	Telemetry & Tele-command
UUT	Unit Under Test

4. PARTICIPANTS REQUIRED

4.1 GENERAL

All test will be performed under QA surveillance in accordance with, and following detailed procedure of applicable PA Plan. Start of the Test shall be notified to Prime Contractor and/or Customer as applicable.

4.2 RESPONSIBILITY

The technical responsibility for testing and test results is up to the Engineering department.

QA is responsible for ensuring that all the agreed procedures are carefully observed, that test equipment and instrumentation used during testing is calibrated and within validity date: that the test data sheets are recorded in the Test Report and signed by the operators and QA witnesses, that all non conforming condition and test results are properly documented and notified to the Prime Contractor, and that all requirements of applicable PA Plan, specification and Statement of Work pertaining to the acceptance tests, are fully satisfied.

4.3 QA WITNESS OF TEST AND SIGN-OFF

QA inspector, or its delegate, shall witness the tests described in this procedure in accordance to the requirement specified in the applicable PA Plans.

4.4 NON CONFORMANCE AND FAILURES

Any malfunction/defect which occurs during the test will be processed along the Non Conformance Procedure described in the applicable PA Plans.

4.5 CALIBRATION REQUIREMENTS

All instruments used for testing shall be calibrated.

Evidence of certification shall be provided by a label attached to the instruments itself, showing the calibration date, the expiring date and the signature of the operator.

5. TEST ARTICLE

The test article consists as in following table:

Item	Model	Remarks
DC/DC converter SPIRE	EM/QM/FM	DPU Version
DC/DC converter HIFI	EM/QM/FM	DPU +PL Version
DC/DC converter PACS	EM/QM/FM	DPU Version

Before starting the test, the P/N and S/N of the test article(s) to be tested shall be recorded on the step-by-step procedure sheets under the table cell “UNIT UNDER TEST”.

5.1 DESCRIPTION

The DC/DC board (Push-Pull topologies) must provide a set of supply voltages for to the DPU internal electronics of the payload experiments HIFI, PACS and SPIRE. For the payload experiment HIFI only, the DC/DC board must provide a further external set of supply voltages for the HIFI/FCU unit.
Therefore the board must provide, considering the DPU+PL version, the following two sets of output voltages:

- “DPU-Outputs” to supply the DPU internal electronics
- “PL-Outputs” to supply the payload instrument HIFI/FCU unit.

In the DPU version only the DPU-Outputs shall be provided.

DPU-Outputs and PL-Outputs shall be isolated from primary power side and from each other (except for DPU RTN output that are connected together at board side) as described in [AD5].
The DC/DC board shall switch on automatically when the input voltage is within the range established in [AD5].

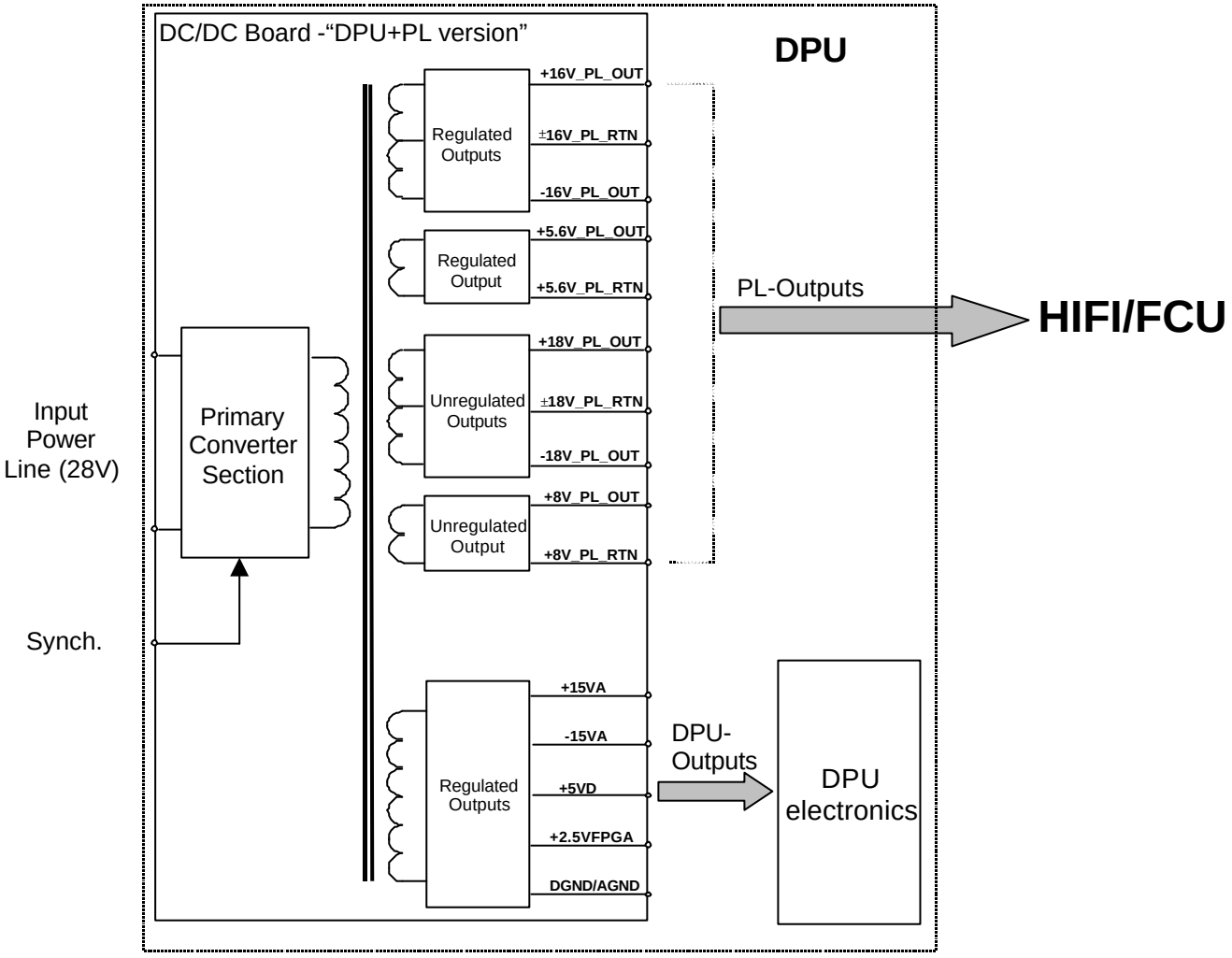

Fig. 5-1 DC/DC Board functional diagram ("DPU+PL version")

5.1.1 PIN FUNCTION

In the following tables the pin function of the board is reported

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+5VD	33	+5VD	65	+5VCORE
2	+VEEPROM	34	+2.5VFPGA	66	+5VCORE
3	+VFIFO	35	+5VBU61582	67	NOT USED
4	NOT USED	36	+VIFMEZZ	68	NOT USED
5	NOT USED	37	NOT USED	69	NOT USED
6	NOT USED	38	NOT USED	70	NOT USED
7	NOT USED	39	NOT USED	71	NOT USED
8	NOT USED	40	NOT USED	72	NOT USED
9	NOT USED	41	NOT USED	73	NOT USED
10	NOT USED	42	NOT USED	74	NOT USED
11	NOT USED	43	NOT USED	75	NOT USED
12	NOT USED	44	NOT USED	76	NOT USED
13	NOT USED	45	NOT USED	77	NOT USED
14	NOT USED	46	NOT USED	78	NOT USED
15	NOT USED	47	NOT USED	79	NOT USED
16	NOT USED	48	NOT USED	80	NOT USED
17	DGND	49	NOT USED	81	DGND
18	BONDING	50	BONDING	82	BONDING
19	BONDING	51	BONDING	83	BONDING
20	NOT USED	52	NOT USED	84	NOT USED
21	NOT USED	53	NOT USED	85	NOT USED
22	NOT USED	54	NOT USED	86	NOT USED
23	NOT USED	55	NOT USED	87	NOT USED
24	NOT USED	56	NOT USED	88	NOT USED
25	NOT USED	57	NOT USED	89	NOT USED
26	NOT USED	58	NOT USED	90	NOT USED
27	NOT USED	59	NOT USED	91	NOT USED
28	NOT USED	60	NOT USED	92	NOT USED
29	-15VA	61	-15VA	93	-15VA
30	AGND	62	AGND	94	AGND
31	+15VA	63	+15VA	95	+15VA
32	DGND	64	DGND	96	DGND

Tab. 5-1 DC-DC Converter board: P1 pin function

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+28V	33	+28V	65	+28V
2	NOT USED	34	NOT USED	66	NOT USED
3	+28V_RTN	35	+28V_RTN	67	+28V_RTN
4	NOT USED	36	NOT USED	68	NOT USED
5	SYNCH_MAIN+	37	SYNCH_MAIN+	69	SYNCH_MAIN+
6	SYNCH_MAIN-	38	SYNCH_MAIN-	70	SYNCH_MAIN-
7	SYNCH_RED+	39	SYNCH_RED+	71	SYNCH_RED+
8	SYNCH_RED-	40	SYNCH_RED-	72	SYNCH_RED-
9	NOT USED	41	NOT USED	73	NOT USED
10	INCUR_MNT	42	+5V_MNT	74	+15V_ MNT
11	RTN_MNT0	43	RTN_MNT1	75	RTN_MNT2
12	-15V_MNT	44	+TEMP_MNT	76	AINP5
13	RTN_MNT3	45	RTN_MNT4	77	RTN_MNT5
14	AINP6	46	NOT USED	78	NOT USED
15	RTN_MNT6	47	AGND	79	AGND
16	NOT USED	48	NOT USED	80	NOT USED
17	NOT USED	49	NOT USED	81	NOT USED
18	NOT USED	50	NOT USED	82	NOT USED
19	NOT USED	51	NOT USED	83	NOT USED
20	NOT USED	52	NOT USED	84	NOT USED
21	NOT USED	53	NOT USED	85	NOT USED
22	+16V_PL_OUT	54	+16V_PL_OUT	86	+16V_PL_OUT
23	-16V_PL_OUT	55	-16V_PL_OUT	87	-16V_PL_OUT
24	±16V_PL_RTN	56	±16V_PL_RTN	88	±16V_PL_RTN
25	+5.6V_PL_OUT	57	+5.6V_PL_OUT	89	+5.6V_PL_OUT
26	+5.6V_PL_RTN	58	+5.6V_PL_RTN	90	+5.6V_PL_RTN
27	+18V_PL_OUT	59	+18V_PL_OUT	91	+18V_PL_OUT
28	-18V_PL_OUT	60	-18V_PL_OUT	92	-18V_PL_OUT
29	±18V_PL_RTN	61	±18V_PL_RTN	93	±18V_PL_RTN
30	+8V_PL_OUT	62	+8V_PL_OUT	94	+8V_PL_OUT
31	+8V_PL_RTN	63	+8V_PL_RTN	95	+8V_PL_RTN
32	NOT USED	64	NOT USED	96	NOT USED

Tab. 5-2 DC-DC Converter board: P2 pin function

5.2 TEST MATRIX

This procedure is applicable to EM, QM and FM models according to the following test matrix.

- Electrical procedure (E)
- Functional procedure (F)

Procedure Step	TEST	EM	QM	FM
E1	Isolation verification	X	X	X
E2	Minimum loads and DC/DC internal power consumption during shut-down	X	X	X
E3	Switching Frequency	X	X	X
F1	Output voltage regulation-Load regulation	X	X	X
F2	Output voltage regulation-Line regulation	X	X	X
F3	Ripple and Spikes	X	X	X
F4	Efficiency and power consumption	X	X	X
F5	Inrush Current	X	X	X
F6	Input Impedance	X		
F7	Input protection	X	X	X
F8	DPU Output protections	X	X	X
F9	Regulated PL Outputs Protections	X	X	X
F10	Voltage monitors	X	X	X
F11	Temperature monitor	X	X	X
F12	CE on Input Power Line; Frequency Domain, Differential Mode, NB	X	X	
F13	CE on Input Power Line; Frequency Domain, Common Mode, NB	X	X	
F14	Current Ripple, Time Domain, Differential Mode	X	X	

Tab. 5-3 TEST MATRIX

6. TEST CONFIGURATION

Test set up are described in the step-by-step procedure sheets provided in § 11.

6.1 REQUIREMENTS CROSS REFERENCE

Cross reference among requirements and procedure steps is provided in table 6.-1

Tab. 6-1 REQUIREMENTS CROSS REFERENCE

REQ. n° (of DPU-SP-CGS-004 Is_1)	CGS SPEC.	PROCEDURE STEP	REMARKS
Paragraph 9.1	DPU-SP-CGS-004 Issue1	E1	
Paragraph 9.2	DPU-SP-CGS-004 Issue1	E1	
Paragraph 9.3	DPU-SP-CGS-004 Issue1	E1	
Paragraph 7.1	DPU-SP-CGS-004 Issue1	F1, F2, F3	
Paragraph 7.2.1	DPU-SP-CGS-004 Issue1	F1, F2, F3	
Paragraph 7.2.2	DPU-SP-CGS-004 Issue1	F1, F2, F3	
Chapter 7.	DPU-SP-CGS-004 Issue1	F4	
Paragraph 8.2	DPU-SP-CGS-004 Issue1	F5	
Paragraph 8.1.4	DPU-SP-CGS-004 Issue1	F6	
Paragraph 8.4	DPU-SP-CGS-004 Issue1	F7	
Paragraph 7.1.1	DPU-SP-CGS-004 Issue1	F8	
Paragraph 7.2.1.1	DPU-SP-CGS-004 Issue1	F9	
Paragraph 8.5	DPU-SP-CGS-004 Issue1	F10, F11	
Paragraph 10.1.1	DPU-SP-CGS-004 Issue1	F12	
Paragraph 10.1.2	DPU-SP-CGS-004 Issue1	F13	
Paragraph 10.1.3	DPU-SP-CGS-004 Issue1	F14	

6.2 TESTS APPLICABILITY

Item	Applicable Tests
DC/DC converter SPIRE	E1;E2;E3;F1;F2:F3;F4;F5;F6;F7;F8;F10;F11;F12;F13
DC/DC converter HIFI	E1;E2;E3;F1;F2:F3;F4;F5;F6;F7;F8;F9;F10;F11;F12;F13
DC/DC converter PACS	E1;E2;E3;F1;F2:F3;F4;F5;F6;F7;F8;F10;F11;F12;F13

7. INSTRUMENTATION AND TEST EQUIPMENT

The complete list of the instrumentation used during the test shall be recorded in table 7.-1.

The list shall be filled up during tests and reported in Test Report.

Tab. 7-1 INSTRUMENT LIST

N.	EQUIPMENT	MANUFACTURER	P/N	S/N	NEXT CAL. DATE	REMARKS

8. TEST CONDITION

- The CI shall be tested in its defined configuration: all electrical loads shall be present and the CI interface function(s) shall be simulated.

- Unless otherwise specified, all measurements are to be performed at the following ambient condition:

Temperature	25 °C +/- 3°C
Relative humidity	between 30 % and 60 % RH
Pressure	Ambient
Cleanliness	100000 class

- All tests, unless otherwise specified, shall be performed internally to CGS laboratories in a proper area. General disposition shall be applied to maximize personnel safety from potential hazards

- Connectors savers shall be used on FM/QM model as applicable to protect the UUT interface connectors.

- Skilled personnel shall be employed

- All used instruments shall meet the necessary accuracy and shall not degrade the UUT performances.

9. TEST PROCEDURE VARIATION SHEET

In case that for any reason the test procedure has to be changed, the change shall be described in a Procedure Variation Sheet (PVS) as shown in the next page.

The PVS shall contain:

- Reference to the test procedure to be changed
- Reference to the relevant test, procedure page and paragraph
- Description of the change, possibly in the form was….is…..
- Reason for change
- Test Engineer, QA, Test conductor signatures and dates
- Customer signature and date (when required).

Each PVS shall be identified by a reference number provided in sequential order.

All the generated PVS shall be collected in a dedicated section of the Test Report.

PROCEDURE VARIATION SHEET ref. N°:

Test Procedure Ref.:	Page Revised:	Paragraph Revised:

Description of Change:

Reason for Change:

CONCURRENCE

Test Cond.	QA	System Eng.		Customer

10. TEST DATA SHEETS

The step-by-step procedure sheets are provided in the following pages.

10.1 DATA SHEETS FILLING UP

The following fields of the data sheets:

- UUT DATA (including Model, Item, C.I., S/N)
- Measured value

shall be filled up during the test performances and shall be part of the Test Report together with photographs, sketches, etc. eventually useful to document the test execution/result.

Remarks field shall be used as a minimum to provide, where appropriate, reference to NCRs and PVS.

Test Report reference data shall be added in the relevant field.

Each data sheet (including the attachments) shall be certified by QA stamp and signature together with the Test Conductor signature and date.

UUT DATA :	**Model**	**Item**	**C.I.**	**S/N**

STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
E1	**ISOLATION VERIFICATION** The board shall be in OFF condition, disconnected from any cable or test equipment and placed on an insulated table.	OK		If the board under test is a "DPU Version", only the DPU pins are object of this test. OBJECTIVE: Verification of isolation between each output power return line and between power return lines and chassis. INSTRUMENTATION: Mega Ohm Meter and LRC Meter
E1.1	Verify that DC isolation between each outputs power return lines is higher than 1MΩ (except for DPU output return lines that are tied together at board level)	OK		
E1.2	Verify that DC isolation between each outputs power return line and bonding pins is higher than 1MΩ	OK		
E1.3	Verify that DC isolation between each output power return lines and input return line is higher than 1MΩ	OK		
E1.4	Verify that AC isolation between each output power return lines and bonding pins is lower than 50nF	OK		
E1.5	Verify that AC isolation between each output power return lines and input line is lower than 5nF	OK		
E1.6	Verify that DC isolation between input power return line and chassis is higher than 1MΩ shunted by no more than 5nF	OK		

DATE:	TEST CONDUCTOR	QA	CUSTOMER

UUT DATA :	Model	Item	C.I.	S/N

STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
E2	Minimum loads and DC/DC internal power consumption during shut-down			OBJECTIVE: Verification of power consumption INSTRUMENTATION: Power supply Voltmeter and Ammeter.
E2.1	Power the board through the input connectors at 26V (Ilimit=1A) with minimum loads connected as for table below			

Output	Voltage (V)	Min Current (mA)
DPU Electronic	+5	1000
DPU Electronic	+15	0
DPU Electronic	-15	0
DPU Electronic	+2,5	0
HIFI	5,6	0
HIFI	16	0
HIFI	-16	0
HIFI	8	0
HIFI	18	0
HIFI	-18	0

Measure the value of current absorbed by the board	<0.5A		

DATE:	TEST CONDUCTOR	QA	CUSTOMER

UUT DATA : Model	Item	C.I.	S/N

STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
E2.2				
E2.3	Power the board through the input connectors at 28V with minimum loads connected			
E2.4	Measure the value of current absorbed by the board	<0.5A		
E2.5	Power the board through the input connectors at 29V with minimum loads connected Measure the value of current absorbed by the board			
E2.6		<0.5A		
E.2.7	Decrease the input voltage until the UV protection is reached (at about 24V the DC/DC converter shut-down)			
E.2.8	Measure the input power consumption and report the value.	< 1W < 2,8W		DPU Version DPU+PL Version

DATE:	TEST CONDUCTOR	QA	CUSTOMER

UUT DATA :	Model	Item	C.I.	S/N

STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
E3	**SWITCHING FREQUENCY**			OBJECTIVE: Verification of switching frequency INSTRUMENTATION: Oscilloscope
E3.1	Connect an oscilloscope probe between, gate and source dedicated test points of Q9.(DPU section)			
E3.2	Measure the frequency of the driving signal and verify that the frequency is within the expected value	55kHz ± 10%		
E3.3	Connect an oscilloscope probe between gate and source dedicated test points of Q10. .(DPU section)			
E3.4	Measure the frequency of the driving signal and verify that the frequency is within the expected value	55kHz ± 10%		
	Measure the time between Gate rise edge of MOSFETs Q9 and Q10 and verify that the corresponding frequency is within the expected value. .(DPU section)	110KHz ± 10%		
E3.3	Connect an oscilloscope probe between gate and source dedicated test points of Q7.(PL section)			
E3.4	Measure the frequency of the diving signal and verify that the frequency is within the expected value	55Hz ± 10% 55kHz ± 10%		

DATE:	TEST CONDUCTOR	QA	CUSTOMER

UUT DATA : Model	Item	C.I.	S/N

STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
	Connect an oscilloscope probe between gate and source dedicated test points of Q8.(PL section) Measure the frequency of the diving signal and verify that the frequency is within the expected value	110KHz ± 10%		
	Measure the time between Gate rise edge of MOSFETs Q7 and Q8 and verify that the corresponding frequency is within the expected value. .(PL section)			
E3.5	Verify that the switching frequency of DPU and PL are synchronized	OK		
F1	**OUTPUT VOLTAGE REGULATION/LOAD REGULATION**			OBJECTIVE: Verify output voltage regulation with different load conditions

UUT must be powered at 28Vin and load condition as in the following table:

Output	Voltage (V)	Min Current (mA)	Max Current (mA)
DPU Electronic	+5	1000	3.500
DPU Electronic	+15	0	100
DPU Electronic	-15	0	250
DPU Electronic	+2,5	0	200
HIFI	5,6	0	240
HIFI	16	0	190
HIFI	-16	0	150
HIFI	8	0	350
HIFI	18	0	330
HIFI	-18	0	230

UUT DATA : **Model** **Item** **C.I.** **S/N**

STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
				INSTRUMENTATION: Voltmeter, Ammeter
F1.1	Set the outlet +5VD at Imax			
F1.2	Set the other outlets at Imin			
F1.3	Measure voltage across outlet +5VD (DPU)	Vmin = 4.75V Vmax = 5.25V		
F1.4	Set the outlet +5VD at Imin			
F1.5	Set the other outlets at Imax			
F1.6	Measure voltage across outlet +5VD(DPU)	Vmin = 4.75V Vmax = 5.25V		
F1.7	Set the outlet +15VA at Imax			
F1.8	Set the other outlets at Imin			
F1.9	Measure voltage across outlet +15VA (DPU)	Vmin = 14.25V Vmax = 15.75V		
F1.10	Set the outlet +15VA at Imin			
F1.11	Set the other outlets at Imax			
F1.12	Measure voltage across outlet +15VA (DPU)	Vmin = 14.25V Vmax = 15.75V		
F1.13	Set the outlet -15VA at Imax			
F1.14	Set the other outlets at Imin			
F1.15	Measure voltage across outlet -15VA (DPU)	Vmin = -15.75V Vmax = -14.25V		
F1.16	Set the outlet -15VA at Imin			
F1.17	Set the other outlets at Imax			
F1.18	Measure voltage across outlet -15VA(DPU)	Vmin = -15.75V Vmax = -14.25V		

DATE:	TEST CONDUCTOR	QA	CUSTOMER

UUT DATA : **Model** **Item** **C.I.** **S/N**

STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F1.19	Set the outlet +2.5VFPGA at Imax			
F1.20	Set the other outlets at Imin			
F1.21	Measure voltage across outlet +2.5VFPGA(DPU)	Vmin = 2.375V Vmax = 2.625V		
F1.22	Set the outlet +2.5VFPGA at Imin			
F1.23	Set the other outlets at Imax			
F1.24	Measure voltage across outlet +2.5VFPGA (DPU)	Vmin = 2.375V Vmax = 2.625V		
F1.25	Set the outlet +5.6V_PL_OUT at Imax			
F1.26	Set the other outlets at Imin			
F1.27	Measure voltage across outlet +5.6V_PL_OUT	Vmin = 5.5V Vmax = 5.8V		
F1.28	Set the outlet +5.6V_PL_OUT at Imin			
F1.29	Set the other outlets at Imax			
F1.30	Measure voltage across outlet +5.6V_PL_OUT	Vmin = 5.5V Vmax = 5.8V		
F1.31	Set the outlet +16V_PL_OUT at Imax			
F1.32	Set the other outlets at Imin			
F1.33	Measure voltage across outlet +16V_PL_OUT	Vmin = +15.6V Vmax = +16.4V		
F1.34	Set the outlet +16V_PL_OUT at Imin			
F1.35	Set the other outlets at Imax			
F1.36	Measure voltage across outlet +16V_PL_OUT	Vmin = +15.6V Vmax = +16.4V		
F1.37	Set the outlet -16V_PL_OUT at Imax			

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F1.38	Set the other outlets at Imin			
F1.39	Measure voltage across outlet -16V_PL_OUT	Vmin = -16.4V Vmax = -15.6V		
F1.40	Set the outlet -16V_PL_OUT at Imin			
F1.41	Set the other outlets at Imax			
F1.42	Measure voltage across outlet -16V_PL_OUT	Vmin = -16.4V Vmax = -15.6V		
F1.43	Set the outlet +8V_PL_OUT at Imax			
F1.44	Set the other outlets at Imin			
F1.45	Measure voltage across outlet +8V_PL_OUT	Vmin = +7V Vmax = +9V		
F1.46	Set the outlet +8V_PL_OUT at Imin			
F1.47	Set the other outlets at Imax			
F1.48	Measure voltage across outlet +8V_PL_OUT	Vmin = +7V Vmax = +9V		
F1.49	Set the outlet +18V_PL_OUT at Imax			
F1.50	Set the other outlets at Imin			
F1.51	Measure voltage across outlet +18V_PL_OUT	Vmin = +17V Vmax = +20V		
F1.52	Set the outlet +18V_PL_OUT at Imin			
F1.53	Set the other outlets at Imax			
F1.54	Measure voltage across outlet +18V_PL_OUT	Vmin = +17V Vmax = +20V		
F1.55	Set the outlet -18V_PL_OUT at Imax			
F1.56	Set the other outlets at Imin			

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE		EXPECTED VALUE	MEASURED VALUE	REMARKS
F1.57	Measure voltage across outlet -18V_PL_OUT		Vmin = -17V Vmax = -20V		
F1.58	Set the outlet -18V_PL_OUT at Imin				
F1.59	Set the other outlets at Imax				
F1.60	Measure voltage across outlet -18V_PL_OUT		Vmin = -17V Vmax = -20V		
F2	**OUTPUT VOLTAGE REGULATION/LINE REGULATION**				OBJECTIVE: Verify output voltage regulation with different line conditions INSTRUMENTATION: Voltmeter, Ammeter
F2.1	Power the board through the input connectors at 26V				
F2.2	Set all outputs to Imax				
F2.3	Measure voltage across outlet +5VD		Vmin = 4.75V Vmax = 5.25V		
F2.4	Measure voltage across outlet +15VA		Vmin = 14.25V Vmax = 15.75V		

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F2.5	Measure voltage across outlet -15VA	Vmin = -15.75V Vmax = -14.25V		
F2.6	Measure voltage across outlet +2.5VFPGA	Vmin = 2.375V Vmax = 2.625V		
F2.7	Measure voltage across outlet +5.6V_PL_OUT	Vmin = 5.5V Vmax = 5.8V		
F2.8	Measure voltage across outlet +16V_PL_OUT	Vmin = +15.6V Vmax = +16.4V		
F2.9	Measure voltage across outlet -16V_PL_OUT	Vmin = -16.4V Vmax = -15.6V		
F2.10	Measure voltage across outlet +8V_PL_OUT	Vmin = +7V Vmax = +9V		
F2.11	Measure voltage across outlet +18V_PL_OUT	Vmin = +17V Vmax = +20V		
F2.12	Measure voltage across outlet -18V_PL_OUT	Vmin = -17V Vmax = -20V		
F2.13	Power the board through the input connectors at 29V			
F2.14	Set all of outputs to Imax			
F2.16	Measure voltage across outlet +5VD	Vmin = 4.75V Vmax = 5.25V		
F2.17	Measure voltage across outlet +15VA	Vmin = 14.25V Vmax = 15.75V		
F2.18	Measure voltage across outlet -15VA	Vmin = -15.75V Vmax = -14.25V		
F2.19	Measure voltage across outlet +2.5VFPGA	Vmin = 2.375V Vmax = 2.625V		
F2.20	Measure voltage across outlet +5.6V_PL_OUT	Vmin = 5.5V Vmax = 5.8V		
F2.21	Measure voltage across outlet +16V_PL_OUT	Vmin = +15.6V		

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UUT DATA :	**Model**	**Item**	**C.I.**		**S/N**
STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE		EXPECTED VALUE	MEASURED VALUE	REMARKS
			Vmax = +16.4V		
F2.22	Measure voltage across outlet -16V_PL_OUT		Vmin = -16.4V Vmax = -15.6V		
F2.23	Measure voltage across outlet +8V_PL_OUT		Vmin = +7V Vmax = +9V		
F2.24	Measure voltage across outlet +18V_PL_OUT		Vmin = +17V Vmax = +20V		
F2.25	Measure voltage across outlet -18V_PL_OUT		Vmin = -17V Vmax = -20V		
F3	**RIPPLE AND SPIKES**				OBJECTIVE: Verify output voltage spikes and ripple INSTRUMENTATION: Oscilloscope. Spikes measurements shall be performed with a

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F3.1	Load the board with a dummy load. The dummy load shall sink a DC load current of Imax in parallel with a 20 uF capacitance in series with a 10 Ohm resistance			50MHz BW Oscilloscope. For ripple measurements, a 2MHz BW limitation shall be introduced.
F3.2	Measure ripple of outlet +5VD in differential mode	200mVpp		
F3.3	Measure spikes of outlet +5VD in differential mode	100mVpp		
F3.4	Measure ripple of outlet +15VA in differential mode	400mVpp		
F3.5	Measure spikes of outlet +15VA in differential mode	200mVpp		
F3.6	Measure ripple of outlet -15VA in differential mode	400mVpp		
F3.7	Measure spikes of outlet -15VA in differential mode	200mVpp		
F3.8	Measure ripple of outlet +2.5VFPGA in differential mode	200mVpp		
F3.9	Measure spikes of outlet +2.5VFPGA in differential mode	100mVpp		
F3.10	Measure ripple of outlet +5.6V_PL_OUT in differential mode	140mVpp		
F3.11	Measure spikes of outlet +5.6V_PL_OUT in differential mode	100mVpp		
F3.12	Measure ripple of outlet +16V_PL_OUT in differential mode	140mVpp		
F3.13	Measure spikes of outlet +16V_PL_OUT in differential mode	100mVpp		
F3.14	Measure ripple of outlet -16V_PL_OUT in differential mode	140mVpp		
F3.15	Measure spikes of outlet -16V_PL_OUT in differential mode	100mVpp		
F3.16	Measure ripple of outlet +8V_PL_OUT in differential mode	850mVpp		
F3.17	Measure spikes of outlet +8V_PL_OUT in differential mode	200mVpp		
F3.18	Measure ripple of outlet +18V_PL_OUT in differential mode	1400mVpp		

UUT DATA :	**Model**	**Item**	**C.I.**	**S/N**

STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F3.19	Measure spikes of outlet +18V_PL_OUT in differential mode	200mVpp		
F3.20	Measure ripple of outlet -18V_PL_OUT in differential mode	1400mVpp		
F3.21	Measure spikes of outlet -18V_PL_OUT in differential mode	200mVpp		

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UUT DATA :	Model	Item	C.I.	S/N

STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F4	**EFFICIENCY AND POWER CONSUMPTION**			OBJECTIVE: Verify efficiency of the DC/DC board
	UUT must be powered at Vin =28V			INSTRUMENTATION: Voltmeter, Amperometer r
F4.1	Set at Imax all outputs as following table:			Full load is obtained only in DPU+PL Version
	Measure input current	<2.6A and >1.9A		DPU+PL Version
		<1.5A and >0.9A		DPU Version
	Calculate Pin=Vin*Iin	<72.8W and >67.2W		DPU+PL Version
		<42W and >28W		DPU Version

Output	Voltage (V)	Max Current (mA)
DPU Electronic	+5	3.500
DPU Electronic	+15	100
DPU Electronic	-15	250
DPU Electronic	+2,5	200
HIFI	5,6	240
HIFI	16	190
HIFI	-16	150
HIFI	8	350
HIFI	18	330
HIFI	-18	230

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE		EXPECTED VALUE	MEASURED VALUE	REMARKS
F4.2	Calculate Pout as the sum of all power outputs		<50W and >40W		DPU+PL Version
			<25W and >20W		DPU Version
F4.3	Calculate DC/DC Converter efficiency with Efficiency is given by: $Eff = \frac{Pout}{Pin} * 100$ [%]		>70%		DPU+PL Version
			>65%		DPU Version

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS	
F5	**INRUSH CURRENT**			OBJECTIVE: Verify the inrush current INSTRUMENTATION: Multimeter, Oscilloscope, Current Probe	
F5.1	Place the current probe on positive power lead of the 28V Main Bus				
F5.2	Set Vbus at 29V				
F5.3	Set at Imax all outlets				
F5.4	Switch ON the Main Bus				
F5.5	Make hardcopy of the inrush current	See Remark		Note: The DC/DC board inrush current due to DC/DC board switch on shall be limited to 1.5 times the DC/DC input peak current, specified as 1.2 the nominal current. The duration of the inrush peak shall not exceed 0.5ms The rate of change (slope) of the inrush current shall not exceed 50mA/usec	
F5.6	Set Vbus at 26V				
F5.7	Set at Imax all outlets				
F5.8	Switch ON the Main Bus				
F5.9	Make hardcopy of the inrush current	See Remark		Note: The DC/DC board inrush current due to DC/DC board switch on shall be limited to 1.5 times the DC/DC input peak current, specified as 1.2 the nominal current. The duration of the inrush peak shall not exceed 0.5ms	

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE		EXPECTED VALUE	MEASURED VALUE	REMARKS
					The rate of change (slope) of the inrush current shall not exceed 50mA/usec
F6	**INPUT IMPEDANCE**				OBJECTIVE: Verify input impedance of DC/DC board INSTRUMENTATION: Oscilloscope, gain phase Analyzer with test set-up of annex 1A
F6.1	The measurement of input impedance of the DC/DC board shall be performed with a set-up as shown in ANNEX 1				
F6.2	Set at Imax all outputs				
F6.3	Measure the input impedance of the DC/DC board and annex the plot				
F6.4	Verify that impedance measurement is 6dB higher than the power bus impedance mask.		OK		NOTE: The power bus impedance mask is shown in the ANNEX 2

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE		EXPECTED VALUE	MEASURED VALUE	REMARKS
F7	**INPUT PROTECTION**				OBJECTIVE: Verify input protection INSTRUMENTATION: Voltmeter
F7.1	Starting from 28V decrease the input voltage power bus and verify that DC/DC converter output voltages switch OFF.		>23V < 25V		
F7.2	Increase than input voltage and verify that DC-DC properly works		>23V < 25V		

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F8	**DPU OUTPUT PROTECTIONS**			OBJECTIVE: Verify DPU output protections INSTRUMENTATION: Voltmeter, Ammeter
F8.1	Check the over-voltage protection (OVP) on +5VD outlet (this test will be done before the board closure)			
F8.2	Power on the UUT at 28Vdc and maximum load: -Via dedicated jumper, placed in series to R158 (+5VD output voltage sense), connect a voltage generator referred to DGND .			
F8.3	Starting from 0V increase the voltage until the protection voltage value is reached (controller shut-down and all outlet switch to OFF) and report the voltage value. Verify that the input power consumption is lower than 2.8W.	5.5V		
F8.7	Check the over-current protections on +5VD outlet.			
F8.8	The test shall be performed as follow:			
F8.9	-Connect to the +5VD outlet a variable load.			
F8.10	-Place the current probe on positive power lead of the +5VD outlet. -By reducing the load resistance increase the current through the +5VD outlet.			
F8.11	When the OVC protection threshold is reached the DC/DC outlets switch to OFF and the power consumption became lower than 2,8W.	2W (DPU+PL) 1W (DPU)		
F8.12	Verify that the measured over-current protection values is as expected.	4000±10%mA TBC		
F8.13	Check the over-current protections on +15VA outlet .			

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F8.14	The test shall be performed in the following manner:			
F8.15	-Connect to the +15VA outlet a variable load.			
F8.16	-Place the current probe on positive power lead of the +15VA outlet.			
	-By reducing the load resistance increase the current across the +15VA outlet .			
F8.17	When the OVC protection threshold is reached the DC/DC outlets switch to OFF and the power consumption became lower than 2,8W.	2W (DPU+PL) 1W (DPU)		
F8.18	Verify that the measured over-current protection values is as expected.	200±10%mA		
F8.19	Check the over-current protections on -15VA outlet.			
F8.20	The test shall be performed in the following manner:			
F8.21	-Connect to the -15VA outlet a variable load.			
F8.22	-Place the current probe on negative power lead of the -15VA outlet.			
	-By reducing the load resistance increase the current across the -15VA outlet .			
F8.23	When the OVC protection threshold is reached the DC/DC outlets switch to OFF and the power consumption became lower than 2,8W.	2W (DPU+PL) 1W (DPU)		
F8.24	Verify that the measured over-current protection values is as expected.	500±10%mA		

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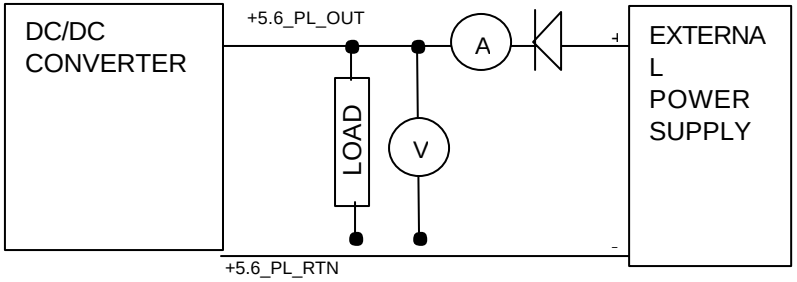
STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F9	**REGULATED PL OUTPUTS PROTECTIONS (IS)** Check the over-voltage protections with crow-bar on +5.6V_PL_OUT outlet using the following set-up			OBJECTIVE: Verify the regulated output protections INSTRUMENTATION: Voltmeter, Ammeter
F9.1				

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
	Power on the UUT with 28V input . Connect all output to the loads. By means of external power voltage generator (limited to 2Amax)simulate an Over Voltage condition on the output. Starting from 0V increase the external voltage generator to about 6V on outlet DC/DC pin. Disconnect the output voltage generator and verify that the output is in on condition (5,6V) Reconnect the generator at 0V Increase the voltage to about 6,5V (over voltage threshold).and when the current flown into outlet line (due to shunt transistor of the outlet) switch off the external generator and report the voltage and current values. Remove the external power supply and verify that the output voltage is equal to 0V. Verify that all other outputs properly work	6.5±5%V <2A		
F9.2	Check the over-voltage protections on +16V_PL_OUT outlet			
F9.3	Power on the UUT with 28V input . Connect all output to the loads. By means of external power voltage generator (limited to 100mA)simulate an Over Voltage condition on the output. Starting from 0V increase the external voltage generator to about 16,3V on outlet DC/DC pin. Disconnect the output voltage generator and verify that the output is in on condition (16V) Reconnect the generator at 0V Increase the voltage to 18V (over voltage threshold) ,and switch off the external generator . Remove the external power supply and verify that the output voltage is equal to 0V. Verify that all other outputs properly work	Ok 17.2±5%V		

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F9.4	Check the over-voltage protections on -16V_PL_OUT outlet Power on the UUT with 28V input . Connect all output to the loads. By means of external power voltage generator (limited to 100mA)simulate an Over Voltage condition on the output. Starting from 0V increase the external voltage generator to about -16,3V on outlet DC/DC pin.			
F9.5	Disconnect the output voltage generator and verify that the output is in on condition (-16V) Reconnect the generator at 0V Increase the voltage to - 18V (over voltage threshold) ,and switch off the external generator . Remove the external power supply and verify that the output voltage is equal to 0V. Verify that all other outputs properly work	-17.2±5%V		
F9.6	Check the current limitation on +5.6V_PL_OUT outlet.			
F9.7	The test shall be performed in the following manner:			
F9.8	-Connect to the +5.6V _PL_OUT outlet a variable load.			
F9.9	-Place the current probe on negative power lead of the +5.6V _PL_OUT outlet.			
F9.9	-By reducing the load resistance increase the current through the +5.6V _PL_OUT outlet.			
F9.10	Verify that the measured current limitation value is as expected.	285±5%mA		
F9.11	Check the current limitation on +16V_PL_OUT outlet.			
F9.12	The test shall be performed in the following manner:			
F9.13	-Connect to the +16V_PL_OUT outlet a variable load.			
F9.14	-Place the current probe on negative power lead of the +16V_PL_OUT outlet.			
F9.15	-By reducing the load resistance increase the current through the +16V_PL_OUT outlet.			
F9.16	Verify that the measured current limitation value is as expected.	285±5%mA		
F9.17	Check the current limitation on -16V_PL_OUT outlet.			
F9.18	The test shall be performed in the following manner:			

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F9.19	-Connect to the -16V_PL_OUT outlet a variable load.			
F9.20	-Place the current probe on negative power lead of the -16V_PL_OUT outlet.			
F9.21	-By reducing the load resistance increase the current through the -16V_PL_OUT outlet.			
F9.22	Verify that the measured current limitation value is as expected.	285±5%mA		
F10	**VOLTAGE MONITORS**			OBJECTIVE: Verify voltage monitors INSTRUMENTATION: Voltmeter
F10.1	Check the telemetry of +5V_MNT outlet			
F10.2	Measurement has to be performed between pin 42 of connector P2B and pin 43f connector P2B	4.17±5%		Notes: Scale of telemetry: 0V⇒ 0V, 6V⇒ 5V Accuracy: ±5%
F10.3	Check the telemetry of +15V_MNT outlet			
F10.4	Measurement has to be performed between pin 74 of connector P2C and pin 75 connector P2C	4.17±5%		Notes: Scale of telemetry: 0V⇒ 0V, 18V⇒5V

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE		EXPECTED VALUE	MEASURED VALUE	REMARKS
					Accuracy: ±5%
F10.5	Check the telemetry of -15V_MNT outlet				
					Notes:
F10.6	Measurement has to be performed between pin 12 of connector P2A and pin 13f connector P2A		4.17±5%		Scale of telemetry: 0V⇒ 0V, -18V⇒ 5V
					Accuracy: ±5%
F11	**TEMPERATURE MONITOR**				OBJECTIVE: Verify temperature monitor
					INSTRUMENTATION: Power supply, multimeter
F11.1	Check the telemetry of +TEMP_MNT				
					Notes:
	Set limitation current of power supply to 50mA				Scale of telemetry: -50°C⇒ 0V, +80°C⇒ 5V
					Accuracy: ±5%
	Measure resistance Rmis between TP1 and TP3		Rmis		
	Supply TP1 (Positive) and TP3(Negative) with the following voltage: $V = (273 - 50) * Rmis$				
F11.2	Measure voltage between pin 44 and 45 of connector P2B		0±96mV		-50°C Case

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
	Supply TP1 (Positive) and TP3(Negative) with the following voltage V: $V = (273 + 80) * Rmis$			
F11.2	Measure voltage between pin 44 and 45 of connector P2B	5V±154mV		80°C Case
F12	**CE ON INPUT POWER LINE; FREQUENCY DOMAIN, DIFFERENTIAL MODE, NB**			OBJECTIVE: Verify the conducted emission differential mode on input power line INSTRUMENTATION: Spectrum analyzer with preselector
F12.1	The measurement shall be performed with a test set-up as shown on ANNEX 3			
F12.2	Set the outputs at Imax			
F12.3	Take measurements of the ambient noise (positive input line) and make hardcopy			

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE		EXPECTED VALUE	MEASURED VALUE	REMARKS
F12.4	Switch on the UUT, repeat the measurements and make hardcopy (positive input line)				
F12.5	Verify that the measurements are as expected		OK		
F12.6	Set the outputs at Imax				
F12.7	Take measurements of the ambient noise (return line) and make hardcopy				
F12.8	Switch on the UUT, repeat the measurements and make hardcopy (return line)				
					NOTE: Narrow-Band conducted emission Differential Mode in the frequency range 30Hz 50MHz generated by the DC/DC board on the input power line shall not exceed the following adjustable limit:
F13.9	Verify that the measurements are as expected		OK		A) For Nominal DC input current less than 1A, use the curve in ANNEX 4 B) For Nominal DC input current greater than 1A, increase the level (in dBmA) of the curve in ANNEX 4 by 10*Log[I (A)]. I(A) is the nominal input current in Ampere.
F13	**CE ON INPUT POWER LINE; FREQUENCY DOMAIN, COMMON MODE, NB**				OBJECTIVE: Verify the conducted emission common mode on input power line INSTRUMENTATION: Spectrum analyzer with preselector
F13.1	The measurement shall be performed with a test set-up as shown in ANNEX 5				

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STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE		EXPECTED VALUE	MEASURED VALUE	REMARKS
F13.2	Set the outputs at Imax				
F13.3	Take measurements of the ambient noise and make hardcopy				
F13.4	Switch on the UUT, repeat the measurements and make hardcopy				NOTE: Narrow-Band conducted emission Differential Mode in the frequency range 10kHz 50MHz generated by the DC/DC board on the input power line shall not exceed the following adjustable limit:
F13.5	Verify that the measurements are as expected				A) For Nominal DC input current less than 1A, use the curve in ANNEX 6 B) For Nominal DC input current greater than 1A, increase the level (in dBmA) of the curve in ANNEX 6 by 10*Log[I (A)]. I(A) is the nominal input current in Ampere.
F14	**CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE**				OBJECTIVE: Verify current ripple on input power line INSTRUMENTATION: Oscilloscope
F14.1	The measurement shall be performed with a test set-up as shown in ANNEX 7				

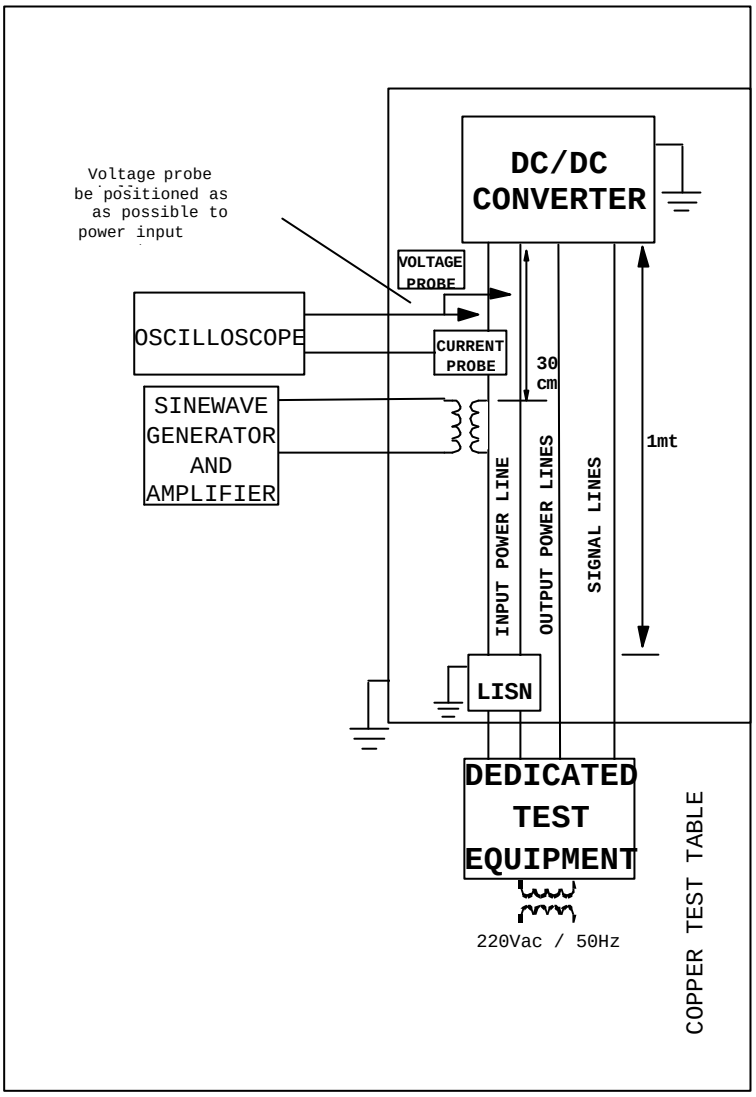
UUT DATA :	Model	Item	C.I.	S/N

STEP n°	TEST SEQUENCE F14: CURRENT RIPPLE, TIME DOMAIN, DIFFERENTIAL MODE	EXPECTED VALUE	MEASURED VALUE	REMARKS
F14.2	Set the outputs at Imax			
F14.3	Place the current probe on positive power lead of the power line			
F14.4	Record the current ripple and make hardcopy			
F14.5	Place the current probe on return power lead of the power line.			
F14.6	Record the current ripple and make hardcopy			
F14.7	Verify that the measurements are as expected			NOTE: Differential mode, time domain current ripple and spikes on the input power line of the DC/DC board shall not exceed the following limits: A) For nominal DC input current less than 1A: Ripple: less than 20mApp. Spikes, including ripple: less than 60mA pp B) For nominal DC input current greater than 1A: Ripple: multiply 20mApp by a factor $\sqrt{I(A)}$, I(A) is the nominal input current in Ampere Spikes, including ripple: multiply 60mApp by a factor $\sqrt{I(A)}$, I(A) is the nominal input current in Ampere.

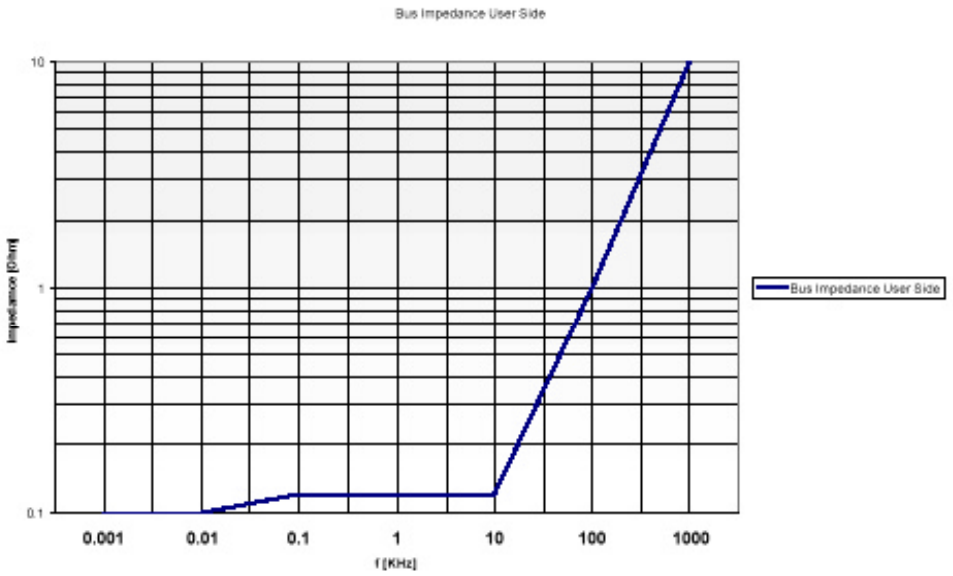
DATE:	TEST CONDUCTOR	QA	CUSTOMER

11. ANNEX TO THE PROCEDURE

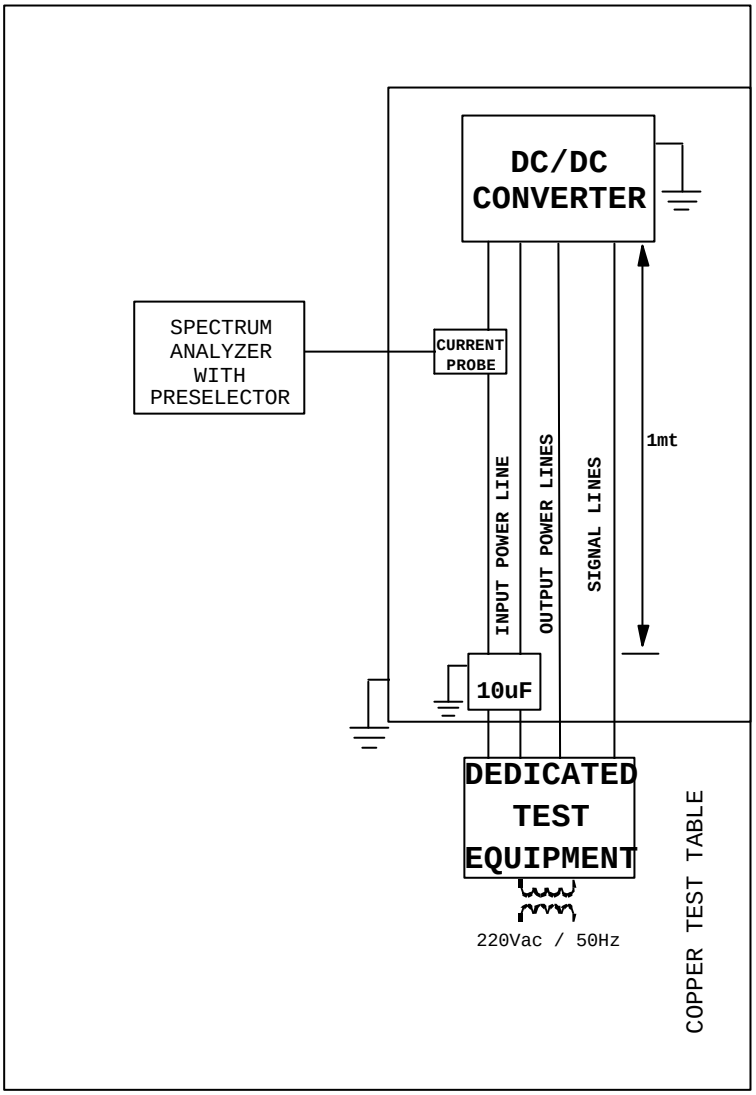
11.1 ANNEX 1: TEST SET UP FOR INPUT IMPEDANCE MEASUREMENT



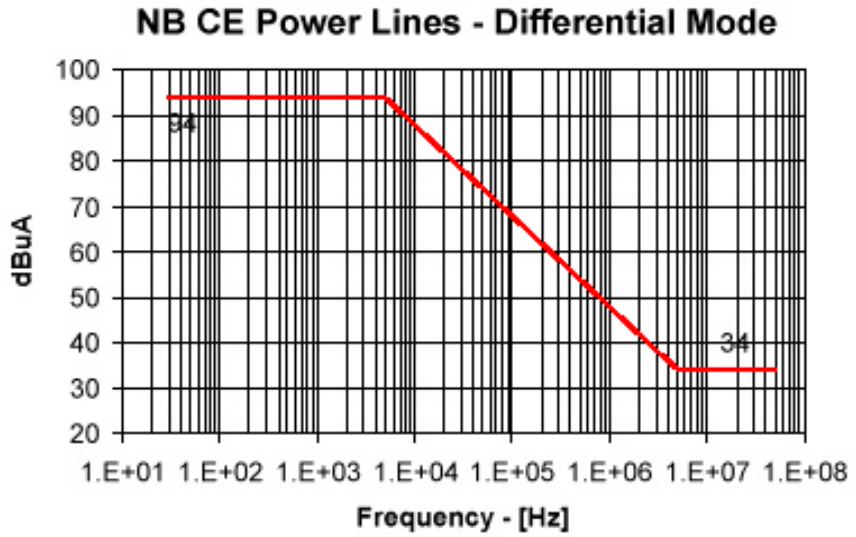
11.2 ANNEX 2: POWER BUS IMPEDANCE



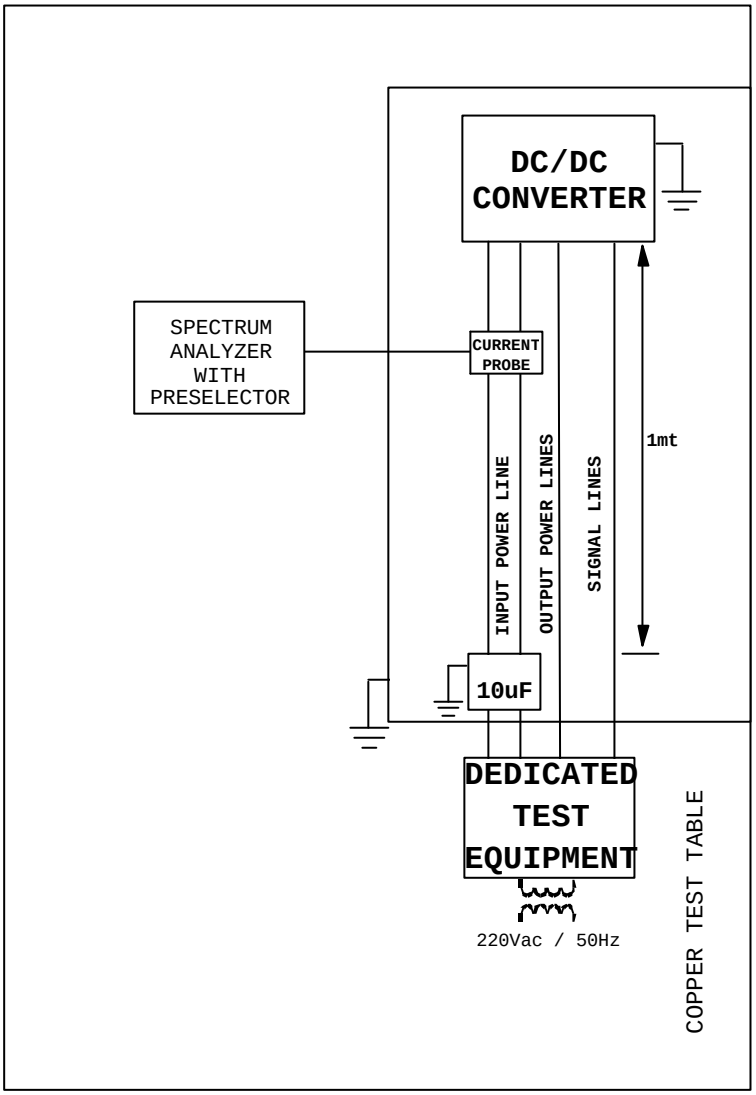
11.3 ANNEX 3: TEST SET UP FOR CONDUCED EMISSION FREQUENCY DOMAIN DM



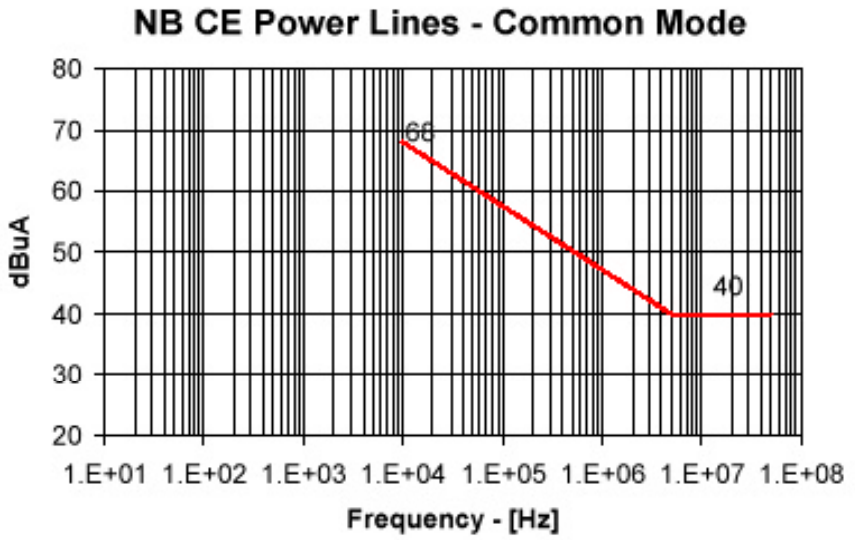
11.4 ANNEX 4: LIMIT FOR CEP-DIFFERENTIAL MODE



11.5 ANNEX 5: TEST SET UP FOR CONDUCED EMISSION FREQUENCY DOMAIN CM



11.6 ANNEX 6: NB CE POWER LINES-COMMON MODE



11.7 ANNEX 7: TEST SET UP FOR CONDUCED EMISSION TIME DOMAIN