

A note on the required reliability for the DCU LIA Channels

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Introduction

The large number of pixels in any one array of the SPIRE instrument means that failure or degraded performance in any one channel does not lead to commensurate degradation in the overall instrument performance. In this note I analyse the end to end detection system in terms of the items where a failure might occur with a view to assessing what reliability is required – in terms of a probability of failure over the lifetime of the mission – in the warm electronics part of the system. Of especial interest is the reliability required for the amplifier channels where there are a large number of duplicated circuits with potentially large cost implications of using high reliability electronics parts.

The detector system

Figure 1 shows a diagrammatic representation of the detector system. There are five bolometer arrays (BDAs) in SPIRE – three in the photometer and two in the spectrometer. These are cooled to 300 mK by a single sorption cooler linked to the detectors by a thermal strap. Both the cooler and the “300-mK system” are single point failures within SPIRE and their design and implementation reflect this. Each “side” of the instrument has a separate bias supply (BBIAS) for the BDAs located in the warm electronics unit. In figure 1 I show the photometer side of the instrument only – the analysis applies equally to the spectrometer.

From the detectors the signal is taken via a harness (JFHAR) to the JFET unit on the outside of the FPU. This harness has connectors at the detectors; connectors at the FPU wall and connectors at the JFET box. The JFETs are arranged in modules (MOD) addressing 24 detector channels. Each MOD has its own separately switched supply rails from the warm electronics (JBIAS). The supplies to the JFET modules arrive at the JFET boxes via the system cryoharness (CHAR) and are distributed through a back harness on the JFET box (BHAR). Similarly the detector bias supplies arrive at the JFET boxes via the CHAR where they are filtered and passed into the FPU through the JFHAR. To ensure robustness through both the CHAR and the JFHAR the bias supplies to the detectors are double wired – i.e. two pins at each connector and two physically separate wires carry each of the bias connections.

The output of the JFETs is taken to the warm electronics units via the CHAR. This has connectors at the JFET units; the Cryostat Vacuum Vessel (CVV) and on the warm electronics unit. It may be that an extra set of connectors is used at the warm end to transfer between the cryoharness (made in stainless steel or brass) to the warm electronics units through a more flexible copper harness. This would ease the integration of the warm electronics in the Service Module (SVM).

The Detector Control Unit (DCU) is arranged for the photometer channels with 16 Lock In Amplifiers (LIA) per card and each card contains a 16:1 multiplexer. These cards are non redundant. The LIAs are addressed by an interface and control FPGA that controls further multiplexers that take either 3 or 6 LIA cards into an ADC. This FPGA controls the sampling rate and transmission of data to the Data Processing Unit (DPU); the generation of the bias and reference waveforms and the receipt and decoding of commands from the DPU. The 3 or 6:1 mux; the ADCs; the bias generators and the FPGA are all on cold redundant sub-units. The DPU is the unit with overall control of the instrument and is again fully cold redundant with fully redundant interfaces to the DCU through a fully redundant part of the WIH.

The DCU is powered from a power supply unit (PSU) via a power distribution unit (PDU) both of which are housed in a physically separate box – the Focal plane Control Unit (FCU). They are connected through the warm interconnect harness (WIH). The PSU and PDU are fully cold redundant and connected to the DCU through redundant harnesses.

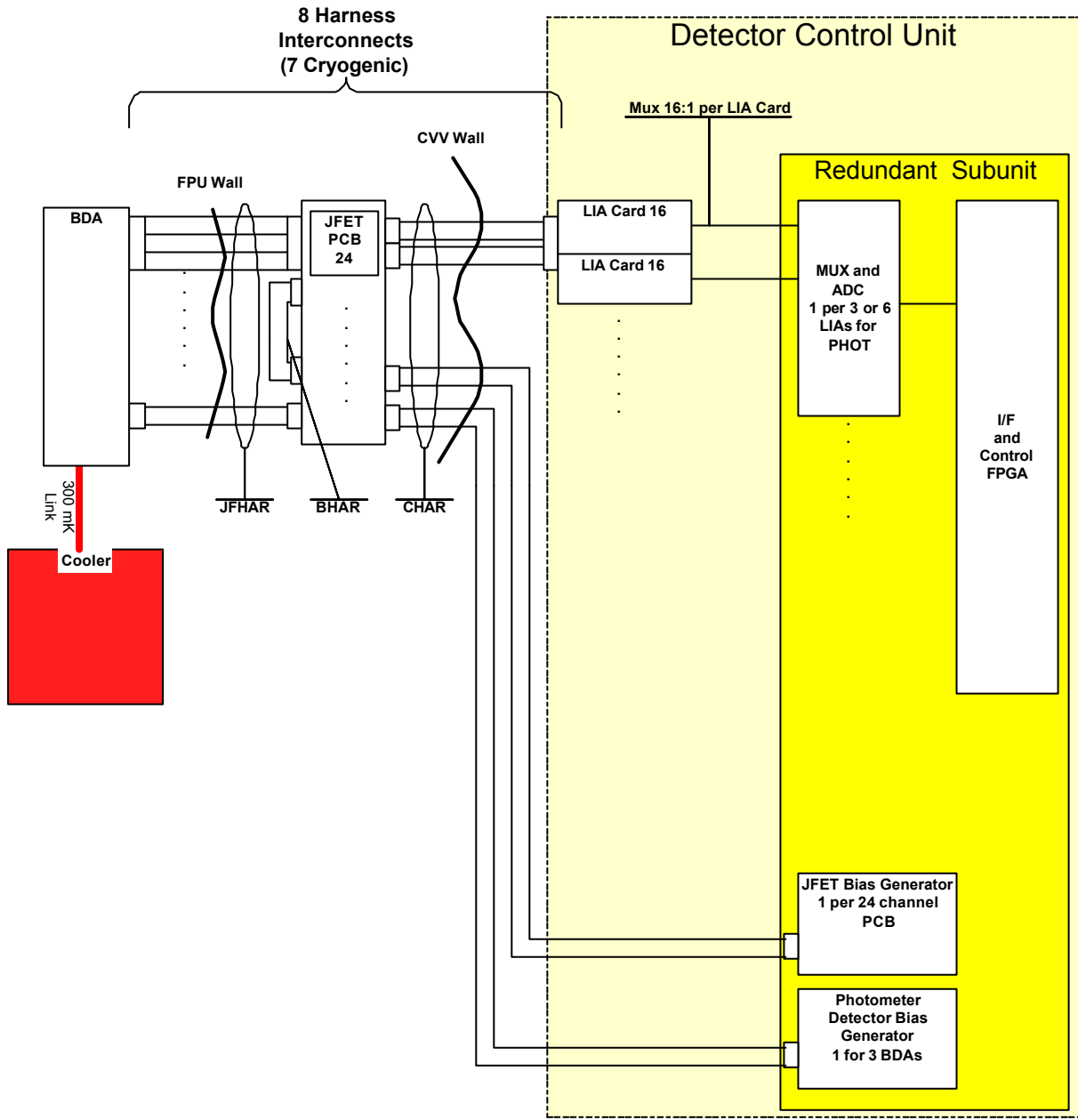


Figure 1: Diagrammatic representation of the detector systems from the warm electronics to the cold detector arrays. The light yellow box represents the entire DCU, the darker yellow inner box that part of it which is fully cold redundant.

Probability of a Single Channel Failure

We can calculate the probability of any one channel failing by taking the product of the probably of any single failure within the chain, thus:

$$(1) P(\text{CHAN}) = P(\text{BDA}) P(\text{BOL}) P(\text{JFET}) P(\text{MOD}) P(\text{CHAR}) P(\text{LIA}) P(\text{MUX}) P(\text{ADC}) P(\text{FPGA}) P(\text{WIH}) P(\text{DPU}) P(\text{PSU})$$

Where P(...) represents the probability of a failure occurring in that part of the system over the lifetime of the mission following launch – or at after such time as we can't do anything about it.

Here we have P(BDA) representing the probability that an entire detector array fails. This can be further broken down as:

$$(2) P(BDA) = P(MECH)_{BDA} \cdot P(BHAR) \cdot P(JFHAR) \cdot P(BBIAS) \cdot P(CHAR) \cdot P(COOL) \cdot P(300MK) \cdot P(FPGA)$$

Where P(MECH)_{BDA} represents the probability of the mechanical failure within the BDA causing its malfunction; P(COOL) the probability of a failure within the ³He cooler (electrical or mechanical) and P(300MK) the probability of a mechanical failure within the system that connects the cooler to the particular BDA. The probability of a single failure within a harness is square rooted here because all the bias connections (i.e. those that may cause the loss of a whole array) are double wired as described above. P(FPGA) - the probability of a failure within the FPGA - comes in here because the same component is used to generate the bias waveform as is used for the interface and control.

The probability of a whole 24 channel JFET modules failing (P(MOD) in equation 1) is given by:

$$(3) P(MOD) = P(MECH)_{MOD} \cdot P(JBIAS) \cdot P(CHAR) \cdot P(BHAR)$$

where again P(MECH)_{MOD} is the probability of a mechanical failure within the JFET unit or the membrane causing the loss of the module.

We can isolate those parts of the system which are delivered by JPL – essentially the cold parts – from the others – thus:

$$(4) P(BDA)_{JPL} = P(MECH)_{BDA} \cdot P(BHAR) \cdot P(JFHAR)$$

$$(5) P(MOD)_{JPL} = P(MECH)_{MOD} \cdot P(BHAR)$$

The failure probability that is associated with the cold units is therefore:

$$(6) P(JPL) = P(BDA)_{JPL} \cdot P(MOD)_{JPL} \cdot P(BOL) \cdot P(JFHAR) \cdot P(JFET)$$

The probability for the rest of the system is given as:

$$(7) P(OTH) = \{P(BBIAS) \cdot P(CHAR) \cdot P(COOL) \cdot P(300MK) \cdot P(FPGA)\} \cdot \{P(JBIAS) \cdot P(CHAR)\} \cdot \{P(CHAR) \cdot P(LIA) \cdot P(MUX) \cdot P(ADC) \cdot P(FPGA) \cdot P(WIH) \cdot P(DPU) \cdot P(PSU)\}$$

We can isolate the DCU signal chain from the other components up to the output of the ADC

$$(8) P(DCUSIG) = P(LIA) \cdot P(MUX) \cdot P(ADC)$$

So combining (6), (7) and (8) we come to

$$(9) P(CHAN) = \frac{P(JPL) \cdot P(BBIAS) \cdot P(COOL) \cdot P(CHAR)^2 \cdot P(JBIAS) \cdot P(FPGA)^2 \cdot P(WIH) \cdot P(DPU)}{P(PSU) \cdot P(DCUSIG)}$$

Estimating the Failure Probabilities

We can estimate the failure probabilities of the non-DCUSIG parts as follows:

P(JPL) – the yield for the cold detector parts up to the output of the JFETs is specified as being >0.9 at delivery to the instrument. Whilst this isn't really a failure probability over the lifetime we could assume that the failures are entirely dominated by "infant mortality" and

treat this figure as if it were a failure probability for the entire instrument build and operation phase.

P(BBIAS) – this is redundant and, because it represents a single point failure for the prime side, it must be inherently reliable. I allocate it a reliability of 0.995.

P(COOL) – this is a single point failure in the SPIRE instrument – many of its parts and the whole of its electronics are redundant. It must be at least 0.999 reliable.

P(CHAR) – This is extremely interesting – despite the use of robust wiring we still find that the cryoharness failure probability enters as a squared term here. To estimate the probability I use the ISO experience where 3 wires (at least) failed on the harness (all failures were open circuit). They were something of the order of 1300 connections (?) in the ISO harness so the failure probability can be estimated as $(1 - 3/1300) = 0.998$.

P(JBIAS) – same as for BBIAS – 0.995

P(FPGA) – this is a multiple function item failure of any function within it represents a single point failure for the prime side. It comes in as a squared term therefore I allocate in a reliability figure of 0.999.

P(WIH) – this is a standard copper spaceflight harness – we should expect no reliability issues here – I allocate it 1

P(DPU) – this represents a single point failure for the prime side – it is specified as having a reliability of 0.995 (in line with all other single point failures on the prime side).

P(PSU) – this has the same status as the DPU – i.e. a single point failure on the prime side – therefore the PSU reliability should be 0.995.

Required Reliability of the LIA Cards

If we denote P(DCUSIG) as X we can write from equation 9:

$$(10) P(\text{CHAN}) = 0.9 \cdot 0.995 \cdot 0.999 \cdot (0.998)^2 \cdot 0.995 \cdot (0.999)^2 \cdot 1 \cdot 0.995 \cdot 0.995 \cdot X$$

$$(11) P(\text{CHAN}) = \{0.9\} \{0.97\} X = 0.87X$$

We see that P(CHAN) can never be better than 0.87. Allowing for a small further loss of reliability - say P(CHAN) = 0.85. That is we allow for 15% of the channels to fail or be severely degraded over the lifetime of the mission, then X = 0.97

We can therefore write from equation 8 and taking the MUX and ADC in the “single point failure for prime side” category:

$$(12) P(\text{LIA}) = 0.97 / \{P(\text{MUX}) P(\text{ADC})\} = 0.97 / \{0.995 \cdot 0.995\} = 0.98$$

I conclude therefore that the LIA cards must be built to reliability standard of 0.98.

Notes in Passing

Two extra things are worthy of note here:

1. The working assumption is that sub-units and units that represent single point failures for a single prime/redundant side are built to a reliability of $0.995^2 = 0.99$ in order to achieve the overall 0.995 system level reliability quoted. Here we have six of these – giving the probability of failure for one side of $(1 - 0.99^6) = 0.06$ – is this sensible/reasonable? It may be that the reasoning is flawed here as the probability of a prime side failure would be an overarching consideration independent of the analysis

carried out in this note.

2. The cryoharness needs to be really very reliable – even on this simple minded analysis we find that a reliability of 0.998 – or 3(ish) failures out of 1400 wires is just about acceptable. If it is worse than this then it will begin to have serious implications for the overall system reliability.