CARLO GAVAZZI SPACE S.p.A.

HSO/FIRST - DPU

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TITLE: HSO/FIRST - DPU MOTHERBOARD SPECIFICATION

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ACRONYM LIST

AD#	Applicable Document number #
ASI	Agenzia Spaziale Italiana
ATP	Authorization to proceed
CGS	Carlo Gavazzi Space SpA
CNR	Consiglio Nazionale delle Ricerche
CPP	Coordinated Part Procurement
DPU	Data Processing Unit
DDC	Data Device Corporation
DPR	Dual Port Ram
EDAC	Error Detector And Corrector
EEPROM	Electrically Erasable Programmable Read Only Memory
EF	Empty FIFO
EM	Engineering Model
EPROM	Erasable Programmable Read Only Memory
EQM	Engineering Qualification Model
FIRST	Far Infra-Red and Sub-millimeter Telescope
FF	Full FIFO
FM	Flight Model
FPGA	Field Programmable Gate Array
FS	Flight Spare
FSDL	Fast Science Data Link
HF	Half Full FIFO
HIFI	Heterodyne Instrument for First
HSO	Herschel Space Observatory
IFSI	Istituto per la Fisica dello Spazio Interplanetario
IF	Interface
LSL	Low Speed Link
OBDH	On Board Data Handling
PA	Product Assurance
PACS	Photoconductor Array Camera and Spectrometer

PCB	Printed Circuit Board
PROM	Programmable Read Only Memory
PL	Payload
RAM	Random Access Memory
RD#	Reference Document number #
SEU	Single Event Upset
S/C	Spacecraft
SPIRE	Spectral and Photometric Imaging Receiver

1 SCOPE

The aim of the present document is to define the specifications of the motherboard developed in the framework of the HSO/FIRST-DPU program.

The design of the motherboard shall be compliant to this document.

2 APPLICABLE DOCUMENTS

[AD1]: CNR.IFSI.2000TR01 “Documento di Specifiche Tecniche per il Contratto delle Data Processing Units del Satellite First dell’ESA” IFSI (Issue: 1 - 15/09/2000)

[AD2]: Technical proposal CGS (Ref. S9-030 November 99)

[AD3]: “Allegato Tecnico al Contratto ASI”

3 REFERENCE DOCUMENTS

[RD1]: First CPU Board Specification DPU-SP-CGS-001, Carlo Gavazzi Space Issue 1 date 11/12/2000

[RD2]: Payload & Spacecraft Interface Board Specification DPU-SP-CGS-002, Carlo Gavazzi Space Issue 1 date 11/12/2000

4 MECHANICAL AND ENVIRONMENTAL CONSTRAINTS

The mechanical and environmental constraints of the motherboard are shown in the Table 1 and Table 2 while its overall weight is specified in the Table 3.

Board size:	TBD
Board thickness:	2.2 mm ± 0.1
Board connectors:	Straight, female, DIN41612 type

Table 1 Mechanical constraints

Operating temperature:	-25 ÷ +45 ºC
Non operating temperature:	-35 ÷ +85 ºC

Table 2 Environmental constraints

Overall weight (max):	600 g (TBC)

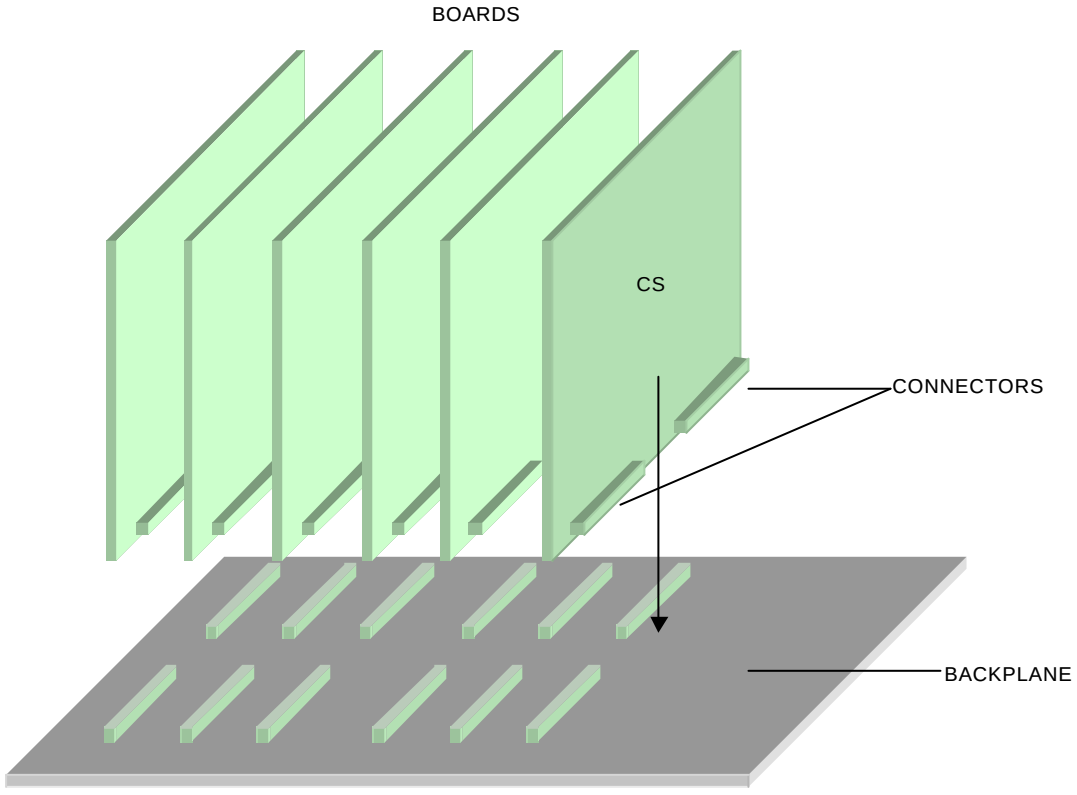
Table 3 Board weight

5 GENERAL DESCRIPTION

The DPU motherboard realises the interconnections between the boards of the DPU and allows the exchange of the signals with the spacecraft and payloads.

DPU is constituted by 3 boards, everyone of which is redundant. Therefore mother board accommodates two indipendent sections constituted by 3 slots. Each board contains two connectors type 96 pin DIN 41612.

The insertion of the six boards with respect to the backplane is vertical, as shown in the Picture 1.



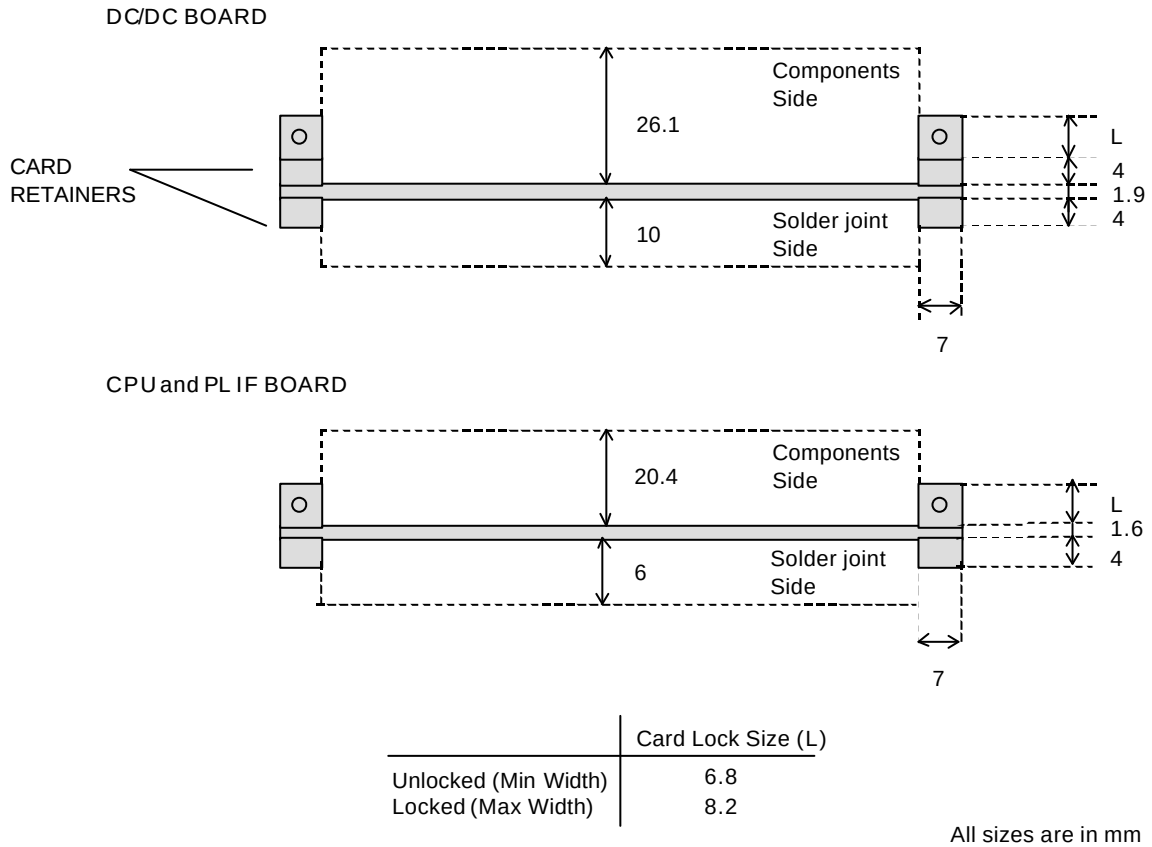
Picture 1 Disposal of the boards with respect to the backplane

The boards shall be inserted in the order specified hereafter (from left to right):

- CPU Board (main)
- PL IF Board (main)
- DC/DC Board (main)
- CPU Board (redundant)
- PL IF Board (redundant)
- DC/DC Board (redundant)

There is no difference between two sections (main/red) and they are in 'cold redundance'; this means that the system supplies power only to main or redundant DPU.

The size of the six boards is double euro; the overall thickness and the space covered by the boards on the backplane are specified in the Picture 2.



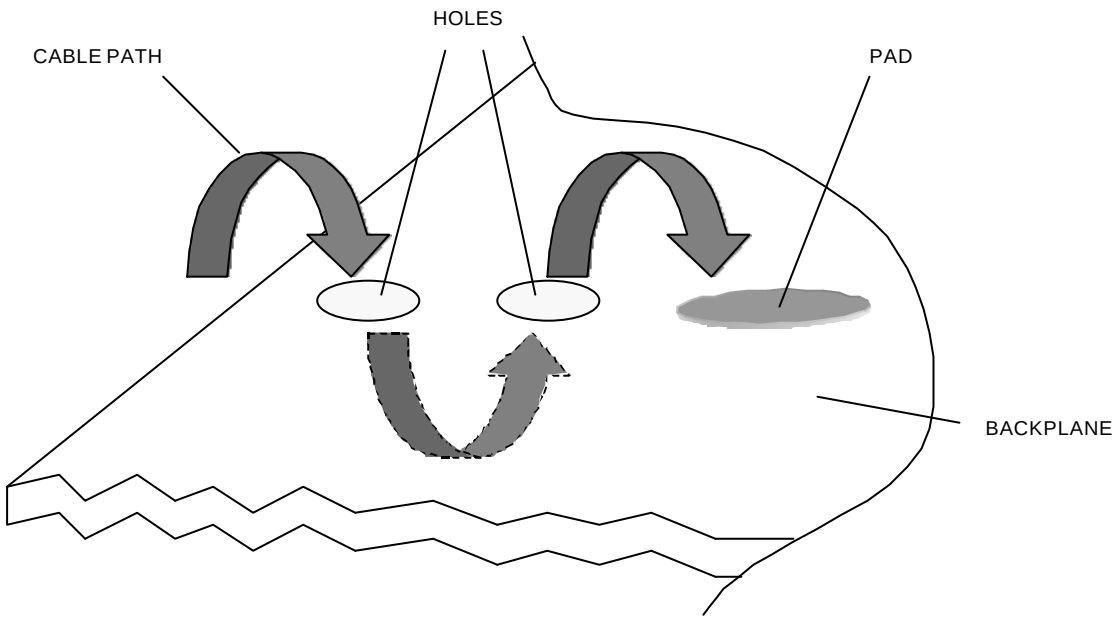
	Card Lock Size (L)
Unlocked (Min Width)	6.8
Locked (Max Width)	8.2

All sizes are in mm

Picture 2 Boards section's sizes

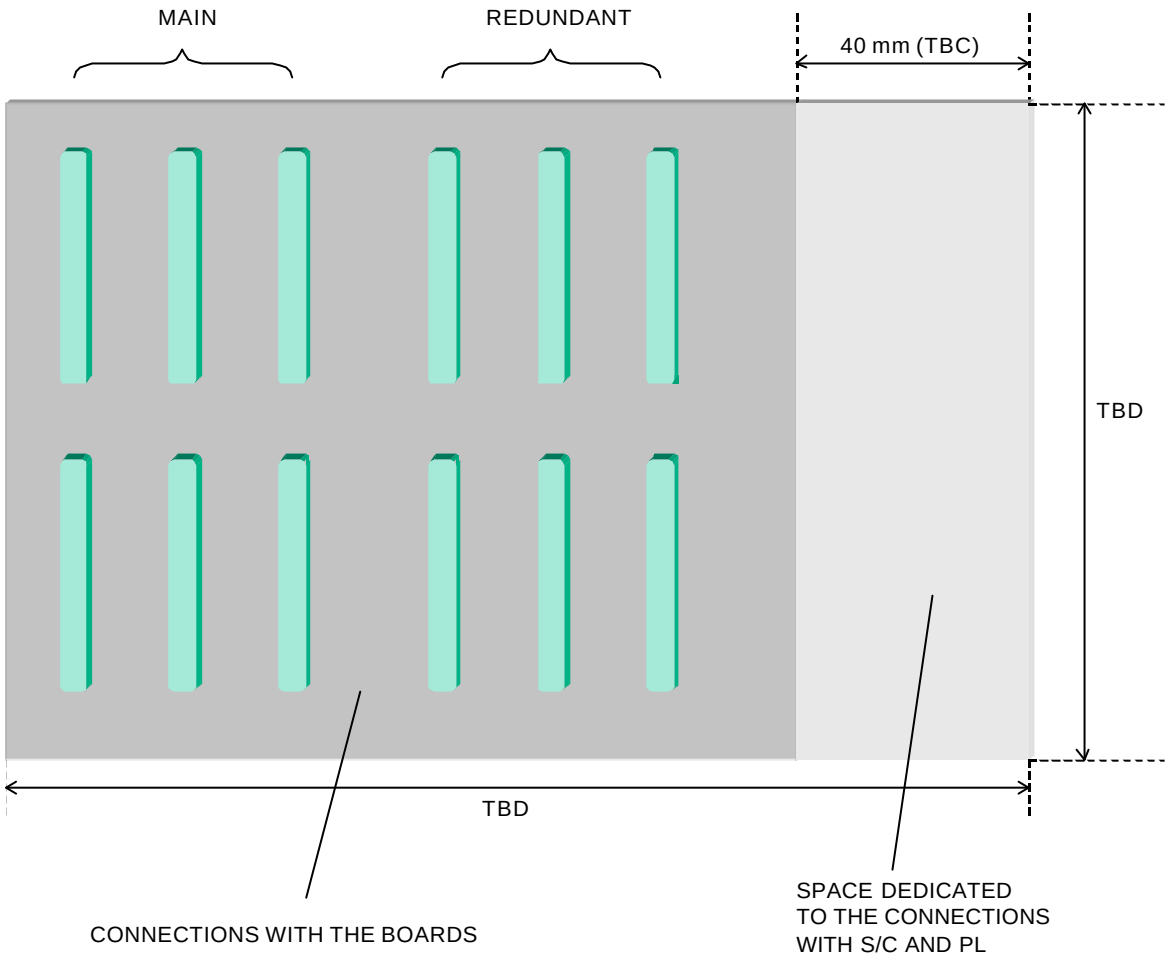
6 SIGNALS DISTRIBUTION

The motherboard supplies the links to the spacecraft and to the payloads for the signals exchange with the CPU. Moreover it receives the input power supply to be sent to DC/DC converter. All these connections are realised by making a double hole and by disposing a metallized area (PAD) on the surface of the backplane.This assures a mechanical anchorage of the cables: they pass through the holes and then are fixed to the PAD, as shown in the Picture 3.



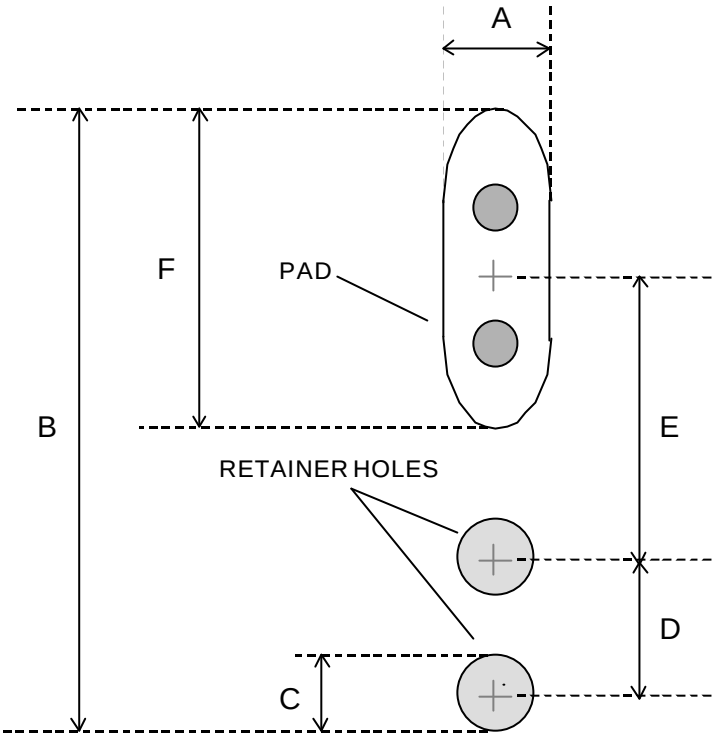
Picture 3 Fixing of the cables on the backplane

The interconnections with the spacecraft and the payloads are disposed on the right side of the motherboard, as shown in the Picture 4.



Picture 4 Mother Board front view

In the following picture the detailed structure of the wiring is shown, whereas in the Table 4 the covered area in accordance with the cable size is specified. All sizes are in mm, so the areas are in mm².



Picture 5 Wiring's structure

	A	B	C	D	E	F	Total Area (A x B)
AWG TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
AWG TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Table 4 Values of the sizes shown in picture 5

All the above indicated dimensions with the relevant wire sizes and PAD position (for DPU internal harness optimization) have to be defined by CNR IFSI.

6.1 FSDL and IEEE 1355 links

The communications with the subsystem PACS occur by IEEE 1355 serial links, whereas the subsystems HIFI and SPIRE send signals via Fast Science Data Links. Due to high speed of the signals (10 Mbit/s for IEEE 1355 links, up to 2.5 Mbit/s for FSDL), the bonding between the cables and the backplane should be allocated away from the other connections. For the same reason, a dedicated layer is used between two ground layers.

In order to minimise common noise effects, the difference in track lenght between the two signals from a differential pair shall be as small as possible.

6.2 Input and output signals

Table 5 shows the list of all PADs present on the motherboard. It must be taken into account that the table lists the input and output signals in the generic configuration of the motherboard; in the HIFI and SPIRE configurations no IEEE 1355 serial link is present, whereas in the PACS configuration no FSDL and LSL are present.

With regard to power supply lines, motherboard receives a 28 DC power supply (POS + RTN) and distributes 3 internal power buses (+5V, ±15V). In the HIFI configuration 6 external power buses are foreseen.

N	Signal	Wire Size	Description	N	Signal	Wire Size	Description
1	L0DI+ MN	TBD	1355 Data0 IN+ (Main)	111	L0DI+ RED	TBD	1355 Data0 IN+ (Redundant)
2	L0DI- MN	TBD	1355 Data0 IN- (Main)	112	L0DI- RED	TBD	1355 Data0 IN- (Redundant)
3	L0SI+ MN	TBD	1355 Strobe0 IN+ (Main)	113	L0SI+ RED	TBD	1355 Strobe0 IN+ (Redundant)

N	Signal	Wire Size	Description	N	Signal	Wire Size	Description
4	L0SI- MN	TBD	1355 Strobe0 IN- (Main)	114	L0SI- RED	TBD	1355 Strobe0 IN- (Redundant)
5	L0DO+ MN	TBD	1355 Data0 OUT+ (Main)	115	L0DO+ RED	TBD	1355 Data0 OUT+ (Redundant)
6	L0DO- MN	TBD	1355 Data0 OUT- (Main)	116	L0DO- RED	TBD	1355 Data0 OUT- (Redundant)
7	L0SO+ MN	TBD	1355 Strobe0 OUT+ (Main)	117	L0SO+ RED	TBD	1355 Strobe0 OUT+ (Redundant)
8	L0SO- MN	TBD	1355 Strobe0 OUT- (Main)	118	L0SO- RED	TBD	1355 Strobe0 OUT- (Redundant)
9	L1DI+ MN	TBD	1355 Data1 IN+ (Main)	119	L1DI+ RED	TBD	1355 Data1 IN+ (Redundant)
10	L1DI- MN	TBD	1355 Data1 IN- (Main)	120	L1DI- RED	TBD	1355 Data1 IN- (Redundant)
11	L1SI+ MN	TBD	1355 Strobe1 IN+ (Main)	121	L1SI+ RED	TBD	1355 Strobe1 IN+ (Redundant)
12	L1SI- MN	TBD	1355 Strobe1 IN- (Main)	122	L1SI- RED	TBD	1355 Strobe1 IN- (Redundant)
13	L1DO+ MN	TBD	1355 Data1 OUT+ (Main)	123	L1DO+ RED	TBD	1355 Data1 OUT+ (Redundant)
14	L1DO- MN	TBD	1355 Data1 OUT- (Main)	124	L1DO- RED	TBD	1355 Data1 OUT- (Redundant)
15	L1SO+ MN	TBD	1355 Strobe1 OUT+ (Main)	125	L1SO+ RED	TBD	1355 Strobe1 OUT+ (Redundant)

N	Signal	Wire Size	Description	N	Signal	Wire Size	Description

16	L1SO- MN	TBD	1355 Strobe1 OUT- (Main)	126	L1SO- RED	TBD	1355 Strobe1 OUT- (Redundant)
17	L2DI+ MN	TBD	1355 Data2 IN+ (Main)	127	L2DI+ RED	TBD	1355 Data2 IN+ (Redundant)
18	L2DI- MN	TBD	1355 Data2 IN- (Main)	128	L2DI- RED	TBD	1355 Data2 IN- (Redundant)
19	L2SI+ MN	TBD	1355 Strobe2 IN+ (Main)	129	L2SI+ RED	TBD	1355 Strobe2 IN+ (Redundant)
20	L2SI- MN	TBD	1355 Strobe2 IN- (Main)	130	L2SI- RED	TBD	1355 Strobe2 IN- (Redundant)
21	L2DO+ MN	TBD	1355 Data2 OUT+ (Main)	131	L2DO+ RED	TBD	1355 Data2 OUT+ (Redundant)
22	L2DO- MN	TBD	1355 Data2 OUT- (Main)	132	L2DO- RED	TBD	1355 Data2 OUT- (Redundant)
23	L2SO+ MN	TBD	1355 Strobe2 OUT+ (Main)	133	L2SO+ RED	TBD	1355 Strobe2 OUT+ (Redundant)
24	L2SO- MN	TBD	1355 Strobe2 OUT- (Main)	134	L2SO- RED	TBD	1355 Strobe2 OUT- (Redundant)
25	FCK0+ MN	TBD	FSDL Clock0+ (Main)	135	FCK0+ RED	TBD	FSDL Clock0+ (Redundant)
26	FCK0- MN	TBD	FSDL Clock0- (Main)	136	FCK0- RED	TBD	FSDL Clock0- (Redundant)
27	FCK1+ MN	TBD	FSDL Clock1+ (Main)	137	FCK1+ RED	TBD	FSDL Clock1+ (Redundant)
28	FCK1- MN	TBD	FSDL Clock1- (Main)	138	FCK1- RED	TBD	FSDL Clock1- (Redundant)
29	FCK2+ MN	TBD	FSDL Clock2+ (Main)	139	FCK2+ RED	TBD	FSDL Clock2+ (Redundant)

N	Signal	Wire Size	Description	N	Signal	Wire Size	Description
30	FCK2- MN	TBD	FSDL Clock2- (Main)	140	FCK2- RED	TBD	FSDL Clock2- (Redundant)
31	FCK3+ MN	TBD	FSDL Clock3+ (Main)	141	FCK3+ RED	TBD	FSDL Clock3+ (Redundant)
32	FCK3- MN	TBD	FSDL Clock3- (Main)	142	FCK3- RED	TBD	FSDL Clock3- (Redundant)
33	FGATE0+ MN	TBD	FSDL Gate0+ (Main)	143	FGATE0+ RED	TBD	FSDL Gate0+ (Redundant)
34	FGATE0- MN	TBD	FSDL Gate0- (Main)	144	FGATE0- RED	TBD	FSDL Gate0- (Redundant)
35	FGATE1+ MN	TBD	FSDL Gate1+ (Main)	145	FGATE1+ RED	TBD	FSDL Gate1+ (Redundant)
36	FGATE1- MN	TBD	FSDL Gate1- (Main)	146	FGATE1- RED	TBD	FSDL Gate1- (Redundant)
37	FGATE2+ MN	TBD	FSDL Gate2+ (Main)	147	FGATE2+ RED	TBD	FSDL Gate2+ (Redundant)
38	FGATE2- MN	TBD	FSDL Gate2- (Main)	148	FGATE2- RED	TBD	FSDL Gate2- (Redundant)
39	FGATE3+ MN	TBD	FSDL Gate3+ (Main)	149	FGATE3+ RED	TBD	FSDL Gate3+ (Redundant)
40	FGATE3- MN	TBD	FSDL Gate3- (Main)	150	FGATE3- RED	TBD	FSDL Gate3- (Redundant)
41	FDATA0+ MN	TBD	FSDL Data0+ (Main)	151	FDATA0+ RED	TBD	FSDL Data0+ (Redundant)
42	FDATA0- MN	TBD	FSDL Data0- (Main)	152	FDATA0- RED	TBD	FSDL Data0- (Redundant)
43	FDATA1+ MN	TBD	FSDL Data1+ (Main)	153	FDATA1+ RED	TBD	FSDL Data1+ (Redundant)
44	FDATA1- MN	TBD	FSDL Data1- (Main)	154	FDATA1- RED	TBD	FSDL Data1- (Redundant)

N	Signal	Wire Size	Description	N	Signal	Wire Size	Description
45	FDATA2+ MN	TBD	FSDL Data2+ (Main)	155	FDATA2+ RED	TBD	FSDL Data2+ (Redundant)
46	FDATA2- MN	TBD	FSDL Data2- (Main)	156	FDATA2- RED	TBD	FSDL Data2- (Redundant)
47	FDATA3+ MN	TBD	FSDL Data3+ (Main)	157	FDATA3+ RED	TBD	FSDL Data3+ (Redundant)
48	FDATA3- MN	TBD	FSDL Data3- (Main)	158	FDATA3- RED	TBD	FSDL Data3- (Redundant)
49	LCK0+ MN	TBD	LSL Clock0+ (Main)	159	LCK0+ RED	TBD	LSL Clock0+ (Redundant)
50	LCK0- MN	TBD	LSL Clock0- (Main)	160	LCK0- RED	TBD	LSL Clock0- (Redundant)
51	LCK1+ MN	TBD	LSL Clock1+ (Main)	161	LCK1+ RED	TBD	LSL Clock1+ (Redundant)
52	LCK1- MN	TBD	LSL Clock1- (Main)	162	LCK1- RED	TBD	LSL Clock1- (Redundant)
53	LCK2+ MN	TBD	LSL Clock2+ (Main)	163	LCK2+ RED	TBD	LSL Clock2+ (Redundant)
54	LCK2- MN	TBD	LSL Clock2- (Main)	164	LCK2- RED	TBD	LSL Clock2- (Redundant)
55	LCK3+ MN	TBD	LSL Clock3+ (Main)	165	LCK3+ RED	TBD	LSL Clock3+ (Redundant)
56	LCK3- MN	TBD	LSL Clock3- (Main)	166	LCK3- RED	TBD	LSL Clock3- (Redundant)
57	LCK4+ MN	TBD	LSL Clock4+ (Main)	167	LCK4+ RED	TBD	LSL Clock4+ (Redundant)
58	LCK4- MN	TBD	LSL Clock4- (Main)	168	LCK4- RED	TBD	LSL Clock4- (Redundant)
59	LCK5+ MN	TBD	LSL Clock5+ (Main)	169	LCK5+ RED	TBD	LSL Clock5+ (Redundant)

N	Signal	Wire Size	Description	N	Signal	Wire Size	Description
60	LCK5- MN	TBD	LSL Clock5- (Main)	170	LCK5- RED	TBD	LSL Clock5- (Redundant)
61	LCK6+ MN	TBD	LSL Clock6+ (Main)	171	LCK6+ RED	TBD	LSL Clock6+ (Redundant)
62	LCK6- MN	TBD	LSL Clock6- (Main)	172	LCK6- RED	TBD	LSL Clock6- (Redundant)
63	LTX0+ MN	TBD	LSL Transmitter0+ (Main)	173	LTX0+ RED	TBD	LSL Transmitter0+ (Redundant)
64	LTX0- MN	TBD	LSL Transmitter0- (Main)	174	LTX0- RED	TBD	LSL Transmitter0- (Redundant)
65	LTX1+ MN	TBD	LSL Transmitter1+ (Main)	175	LTX1+ RED	TBD	LSL Transmitter1+ (Redundant)
66	LTX1- MN	TBD	LSL Transmitter1- (Main)	176	LTX1- RED	TBD	LSL Transmitter1- (Redundant)
67	LTX2+ MN	TBD	LSL Transmitter2+ (Main)	177	LTX2+ RED	TBD	LSL Transmitter2+ (Redundant)
68	LTX2- MN	TBD	LSL Transmitter2- (Main)	178	LTX2- RED	TBD	LSL Transmitter2- (Redundant)
69	LTX3+ MN	TBD	LSL Transmitter3+ (Main)	179	LTX3+ RED	TBD	LSL Transmitter3+ (Redundant)
70	LTX3- MN	TBD	LSL Transmitter3- (Main)	180	LTX3- RED	TBD	LSL Transmitter3- (Redundant)
71	LTX4+ MN	TBD	LSL Transmitter4+ (Main)	181	LTX4+ RED	TBD	LSL Transmitter4+ (Redundant)

N	Signal	Wire Size	Description	N	Signal	Wire Size	Description
72	LTX4- MN	TBD	LSL Transmitter4- (Main)	182	LTX4- RED	TBD	LSL Transmitter4- (Redundant)
73	LTX5+ MN	TBD	LSL Transmitter5+ (Main)	183	LTX5+ RED	TBD	LSL Transmitter5+ (Redundant)
74	LTX5- MN	TBD	LSL Transmitter5- (Main)	184	LTX5- RED	TBD	LSL Transmitter5- (Redundant)
75	LTX6+ MN	TBD	LSL Transmitter6+ (Main)	185	LTX6+ RED	TBD	LSL Transmitter6+ (Redundant)
76	LTX6- MN	TBD	LSL Transmitter6- (Main)	186	LTX6- RED	TBD	LSL Transmitter6- (Redundant)
77	LRX0+ MN	TBD	LSL Receiver0+ (Main)	187	LRX0+ RED	TBD	LSL Receiver0+ (Redundant)
78	LRX0- MN	TBD	LSL Receiver0- (Main)	188	LRX0- RED	TBD	LSL Receiver0- (Redundant)
79	LRX1+ MN	TBD	LSL Receiver1+ (Main)	189	LRX1+ RED	TBD	LSL Receiver1+ (Redundant)
80	LRX1- MN	TBD	LSL Receiver1- (Main)	190	LRX1- RED	TBD	LSL Receiver1- (Redundant)
81	LRX2+ MN	TBD	LSL Receiver2+ (Main)	191	LRX2+ RED	TBD	LSL Receiver2+ (Redundant)
82	LRX2- MN	TBD	LSL Receiver2- (Main)	192	LRX2- RED	TBD	LSL Receiver2- (Redundant)
83	RTAD0 MN	TBD	1553 Address0 (Main)	193	RTAD0 RED	TBD	1553 Address0 (Redundant)

N	Signal	Wire Size	Description	N	Signal	Wire Size	Description

		Size				Size	
84	RTAD1 MN	TBD	1553 Address1 (Main)	194	RTAD1 RED	TBD	1553 Address1 (Redundant)
85	RTAD2 MN	TBD	1553 Address2 (Main)	195	RTAD2 RED	TBD	1553 Address2 (Redundant)
86	RTAD3 MN	TBD	1553 Address3 (Main)	196	RTAD3 RED	TBD	1553 Address3 (Redundant)
87	RTAD4 MN	TBD	1553 Address4 (Main)	197	RTAD4 RED	TBD	1553 Address4 (Redundant)
88	RTADP MN	TBD	1553 Address Parity (Main)	198	RTADP RED	TBD	1553 Address Parity (Redundant)
89	SCTX/RXA+ MN	TBD	1553 Trans/Rec ChA+ (Main)	199	SCTX/RXA+ RED	TBD	1553 Trans/Rec ChA+ (Redundant)
90	SCTX/RXA- MN	TBD	1553 Trans/Rec ChA- (Main)	200	SCTX/RXA- RED	TBD	1553 Trans/Rec ChA- (Redundant)
91	SCTX/RXB+ MN	TBD	1553 Trans/Rec ChB+ (Main)	201	SCTX/RXB+ RED	TBD	1553 Trans/Rec ChB+ (Redundant)
92	SCTX/RXB- MN	TBD	1553 Trans/Rec ChB- (Main)	202	SCTX/RXB- RED	TBD	1553 Trans/Rec ChB- (Redundant)
93	+ 28V MN	TBD	Input Power Supply (Main)	203	+ 28V RED	TBD	Input Power Supply (Redundant)
94	+28V RTN MN	TBD	IPS Return (Main)	204	+28V RTN RED	TBD	IPS Return (Redundant)
95	+5.6V MN	TBD	Voltage to HIFI (Main)	205	+5.6V RED	TBD	Voltage to HIFI (Redundant)
96	+5.6V RTN MN	TBD	Voltage to HIFI Return (Main)	206	+5.6V RTN RED	TBD	Voltage to HIFI Return (Redundant)

N	Signal	Wire Size	Description	N	Signal	Wire Size	Description
97	+15.8V MN	TBD	Voltage to HIFI (Main)	207	+15.8V RED	TBD	Voltage to HIFI (Redundant)
98	-15.8V MN	TBD	Voltage to HIFI (Main)	208	-15.8V RED	TBD	Voltage to HIFI (Redundant)
99	±15.8V RTN MN	TBD	Voltage to HIFI Return (Main)	209	±15.8V RTN RED	TBD	Voltage to HIFI Return (Redundant)
100	+8V MN	TBD	Voltage to HIFI (Main)	210	+8V RED	TBD	Voltage to HIFI (Redundant)
101	+ 8V RTN MN	TBD	Voltage to HIFI Return (Main)	211	+ 8V RTN RED	TBD	Voltage to HIFI Return (Redundant)
102	+18V MN	TBD	Voltage to HIFI (Main)	212	+18V RED	TBD	Voltage to HIFI (Redundant)
103	-18V MN	TBD	Voltage to HIFI (Main)	213	-18V RED	TBD	Voltage to HIFI (Redundant)
104	±18V RTN MN	TBD	Voltage to HIFI Return (Main)	214	±18V RTN RED	TBD	Voltage to HIFI Return (Redundant)
105	SYNCH MAIN A+	TBD	DC/DC SynchA+	215	SYNCH MAIN B+	TBD	DC/DC SynchB+
106	SYNCH MAIN A-	TBD	DC/DC SynchA-	216	SYNCH MAIN B-	TBD	DC/DC SynchB-
107	SYNCH RED A+	TBD	DC/DC SynchA+	217	SYNCH RED B+	TBD	DC/DC SynchB+
108	SYNCH RED A-	TBD	DC/DC SynchA-	218	SYNCH RED B-	TBD	DC/DC SynchB-
109	BONDING	TBD		219	BONDING	TBD	
110	BONDING	TBD					

Table 5 List of the PADs present on the motherboard