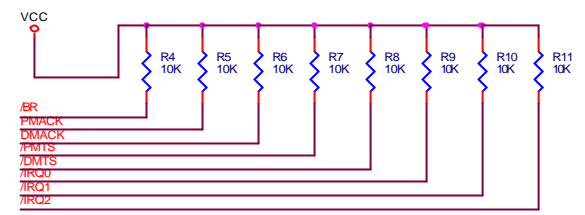
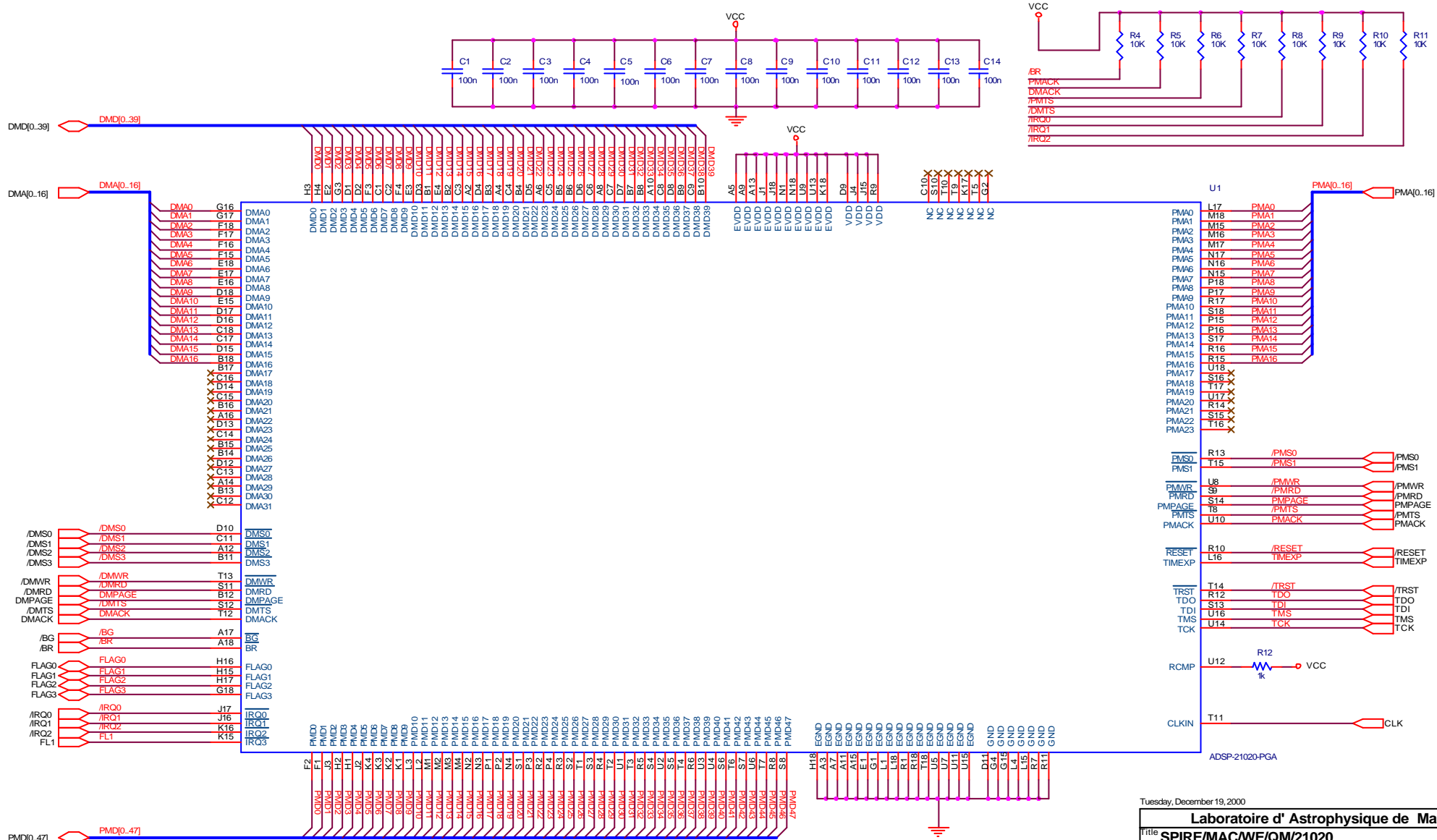


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ROOT Schematic

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SPIRE/MAC/WE/QM/ROOT		
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ADSP 21020

NOTE 1

According to Burr Brown Data sheet:

- 1) analog and digital power pins tied to the same +5V power supply, that can be produced from an analog supply, not the digital supply
- 2) All the grounds tied to the analog ground plane, separated from the system's digital logic ground

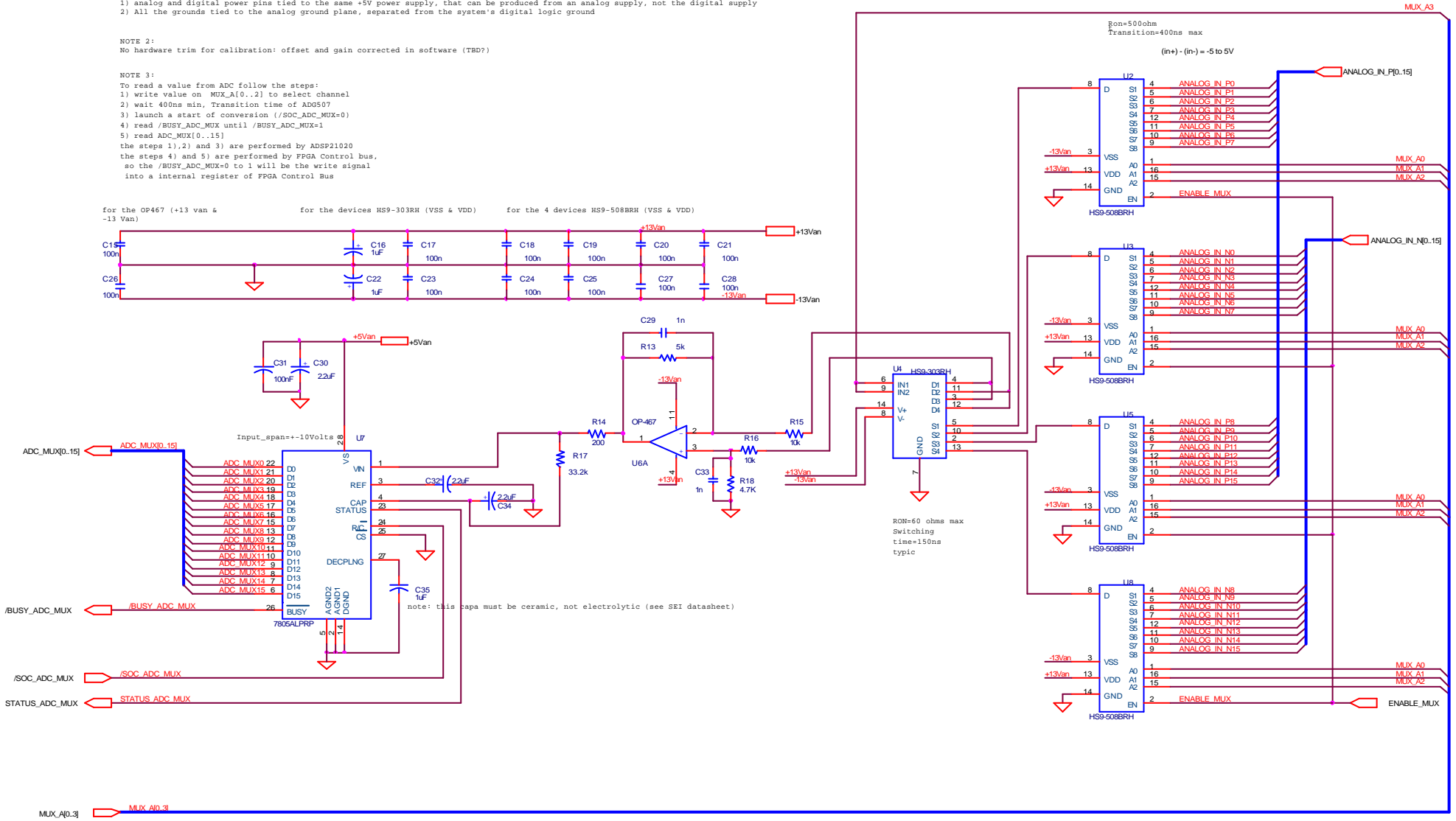
NOTE 2:

No hardware trim for calibration: offset and gain corrected in software (TBD?)

NOTE 3:

- To read a value from ADC follow the steps:
- 1) write value on MUX_A[0..2] to select channel
 - 2) wait 400ns min, Transition time of ADG07
 - 3) launch a start of conversion (/SOC_ADC_MUX=0)
 - 4) read /BUSY_ADC_MUX until /BUSY_ADC_MUX=1
 - 5) read ADC_MUX[0..15]

the steps 1),2) and 3) are performed by ADSP21020
the steps 4) and 5) are performed by FPGA Control bus,
so the /BUSY_ADC_MUX=0 to 1 will be the write signal
into a internal register of FPGA Control Bus



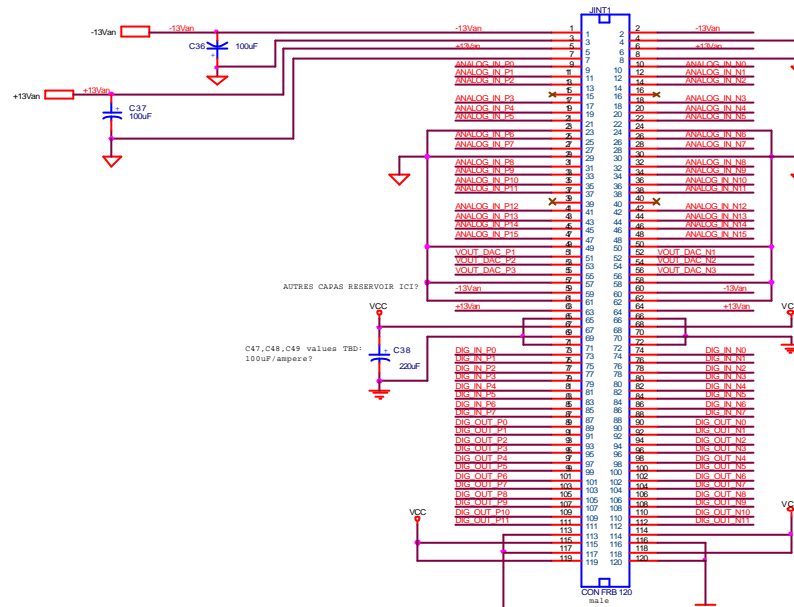
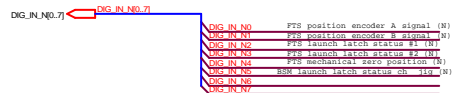
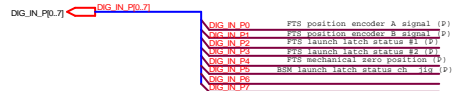
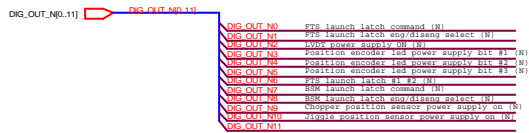
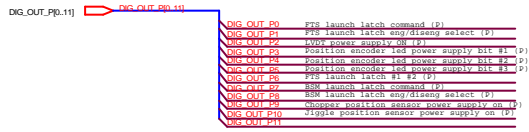
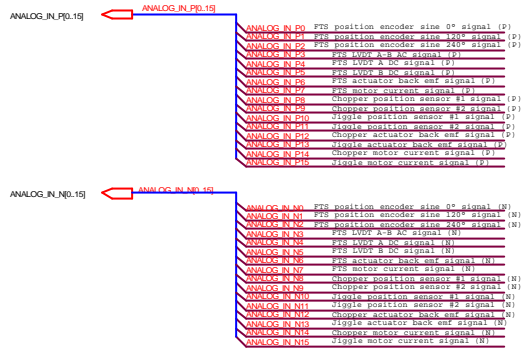
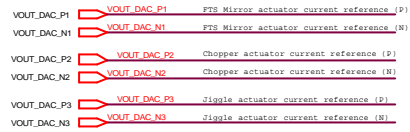
Tuesday, December 19, 2000 **16 input ADCs MUX**

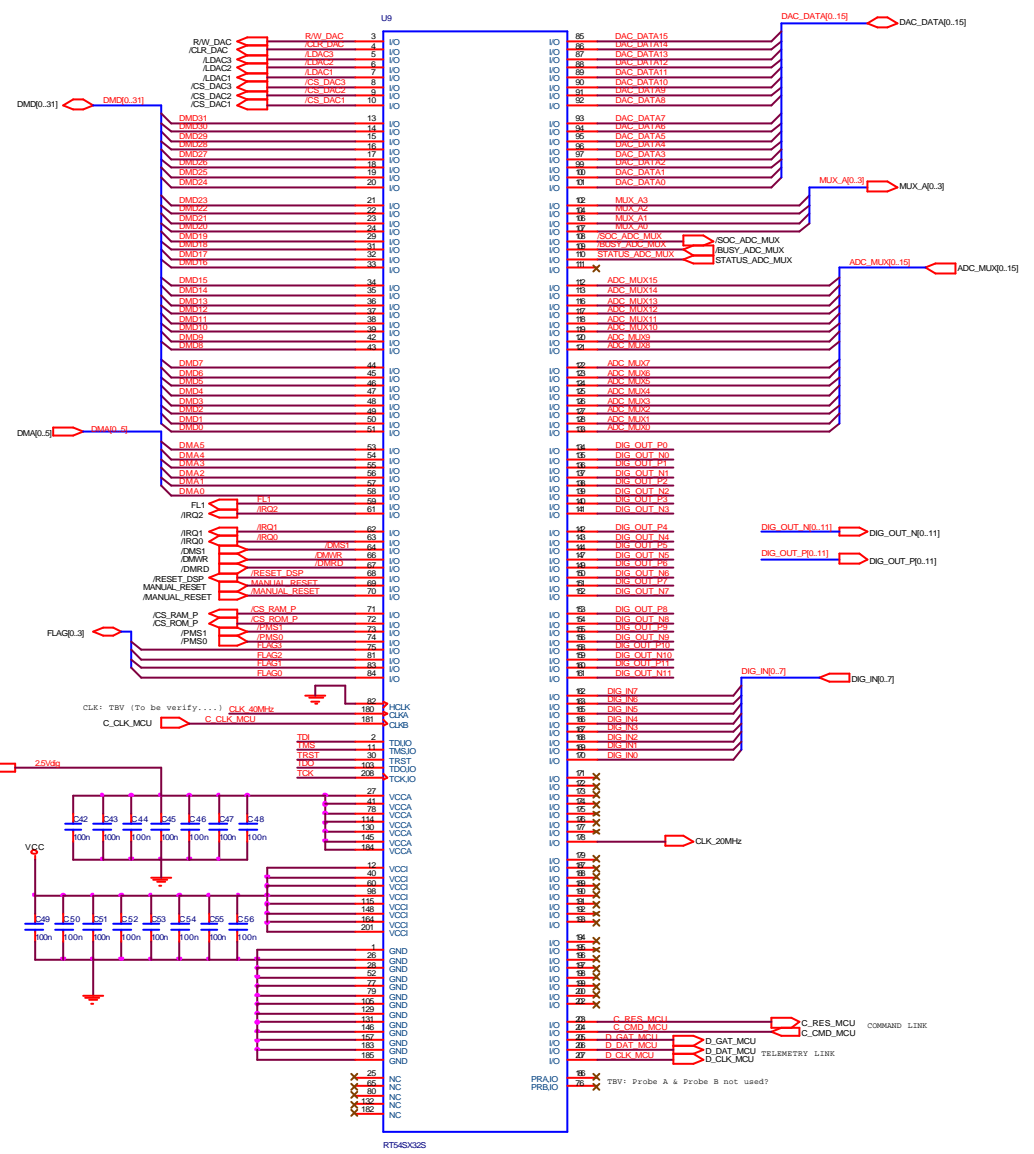
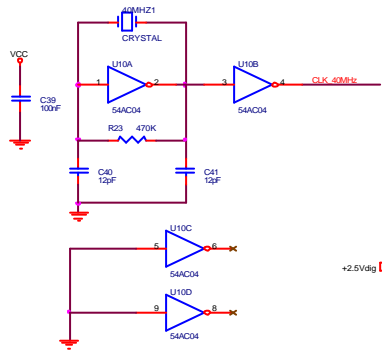
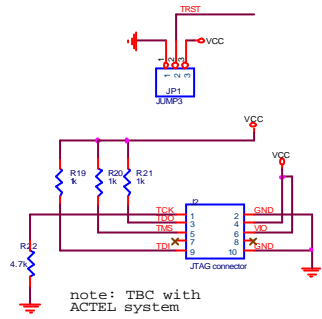
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Title **SPIRE/MAC/QM/ADC_MUX**

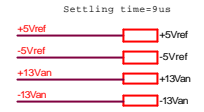
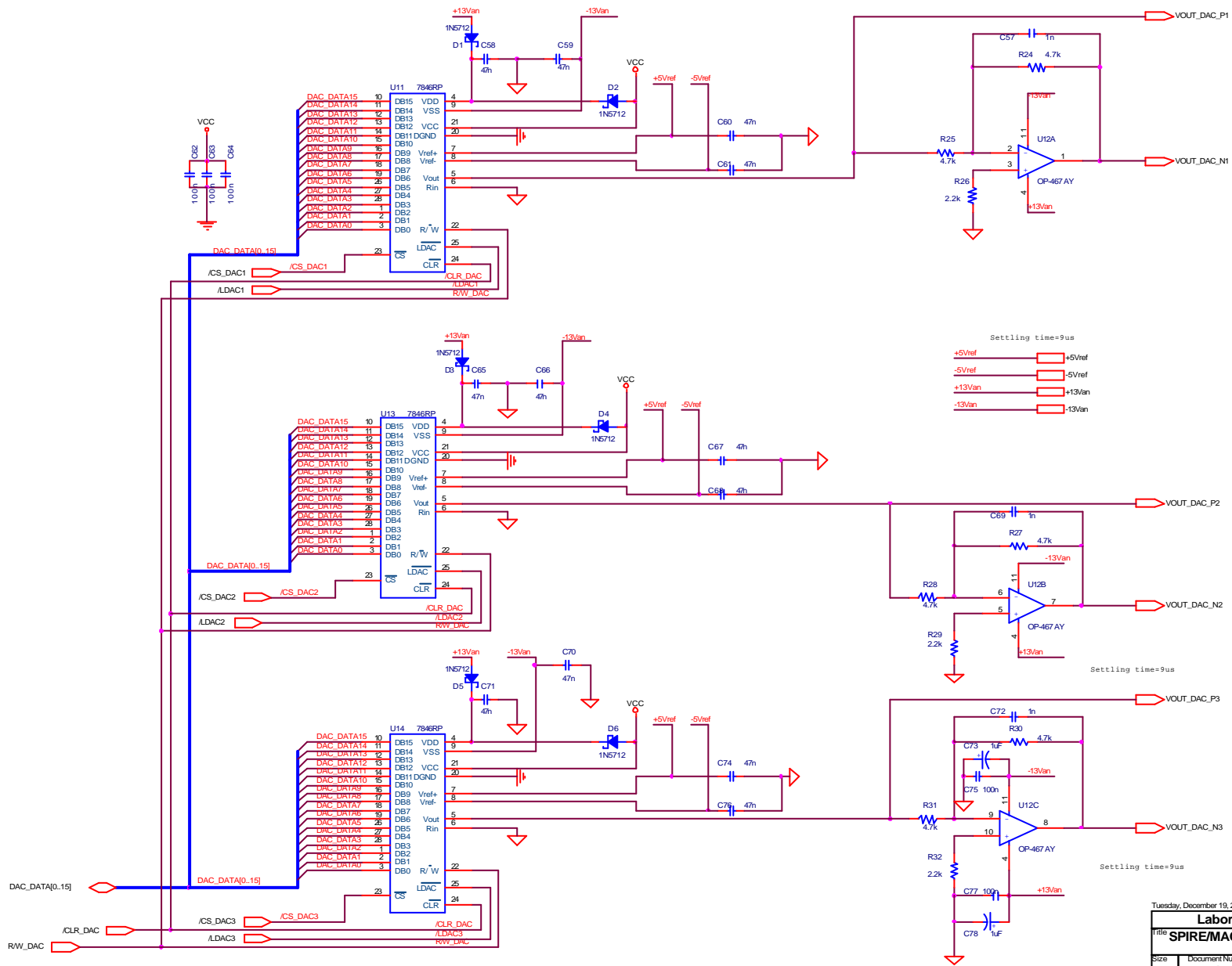
Size	Document Number	Rev
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File:	SPIRE/MAC/WE/QM/CONTROL_BUS_AND_LINK		
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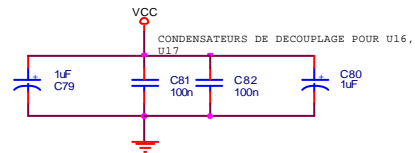
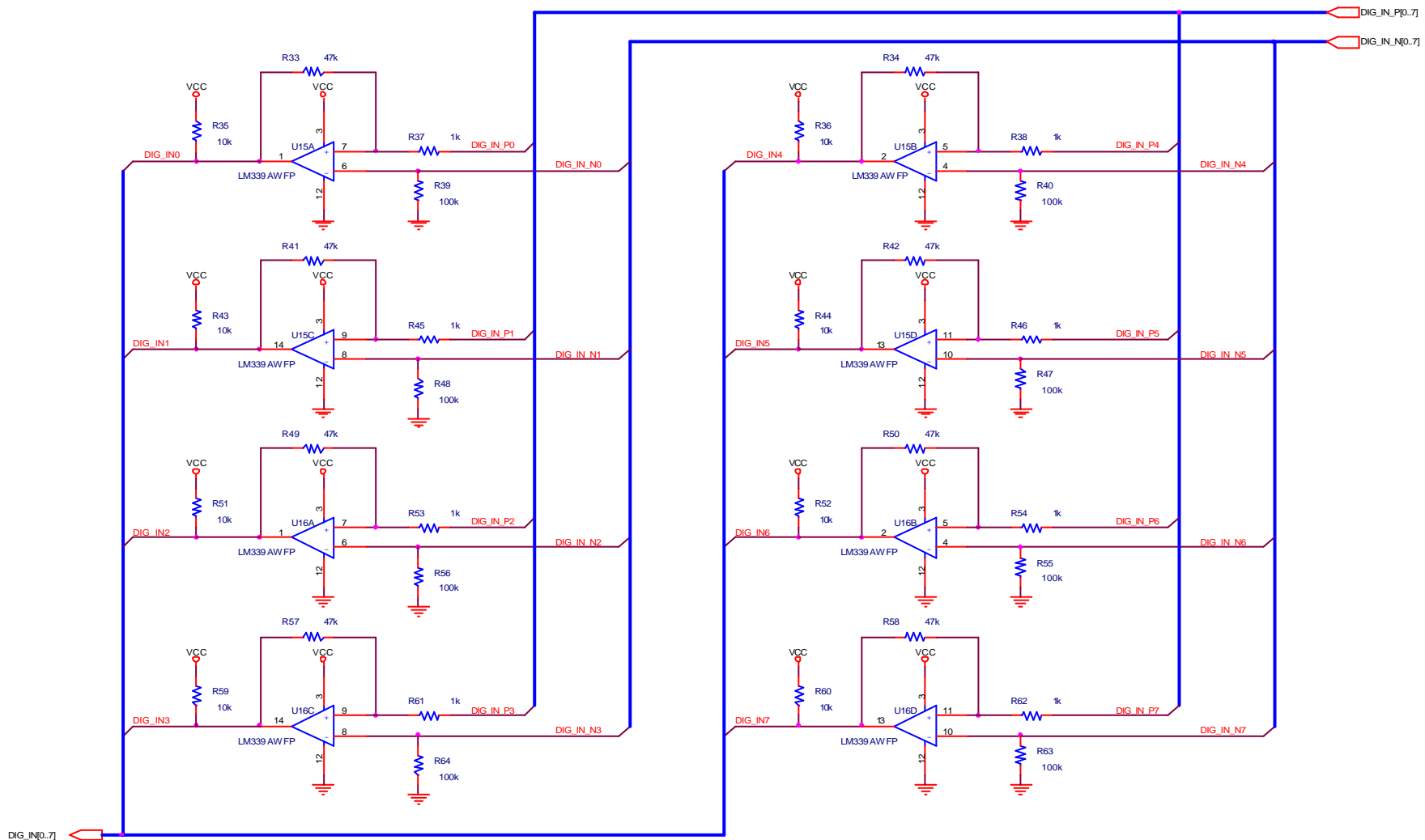


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3 Output DACs

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file SPIRE/MAC/WE/QM/DAC	
Size A3	Document Number LAMELE/MAC/QM/01-10
Date:	Rev 1.0

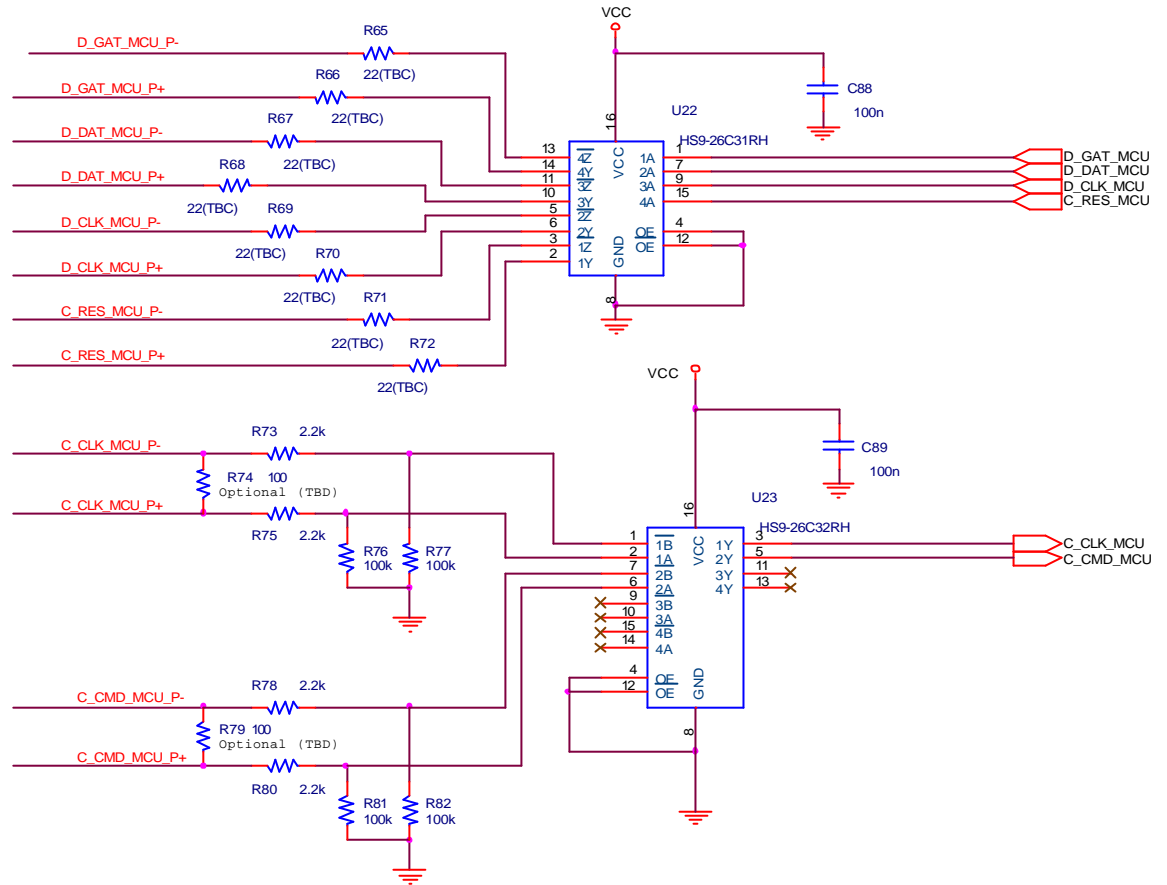
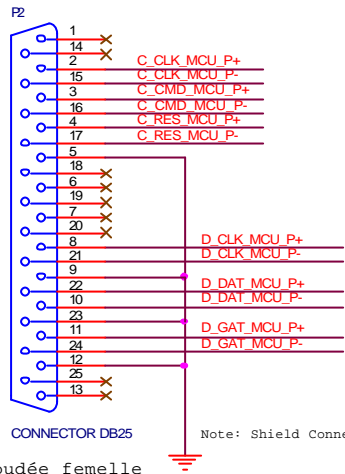
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8 Digital Input

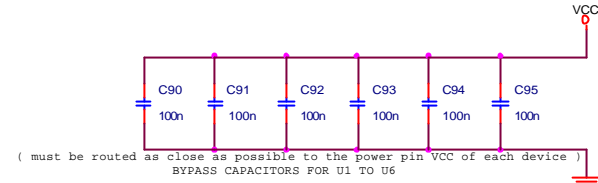
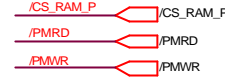
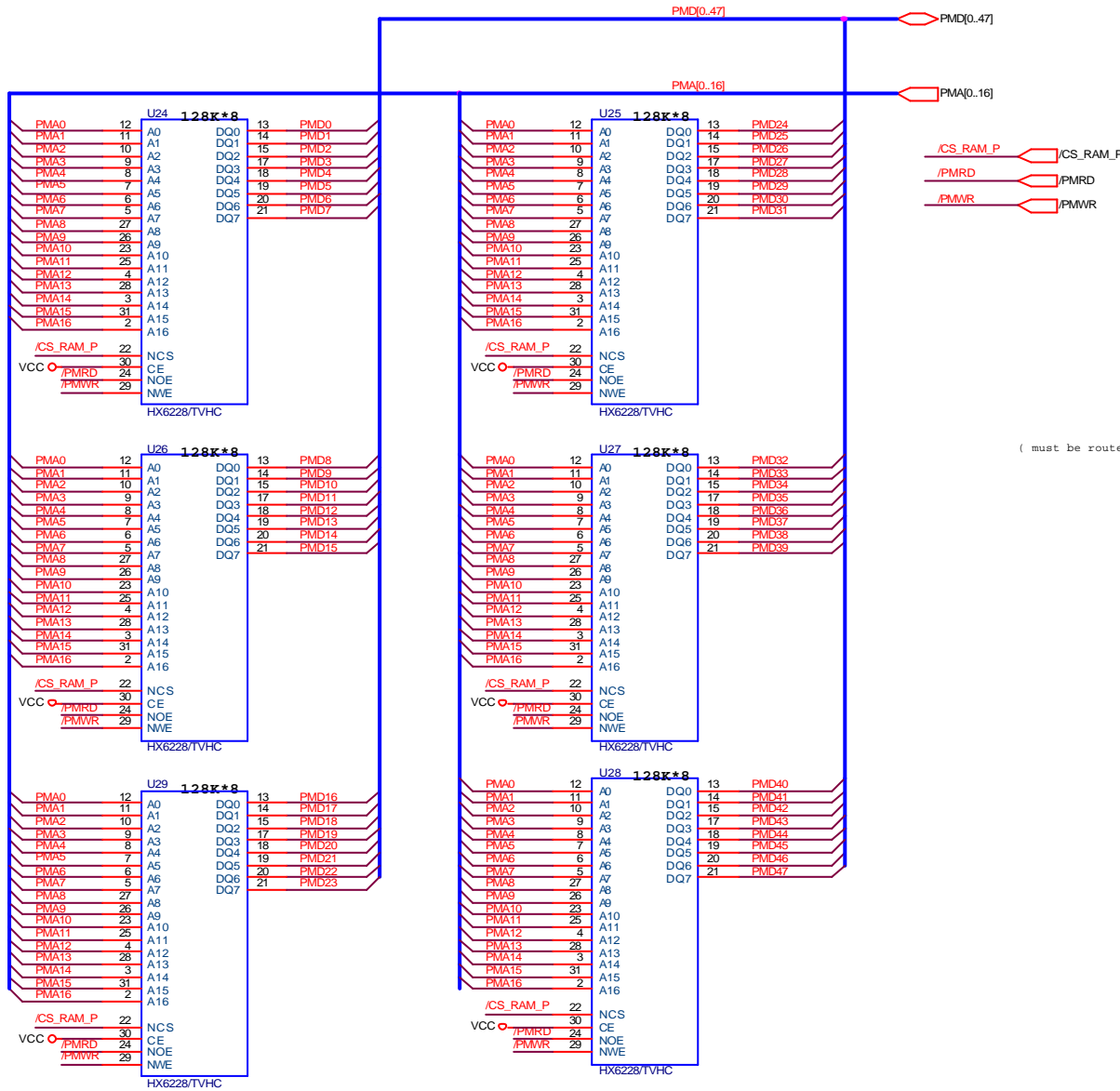
Schematic Modifying Date: = Friday, December 22, 2000

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Title SPIRE/MAC/WE/QM/DIGITAL_INPUT			
Size	Document Number	Rev	
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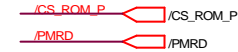
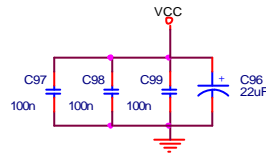
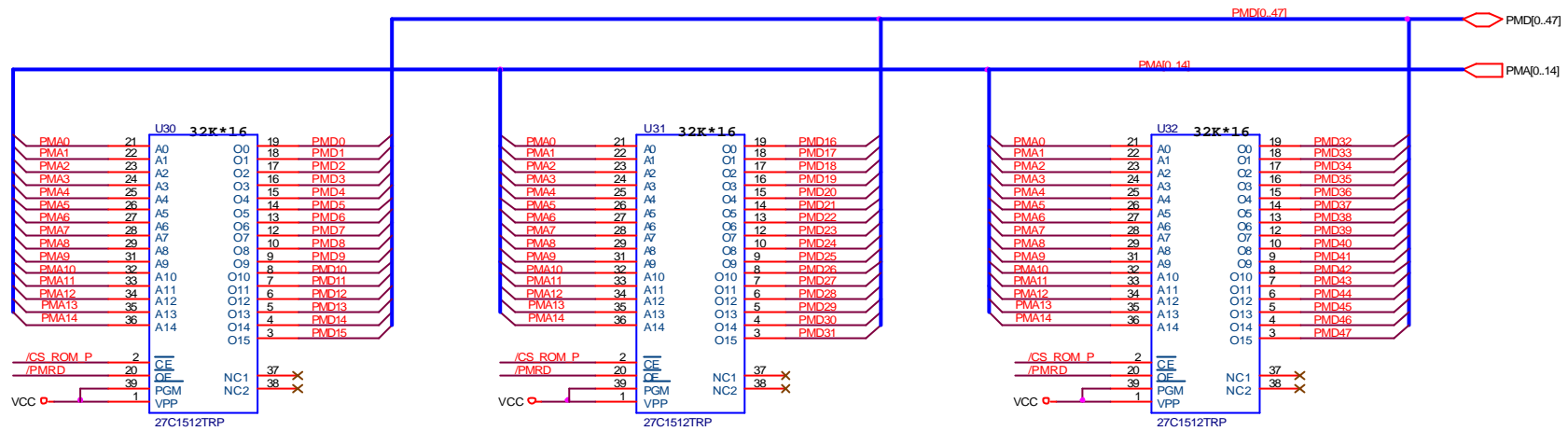
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SPIRE/MAC/WE/QM/LINK_DRIVERS		
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Program memory 128K*8 SRAM

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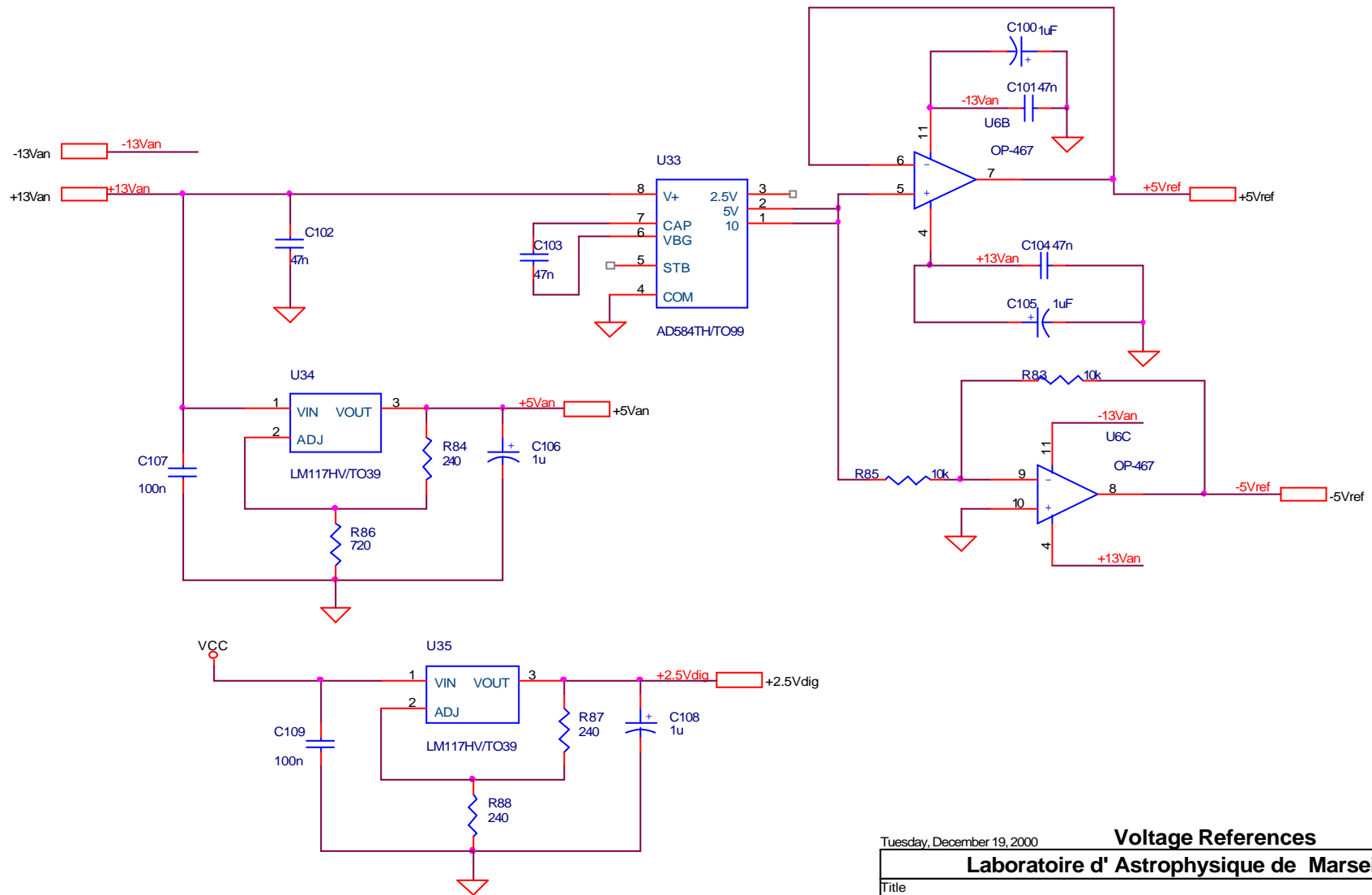
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Program memory 32K*48

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Voltage References

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Title		
SPIRE/MAC/WE/QM/VOLTAGE_REFERENCES		
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A	LAMELE/MAC/QM/01-10	1.0
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