HSO/FIRST - DPU

Herschel/FIRST - DPU Progress Meeting 3

Carlo Gavazzi Space S.p.A.

Milano, 04 September 2001

MITA Meeting Room

HSO/FIRST - DPU

Progress Meeting 3 - Agenda

- Presentation of activities status

- Open Points

- Any Other Business

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EM DELIVERABLES

* CPU BOARD

Qty	Payload	Scope	Tot
1	HIFI	Payload	
1	SPIRE	Payload	
1	PACS	Payload	
1	HIFI	Software dev.	
1	SPIRE	Software dev.	
1	PACS	Software dev.	
Total EM boards			**6**

* PL-SC I/F

Qty	Payload	Scope	Tot
1	HIFI	Payload	
1	SPIRE	Payload	
1	PACS	Payload	
1	HIFI	Software dev.	
1	SPIRE	Software dev.	
1	PACS	Software dev.	
Total EM boards			**6**

* DC/DC CONV

Qty	Payload	Scope	Tot
1	HIFI	Payload	
1	SPIRE	Payload	
1	PACS	Payload	
Total EM boards			**3**

* MOTHER BOARD

Qty	Payload	Scope	Tot
1	HIFI	Payload	
1	SPIRE	Payload	
1	PACS	Payload	
1	HIFI	Software dev.	
1	SPIRE	Software dev.	
1	PACS	Software dev.	
Total EM boards			**6**

No Redundancy

04 September 2001

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EQM DELIVERABLES

CPU BOARD

Qty	Payload	Scope	Tot
1	HIFI	Main	
1	SPIRE	Main	
1	PACS	Main	
1	HIFI	Red	
1	SPIRE	Red	
1	PACS	Red	
Total EQM boards			**6**

PL-SC I/F

Qty	Payload	Scope	Tot
1	HIFI	Main	
1	SPIRE	Main	
1	PACS	Main	
1	HIFI	Red	
1	SPIRE	Red	
1	PACS	Red	
Total EQM boards			**6**

DC/DC BOARD

Qty	Payload	Scope	Tot
1	HIFI	Main	
1	SPIRE	Main	
1	PACS	Main	
1	HIFI	Red	
1	SPIRE	Red	
1	PACS	Red	
Total EQM boards			**6**

MOTHER BOARD

Qty	Payload	Scope	Tot
1	HIFI	Main/Red	
1	SPIRE	Main/Red	
1	PACS	Main/Red	
Total EQM boards			**3**

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FM/FS DELIVERABLES

CPU BOARD

Qty	Payload	Scope	Tot
2	HIFI	Main/Red	
2	SPIRE	Main/Red	
2	PACS	Main/Red	
1	PACS	Spare	
1	SPIRE/HIFI	Spares	
Total FM/FS boards			**8**

PL-SC I/F

Qty	Payload	Scope	Tot
2	HIFI	Main/Red	
2	SPIRE	Main/Red	
2	PACS	Main/Red	
1	PACS	Spares	
1	SPIRE/HIFI	Spares	
Total FM/FS boards			**8**

DC/DC CONV

Qty	Payload	Scope	Tot
1	HIFI	Main/Red	
1	SPIRE	Main/Red	
1	PACS	Main/Red	
1	HIFI	Spare	
1	PACS/SPIRE	Spare	
Total FM/FS boards			**5**

MOTHER BOARD

Qty	Payload	Scope	Tot
1	HIFI	Main/Red	
1	SPIRE	Main/Red	
1	PACS	Main/Red	
2		Spares	
Total FM/FS boards			**5**

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Deliverable Documents

- S/W
  - SRD
  - ADD
  - Test Procedure and Test Result
  - SVVP

- H/W
  - Specification (DSP, I/F, DC/DC, Motherboard)
  - DCL - DML - DPL - DMPL
  - Electrical Drawings
  - Part List
  - Layout
  - Test Procedure - Test Report

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Current Status

- Hardware
  - DSP Board
  - I/F Board
  - DC/DC Converter Board
  - Motherboard

- Software

- Test Equipment

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DSP Board

- ***Electrical Design***: Completed

- ***Kitting***: Completed

- ***Test Procedure Document***: Completed

- ***Artwork***: Completed

- ***PCB Manufacturing***: Completed

- ***FPGA Programming***: Completed

- ***Board Assembly (S/N 01)***: Completed

- ***Board Testing (S/N 01)***: In Progress

- ***Board Assembly (S/N 02)***: In Progress

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I/F Board

- ***Electrical Design***: Completed
- ***Kitting***: Completed
- ***Test Procedure Document***: Completed
- ***Artwork***: Completed
- ***PCB Manufacturing***: Completed
- ***FPGA Programming***: Completed
- ***Board Assembly (S/N 01)***: Completed
- ***Board Testing (S/N 01)***: In Progress
- ***Board Assembly (S/N 02)***: In Progress

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DC/DC Board

- ***Electrical Design***: Completed

- ***Test Procedure Document***: In Progress (delayed, expected within 14/09/2001)

- ***Artwork***: In Progress (delayed, expected within 14/09/2001)

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Motherboard

- ***Electrical Design***: Completed

- ***Test Procedure Document***: In Progress (expected within 14/09/2001)

- ***Artwork***: In Progress (delayed, expected within 07/09/2001)

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Software Status

- ***1355 Coding***: In Progress (80%)

- ***1553 Coding***: In Progress (50%)

- ***Power On Procedure Coding***: In Progress (50%)

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Test Equipment

- Based on two simulators:
  - IFSI Simulator for FSDL and LSL links
  - CGS Simulator for MIL 1553 and IEEE 1355

- CGS Test equipment shall be composed by a PC with two interface boards installed
  - 1355 Link
  - Condor PCI-1553 Board

  - The installation of both boards inside the CGS TE will be performed only after the completion of tests at board level (1355 for CPU and 1553 for PL I/F)

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Open Points

- The delay in the delivery of IFSI FSDL and LSL Simulators is resulting in a delay in the testing of the Payload & Spacecraft Interface board.