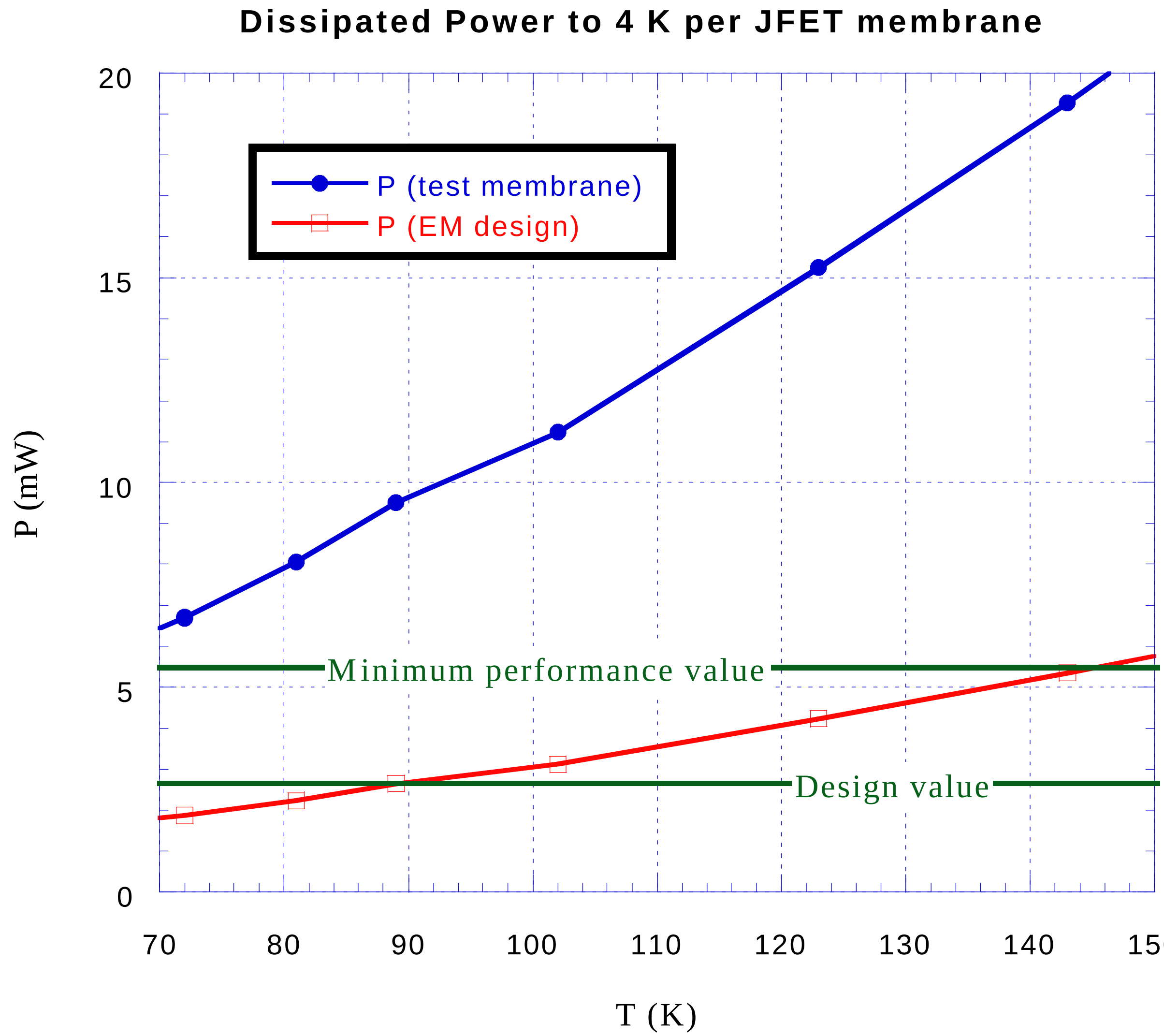
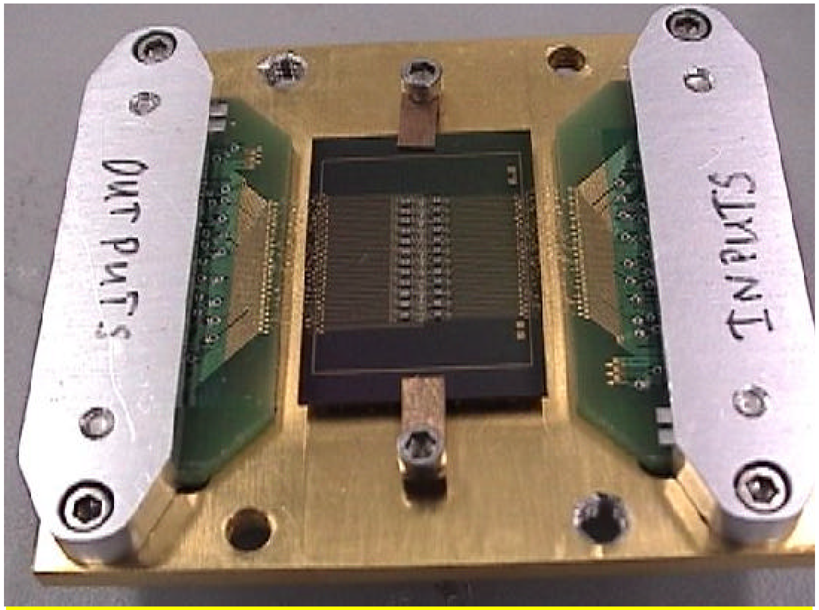
Membrane Thermal Conductivity

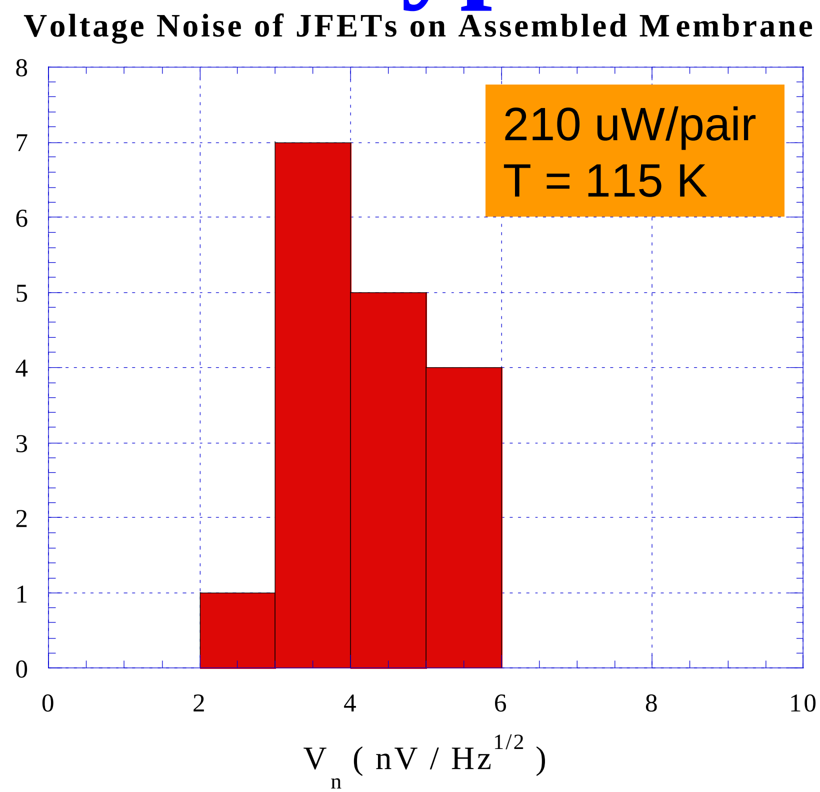
- Conductivity measured on 12 x 12 mm test structure with Δx = 1 mm gap
- Estimated for EM membrane assuming square geometry
- Terry will present detailed thermal analysis for the EM membrane



Tests on Unetched Prototype

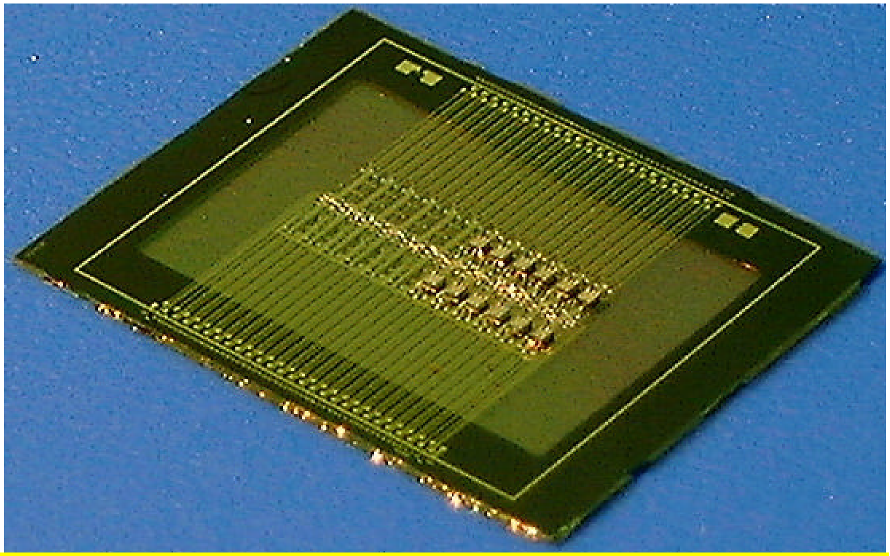


Unetched prototype test sample

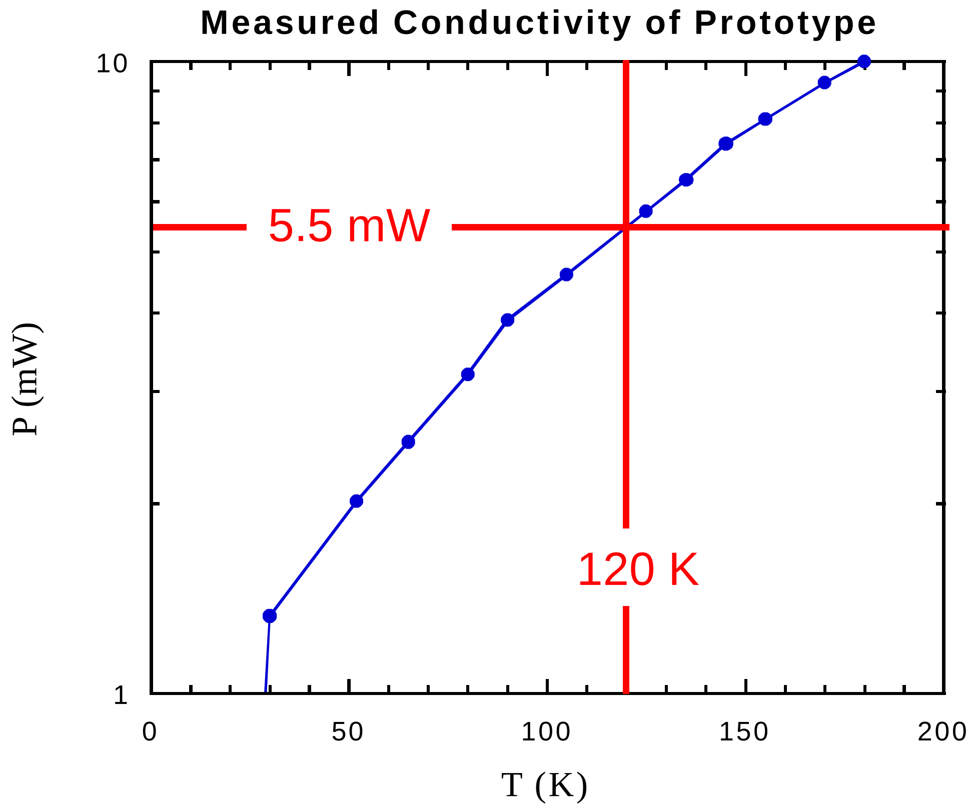


- **No excess noise associated with lithographed resistors**
- **Leads metalization too thick**
- **Some difficulties in etching and yield on source resistors**
- **Open gates are ESD sensitive**

Thermal Conductivity of Etched Prototype



Etched prototype test sample

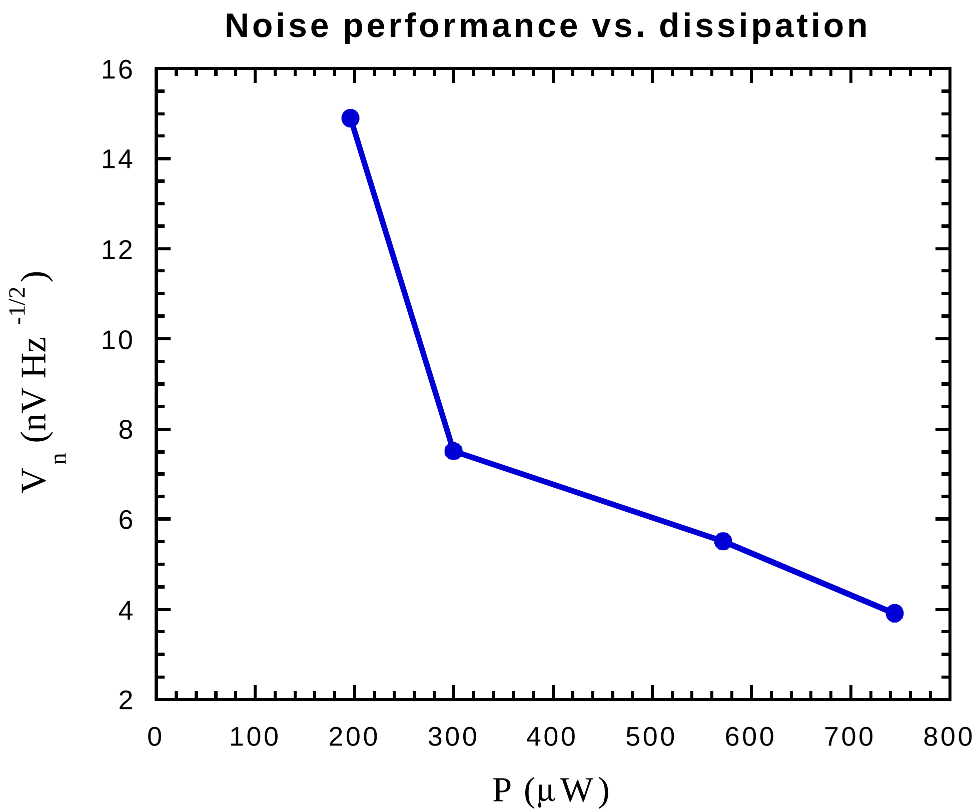


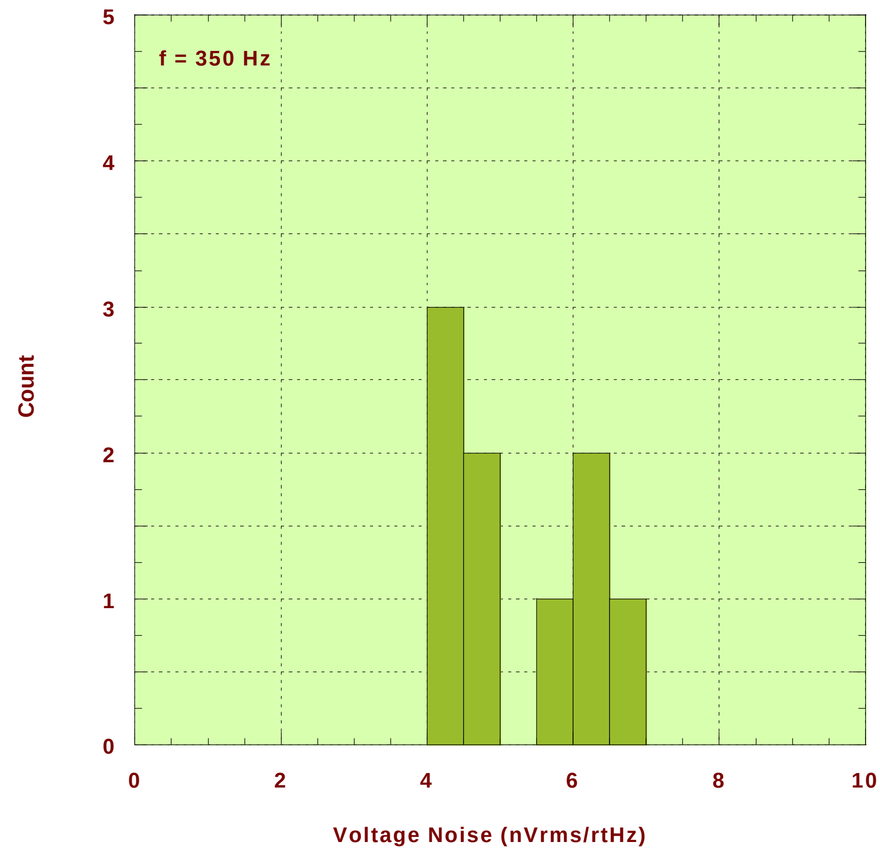
- **Half populated with JFETs**
- **1.8 μm membrane thickness**
- **Difficult geometry to model thermally**
- **Estimated conduction of leads is 3.2 mW based on impedance at 77 K and Wiedemann-Franz relation**

5.5 mW/membrane = “*minimum performance*”

- **90 s start-up time to 120 K (fast!)**

Noise Tests on Etched Prototype



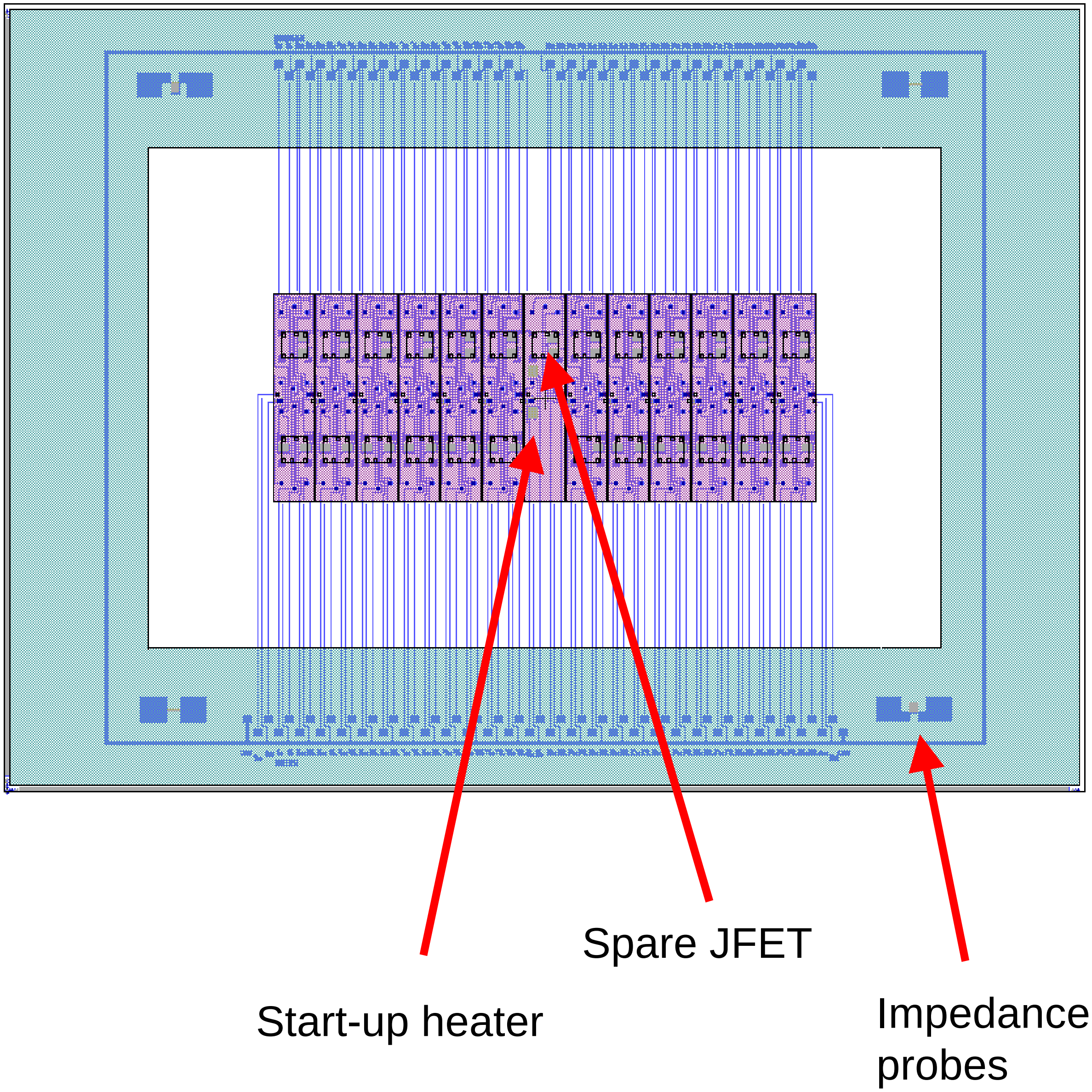


Performance within specification at P > 300 μW/pair, or 3.6 mW/membrane

Performance at 7.5 mW/membrane

Development of EM membranes

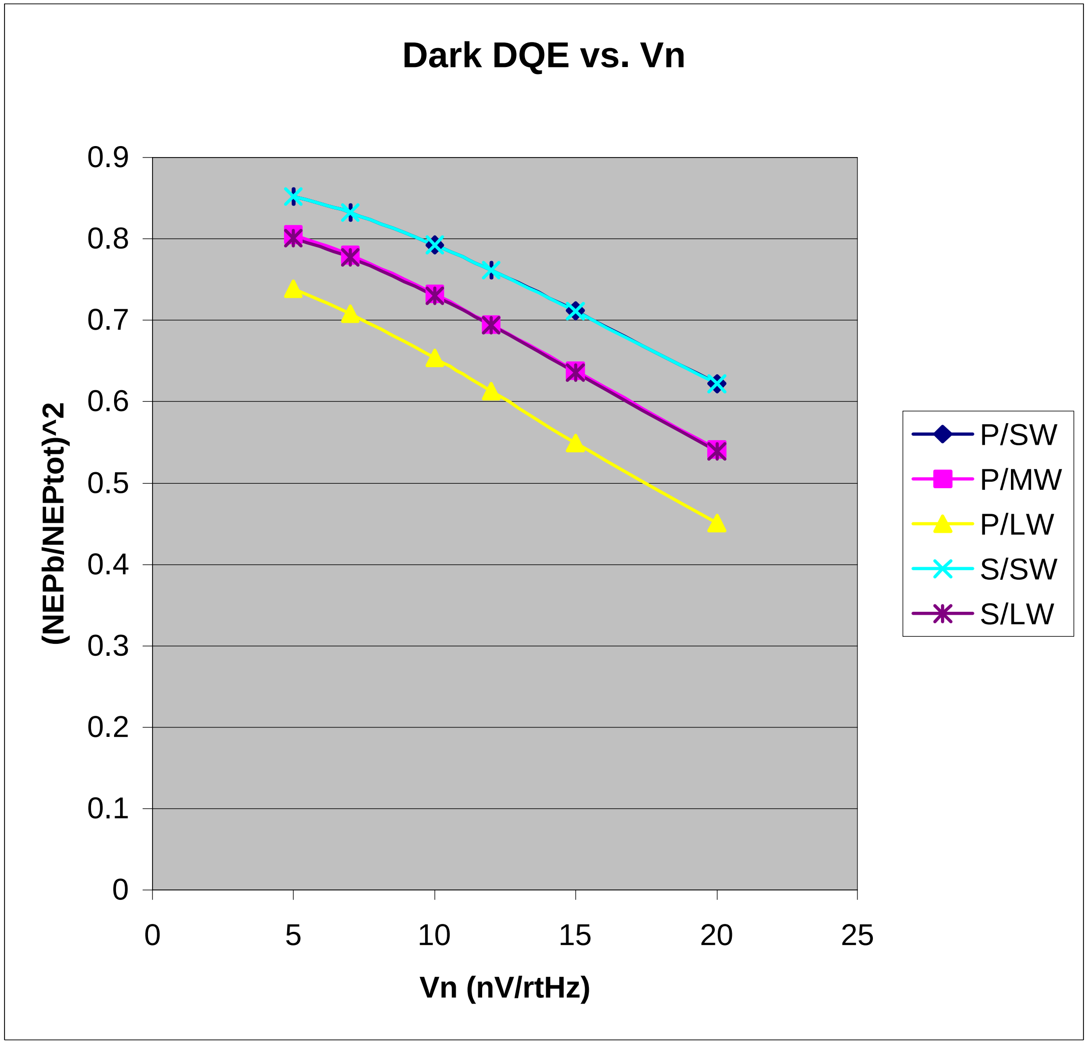
- **E-beam written resistors + passivation layer give high yield, no failures on thermal cycling to 77 K**
- **Thinner leads metalization reduces lead conduction by 9.5 (resistance at 77 K + W-F)**
- **Start-up heater to avoid dissipation on 300 mK stage.**
- **DRCU also has diodes to ground for conventional start up mode.**
- **1.0 μm membranes are too difficult to fabricate.**



Expected Tests Prior to Review

- Vibration and thermal cycle testing of mechanically representative membrane and housing with boards, connectors and RF filters
- Noise testing on unetched EM unit at operating temperature

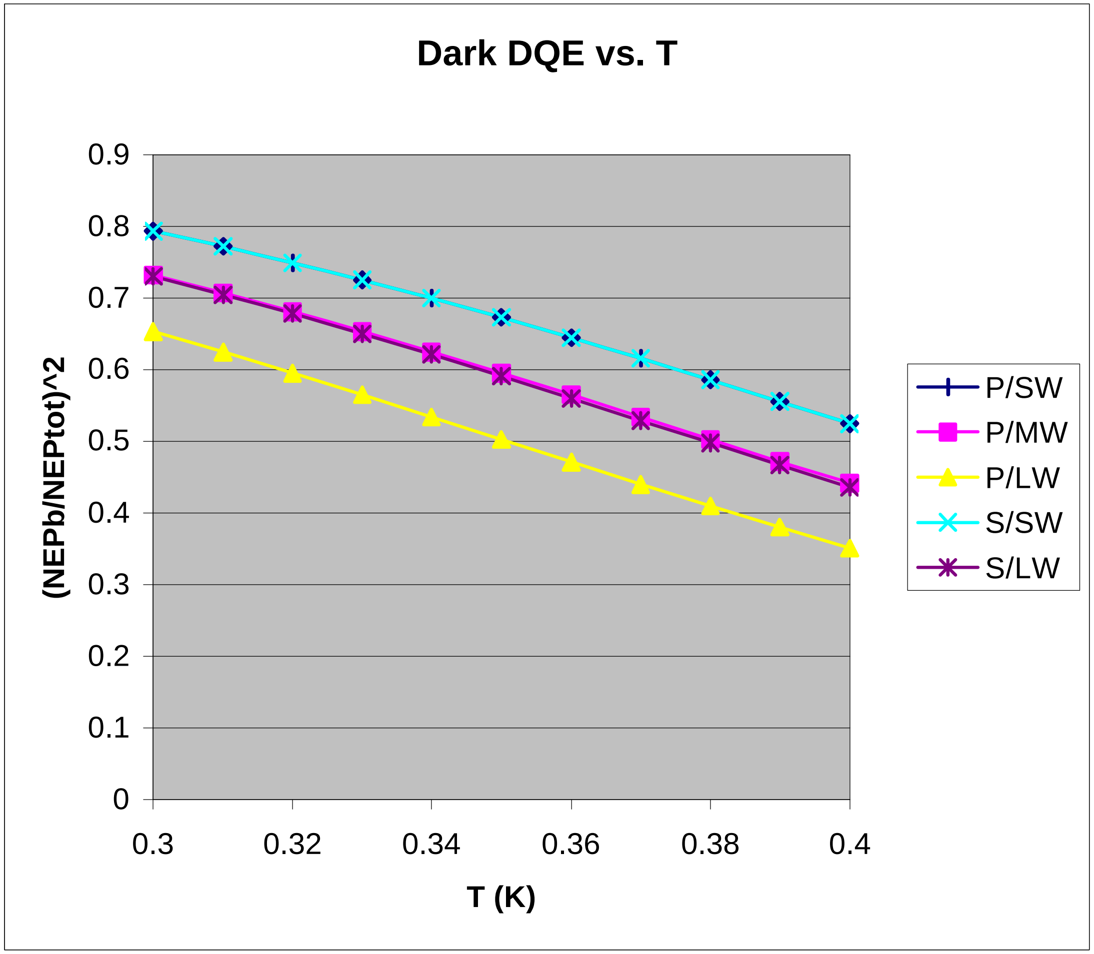
Systems Noise Issues with JFETs



- Reduction in mapping speed with amplifier noise is small

< 20 % reduction if JFET noise increases to 15 nV/√Hz.

Systems Thermal Issues with JFETs



JFET dissipation reduces mission life:

2.3 % reduction in life at 1.5 x DV
4.7 % reduction in life at 2.0 x DV

JFET dissipation increases detector T:

6 mK increase at 1.5 x DV, and
< 4 % reduction in M.S. at 1.5 x DV

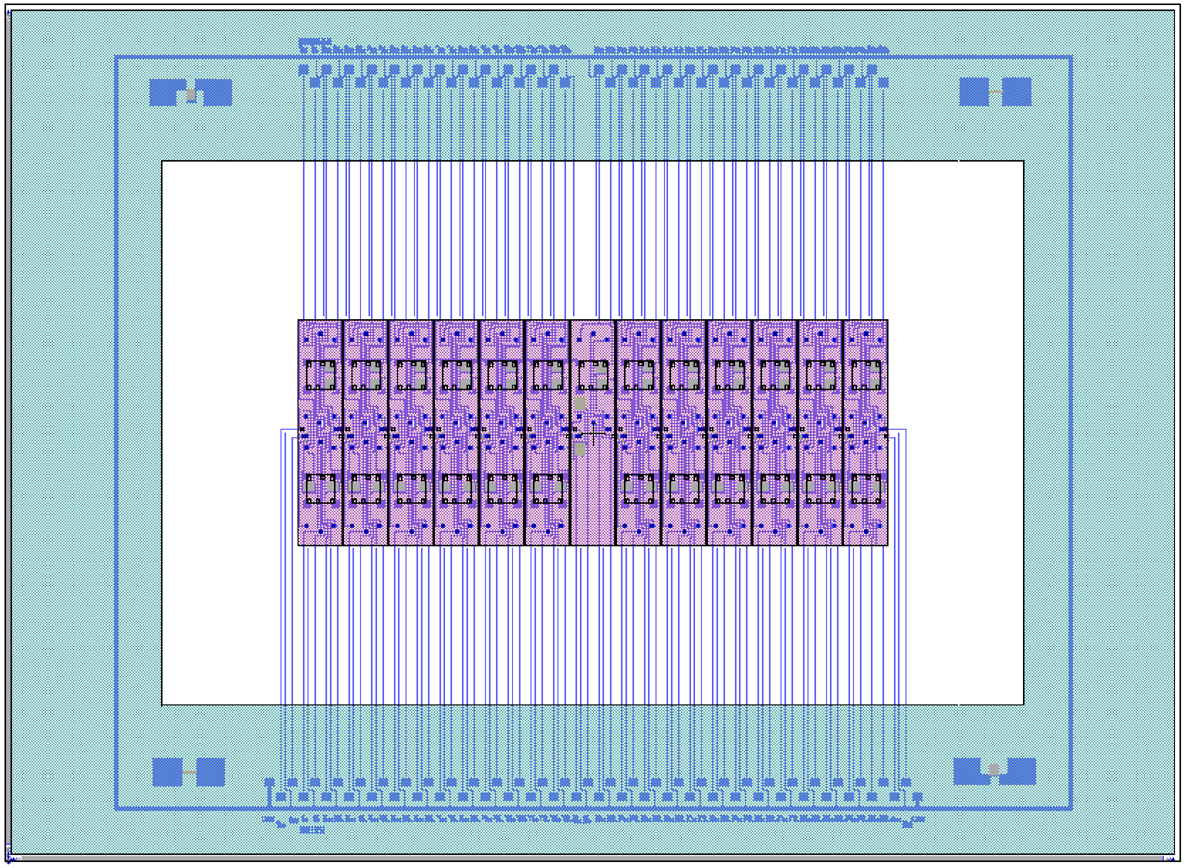
Transient effects from switching JFETs on and off to the instrument performance are uncertain

6.2
JFET Thermal Model

Terry Cafferty

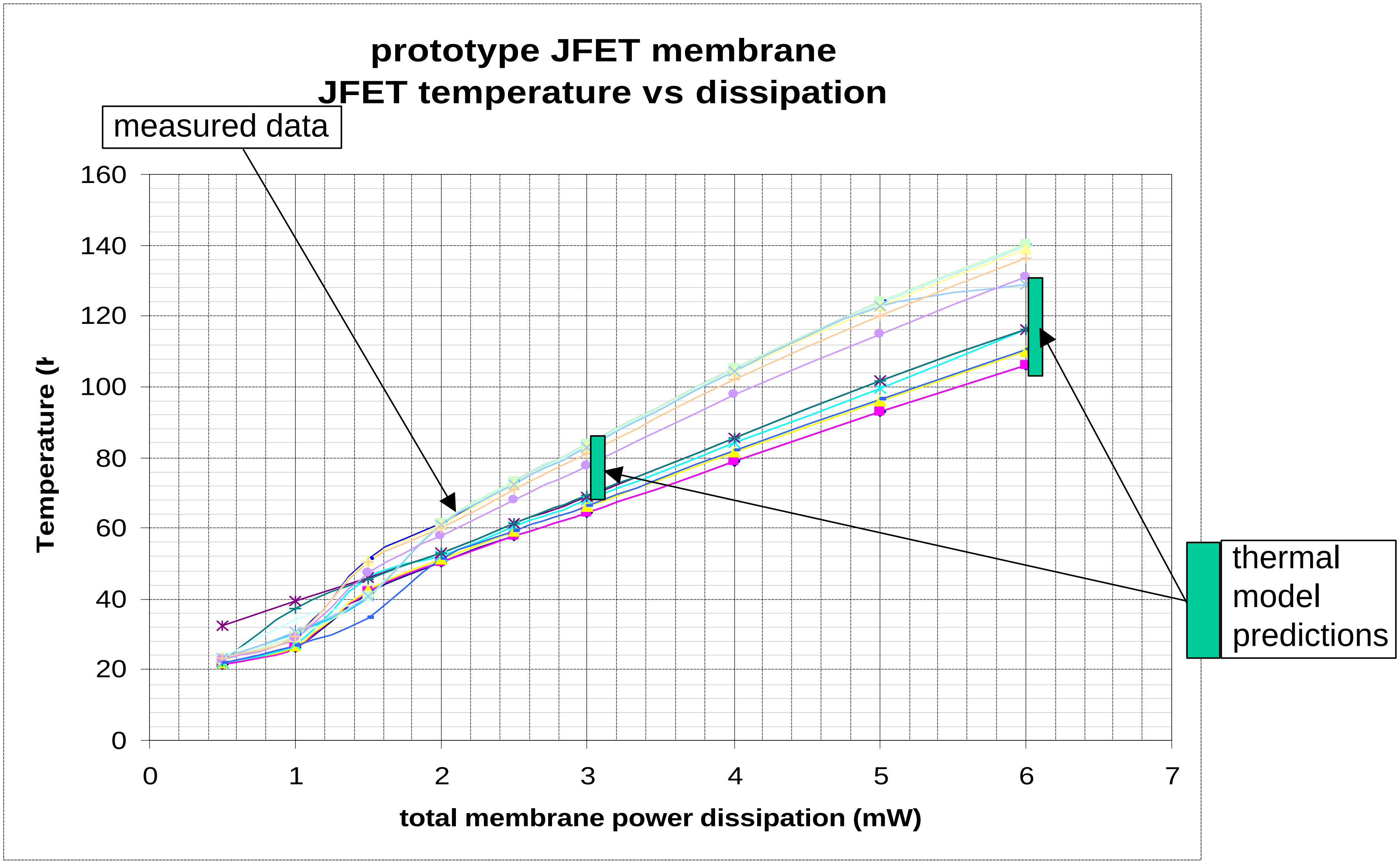
JFET membrane detailed thermal models

Terry Cafferty



2-D SINDA/G model
228 membrane nodes
728 conductors
leads broken into 1 mm lengths
temperature dependent conductances

JFET prototype membrane measured vs predicted thermal performance



JFET EM Membrane Thermal Model Predictions

- Similar to prototype membrane model, symmetrical heat input
- Leads conductance ~ 0.105 x prototype (measured cold)
- Design value module dissipation 5.5 mW

JFET dissipation uW/pair	Module dissipation mW	JFET temp range K
100	4.8	92 – 102
110	5.3	98 – 108
125	6.0	107 - 118
150	7.2	121 - 134

JFET Power Dissipation (JFET-TEC-04)

Power (mW)	/pair	/module	/phot	/spect
Design value	0.115	5.5	33	8.25
1.5 * DV	0.170	8.25	49.5	12.38
Min. P. value	0.230	11	66	16.5

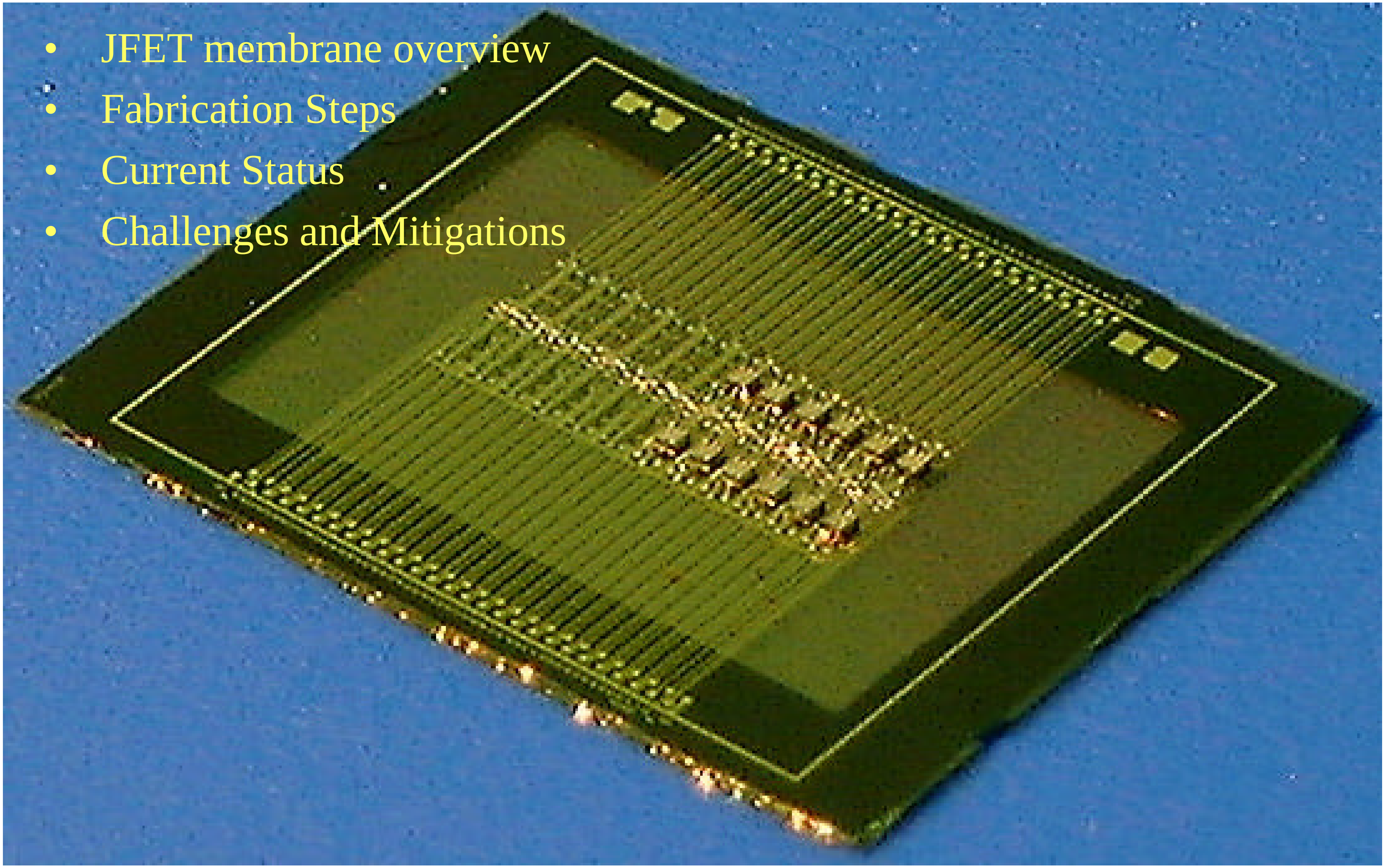
JFET membrane thermal summary

- Prototype membrane thermal measurements correlate well with detailed 2D thermal model
- EM/flight membrane identical to prototype, except lead conductance smaller by a factor of ~10; thermal model probably accurate
- We know JFETs perform well for T > 120 K, maybe colder
- EM membrane thermal model predicts $T_{\mathbf{jfet}}$ > 120 K @ 150 uW/pair
- 150 uW/pair implies module dissipation of 7.2 mW (5.5 mW goal)
- EM membrane JFET thermal tests will be performed to find T_{min} and corresponding minimum dissipation

6.3
JFET Membrane Fabrication

Anthony Turner
Eric Jones
Shrinivasan Sethuramen

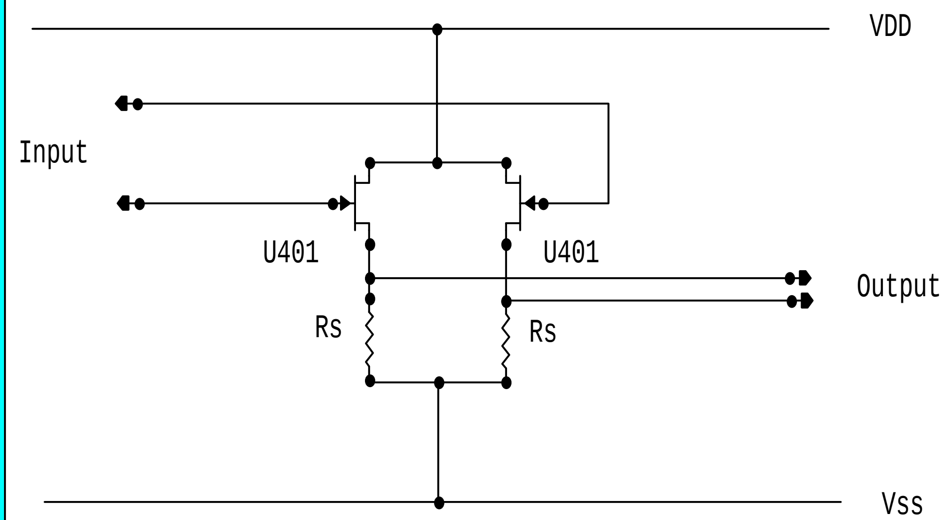
Overview



- JFET membrane overview
- Fabrication Steps
- Current Status
- Challenges and Mitigations

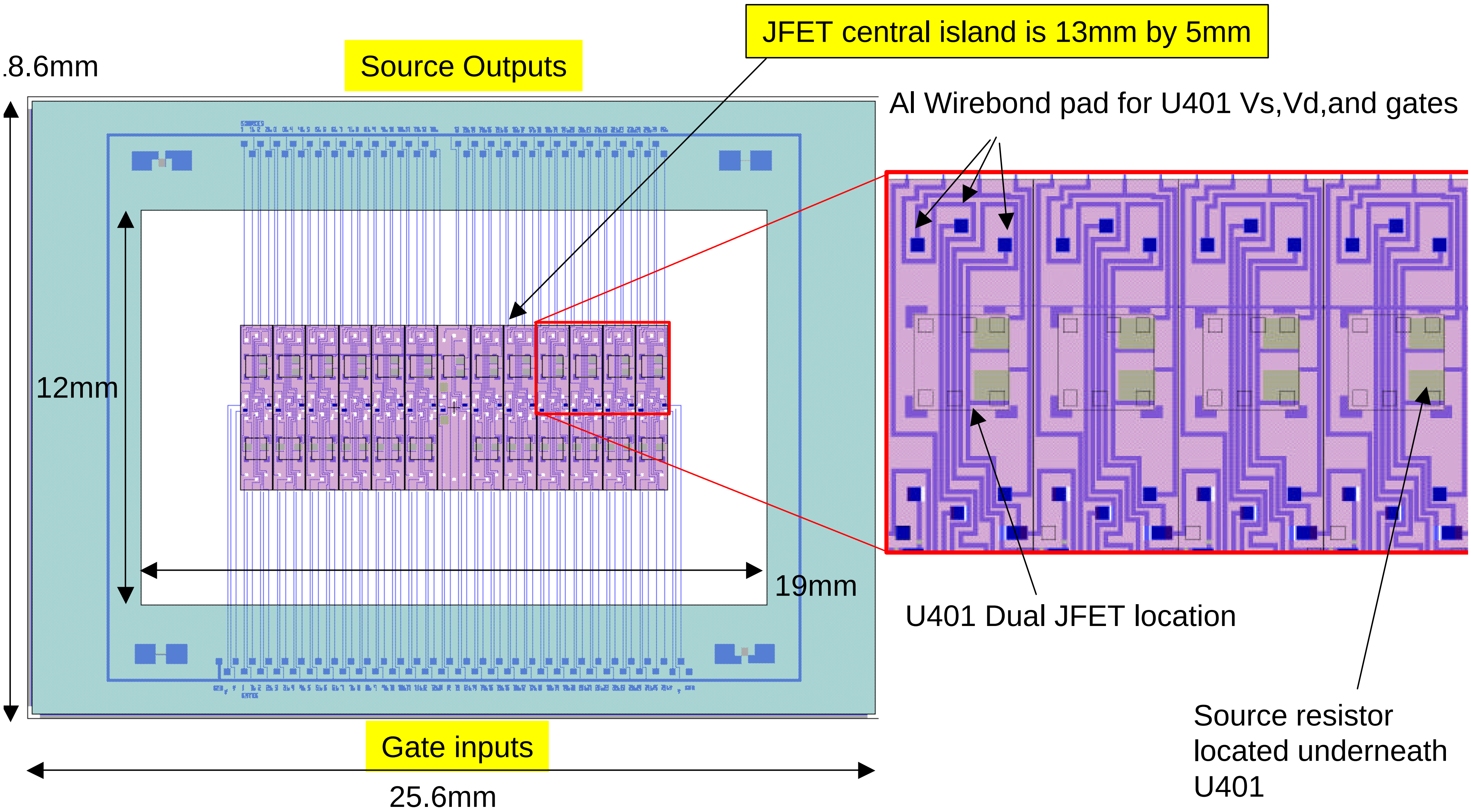
JFET Module Overview

- JFET module forms the detector readout circuitry for all bolometer arrays
- Each JFET module provides:
  - 24 channel differential amplifier readout circuits
  - Differential design reduces susceptibility to microphonics and RF
- Each JFET modules design features changes from EM:
  - 25 channels (24 plus one redundant channel)
  - NiCr thin film source resistors (100kΩ) placed underneath U401 to help heat U401 to operating temperature
  - Au interconnect lines thinned down to 15μm wide and metalization thinned down to 50 nm.
  - 24 dual U401 JFETs wirebonded to center of 1.8μm SiN membrane structure
  - Central membrane heater added onto membrane



A schematic of a single channel of a JFET readout is shown. The source resistors are placed on the membrane to minimize sensitivity to the wiring harness to the cold electronics, although significant power dissipation comes from the source resistors.

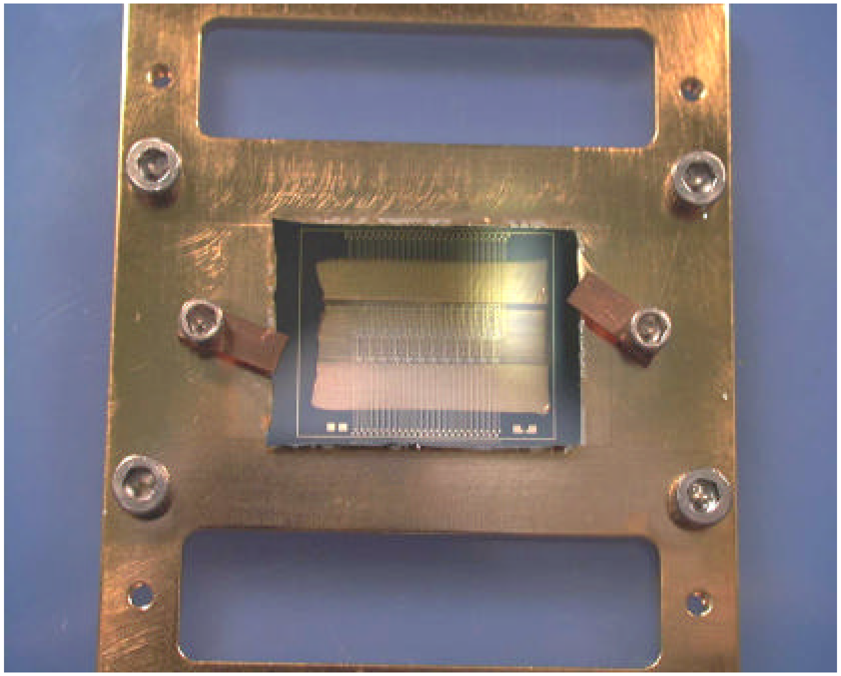
JFET Module Overview



JFET Module Status

- Fabrication notes:
  - Low yield on 1um SiN membranes (<10%)
  - High yield on 1.8um SiN membranes (~50%)
  - 2 partially populated membranes completed
  - 1 fully populated membrane completed
  - Process modifications completed

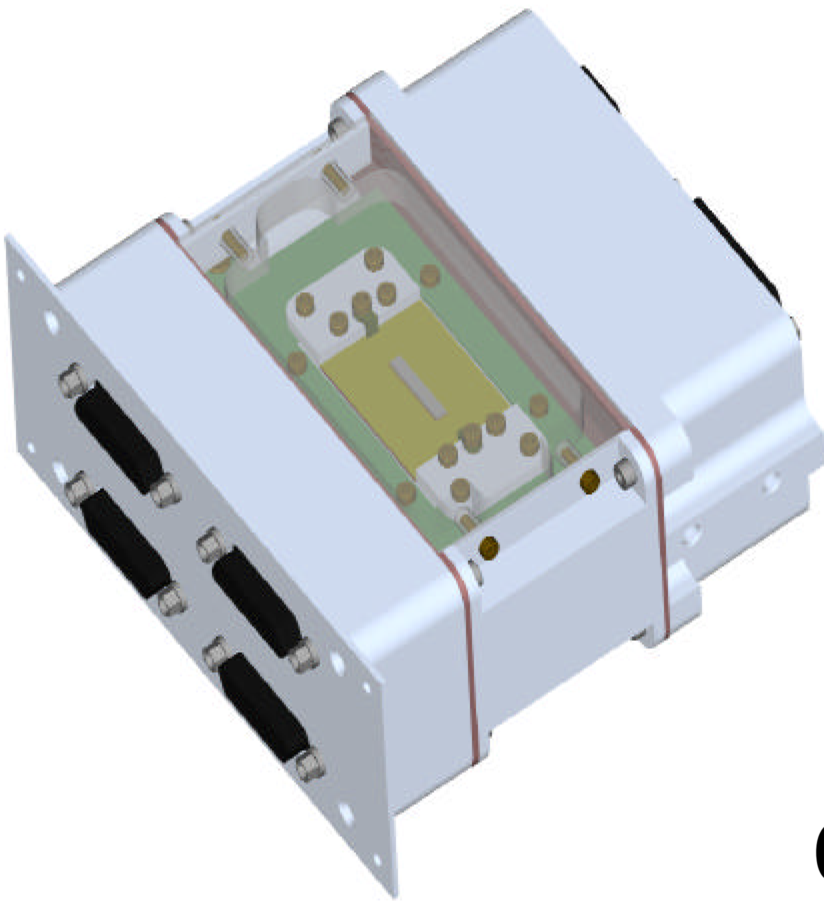
- Testing overview
  - Unetched modules
    - Noise performance completed
  - Representative etched membrane
    - Vibration tested (sine sweep 7.5g amplitude 30-400Hz,15g amplitude 400-2500Hz)
    - Membrane rupture strength is ~ 150g
  - 2 PM modules populated with 12 U401 JFETs
    - Noise and thermal testing completed
  - 1 PM module fully populated
    - Under assembly for environmental testing

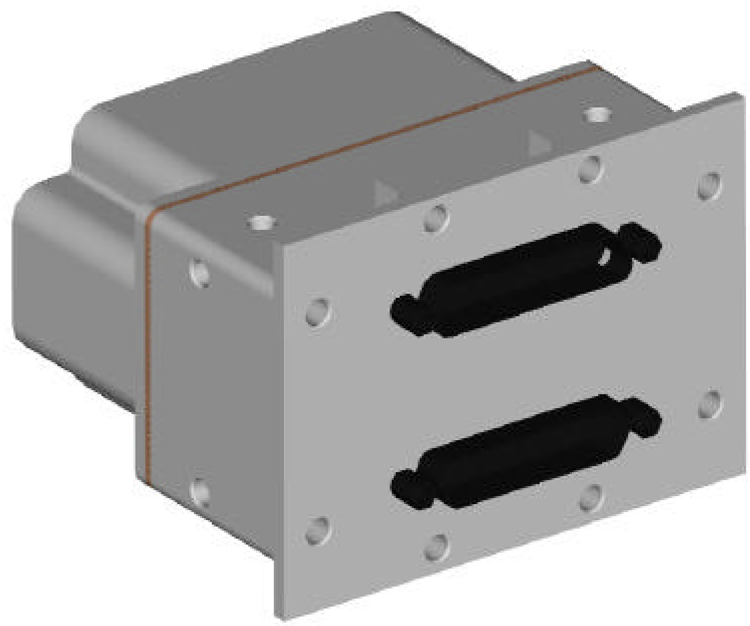


Initial EM JFET module (unpopulated) thru final etch

Open Issues and Mitigations

- Low yield during membrane release etch
  - Increased membrane thickness to 1.8um
  - Utilized lower stress epoxy for bonding U401 dies to membrane
  - Low stress etch fixture implemented in release etch
- Lithography errors
  - Implemented E-beam direct write for resistors and leads
- Yields
  - High yields but yet to be quantified

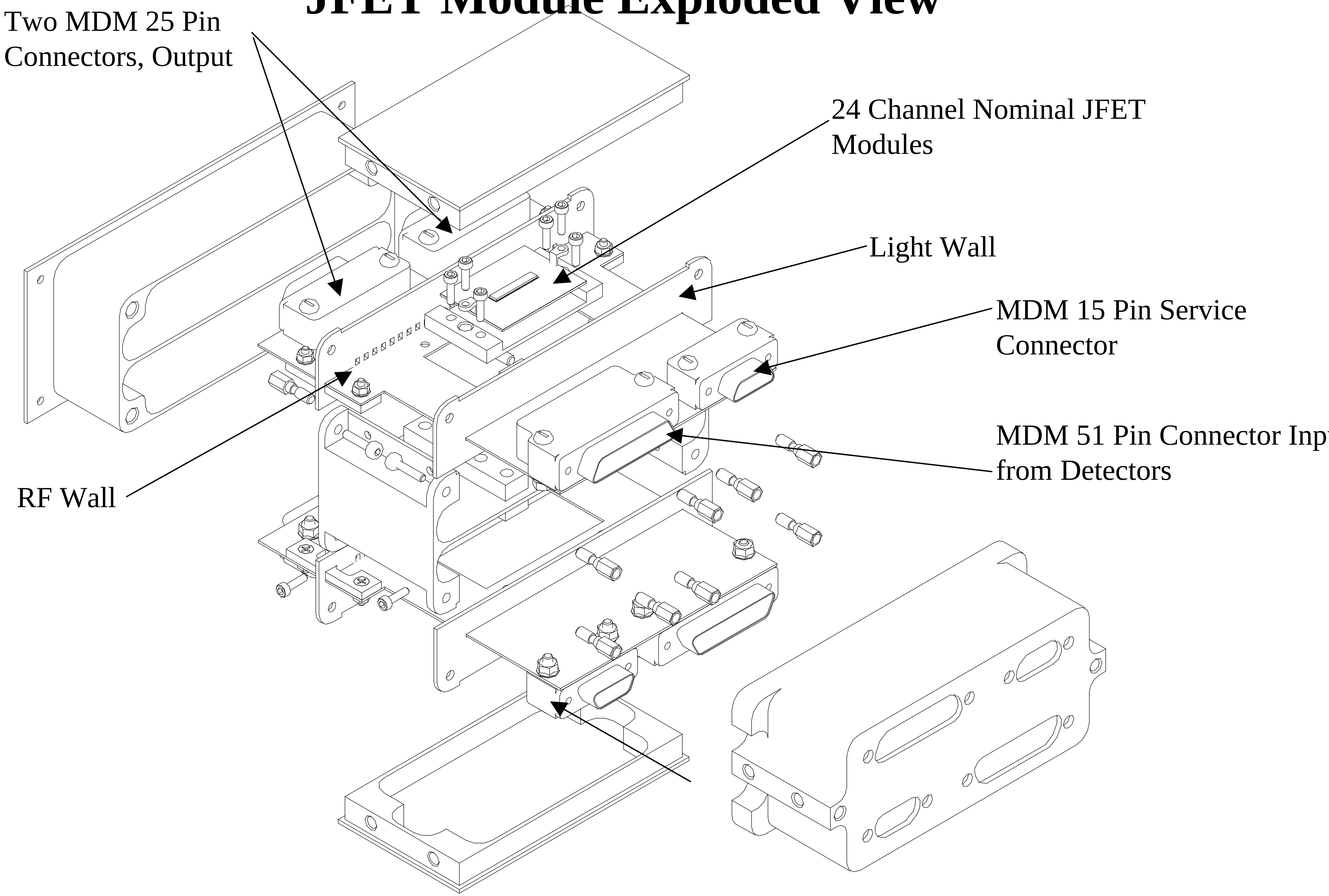




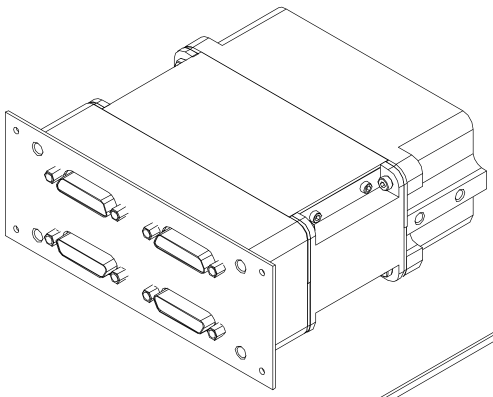
6.4
JFET and RF Module Mechanical Design

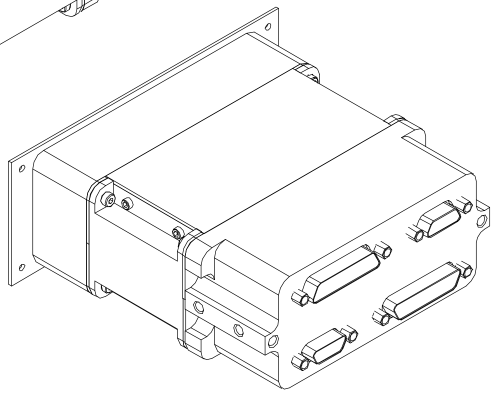
Dustin Crumb

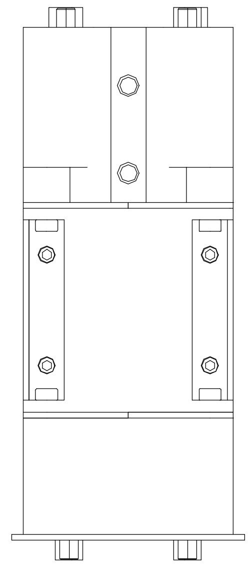
JFET Module Exploded View

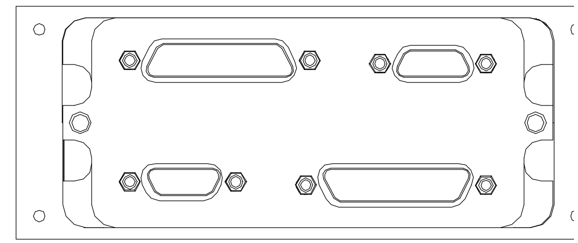


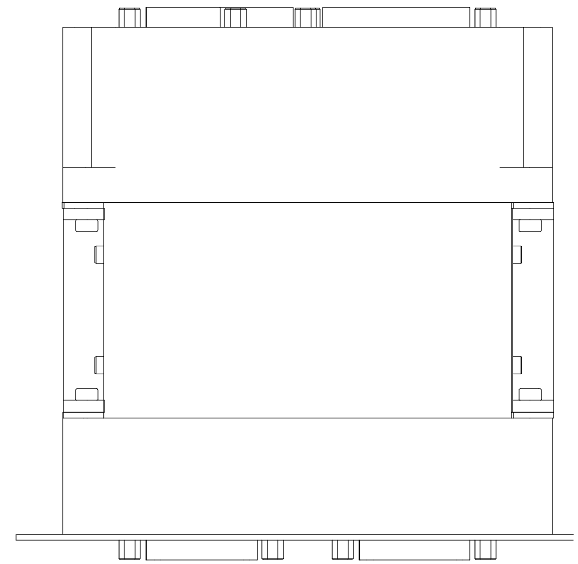
48 Channel JFET Module

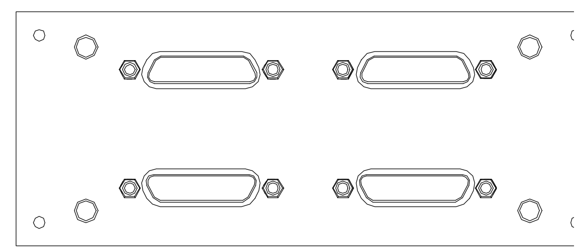




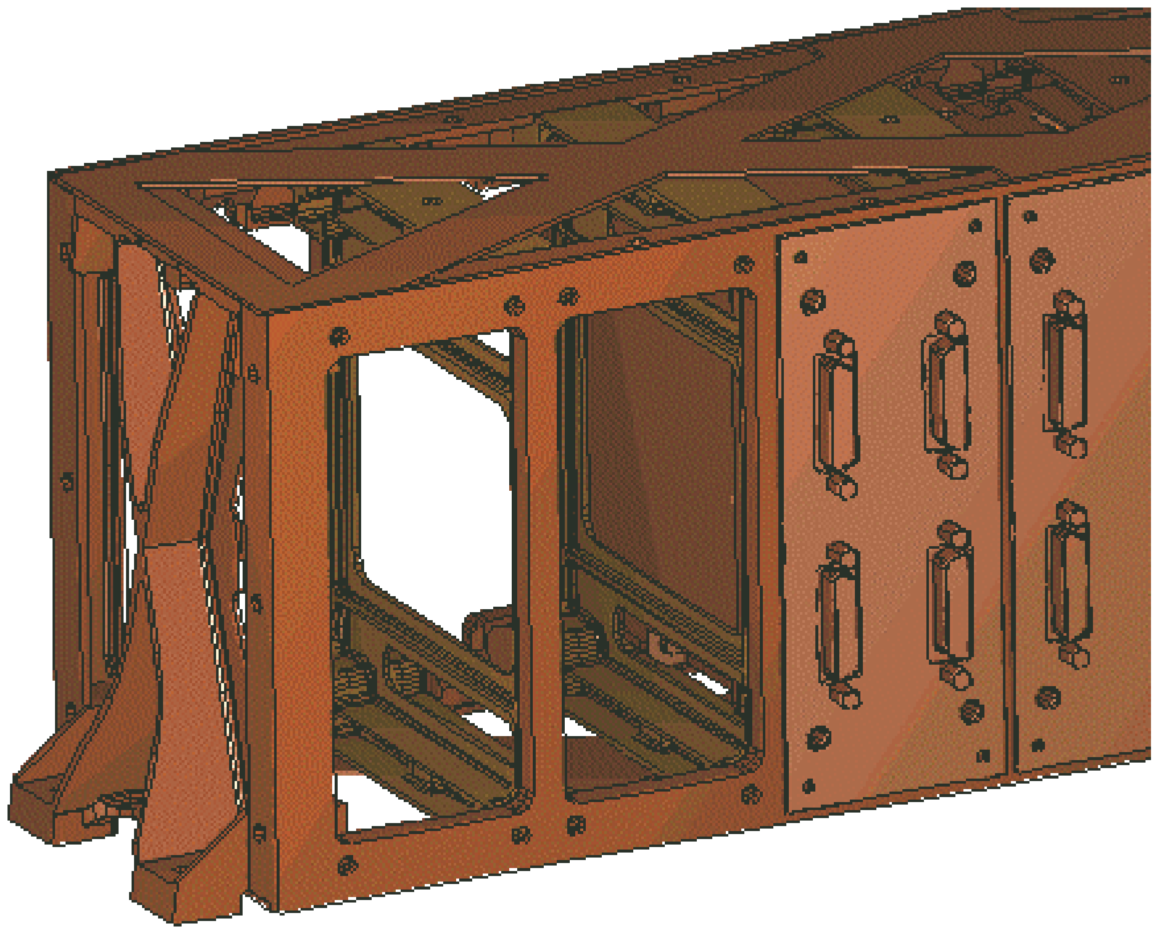






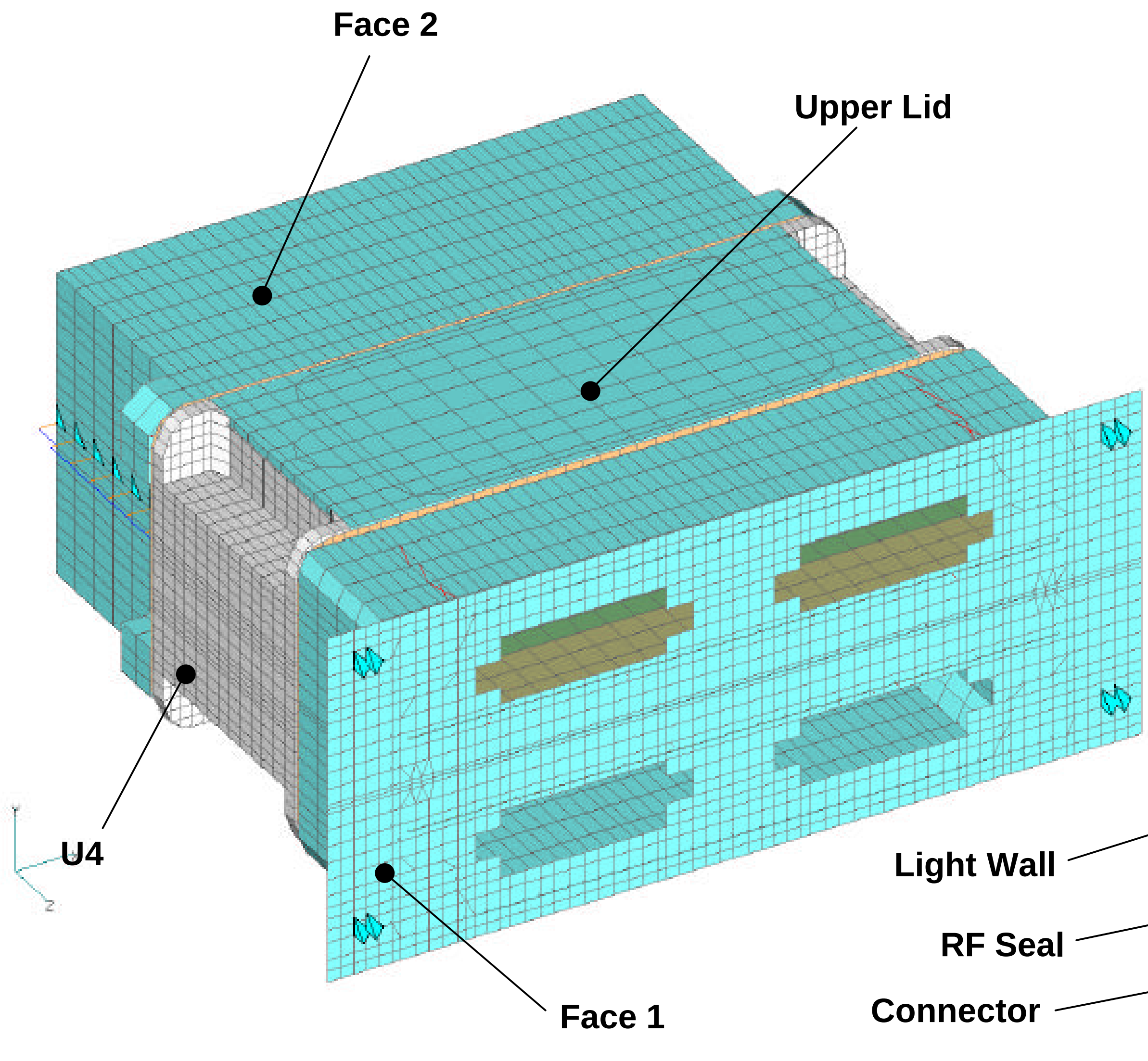


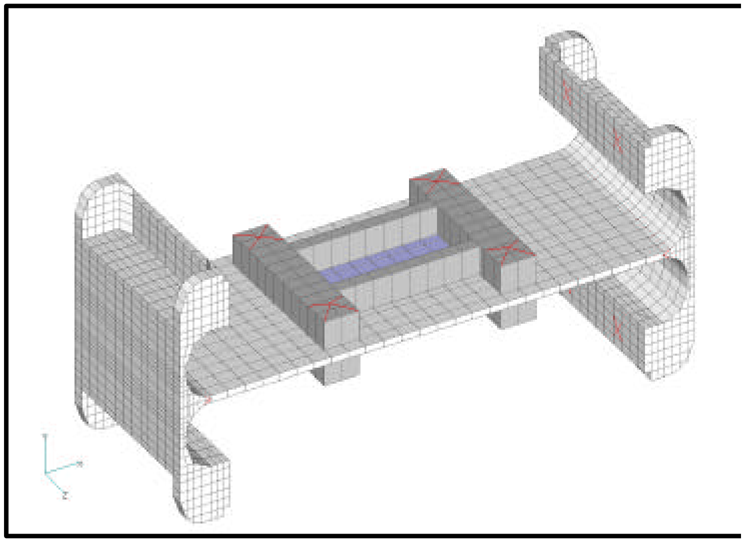
JFET Module Support Structure (RAL Responsibility)



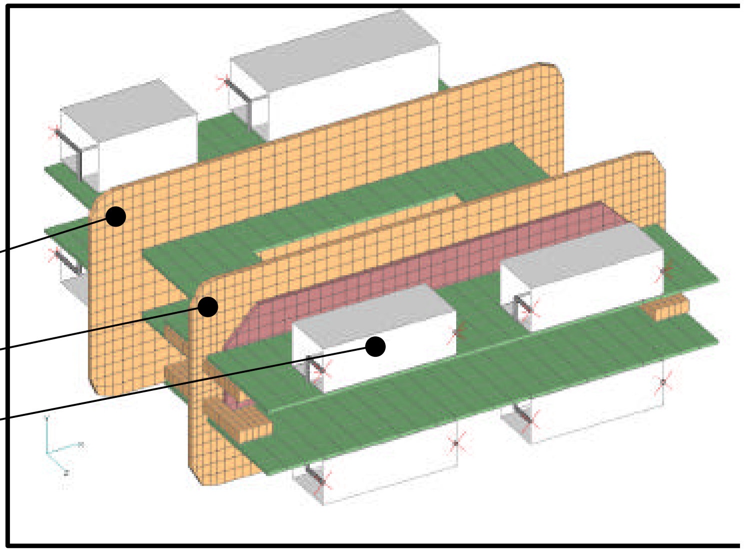
JFET Structural Analysis

Structural Analysis - JFET





U4



Internal Electrical Components

Mass = 277 grams **Elements = 14940** **Nodes = 12100**

Structural Analysis - JFET

Part = = = = = >	**U4, Face 1, Face 2**	**Light Wall & RF Seal**
Material/Temper	Alum 6061-T651 or T62	Alum 6061-T6 or T62
MIL-HDBK-5H Ref	Table 3.6.2.0(b_2)	Table 3.6.2.0(b_1)
Billet Thick Column	.250 - 2.000	.010 - .249
Form	Plate	Sheet
Basis	A	A
Ftu, ksi		
L	42	42
LT	42	42
Fty, ksi		
L	36	36
LT	35	35
Fcy, ksi		
L	35	35
LT	36	36
Fsu, ksi	27	27
Fbru, ksi		
(e/D = 1.5)	67	67
(e/D = 2.0)	88	88
Fbry, ksi		
(e/D = 1.5)	50	50
(e/D = 2.0)	58	58
E, 10^3 ksi	9.9	
G, 10^3 ksi	3.8	
μ	0.33	
ρ, lb/in^3	0.098	

Structural Analysis - JFET

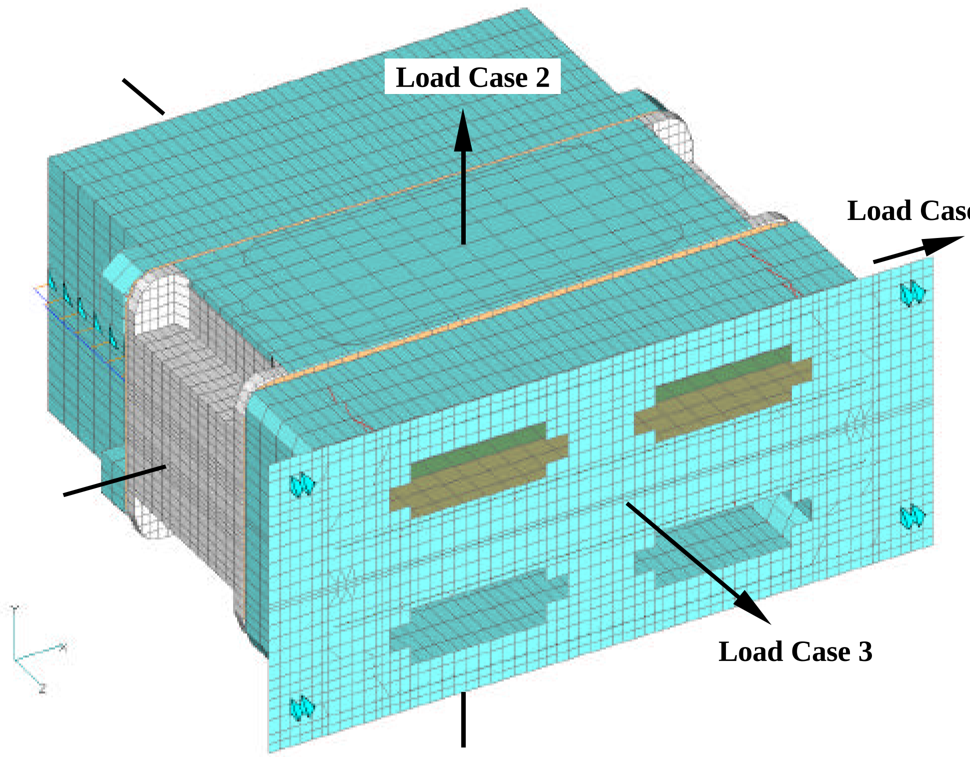
- Analysis Requirements Used to Verify Structural Integrity
  - Qualification Random Vibration (IID - A)

Location	Axis	Freq Range	Density	RMS Value
Herschel Optical Bench	ALL	20 - 80 Hz 80 - 300 Hz 300 - 2000 Hz	+3 db/Oct .077 G^2/Hz -6 db/Hz	6.67 G

  - F
    - FS_{yld} = 1.25
    - FS_{ult} = 1.4
    - Unconventional Material FS_{ult} = 2.0
  - Limit Loads (ERD D-19155)
    - 20G Any Direction

Structural Analysis - JFET

- Load Cases (applied in three directions deemed most critical for stress)
  - Each load case consists of:
    - 32 G Quasi Static Equivalent Load
      - 1.5% Damping used in RV analysis (JPL Std.)
      - 3s Value
      - Value above Limit Load requirement; wanted to assess capability
    - Thermal transistion from 70°F to -442°F
- Constraints
  - Fixed at JFET-to-JFET Rack fastener loacations



Structural Analysis - JFET

Margin of Safety Summary Tables
(In Progress, will be ready by CDR)

Structural Analysis - JFET

- Computer Model Validation - Comparison to Test Data
  - Modal Frequencies
    - Tests still need to be performed

Table of Computer Model's First Three Modes
(In progress, will be ready by CDR)

Structural Analysis - JFET

- Where Are We Now?
  - Incorporate latest design changes and finalize analysis
  - Once testing is complete, verify FEM model results against test data

6.5
JFET Module Assembly/Manufacturing

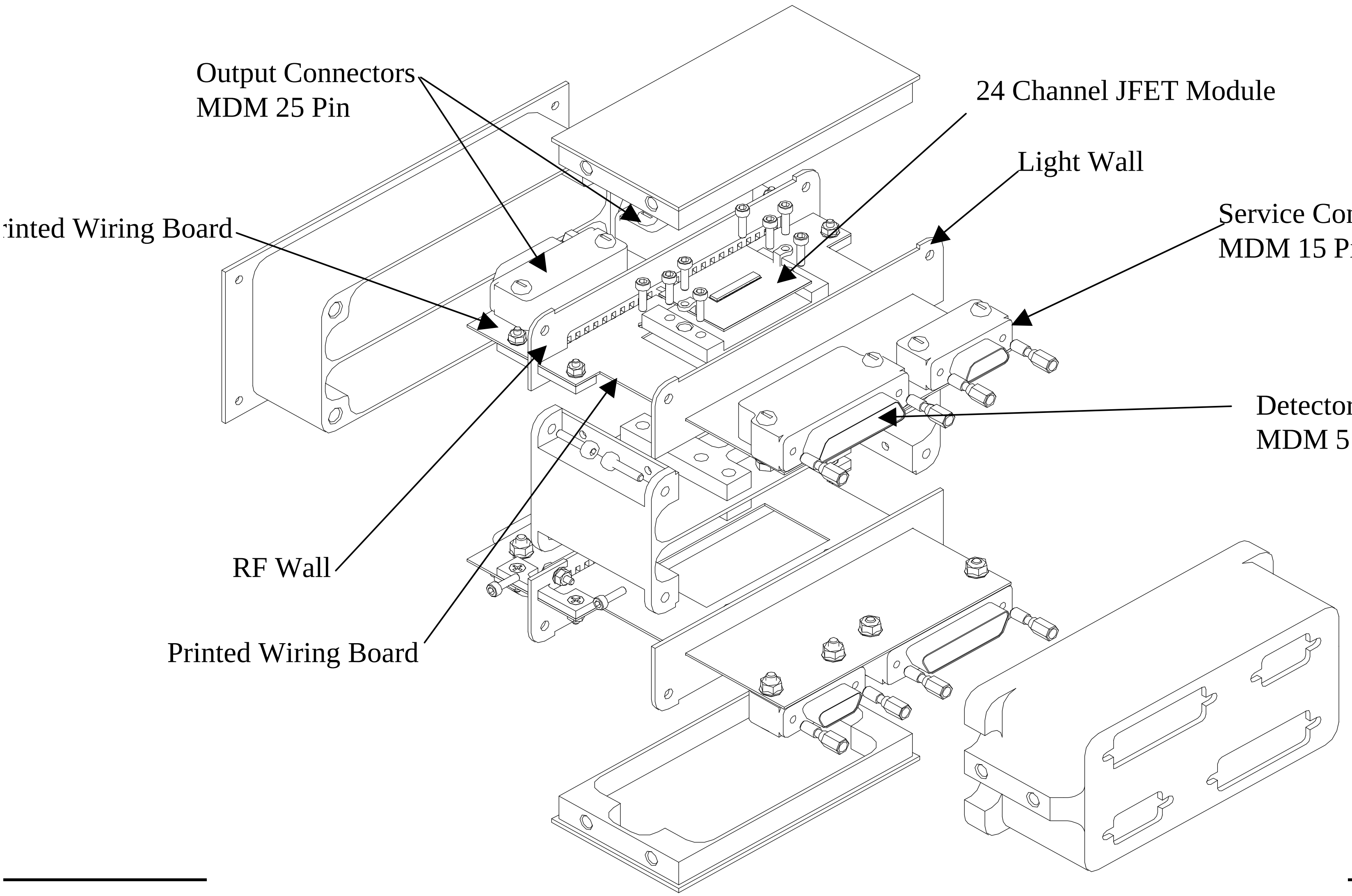
Leonard Husted

JFET Assembly Manufacturing

- Contents
  - Exploded Views
  - Assembly Documentation Required
  - Manufacturing Processes
  - Tooling
  - Manufacturing Process Flow
  - Summary

JFET Assembly Manufacturing

- JFET Assembly Exploded View



JFET Assembly Manufacturing

- Documentation Required

Document Title	Number	Status		
		In work	Complete	Released
JFET Module Assembly Drawing	10209750	x	75%	8/17/01
JFET Isolation Assembly Drawing	10209757	x	75%	8/17/01
JFET PCB Assembly Drawing	10209760	x	75%	8/17/01
JFET Wire Bonding Diagram	TBD			8/24/01
AIDS-JFET Module Assy	TBD	x	60%	8/24/01
AIDS- JFET PCB Assy	TBD			8/24/01

JFET Assembly Manufacturing

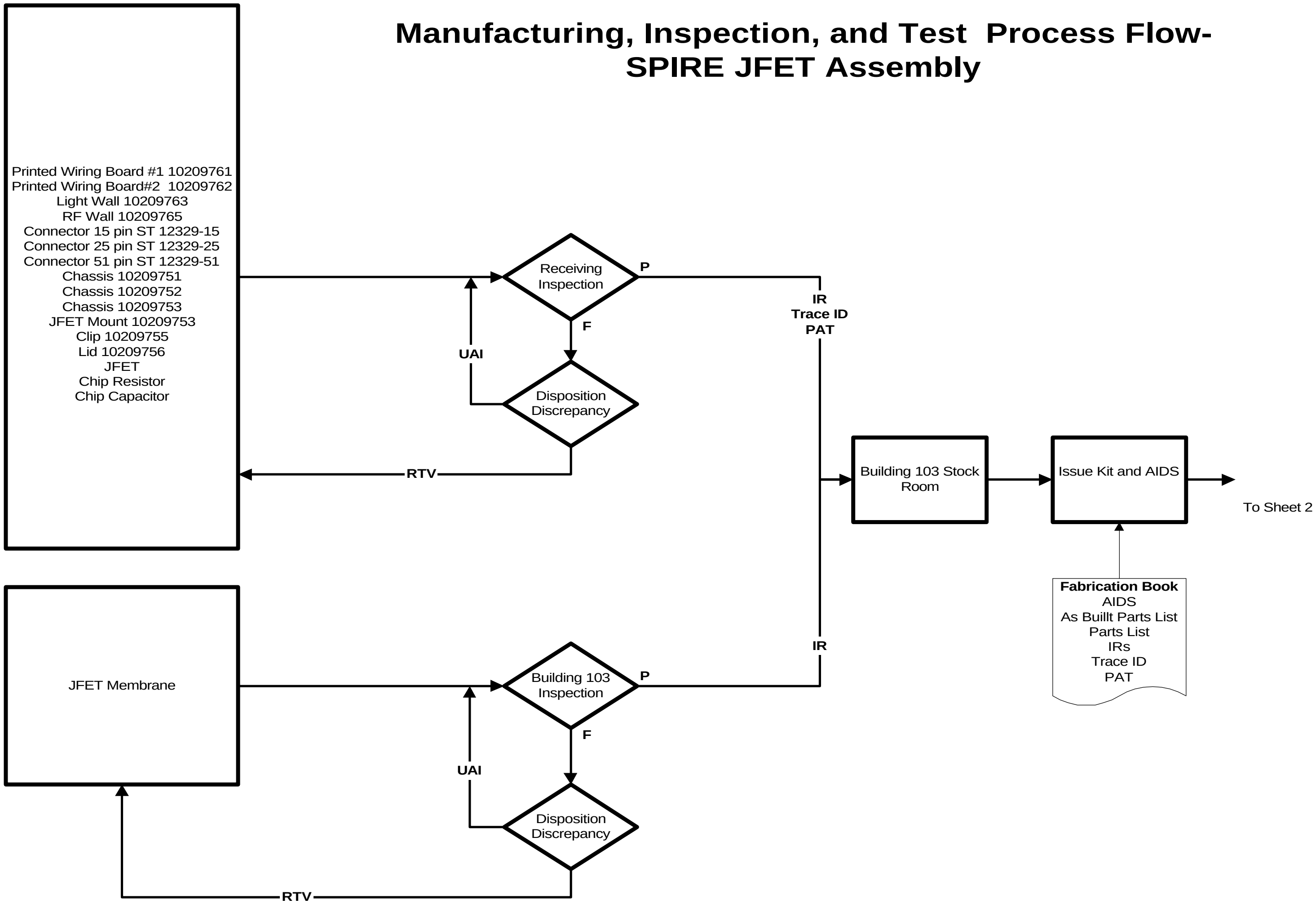
- Manufacturing Processes

Process	Std	Procedure	Requirement
Cleaning	YES	FP 513414	Drawing
Adhesive Bonding	YES	FP 513414 Sect 9.0	Drawing
Wire Bonding	YES	FP 513414 Sect 10.18	Mil-Std-883 M2011.7
Die Attach	YES	FP 513414 Sect 10.14	Mil-Std-883 M2019.5
Soldering	YES	FP 513414 Sect 6.1.2	D 8208
Solder Tinning	YES	FP 513414 Sect 6.2.2	D 8208
Torque	YES	ES 517040	Drawing
Vacuum Bake	YES	FP 513414 Sect 6.1.2	
Mechanical Assembly	YES	AIDS	Drawing
Inspection	YES	AIDS	Drawing
Electrical Test (JFET PCB Assy)	NO	Test Procedure TBD	TBD
Conformal Coat	YES	FP 513414 Sect 9.5	Drawing
Identification	YES	FP 513414 Sect 9.0	Drawing

JFET Assembly Manufacturing

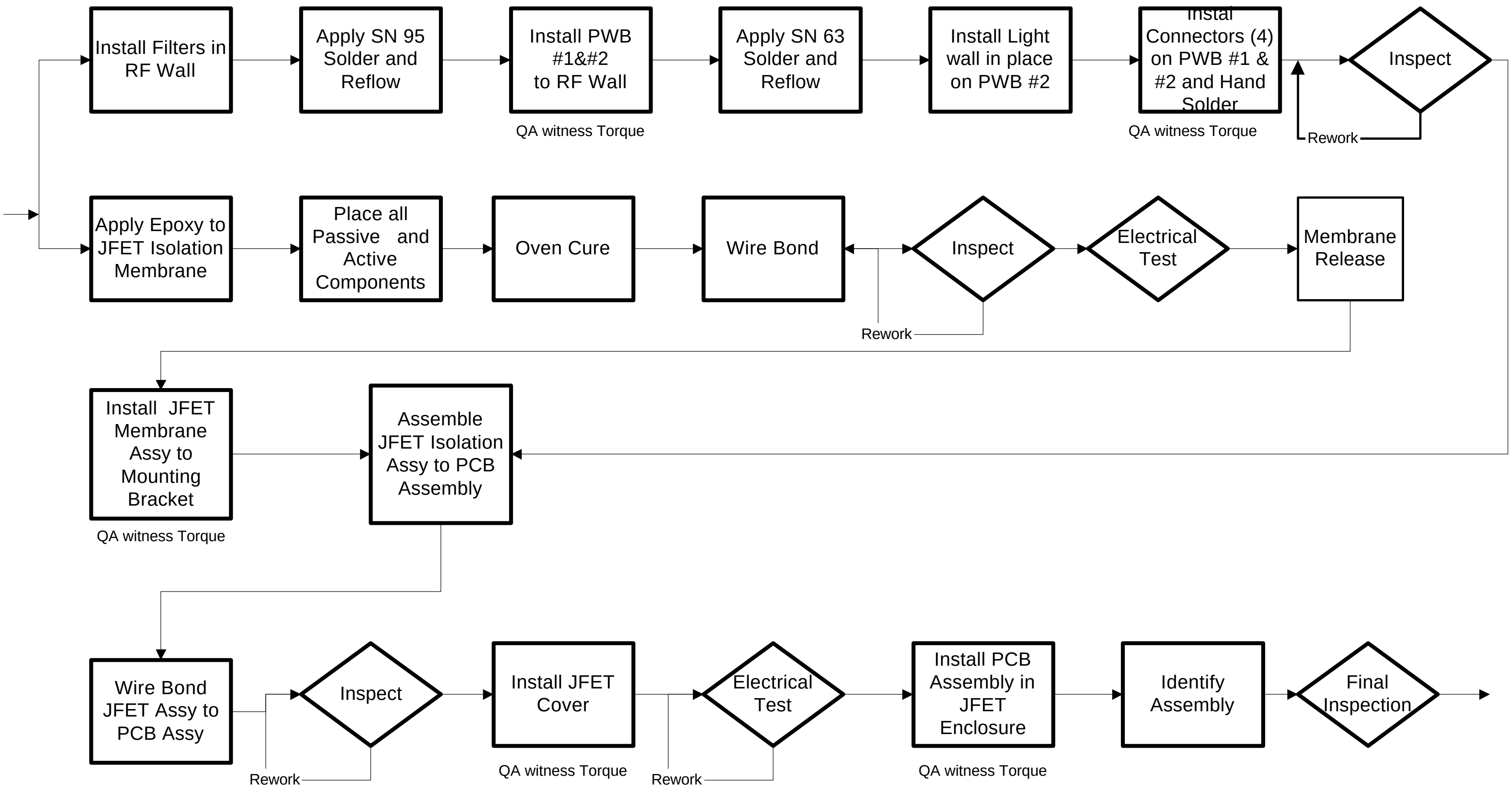
- Tooling Required
  - JFET Assembly
    - RF Wall Reflow Solder Fixture
    - Printed Circuit Board Reflow Solder Fixture
    - JFET Wire Bonding Fixture
    - Holding Fixture

JFET Assembly Manufacturing



JFET Assembly Manufacturing

Manufacturing, Inspection, and Test Process Flow-
SPIRE JFET Assembly



BDA Manufacturing

- Summary

Methods/Process Development Needed

Filter installation in RF Wall

Wire Bonding JFET Module

Wire Bonding JFET Module to PWB

Test Fixture at JFET Module Level

Assembly Tooling

Open Issues

Drawings incomplete

AIDS incomplete

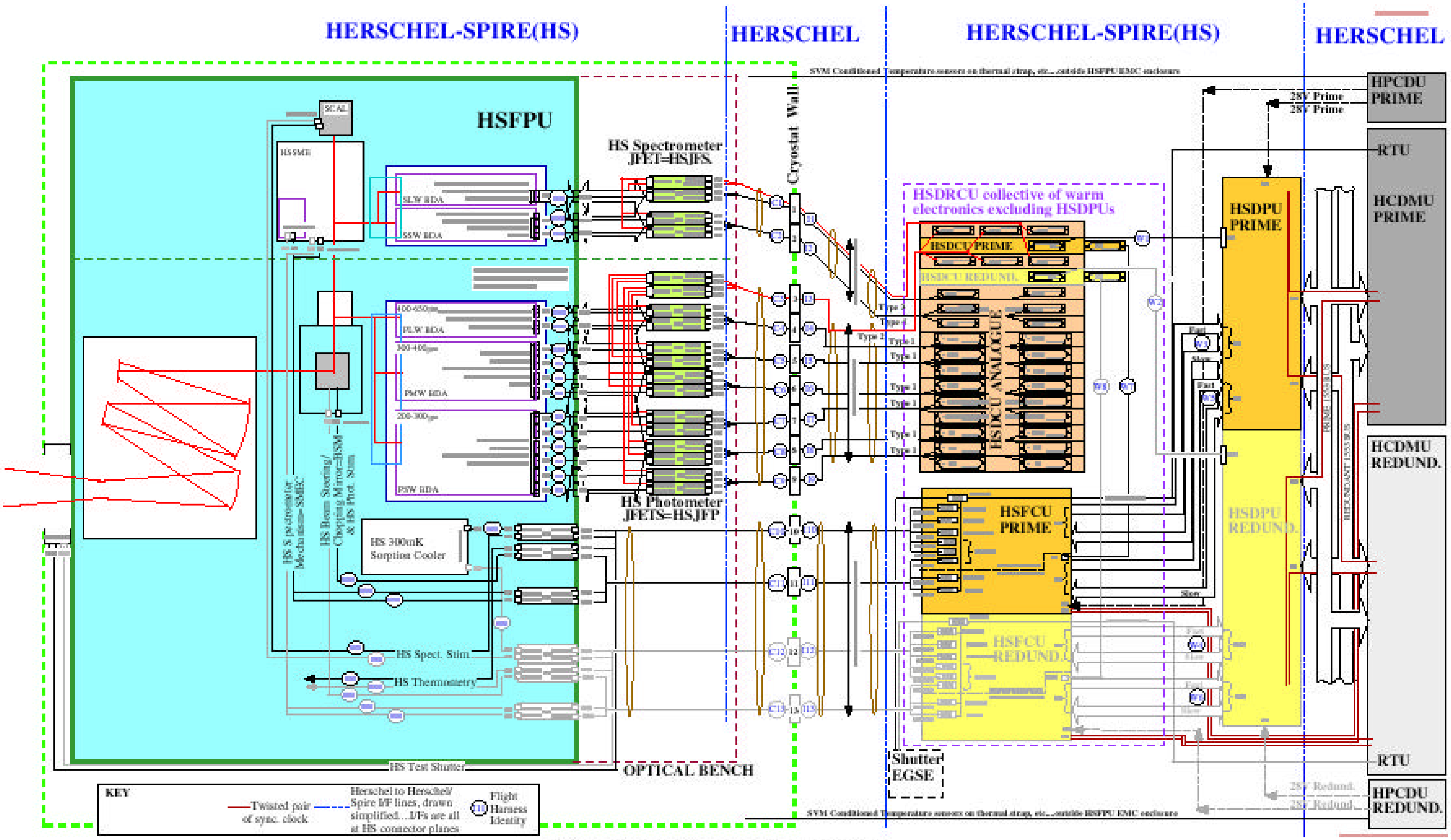
7.0
Harness Definition And Test Procedures

Viktor Hristov

Electrical Interface

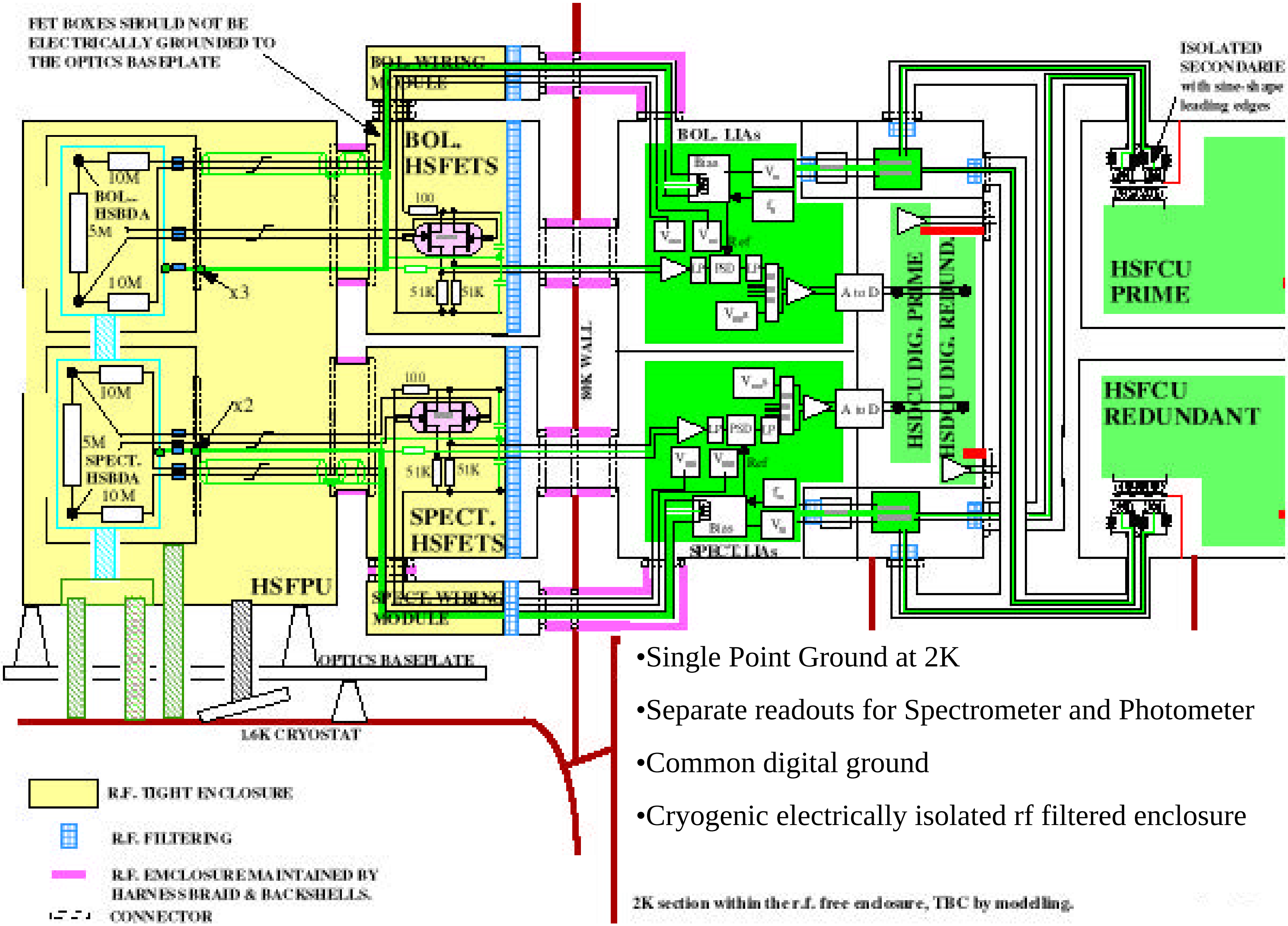
- Harness Definition Document defines the electrical interface for the various Hershel-Spire modules
- This document is written by RAL and agreed to by CEA and JPL
- The document defines the:
  - electrical connections,
  - shielding and bundling of cables,
  - grounding network,
  - cable impedance,
  - microphonics,
  - capacitance,
  - thermal properties.

SPIRE Block Diagram



Spire Block Diagram Figure 5.2.1

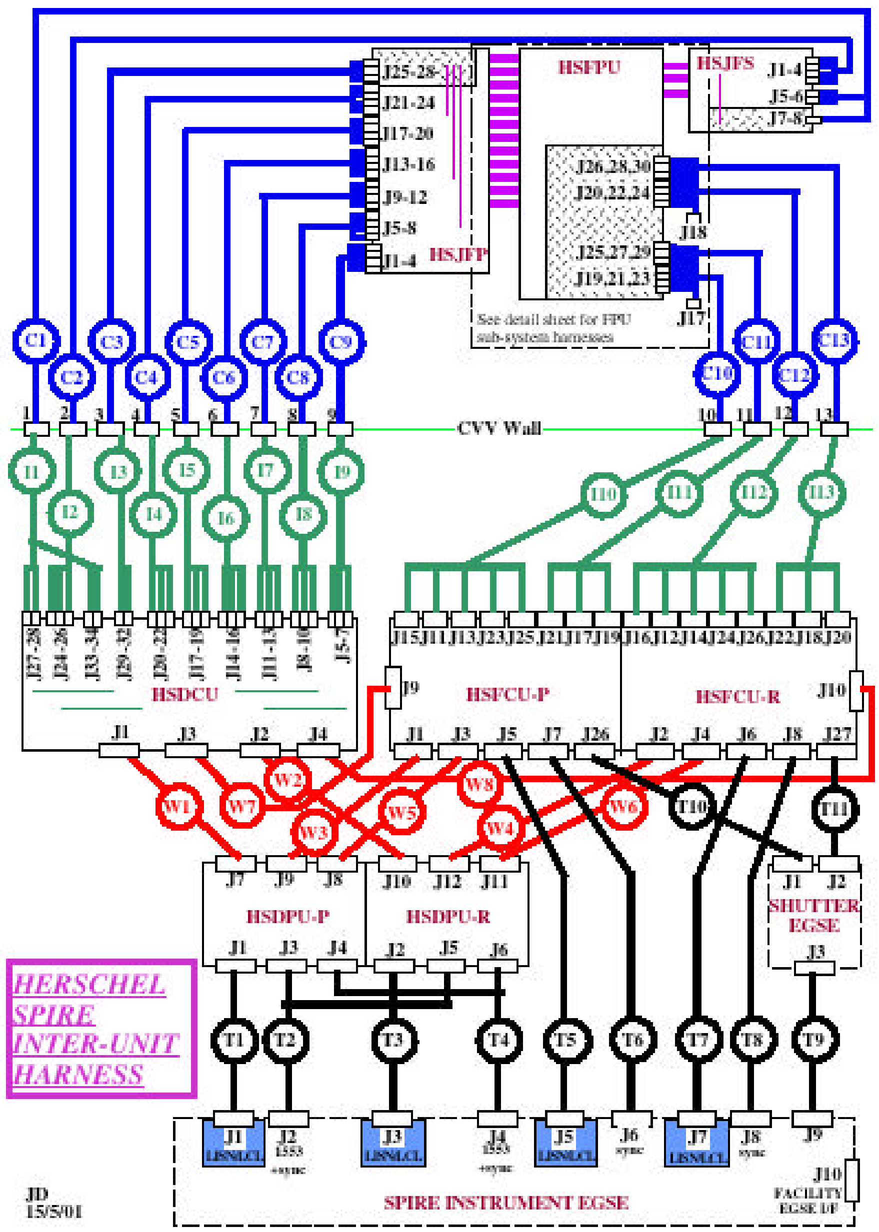
Grounding Diagram

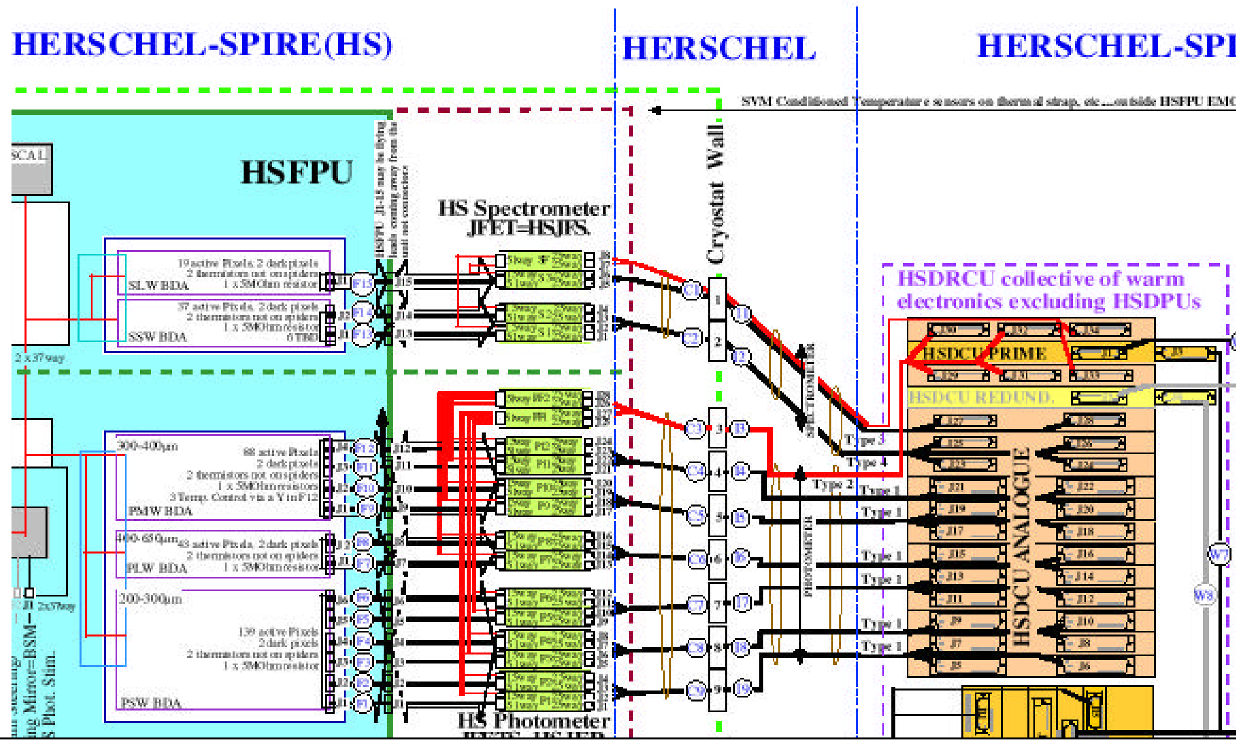


- Single Point Ground at 2K
- Separate readouts for Spectrometer and Photometer
- Common digital ground
- Cryogenic electrically isolated rf filtered enclosure

2K section within the r.f. free enclosure, TBC by modelling.

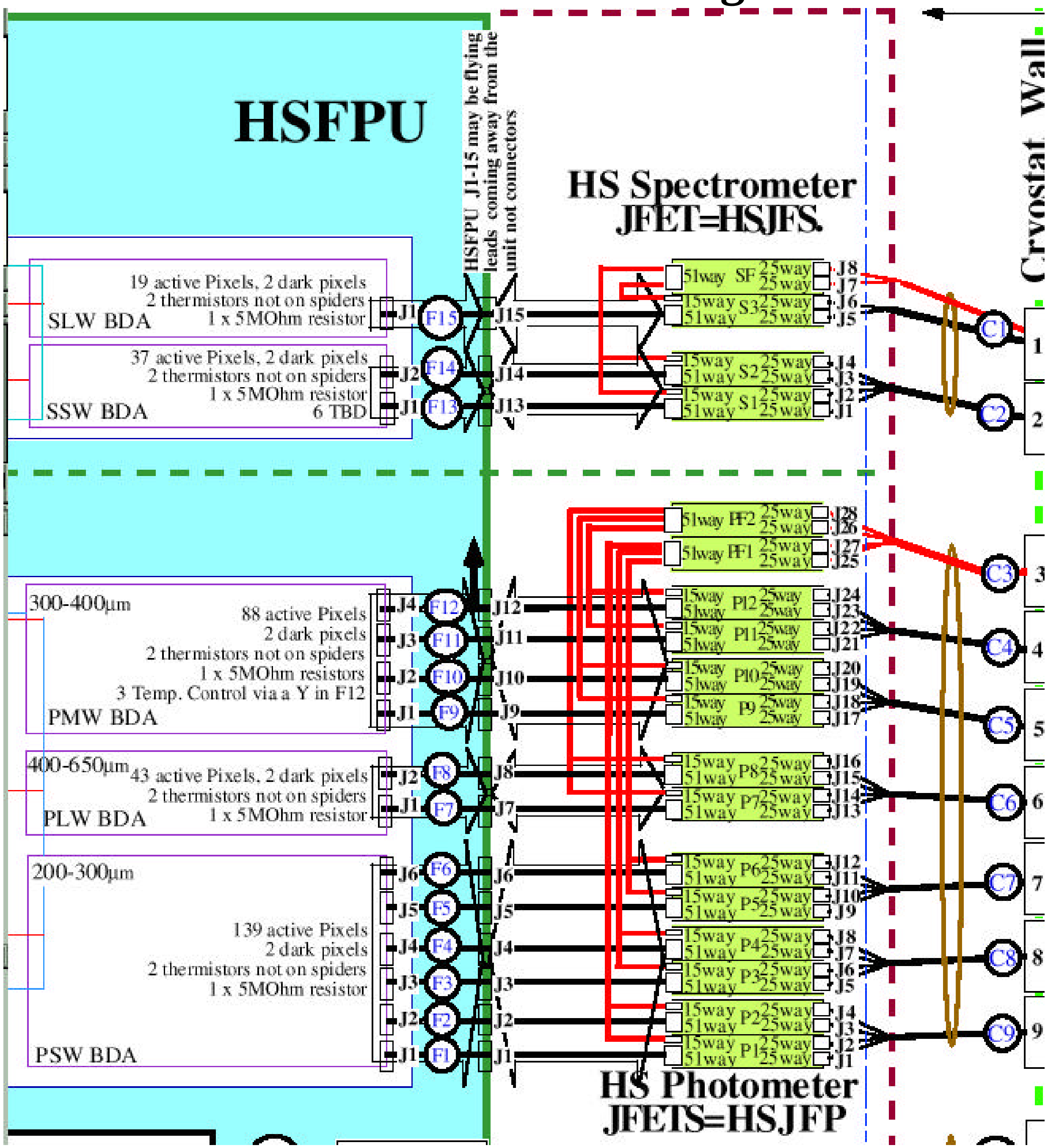
Harness Diagram



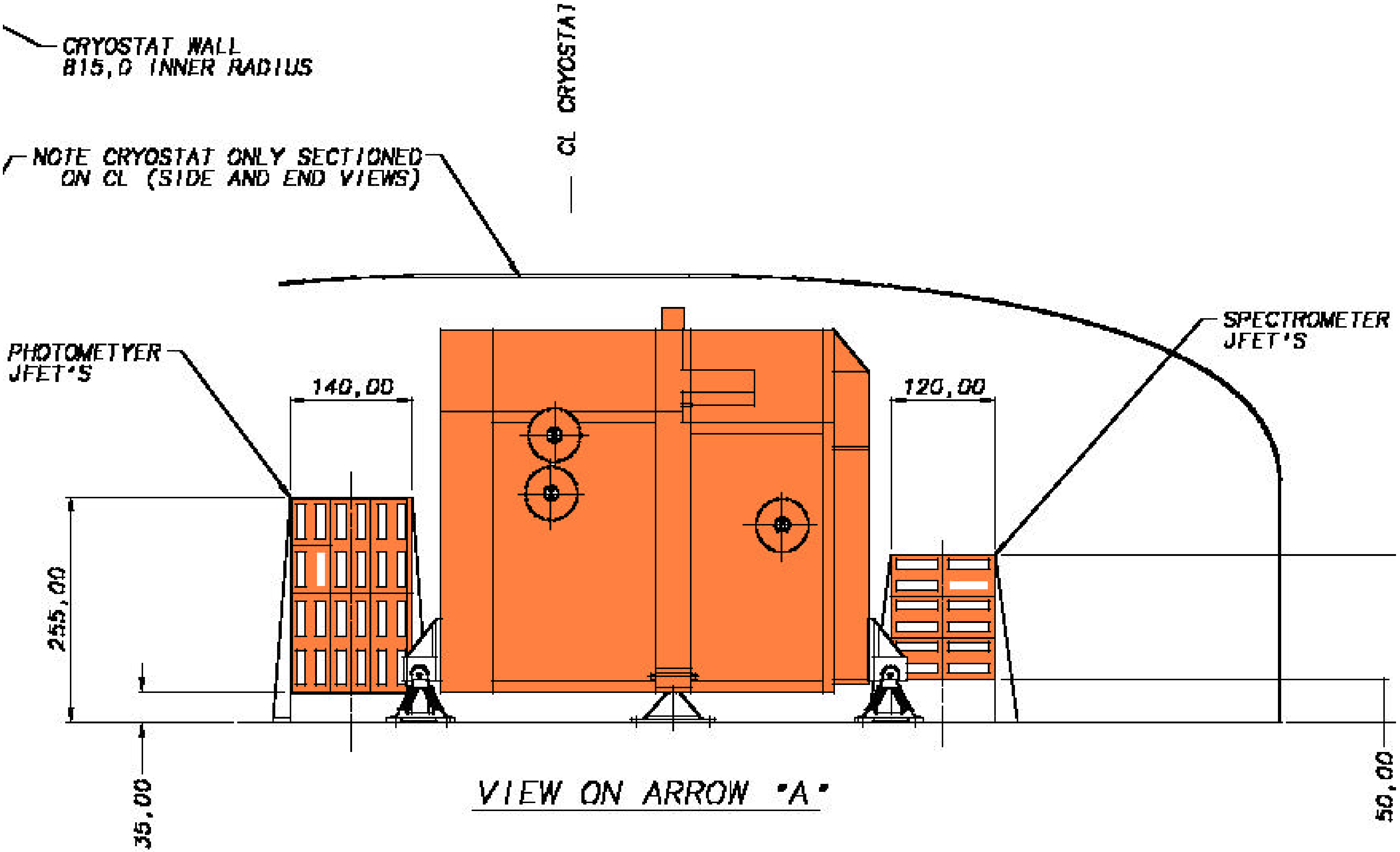


SPIRE Block Diagram
JPL Related

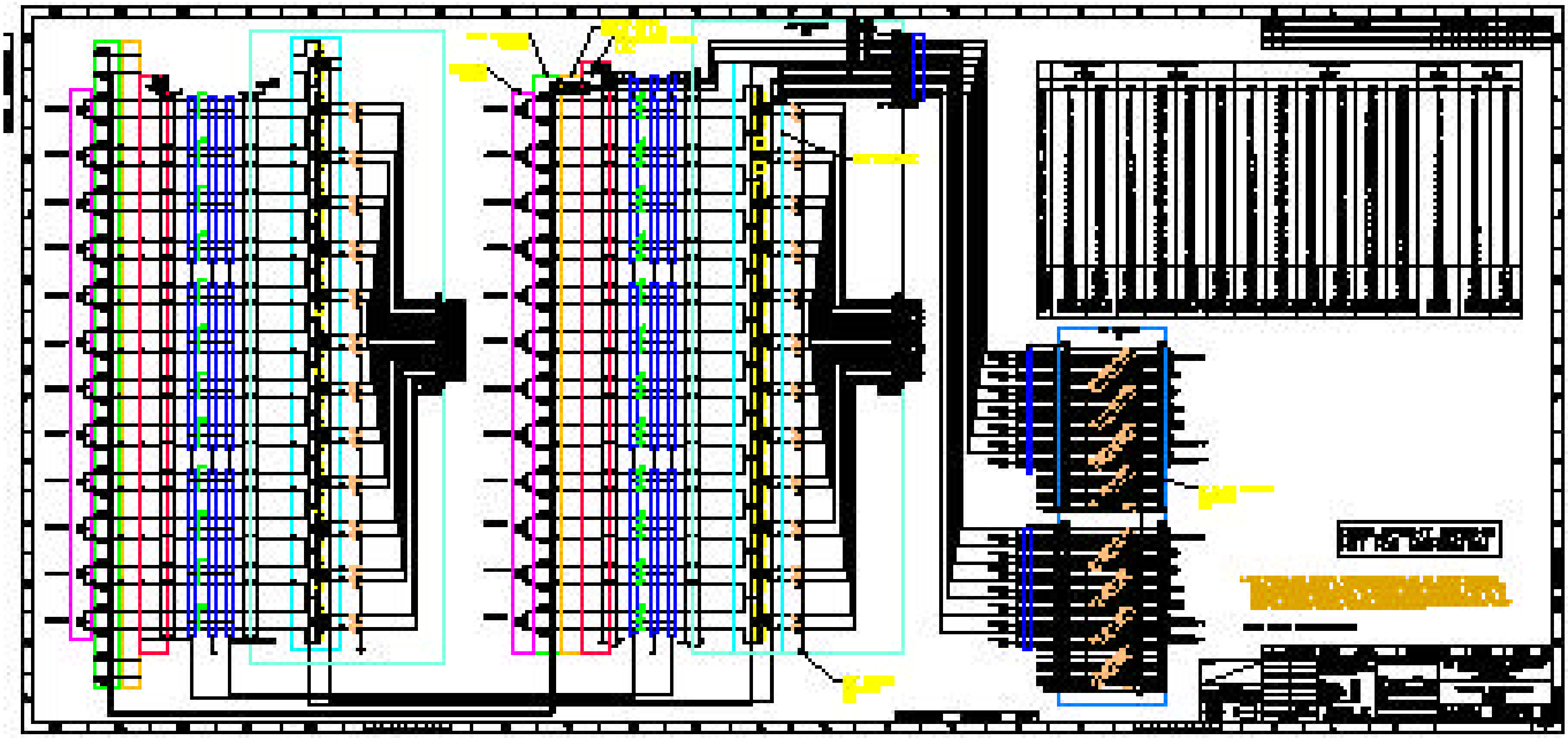
BDA to JFET Wiring



RF Architecture

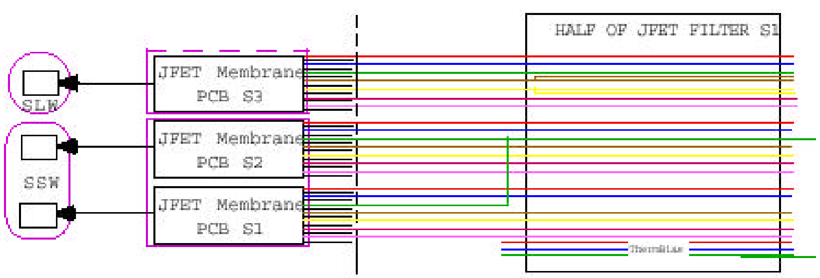


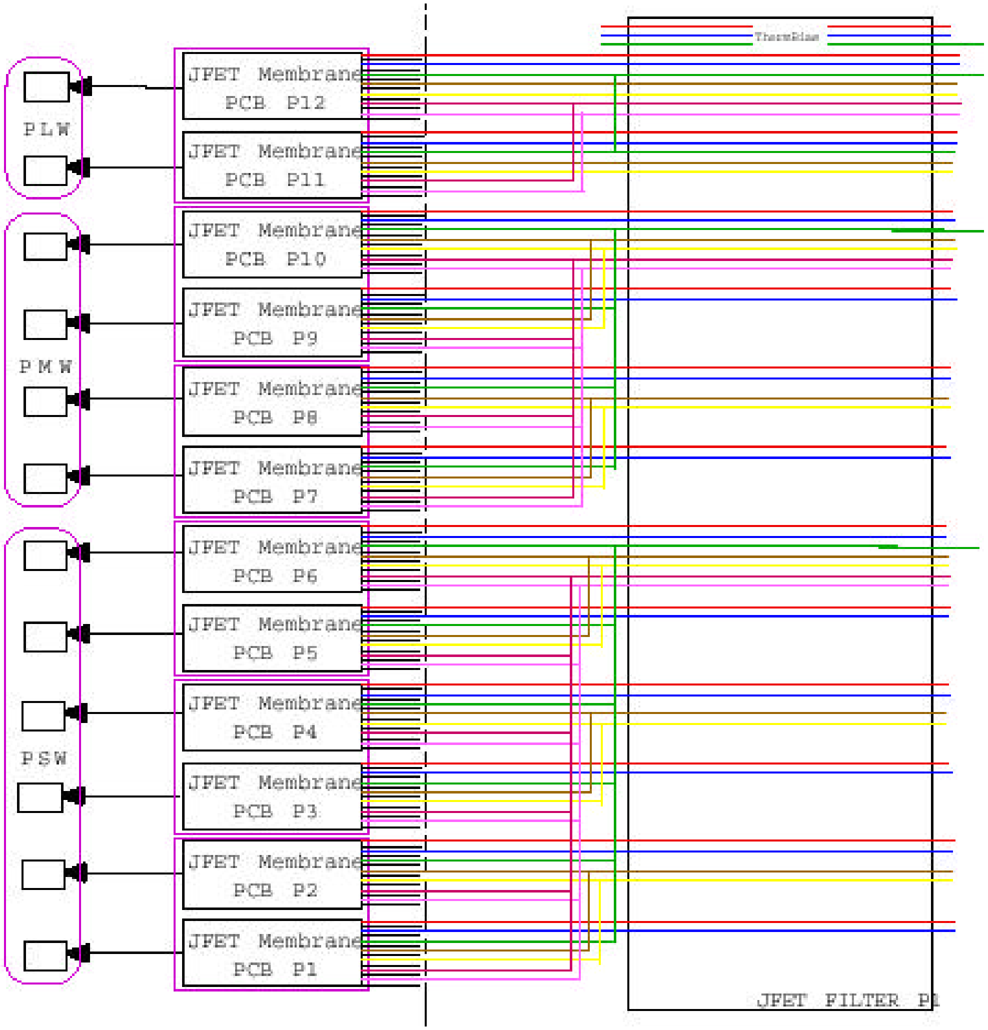
Wiring Chain



COLD RF FILTERS: BIAS AND COLD JFET POWER DISTRIBUTION

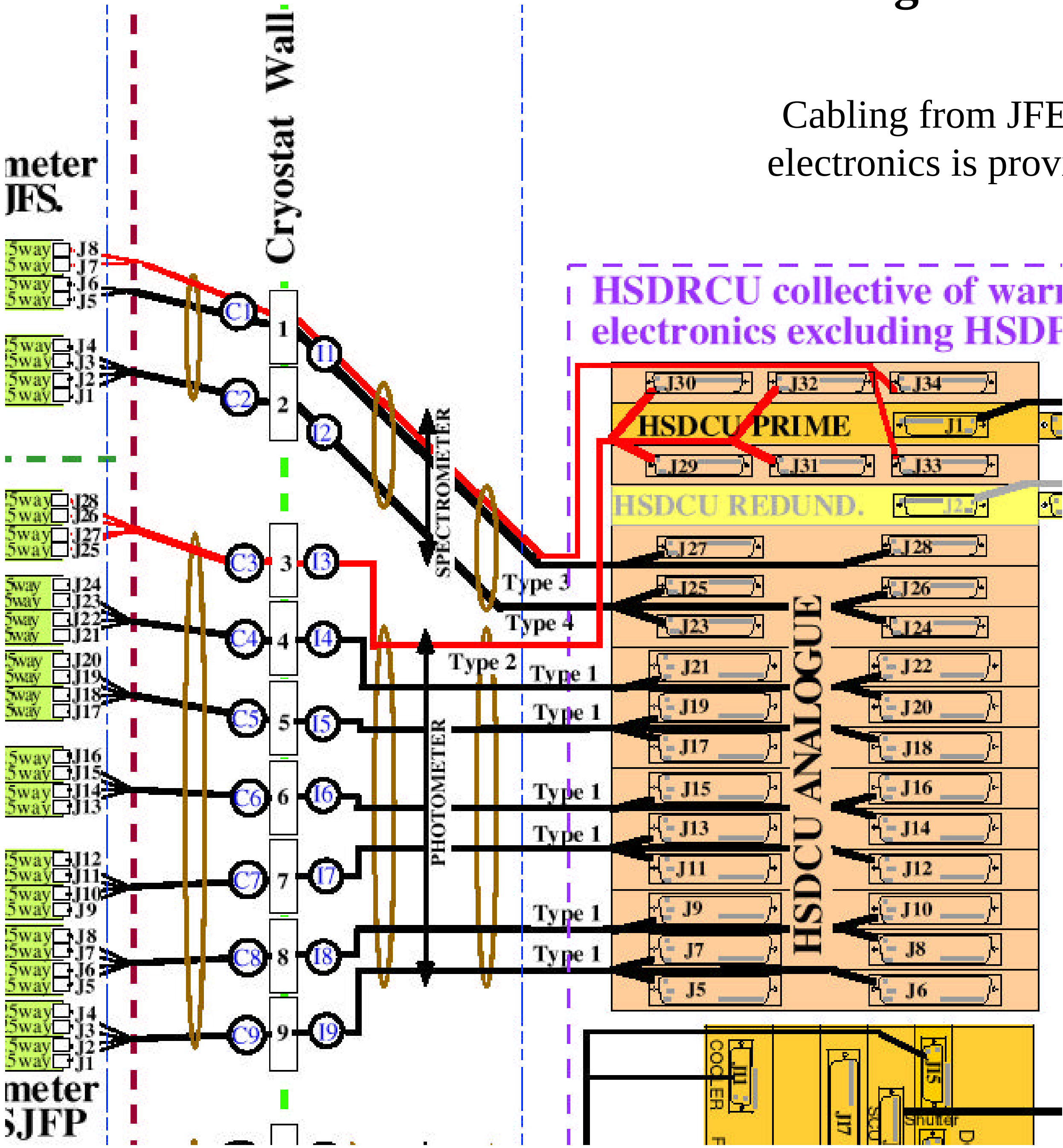
Function	A-wire	B-wire
JFET V-	1	8
JFET V +	10	14
JFET Vgnd	9	15
Bias +	2	7
Bias -	4	5
Heater +	3	6
Heater -	11	13





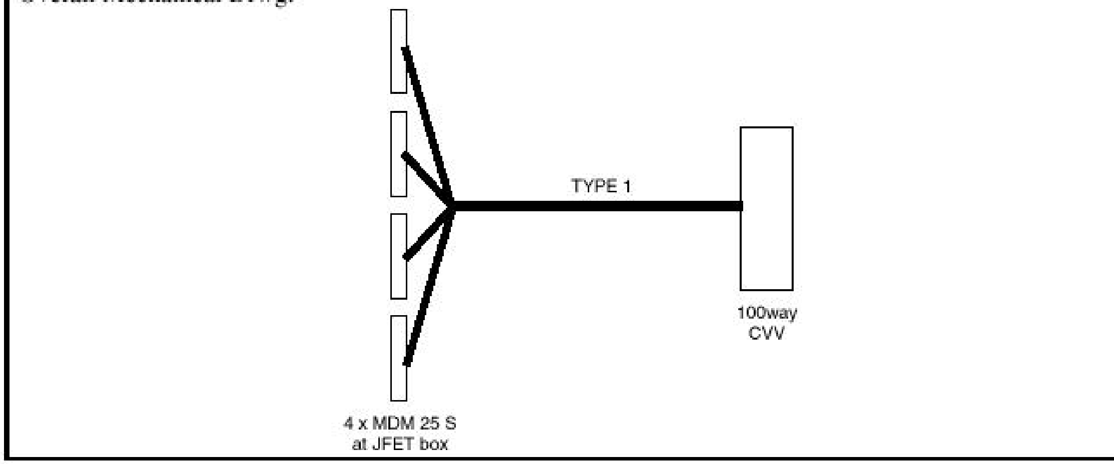
JFET to Warm Electronics Wiring

Cabling from JFETs to warm electronics is provided by ESA

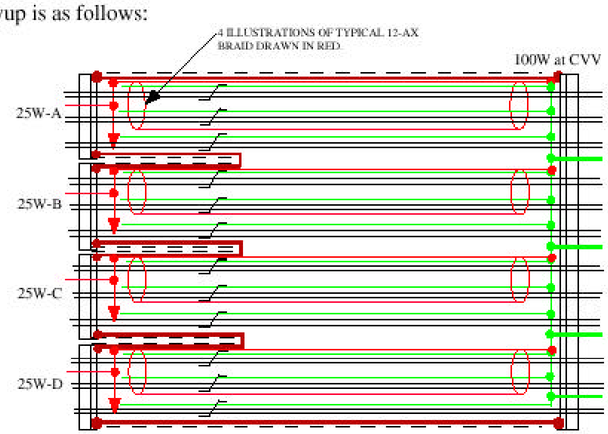


Low Impedance Cabling

Overall Mechanical Drwg.



Harness Layup
The total harness layup is as follows:

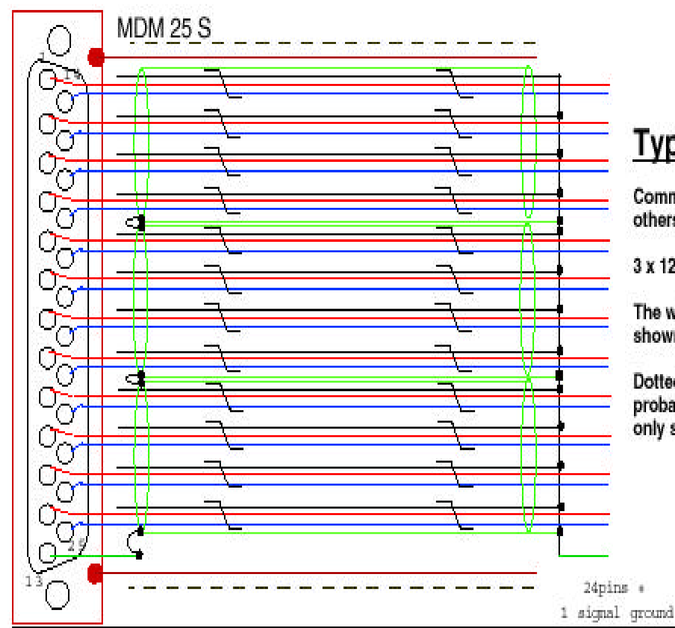


There are 48 channels each carried as a twisted triple, grouped in fours as "12-ax", each with its own insulated screen. So there are 12 x 12-ax in all with three 12-ax to each 25 way MDM. The use of a third wire twisted with each channel's + & - signal wires minimises interchnnel cross-talk inside each 12-ax.

As for the intermediate harness, 4 pins carry ground through the 100 way and carry an isolated ground ring. All the third wires are made off to this, as are all the 12-ax screens.

At the 25way MDMs, the three 12-ax braids (which have a much higher conductivity than that of the sum of all the third twisted wires) are joined and pass through pin7. The third wires are shown as left open here as physically joining them all at MDM geometry seems unfeasible and uncondicive to a neat layup.

To keep RF screening distinct from low noisr bolomter grounds, all of this harness is enclosed in separate outer r.f. screen, EMC sealed to connector boots, overwrapped with insulation.



Type 1 JFET tails

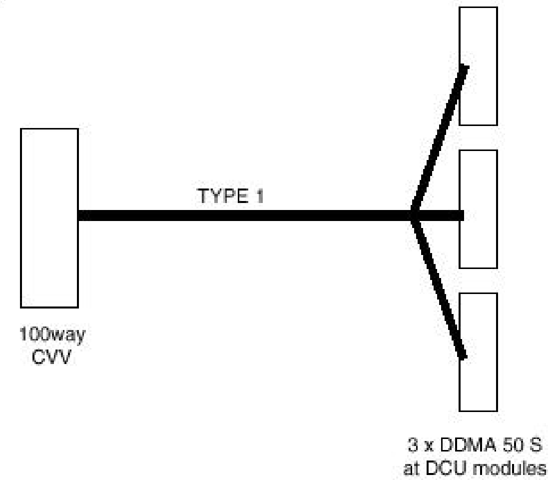
Common to all 3 tails, although others have channels 12-24, etc..

3 x 12-ax cables

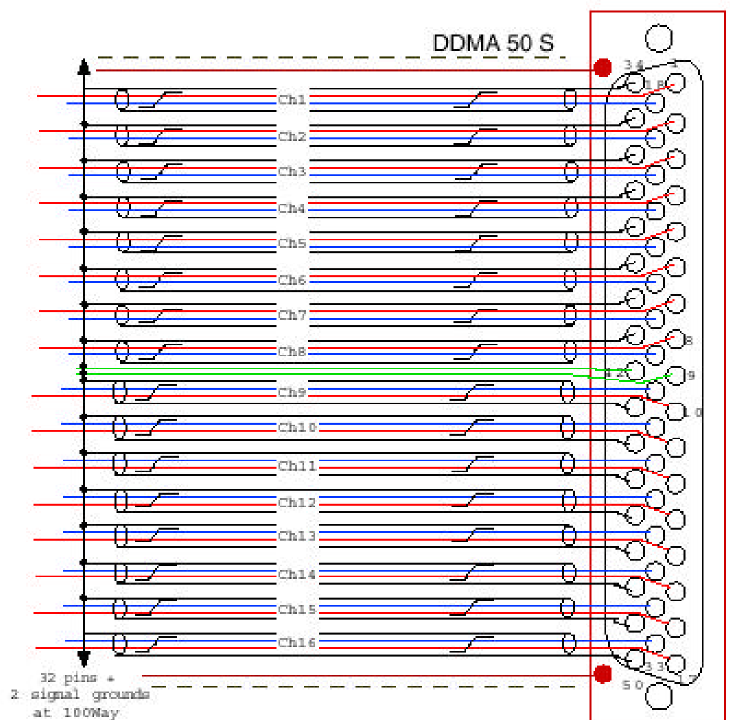
The whole overlain with RF screen shown:

Dotted lines show insulation, probably put around bundles but only strictly needed at clamp points.

Overall Mechanical Drwg.



Harness Layup



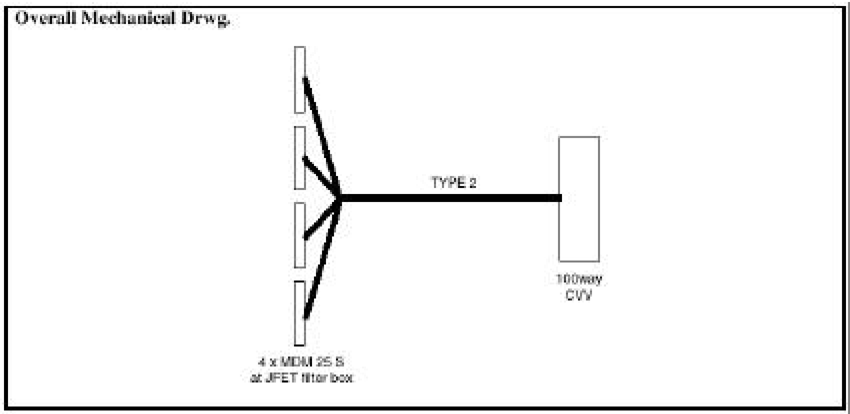
Type 1 DCU tails

Common to all 3 tails, although others have ch. 17-32 and 33-48. Good flat layup for cryoharness

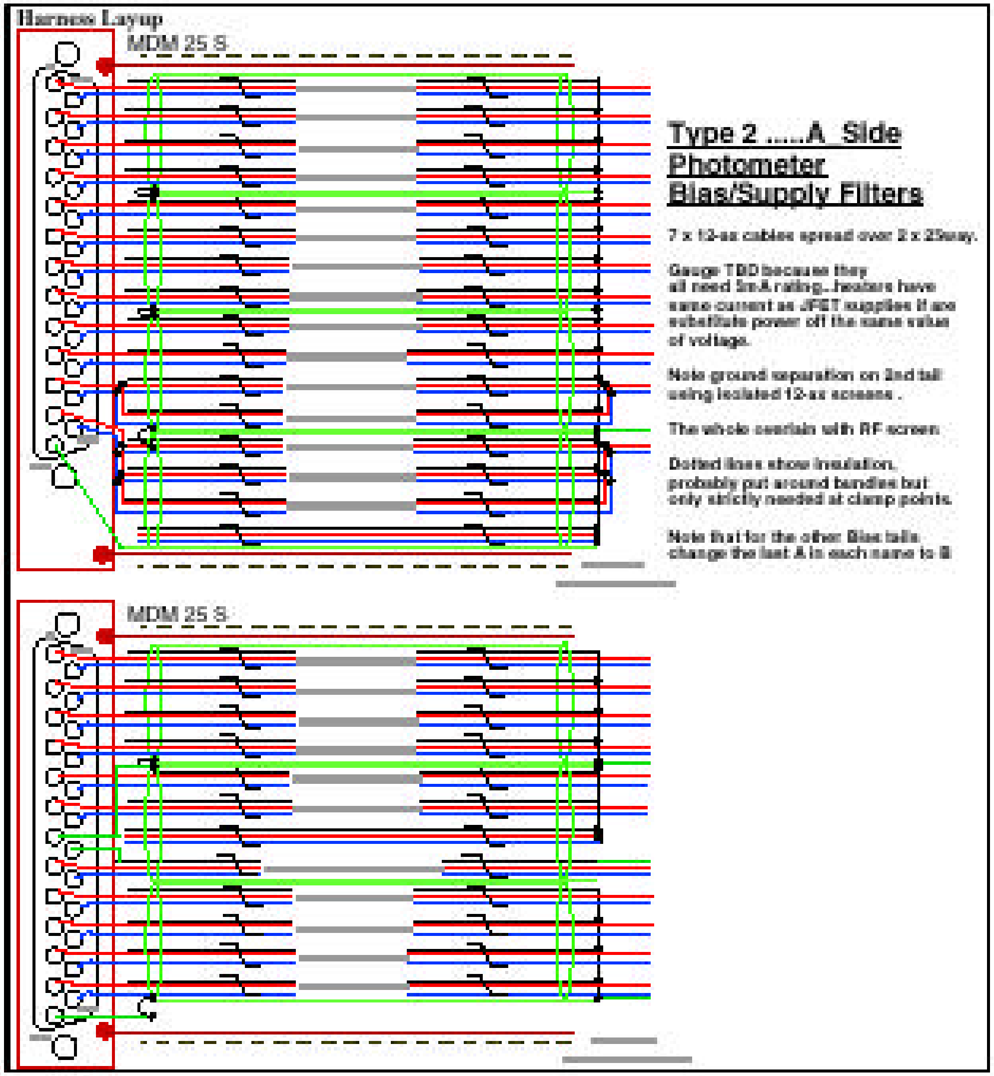
16 insulated screen twisted pairs plus 2 ground pins with single higher conductivity signal gnd. conductors.....even 2 x 28AWG standard copper might add little to total harness' conductivity TBC.

The whole overlain with RF screen shown:

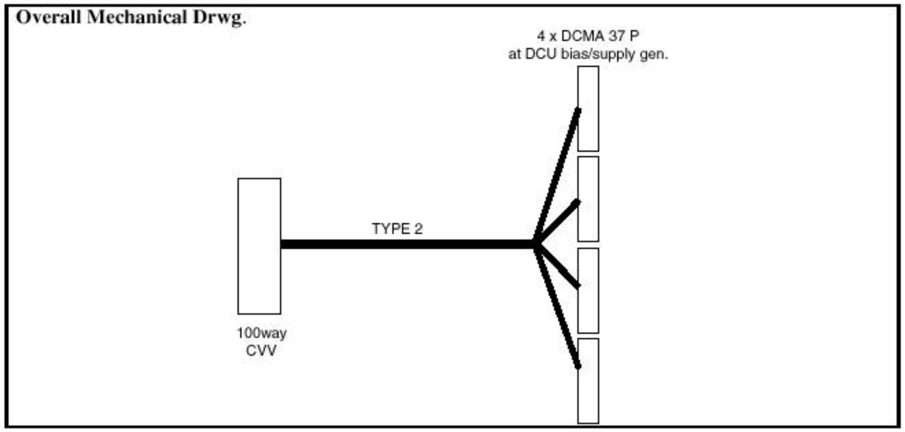
Dotted lines indicate insulation, probably put all around bundles but only strictly needed at clamp points.

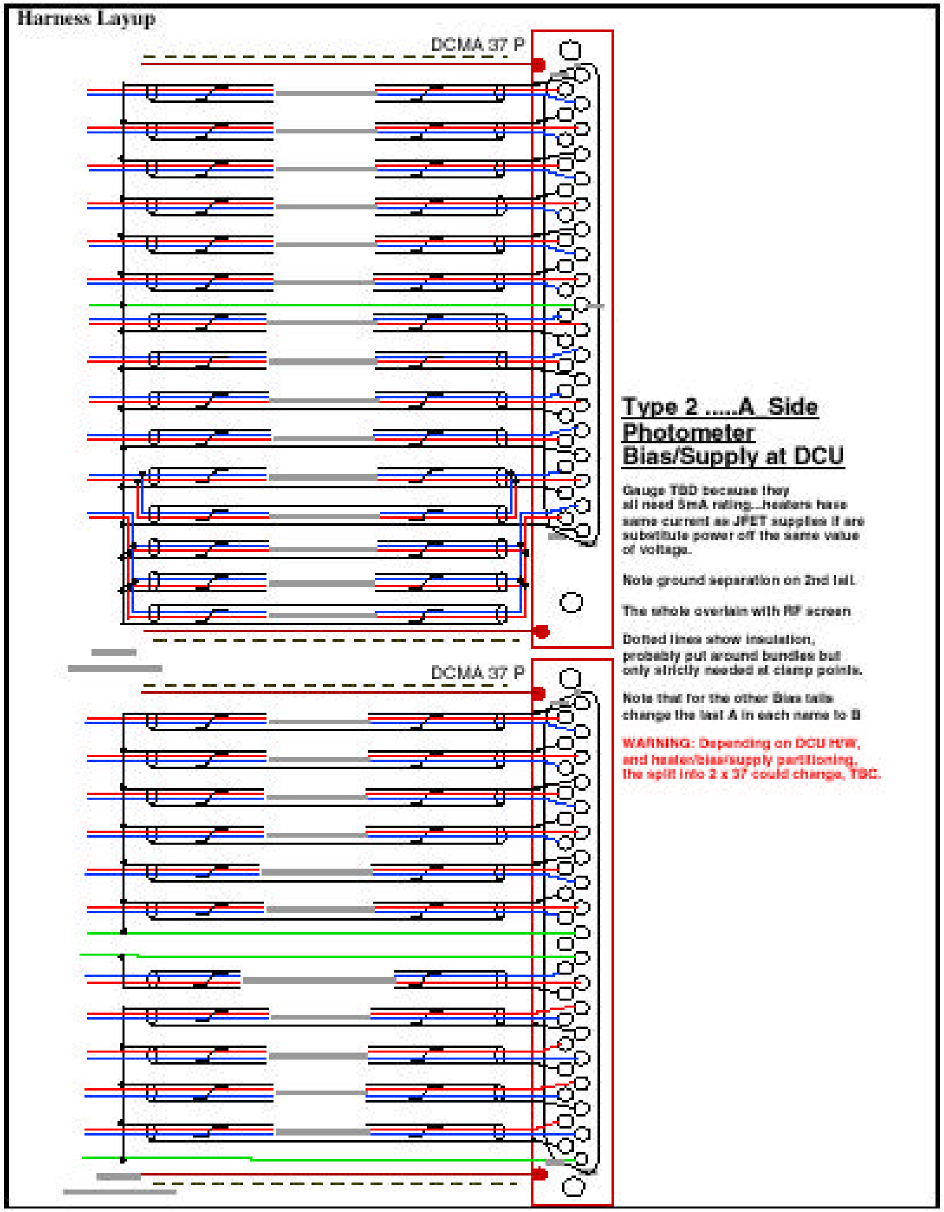


Overall Mechanical Drwg.
TYPE 2
100way
CVV
4 x MDM 25 S
at JFET filter box

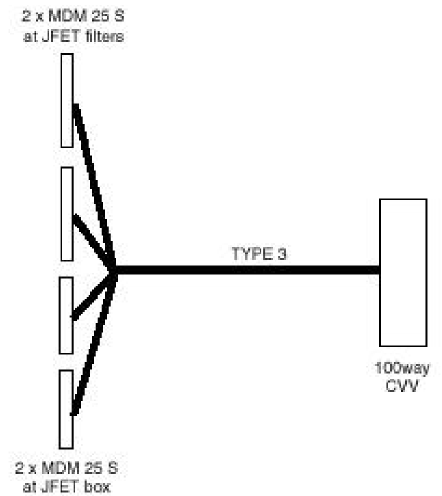


Harness Layup
MDM 25 S
MDM 25 S
Type 2 .....A_Side
Photometer
Bias/Supply Filters
7 x 12-ss cables spread over 2 x 25way.
Gauge TBD because they
all need 5mA rating..heaters have
same current as JFET supplies if are
substitute power off the same value
of voltage.
Note ground separation on 2nd tail
using isolated 12-ss screens .
The whole overlain with RF screen.
Dotted lines show insulation,
probably put around bundles but
only strictly needed at clamp points.
Note that for the other Bias tails
change the last A in each name to B


Overall Mechanical Drwg.
4 x DCMA 37 P
at DCU bias/supply gen.
TYPE 2
100way
CVV


Harness Layup
DCMA 37 P
DCMA 37 P
Type 2 .....A_Side
Photometer
Bias/Supply at DCU
Gauge TBD because they
all need 5mA rating...heaters have
same current as JFET supplies if are
substitute power off the same value
of voltage.
Note ground separation on 2nd tail.
The whole overlain with RF screen
Dotted lines show insulation,
probably put around bundles but
only strictly needed at clamp points.
Note that for the other Bias tails
change the last A in each name to B
WARNING: Depending on DCU H/W,
and heater/bias/supply partitioning,
the split into 2 x 37 could change, TBC.

Overall Mechanical Drwg.

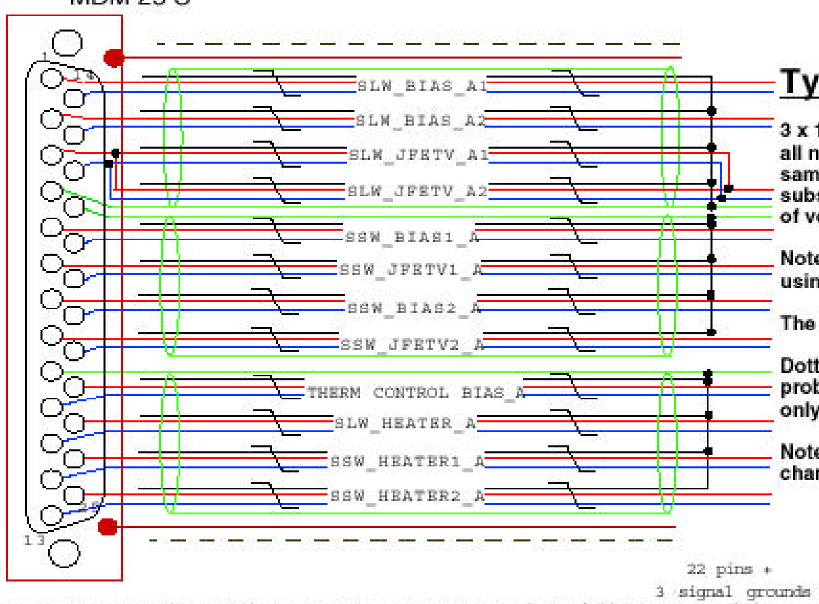


Harness Layup

Two 25way JFET tails, each as those in C4.

Two 25 way Spectrometer JFET Filter tails, each as follows:

MDM 25 S



Type 3 Bias Filters

3 x 12-ax cables. Gauge TBD because all need 5mA rating...heaters have same current as JFET supplies if are substitute power off the same value of voltage.

Note SLW and SSW ground separation using isolated 12-ax screens .

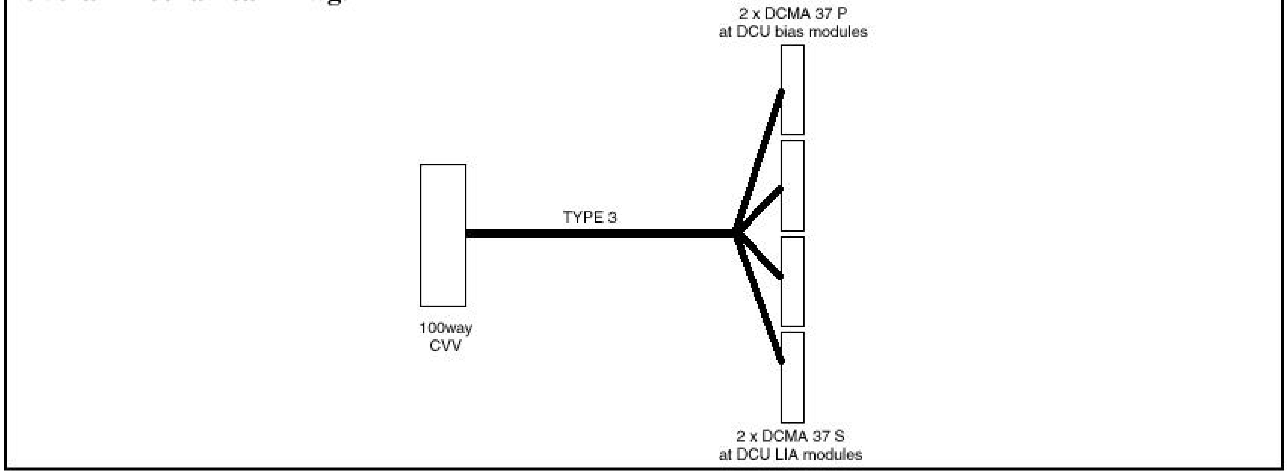
The whole overlain with RF screen

Dotted lines show insulation, probably put around bundles but only strictly needed at clamp points.

Note that for the other Bias tail change the last A in each name to B

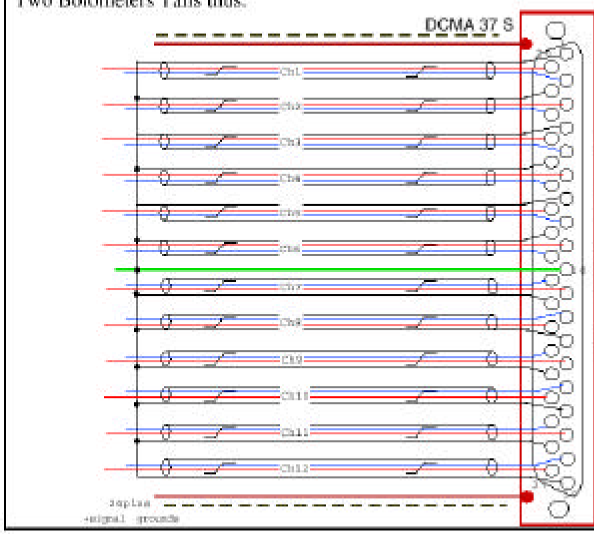
Because the small SLW has no subgroups that might fail, EACH of the two JFET membrane leads is double-wired in this cryoharness, requiring some extra wire-bonds for the bias lines in the filters.

Overall Mechanical Drwg.



Harness Lay-up

Two Bolometers Tails thus:



12 Channel Bolometer Tail (typ)

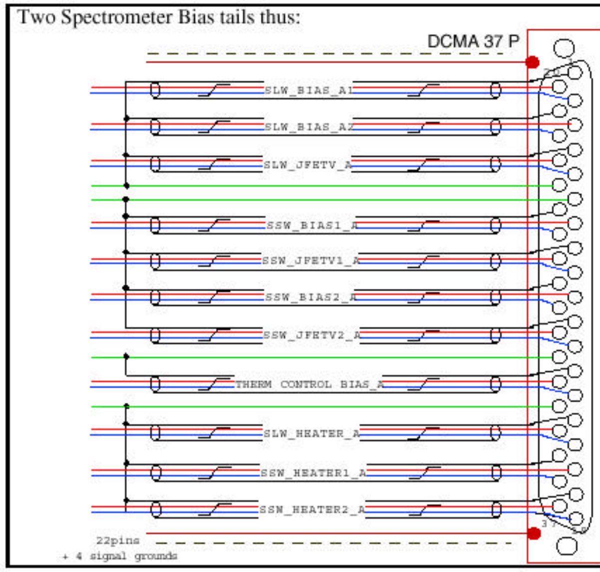
Common to all such tails, although others have ch. 13-24, etc.
Good flat layup for cryoharness

12 insulated screened twisted pairs plus 1 ground pins with a good conductor attached.

The whole overlain with RF screen

Dotted lines show insulation, probably put around bundles but only strictly needed at clamp points.

Two Spectrometer Bias tails thus:



DCU Type 3 Bias.

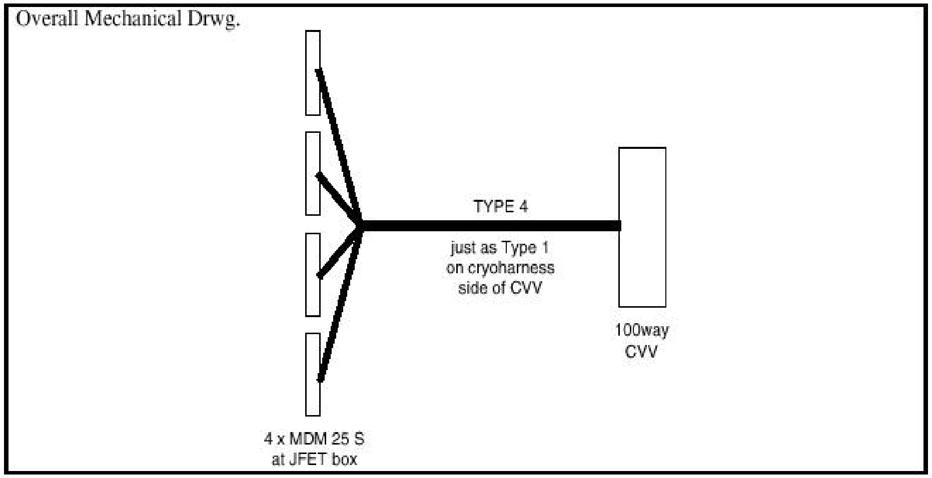
Two such tails, other with B instead of A at end of each name.

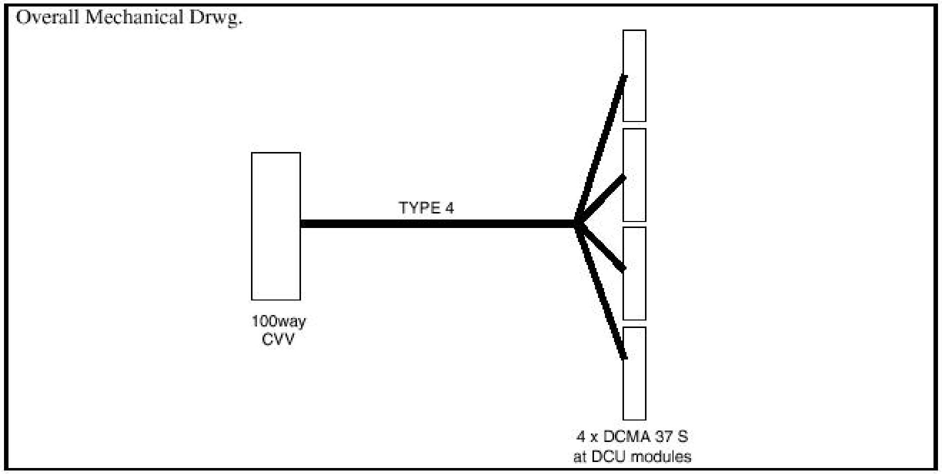
Good flat layup for cryoharness

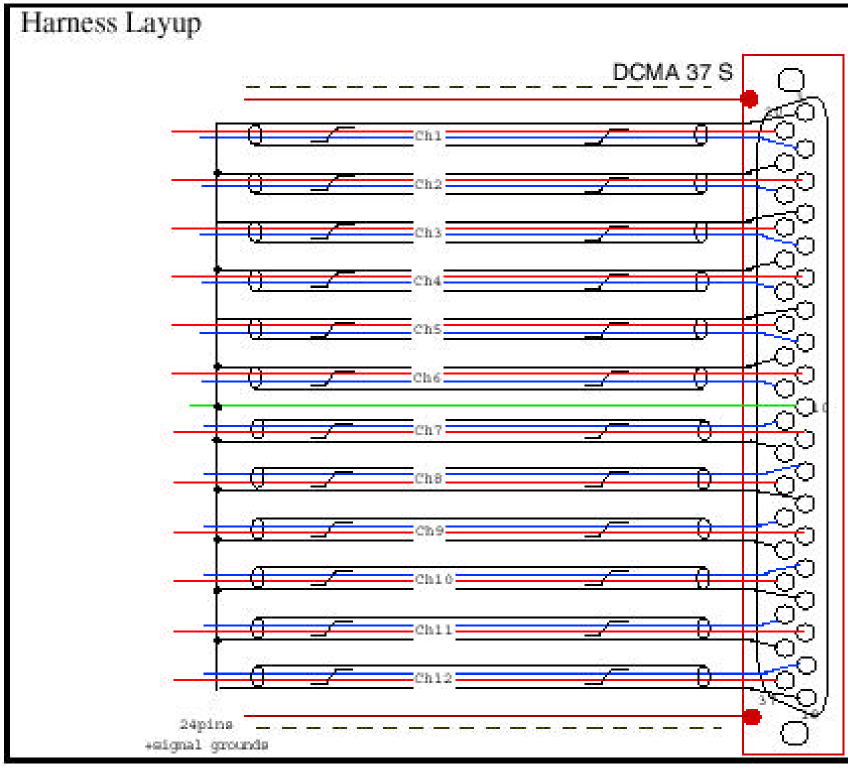
11 insulated screened twisted pairs plus 4 ground wires.
Gauge TBD because all TPs need 5mA rating...heaters have same current as JFET supplies if are substitute power off the same value of voltage.

The whole overlain with RF screen

Dotted lines show insulation, probably put around bundles but only strictly needed at clamp points.







12 Channel Bolometer Tail (typ)

Common to all such tails, although others have ch. 13-24, etc.
Good flat layup for cryoharness

12 insulated screened twisted pairs plus 1 ground pins with a good conductor attached.

The whole overlain with RF screen

Dotted lines show insulation, probably put around bundles but only strictly needed at clamp points.

Cryo Harness Pre-Integration Testing (RAL)

CRYOHARNESS TESTS

- Tests of installed cryoharness.
- Tests after installing the JFETs.
- Tests after installing the internal harness.

EQUIPMENT Needed for the Tests

- Model of flight DCU.
- DC preamplifier with external bias and JFET power supply for 24 channels (JPL Supplied).
- Spectrum analyzer.
- JFET simulator (STM, JPL Supplied).
- JFET x-talk simulator (JPL Supplied).
- .High-impedance bolometer array simulator (STM, JPL Supplied).
- Low-impedance bolometer simulator (JPL supplied).
- Bolometer x-talk simulator (JPL Supplied).

TESTS OF INSTALLED CRYOHARNESS

• Check the electrical continuity and shorts to ground and shield for all signal wires.

• Measure the resistance and the capacitance of each signal wire.

• Measure the microphonics spectrum, using a JFET simulator and Spectrum Analyzer with a loudspeaker attached to the chirp source.

• Measure the demodulated noise using the JFET simulator.

• Measure the electrical x-talk using the JFET x-talk simulator.

TESTS AFTER INSTALLING THE JFETS

• Check for shorts to ground and shield for each signal wire with JFET gates shorted to ground. No JFET power applied.

• Confirm the DC offsets and the offset mismatch for each JFET pair with JFET gates shorted to ground and JFET power applied.

• Measure the demodulated noise using low-impedance bolometer array simulator at room temperature.

TESTS AFTER INSTALLING THE INTERNAL HARNESS

• Measure the electrical x-talk using the bolometer x-talk simulator at room temperature.

• Measure the demodulated noise using the low-impedance bolometer array simulator at room temperature.

• Measure the transfer function of the system, using the high-impedance bolometer array simulator at room temperature.

• Measure the microphonics spectrum using the high-impedance bolometer array simulator, DC bias, loud speaker plugged to the Spectrum analyzer’s chirp source at 2K.

• Measure the transfer function of the system, using the high-impedance bolometer array simulator at 2K.

• Measure the demodulated noise using the high-impedance bolometer array simulator at 300 mK.

• Measure the heatload due to the internal harness, derived from the 3He fridge temperature.

8.0
Warm Electronics
DCU Design

F.PINSARD

Service d'astrophysique CEA/DAPNIA

pinsard@cea.fr

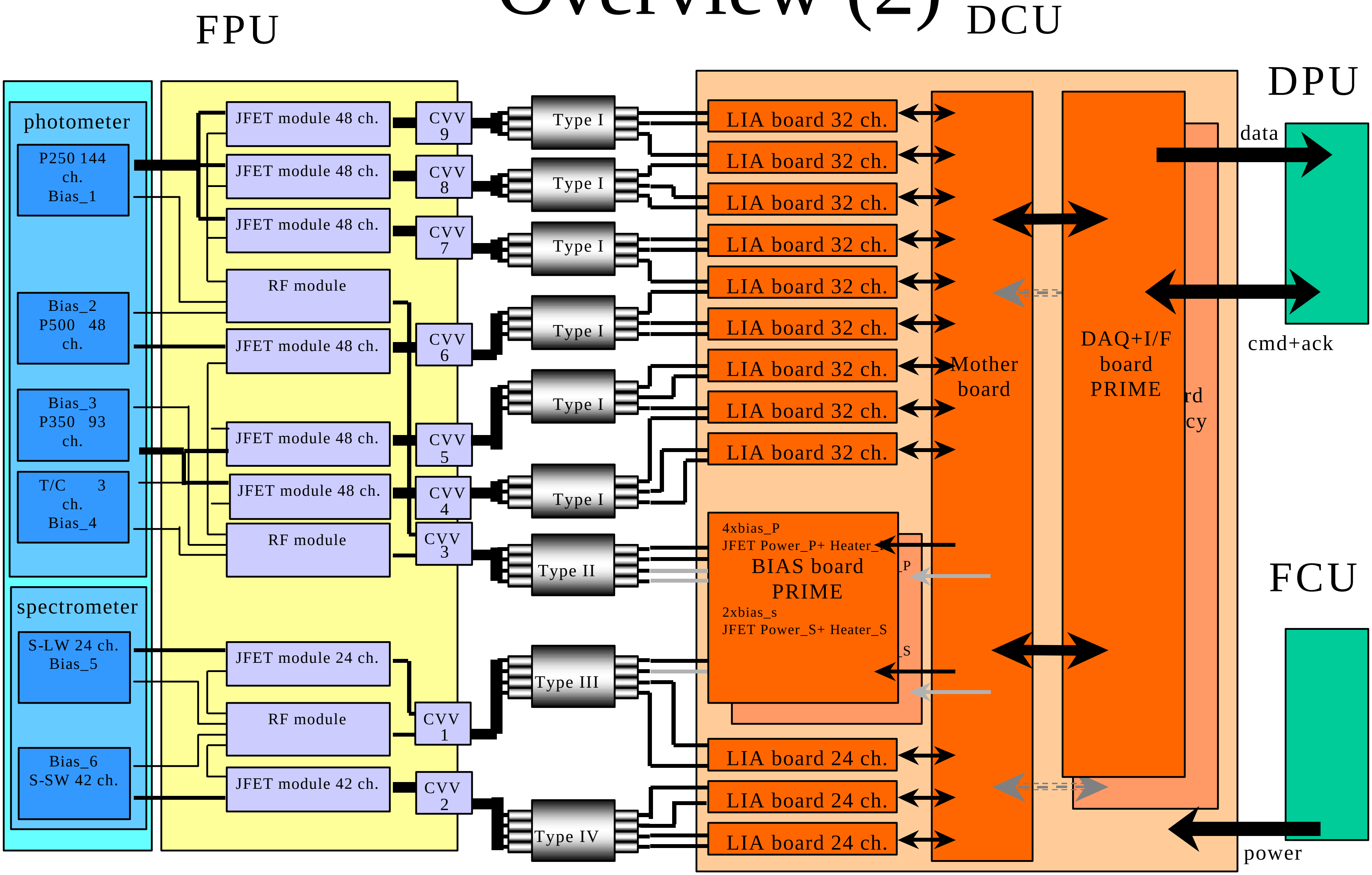
Overview (1)

- The DCU is a one box unit:
  - The Detector Control Unit comprises analog and digital electronics exclusively devoted to bolometers operation
  - In this box, 16 boards will be connect on a back plane printed circuit board
    - 9 LIA_P boards process the photometer analog signals
    - 3 LIA_S boards process the spectrometer analog signals
    - 2 BIAS boards (1 prime & 1 redundant)

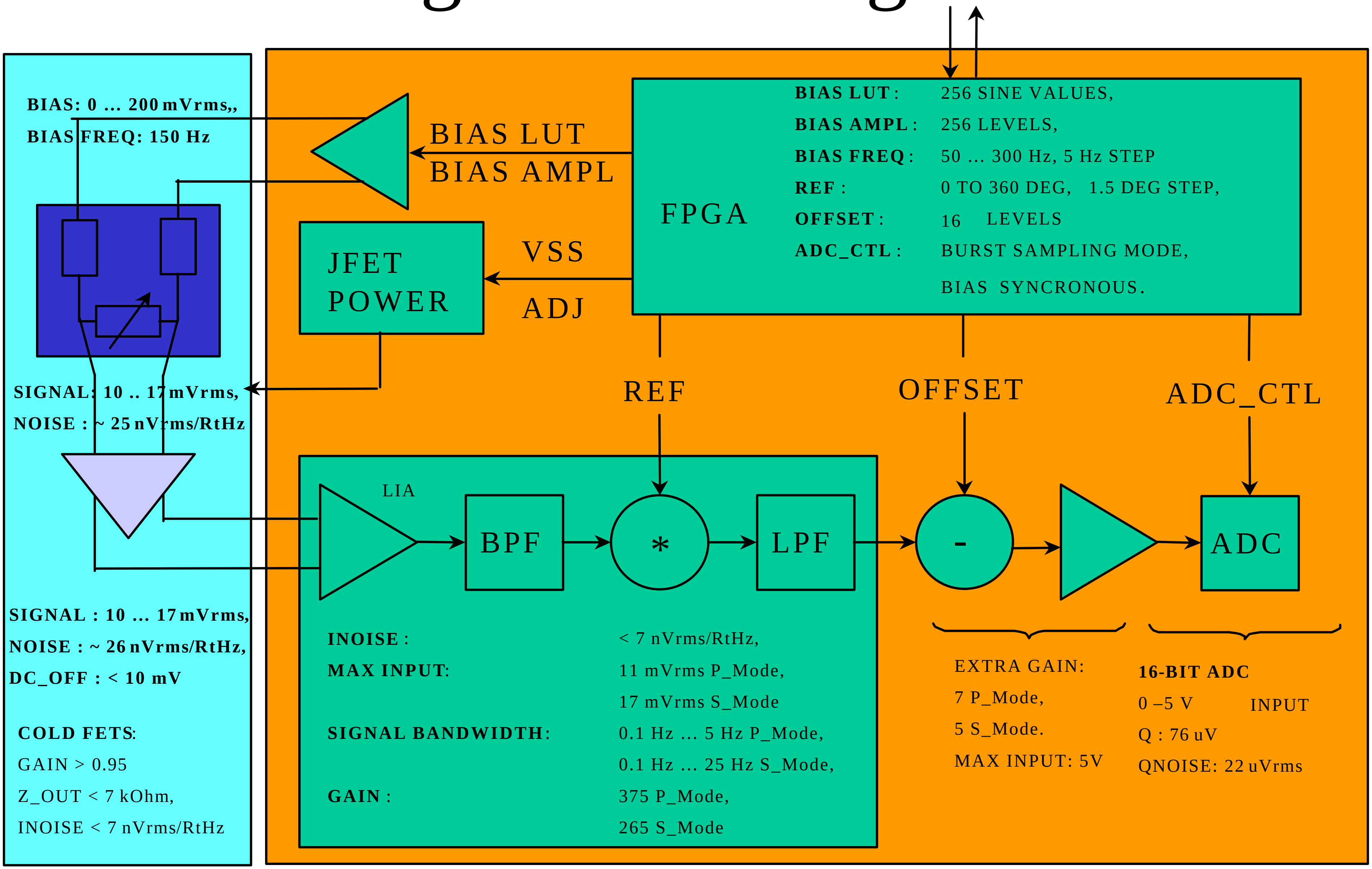
      distribute the bolometers bias and JFETs supply
    - 2 DAQ+IF boards (1 prime & 1 redundant)

      digitize signals, receive /decode commands

Overview (2)


FPU
DCU
DPU
FCU
photometer
P250 144 ch. Bias_1
Bias_2 P500 48 ch.
Bias_3 P350 93 ch.
T/C 3 ch. Bias_4
spectrometer
S-LW 24 ch. Bias_5
Bias_6 S-SW 42 ch.
JFET module 48 ch.
RF module
JFET module 24 ch.
JFET module 42 ch.
CVV 9
CVV 8
CVV 7
CVV 6
CVV 5
CVV 4
CVV 3
CVV 1
CVV 2
Type I
Type II
Type III
Type IV
LIA board 32 ch.
LIA board 24 ch.
4xbias_P
JFET Power_P+ Heater_P
BIAS board PRIME
2xbias_s
JFET Power_S+ Heater_S
Mother board
DAQ+I/F board PRIME
data
cmd+ack
power

Signal flow diagram



DCU Specification (1)

- ***Analog Processing channels***

  - Functions: receive, amplify, demodulate & filter bolometer signals
  - 336 total number : 288 for photometer + 66 for spectrometer
  - Specifications:
    - Gains:
      - Photometer: 375
      - Spectrometer: 265
    - Input signal bandwidth:
      - Photometer: 0.1 to 5Hz
      - Spectrometer: 0.1 to 25Hz
    - Input noise < 7nVrms/rt(Hz)

DCU Specification (2)

- ***Bias generators***

  – Functions: generate sine biases for bolometer and DC biases for JFETs and heaters

    - Adjustable sine biases:
      – Photometer : 1sine generator/ 4 channels with independent amplitudes
      – Spectrometer : 1sine generator/ 2 channels with independent amplitudes
    - Adjustable DC biases:
      – Photometer : 12 generators for JFET + 1 for heater
      – Spectrometer : 3 generators for JFET + 1 for heater

DCU Specification (3)

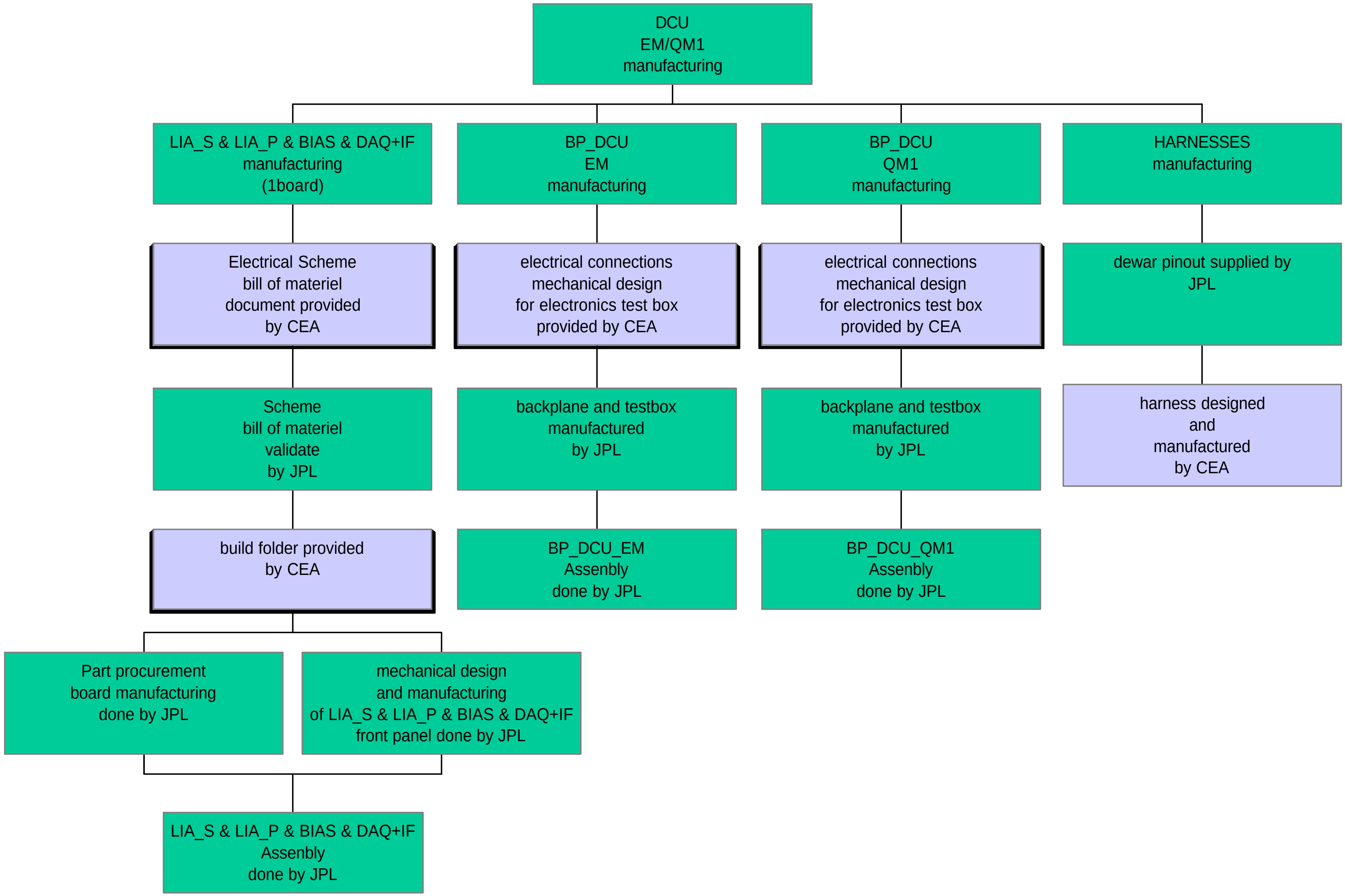
- ***Bias generators …***

  – Specification:
    - Adjustable sine biases:
      – Voltage range: 0 to 200 mVrms for bolometers and
      0 to 500 mVrms for thermometers
      – Accuracy: 1mV (256 levels)
      – Frequency range: 50 to 300Hz
    - Adjustable DC biases:
      – Voltage range: 0 to –5V for JFETs (VSS)
      0 to –8V for heater
      – Output currents : 5mA max for JFETs
      25mA max for heater

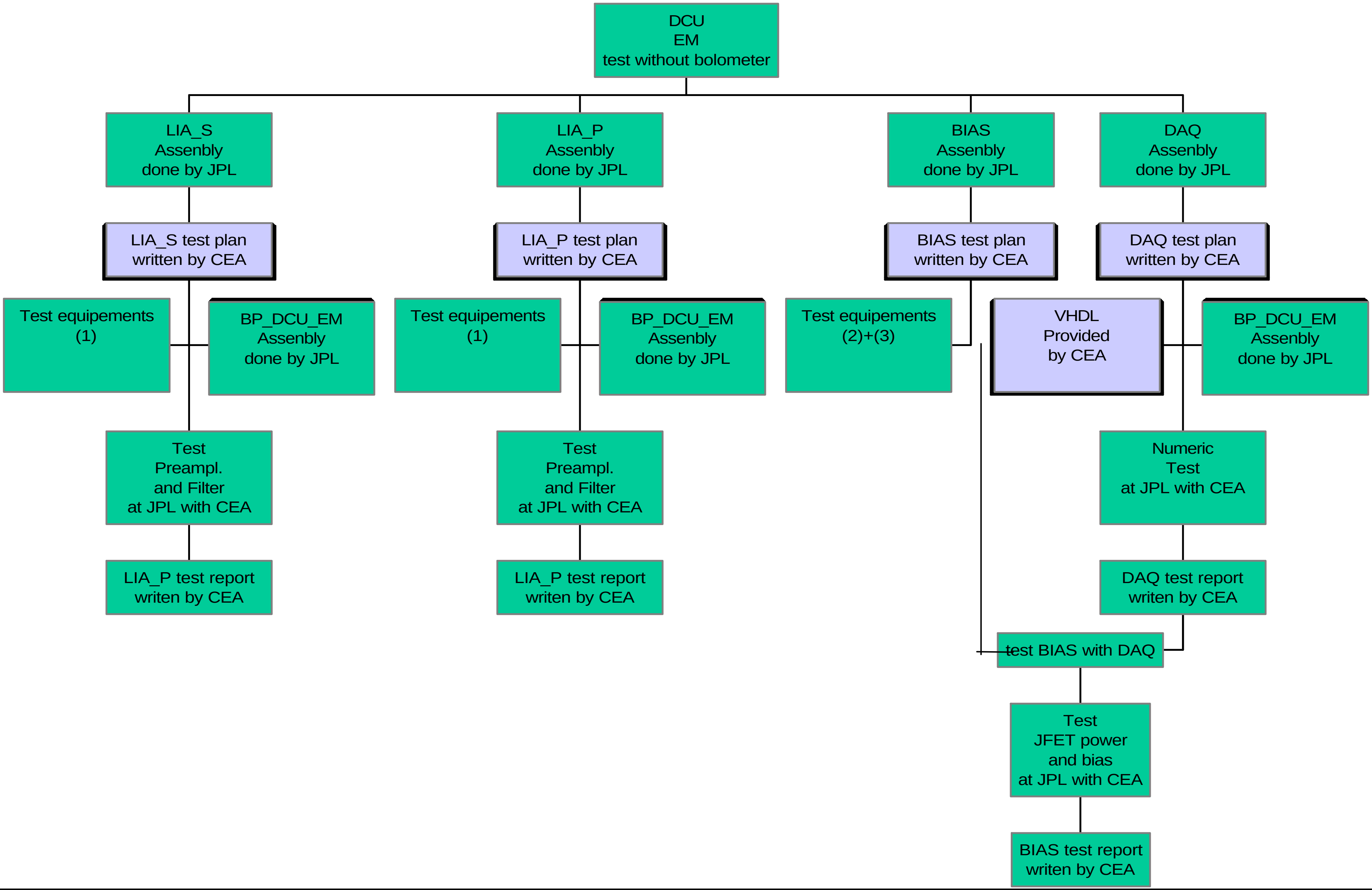
DCU Specification (4)

- ***Data acquisition & DPU interface***
  - Specification:
    - Digitizing resolution:19 bits (16-bit ADC + 4-bit offset)
    - Frame rate : 1/2 to 1/256 of sine bias frequency
    - Frame acquisition time < 3ms
    - Data formats and Command are defined in DRCU ICD
    - Electrical interface :RS422

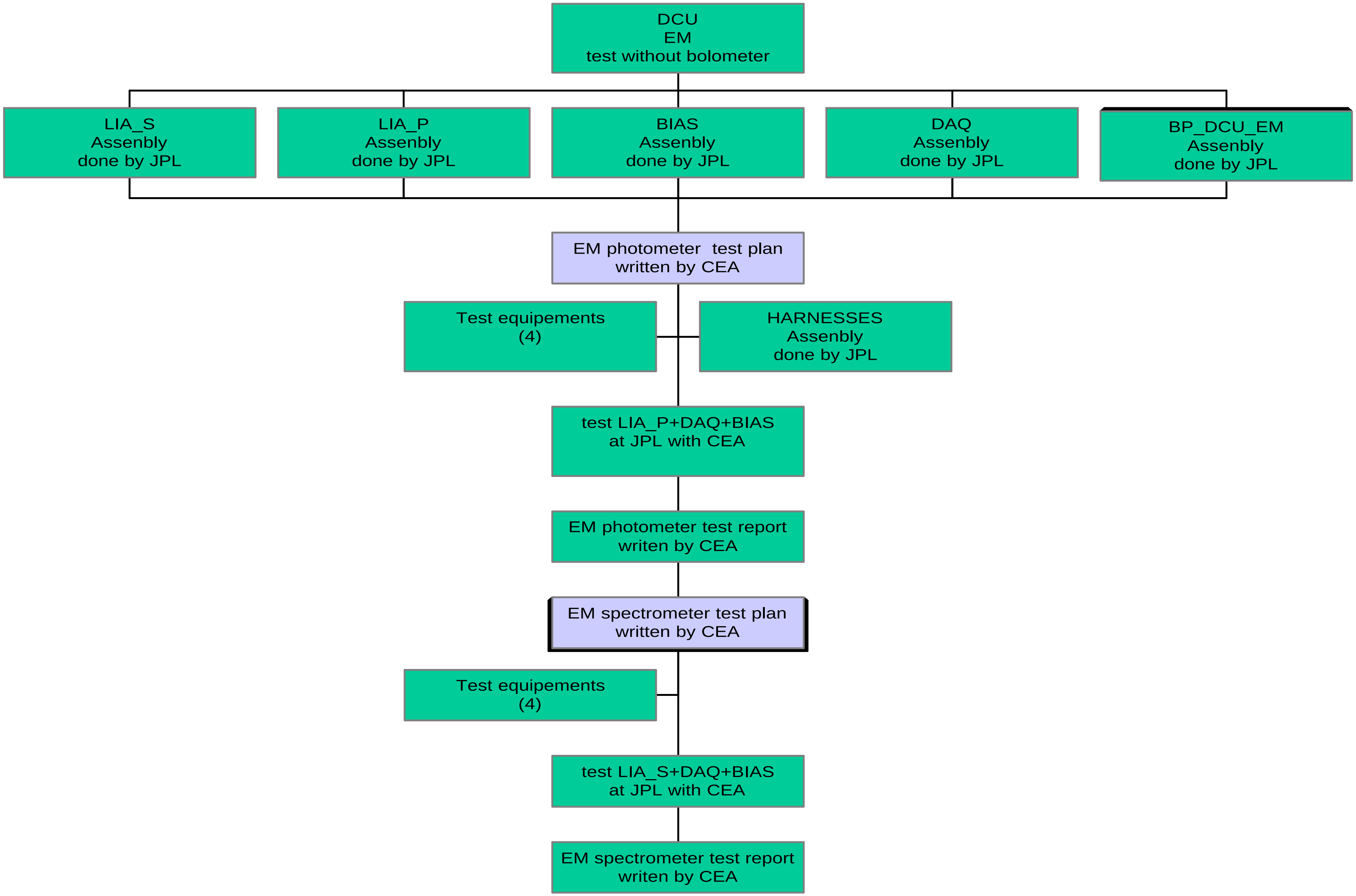
DCU EM/QM1 Development Tree (1)



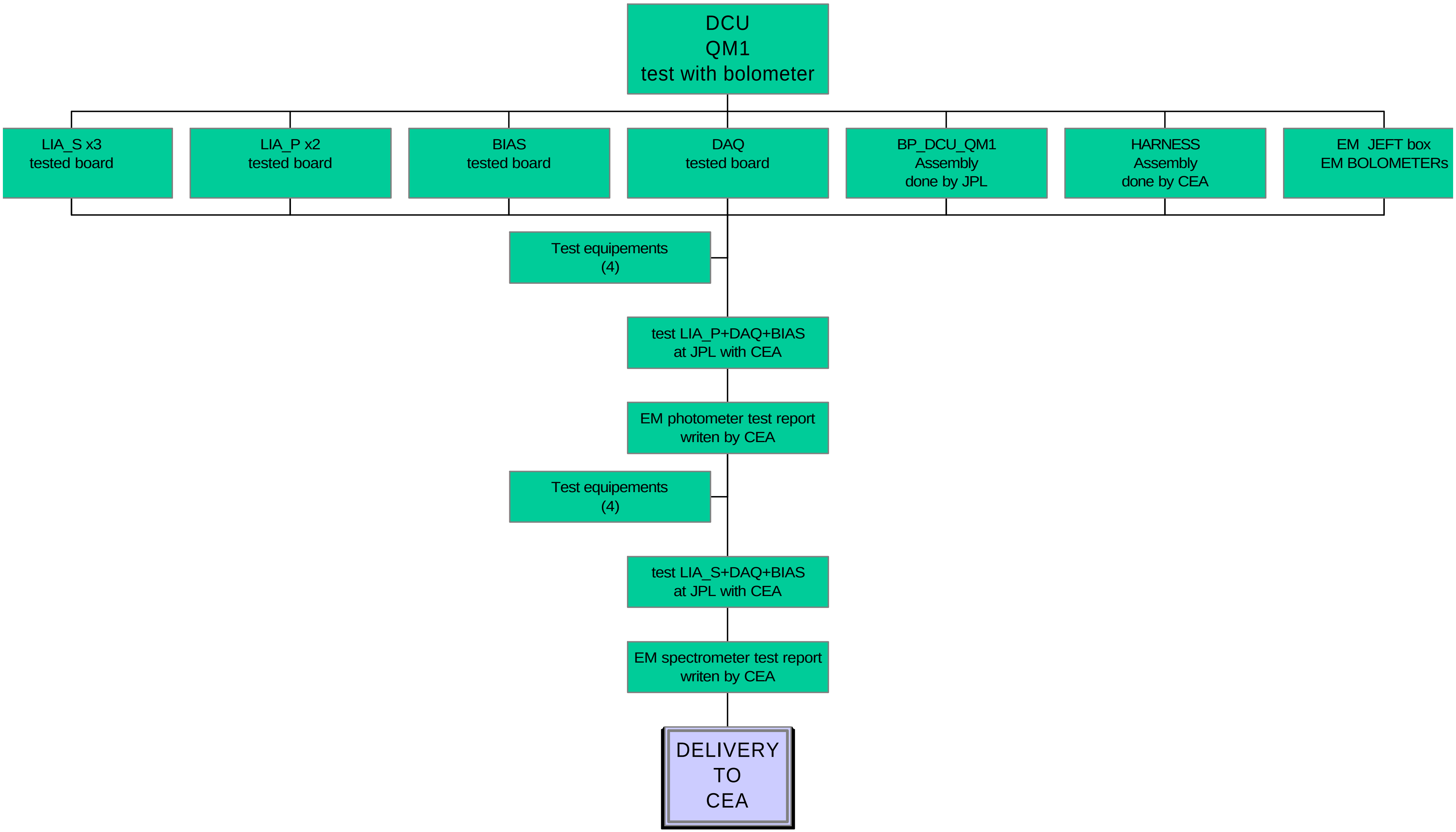
DCU EM Development Tree (2)



DCU EM Development tree (3)



DCU QM1 Development tree (4)



Design status (1)

- **Detector Control Unit**

  – QM1 development is divided into:
    - Phase 1: July 2000 to December 2000
      - Breadboard design & testing including 2 analog channels, 1 bias channel and 1data acquisition channel.
      - Goal : elementary functions & internal interfaces optimization
    - Phase 2: January 2001 to July
      - QM1 design including 4 complete analog boards (1 for photometer and 3 for spectrometer), 1 bias board and 1 data acquisition board.
      - Electrical schematics are done
      - Layout are done except for spectrometer analog board

Design status (2)

- **Detector Control Unit…**
    - Phase 3
        - Realization and test at JPL
    - Phase 4
        - Integration and test at SACLAY

Phase 1 Conclusion

- **Breadboard**

  – For analog processing channels:
    - The chosen solution answers to the photometer noise and bandwidth requirements. For the spectrometer, the Low Pass Filter will have to be adjusted.

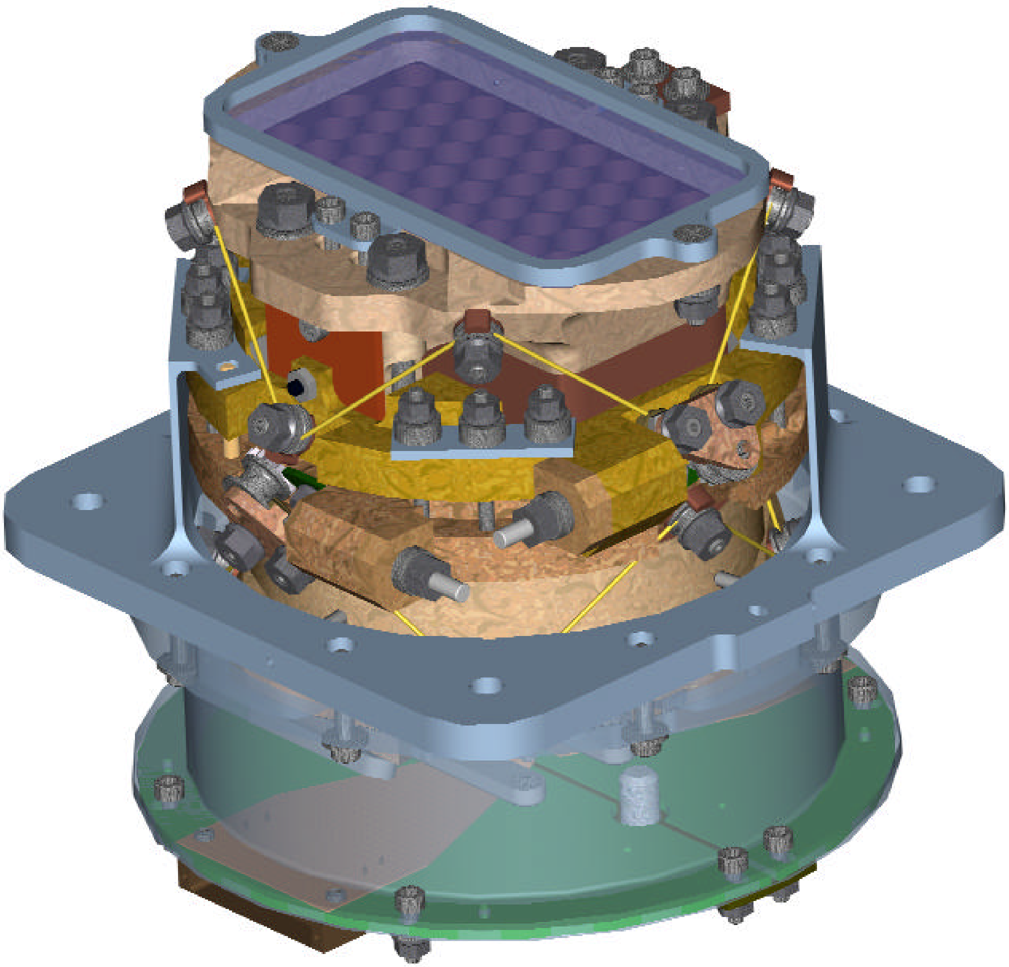
  – For bias generator :
    - The breadboard design is compliant with the bias requirements on the frequency and amplitude ranges and precision.

  – For acquisition :
    - The breadboard design must be improved to solve the ADC noise problem.

9.0 JPL HSO SPIRE Test Program

Presented by

Kalyani Sukhatme



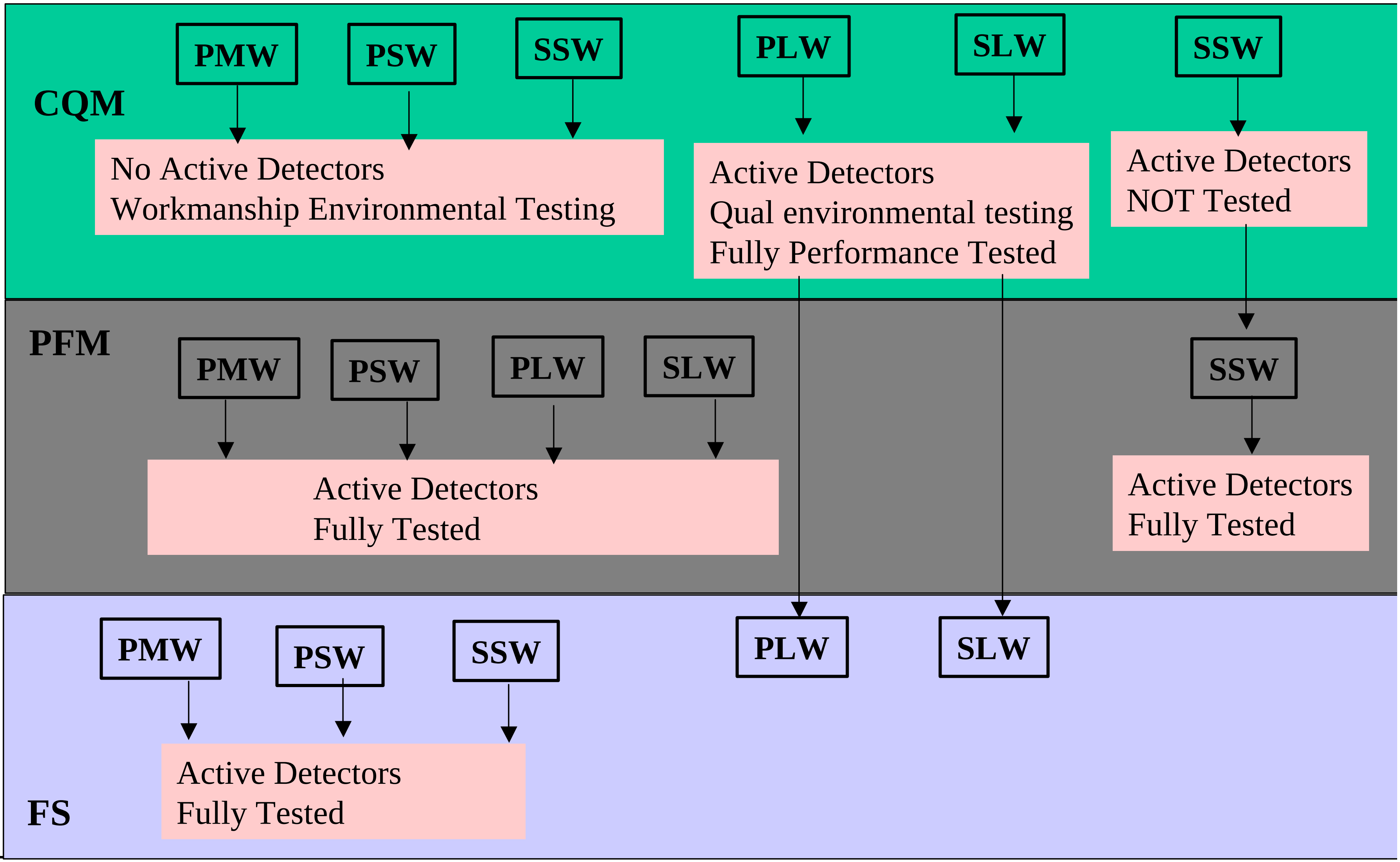
Agenda for Section

- Overview
- Verification Matrix
- HRCR
- Integration and Test Plan

Overview

- Deliverables
  - Bolometer Detector Array Assembly (BDA)
  - JFET Modules
  - RF filter modules
  - BDA to JFET Harness
- Test Program
  - Environmental Testing
  - Performance Characterization/Testing
- Testing Phase
  - EM Testing
  - CQM Testing
  - PFM/Spare Testing

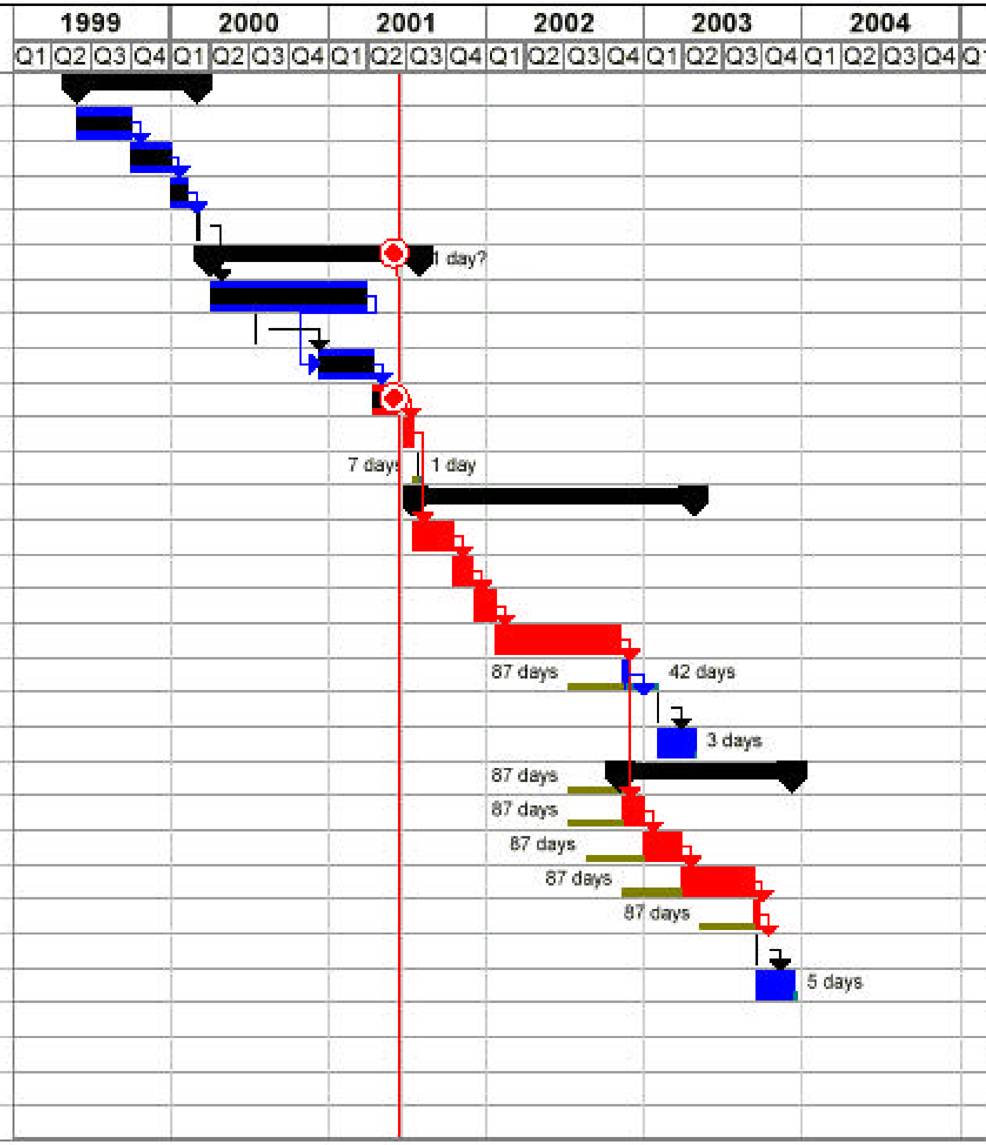
BDA Units


CQM
PMW
PSW
SSW
PLW
SLW
SSW
No Active Detectors
Workmanship Environmental Testing
Active Detectors
Qual environmental testing
Fully Performance Tested
Active Detectors
NOT Tested
PFM
PMW
PSW
PLW
SLW
SSW
Active Detectors
Fully Tested
Active Detectors
Fully Tested
FS
PMW
PSW
SSW
PLW
SLW
Active Detectors
Fully Tested

HSO/Planck Project

SPIRE Detector System

ID	Task Name
1	**Prototype Design and Testing Phase**
2	Design
3	Fabrication and Assembly
4	Testing and Data Reduction
5	Downselect Review
6	**Detail Design & EM Development Phase**
7	EM Design
8	PDR
9	EM Fabrication
10	EM Assembly
11	EM Testing & Data Reduction
12	CDR
13	**CQM Phase**
14	CQM/PFM/Spare Fabrication
15	CQM Assembly
16	CQM Environmental Testing & Data Reduction
17	CQM Performance Testing & Data Reduction
18	CQM HRCR & Shipment
19	CQM Required Date (Business Agreement)
20	CQM Integration Support
21	**PFM and Spare Phase**
22	PFM and Spare Assembly
23	PFM and Spare Environmental Testing and D.R.
24	PFM and Spare Performance Testing & D.R.
25	PFM and Spare HRCR and Shipment
26	PFM Required Date (Business Agreement)
27	PFM Integration Support
28	
29	
30	
31	



Applicable Documents

- SPIRE Bolometer Detector Array Assembly Process and Test Qualification Plan
- SPIRE Bolometer Detector Array Performance Test Plan
- SPIRE JFET Module Process and Test Qualification Plan
- SPIRE JFET Module Performance Test Plan

- All four of the above will get incorporated into a Test Plan Package and will become an Agreed Document as per Business Agreement

Documents

Document Title	Number	Status		
		In Work	Complete	Released
BDA Process and Test Qual Plan	D-19152		100%	X
BDA Performance Test Plan	D-20549	X	75%	
JFET Module Process and Test Qual Plan	D-19153	X	75%	
SPIRE Vibration Test Plan	D-20550	X	75%	
Thermal Cycling Procedure	TP518518	X	25%	
BDA Performance Testing Procedure		-	-	
JFET And RF Filter Characterization Procedure		-	-	

BDA: EM Phase

Unit#1

Environmental Testing :

Warm Vibration
Thermal (LN_2) Cycling
Cold (LN_2) Vibration

Baseline Test:
Tension and Metrology Tests before and after Each Environmental Test

Unit#2

Thermal Characterization

Install Bolometers in the BDA structure

Environmental Testing :

Thermal Cycling
Vibration Testing

Yield Testing :

Warm Continuity Test
Cold (300 mK) Continuity test

BDA: CQM/PFM/FS Phase

Environmental Testing :

Warm Vibration
(with Accelerometer)

Baseline Test:
Tension and Metrology Tests performed before and after Each of the Environmental Tests

---

Install Bolometers in the BDA structure

Environmental Testing :

Thermal Cycling
Cold (LN_2)Vibration

Baseline Tests:
Warm Continuity Check. And Cold Continuity Check on ~20 channels during Thermal Cycling

Cold Alignment Test

Performance Testing :

1) Dark Testing :

- Load Curves
- Noise Measurements

2) Optical Testing:

- Load Curves, Noise Measurements
- Optical Time Constant
- Beam Mapping
- Spectroscopy
- Optical Efficiency, Optical Cross-talk

JFET Modules

Environmental Testing :

Thermal Cycling
Cold (LN_2)Vibration Testing

Baseline Test:
Measure Characteristic Offset Voltages
as a baseline test
before and after each environmental test

Performance Characterization:

Noise Measurements

RF Filter Modules

Environmental Testing :

Thermal Cycling
Vibration Testing

Baseline test :
Continuity Check
before and after each
environmental test

RF Characterization:

RF Attenuation Measurement
(on a few channels, warm)

Environmental Test Matrix for BDA and JFET Modules

Test:	CQM	PFM	FS
Vibration:	**Q**	**A**	**A**
Thermal cycle:	**D/Q**	**A**	**A**
Vacuum cycle	**D/Q**	**A**	**A**
Lifetime:	**D/X**	**-**	**-**
Soak/cycle:	**D**	**-**	**-**
Radiation tolerance:	**D**	**-**	**-**
Thermal range (Bakeout):	**D/X**	**-**	**-**
Thermal stability (Instrument Level):	**Q**	**A**	**A**
Microphonics (Instrument Level):	**Q**	**A**	**A**
Ionising radiation:	**D**	**-**	**-**
EMI (Instrument Level):	**Q**	**A**	**A**
EMC (Satellite Level):	**Q**	**A**	**A**

Q : test carried out at qualification level for qualification times;
A : test carried out at acceptance level;
D : qualification test carried out by design including unit-level testing and engineering analysis.
X : Will rely upon HFI test data on similar devices

BDA: Requirements Verification Matrix

Specification ID	Description	Verified By Test Or Measurement On				
		Prototype	EM	CQM	PFM	FS
BDA-FUN-04	The **positional repeatability** of the focal plane structure shall be < 125 um (TBC) orthogonal to the optical axis, and < 625 um (TBC) along the optical axis. The rotational repeatability around the optical axis shall be < 0.5 degrees (TBC).	X	X	X	X	X
BDA-TEC-03	The **BDA mass** will have a design value of 600 g (TBC) average over 5 detector arrays, including output connectors.	X	X	X	X	X
BDA-TEC-04	The **first resonant frequency** of the BDA will be > 200 Hz (TBC), with a goal of > 250 Hz.	X	X	X	X	X

BDA: Performance Characterization Matrix

Specification ID	Description	Verified By Test On				
		Prototype	EM	CQM	PFM	FS
BDA-PER-01	BDA detector yield.	X	X	X	X	X
BDA-PER-02	The ratio of photon NEP due to radiation absorbed at the detector and total NEP, given as (NEPphoton/NEPtotal)^2 NEP includes all sources of noise at 1 Hz, measured at 300 mK, assuming a total readout noise of 10 nV/rtHz and an operating impedance of 5 MOhm.	X		Y	Y	Y

Y: Noise tests are carried out under dark conditions. The detector noise model and optical efficiency will be used to predict detector noise under optical loading. The model can be confirmed under the optical testing with optical loads approximate to the loads encountered in flight.

BDA: Performance Characterization Matrix (Contd.)

Specification ID	Description	Verified By Test On				
		Prototype	EM	CQM	PFM	FS
BDA-PER-03	The optical efficiency of the FPU horn and bolometer assembly for the photometer arrays over the optical passband.	X	-	X	X	X
BDA-PER-04	The optical efficiency of the short wavelength spectrometer horn arrays and bolometer assembly over the optical passband.	-	-	-	X	X
BDA-PER-05	The optical efficiency of the long wavelength spectrometer horn arrays and bolometer assembly over 300-400 μm.	-	-	X	X	X
BDA-PER-06	The photometer detector time constant, assuming a maximum modulation frequency of 2 Hz.	X	**-**	**Z**	**Z**	**Z**
BDA-PER-07	The spectrometer detector time constant, assuming a maximum modulation frequency of 20 Hz.	-	-	Z	Z	Z

Z: The detector speed of response will be measured under optical loads approximate to the loads encountered in flight.

BDA: Performance Characterization Matrix (contd.)

Specification ID	Description	Verified By Test On				
		Prototype	EM	CQM	PFM	FS
BDA-PER-08	The uniformity of the calibrated responsivity.	-	-	YY	YY	YY
BDA-PER-09	Detector cross-talk.	ZZ	-	ZZ	ZZ	ZZ
BDA-PER-10	The 1/f knee frequency (total noise is sqrt(2) larger than white level).	Y	-	Y	Y	Y

YY: Responsivity calibrated by electrical load curves. Stability of responsivity derived from noise measurements.

ZZ: Optical cross-talk will be tested to the limits of our apparatus, on selected pixels, and from electrical cross-talk on resistor channels. Full cross-talk matrix acquired at instrument level.

Y: Noise tests are carried out under dark conditions. The detector noise model and optical efficiency will be used to predict detector noise under optical loading. The model can be confirmed under the optical testing with optical loads approximate to the loads encountered in flight.

JFET: Verification Matrix

Specification ID	Description	Verified By Test Or Measurement On				
		Prototype	EM	CQM	PFM	FS
JFET-FUN-02	The RF filters will operate without power dissipation	-	-	-	-	-
JFET-FUN-03	The JFET modules must be capable of functioning, without meeting noise specifications, over a temperature range from 4 K to 300 K	-	X	X	X	X
JFET-FUN-04	The JFET module and RF filters will operate from a base temperature between 4 – 20 K.	-	X	X	X	X

JFET: Verification Matrix (Contd.)

Specification ID	Description	Verified By Test Or Measurement On				
		Prototype	EM	CQM	PFM	FS
JFET-TEC-01	The JFET modules will have a mass less than 305 g.	-	X	X	X	X
JFET-TEC-03	The RF filters are to provide –40 dB attenuation from 500 MHz to 3 GHz (TBC, minimum), -60 dB attenuation from 500 MHz to 10 GHz (TBC, goal).	-	X	AA	AA	AA
JFET-TEC-05	The on-state power dissipation of a JFET module is to be < 11 mW (minimum performance); < 5.5 mW (TBC) (design value). This results in a photometer power dissipation < 66 (33) mW, a spectrometer power dissipation < 22 (11) mW, and an average dissipation < 44 (22) mW assuming 50 % operation of the photometer and 50 % operation of the spectrometer. NB: A 50% margin will be held on the design values to reflect the uncertainty in achieving the low thermal dissipation.	X	X	X	X	X

AA: On selected channels

JFET: Performance Characterization Matrix

Specification ID	Description	Verified By Test On				
		Prototype	EM	CQM	PFM	FS
JFET-PER-01	Median noise of JFET module over 100 – 300 Hz.	X	X	X	X	X

HRCR

- List of Documents Available for Delivery with the Hardware
  - Design Documentation (Includes released drawings)
  - Environmental Test Plans and Results
  - Performance Characteristics/ Measurements
  - Handling Specifications
  - Manufacturing or Build Documentation
    - AIDS and IR
    - Verification of ESD requirements and Contamination control
  - Problem Failure Reports (List of all the PFRs and copies of any open PFRs)
  - Materials Review Board Documentation (If Necessary to resolve any discrepancies between the Cog-E and QA)
  - Final Inspection Report

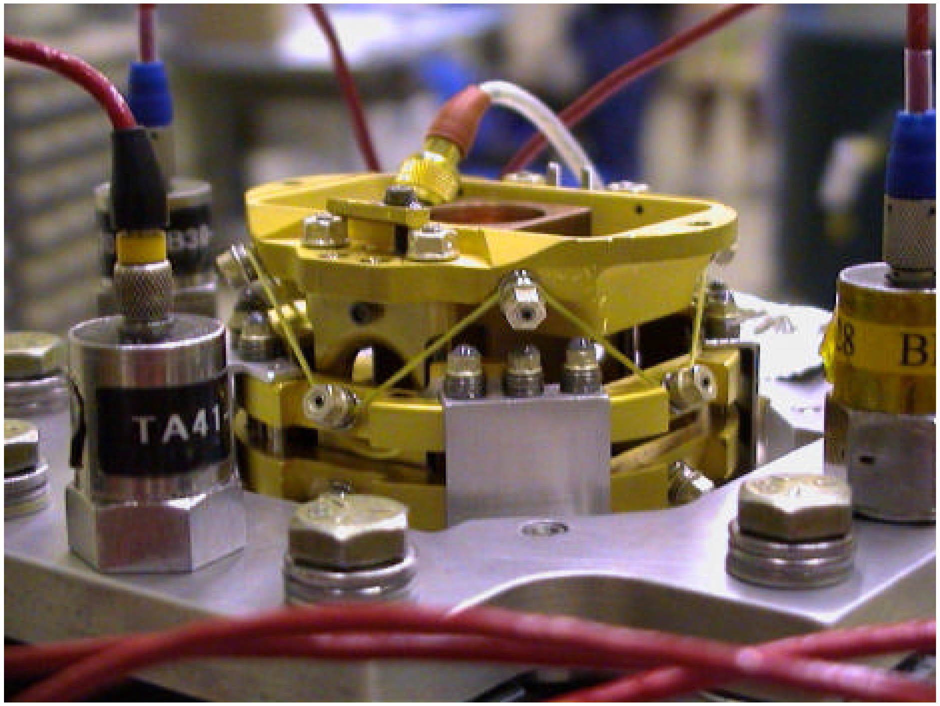
Integration And Test Plan

- Documentation
  - Details of the JPL deliverable hardware integration in Europe
  - Details of the test plan in Europe
- Support for Integration and Testing in Europe
  - Cryoharness Testing Support at RAL
  - Representatives from RAL and Cardiff will visit during JPL Testing Phase
  - Integration support for all JPL deliverables

9.5
EM Vibration Status and Facilities
Kalyani Sukhatme

EM BDA Environmental Testing

- EM Unit #1
- Kevlar Preload = 30 lb
- List of Tests
  - Warm Vibration
  - Thermal Cycling
  - Warm Vibration with Force Transducers
  - Cold Vibration
- Metrology before and after each test

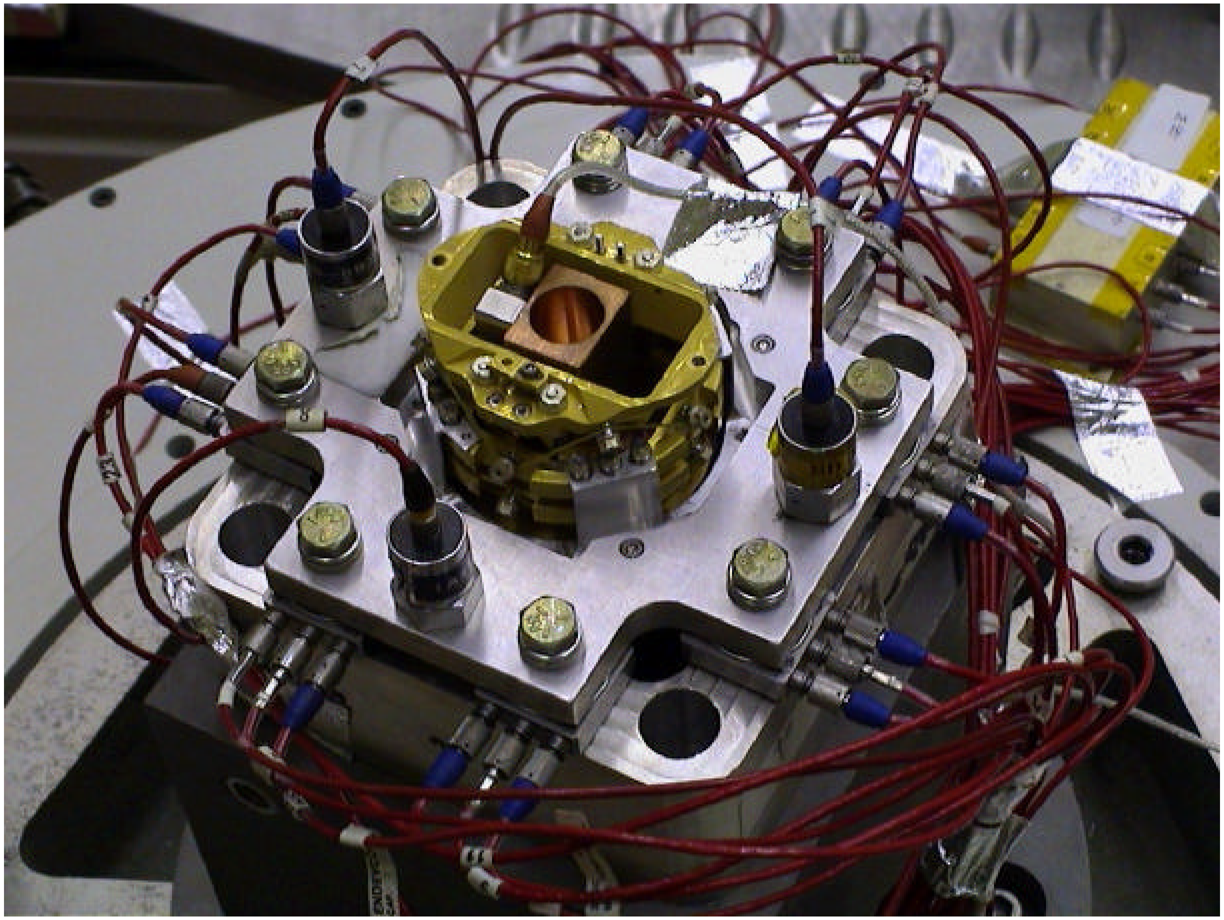


EM Vibration Levels

Axis	Frequency (Hz)	Level
Long/Lat	20-100 Hz	+6 dB/Oct
Long/Lat	100-300 Hz	0.05 g^2/Hz
Long/Lat	300-1000 Hz	-6 db/Oct
Long/Lat	Grms	5.27

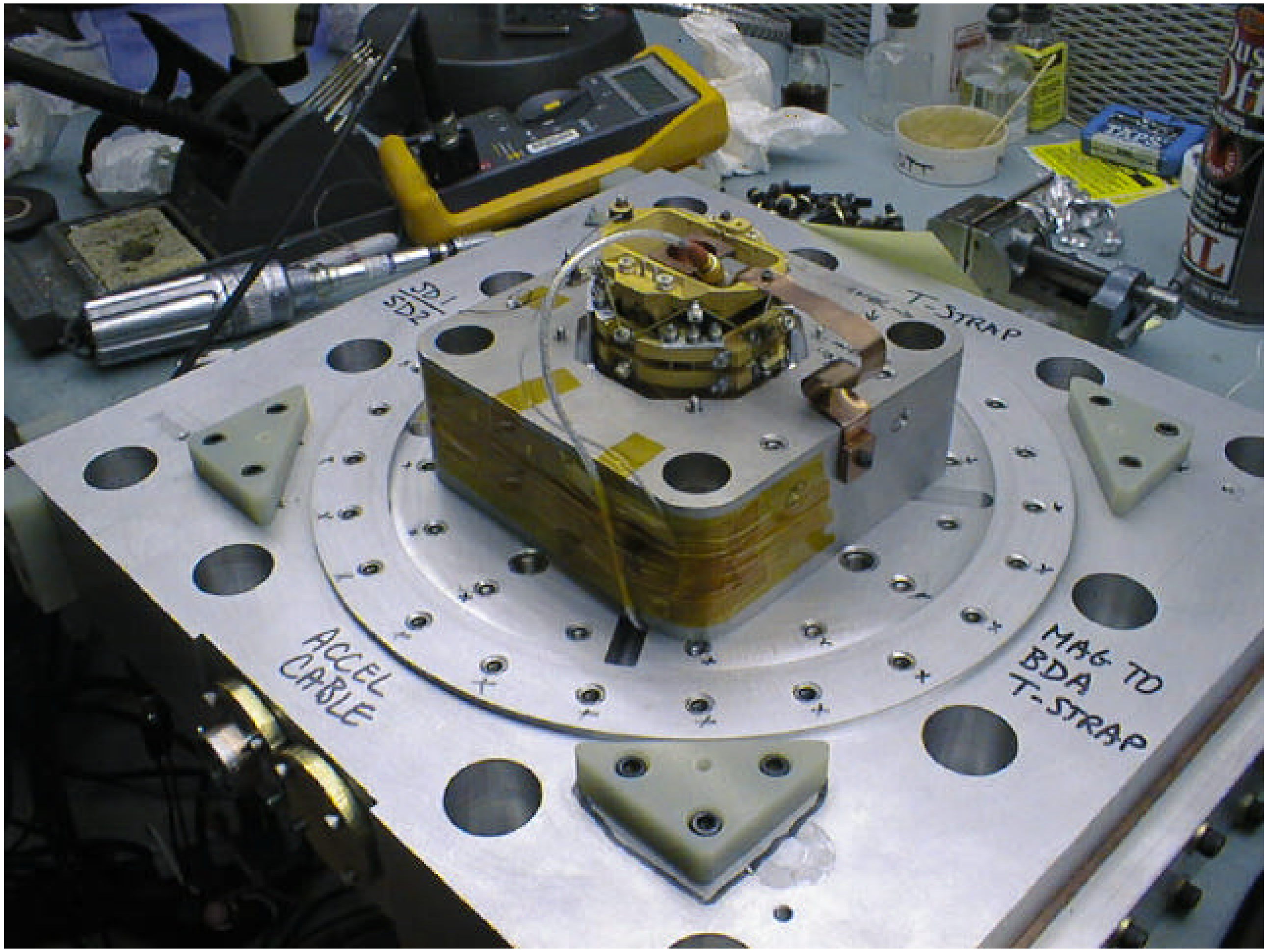
EM BDA Testing

- BDA Warm Vibration with Force Transducers

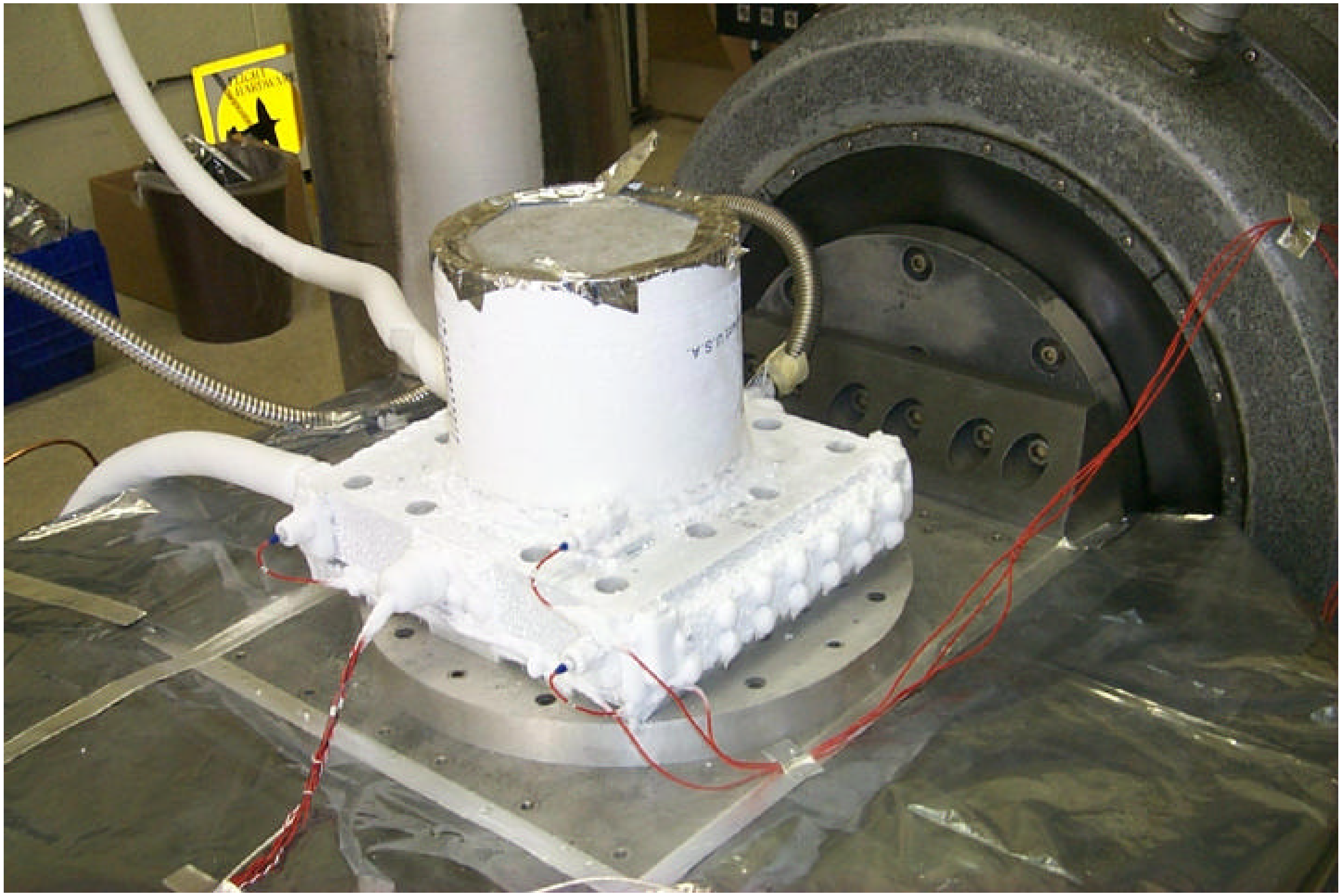


EM BDA Testing

- Cold Vibration Fixture



Cold Vibration



Metrology

Displacement along the z-axis (Optical Axis)
(mm)

Test	pnt17	pnt18	pnt19	pnt20
	0	0	0	0
After Warm Vibration	0.052	0.057	-0.061	-0.064
Install Thermometer	0.057	0.06	-0.064	-0.065
After Thermal Cycling	0.061	0.064	-0.053	-0.051
After Installing Accelerometer	0.053	0.058	-0.052	-0.057
After Warm Vibration with force transducers	0.095	0.108	-0.095	-0.106
After Cold Vibration	0.049	-0.02	-0.017	-0.01

Positional Repeatability Requirement Along z-axis = 0.625 mm

10.0
TEST FACILITIES

Hien Nguyen

Flight Laboratory

- Flight certifiable Lab established in 183-215
  - Contamination Control certification (D-19156) in process
  - ESD certification is in process
  - Safety certification is in process
  - Personnel training is completed
- Test equipment
  - Two laminar flow benches
  - Thermal Characterization/Electronic Interface Dewar
  - JFET Testing Dewar
  - Thermal Cycle Dewar
  - Cold Vibe Fixture
  - BoDAC's, Bolometric Detector Assembly Cryostat
  - Data Acquisition System
  - General Electronics
  - Beam Mapper
  - Spectrometer
- Laboratory is planned to be certified by Nov 01

Thermal Characterization/Electronic Interface Dewar

Also known as Green Dewar

Purpose

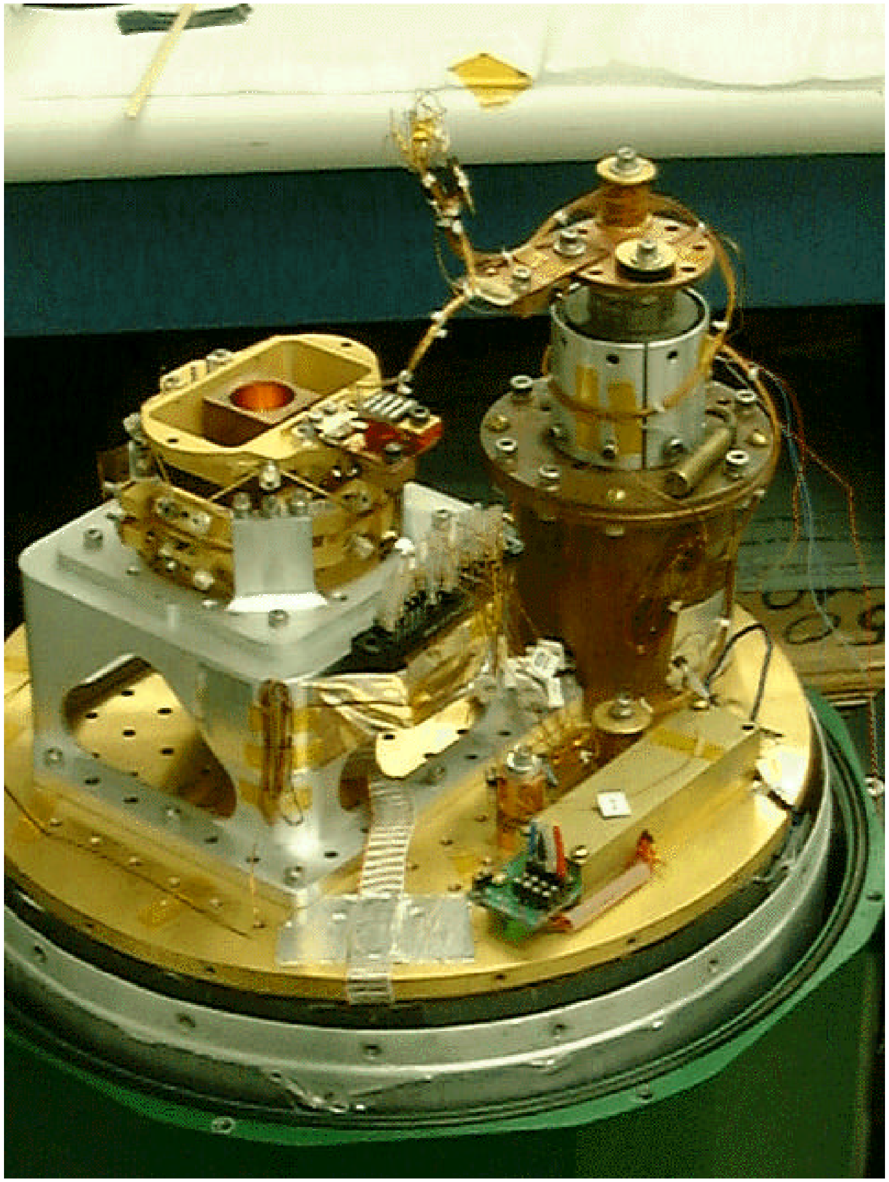
The Green Dewar is to be used for thermal characterization of the BDA. Later it will be used for electronic testing by CEA Team

Status

Functional
Only for EM Testing
Handling Procedure needed for CEA users

Peripherals

Wirings and cables: Completed
^{3}He Fridge: Installed and working



JFET Testing Dewar

Also known as The Blue Dewar

Purpose

To Characterize JFET Performance

Description

Small IR LAB Helium Cryostat

Status

Functional

Procedure and Certification needed

Peripherals

Preamp: Completed

Internal Wiring: Completed

Warm Cable: 80% Completed

Insert Picture Here

Thermal Cycle Dewar

- Cool Down to 77 K in approximately two hours
- Automated
    - Closed Cycle Cryostat (Cryogen Free)
- Optical window for the Optical Alignment Test
- Vacuum Electrical Feed-throughs
    - For thermal housekeeping
    - For measuring detector arrays
- Vendor: Cryomech Inc.
- Delivery: November 2001
- Procedure and Certification needed

Pulse Tube Cooler:

The PT405 PulseTube Cryorefrigerator produces cryogenic temperatures below 2.8 K without the use of displacers. Because there are no displacers, there are no displacer seals, no moving cold parts,and almost no vibration.

Cold Vibe Facility

Purpose

Interface Fixture For The BDA
(Both Warm and Cold (LN2))

Description

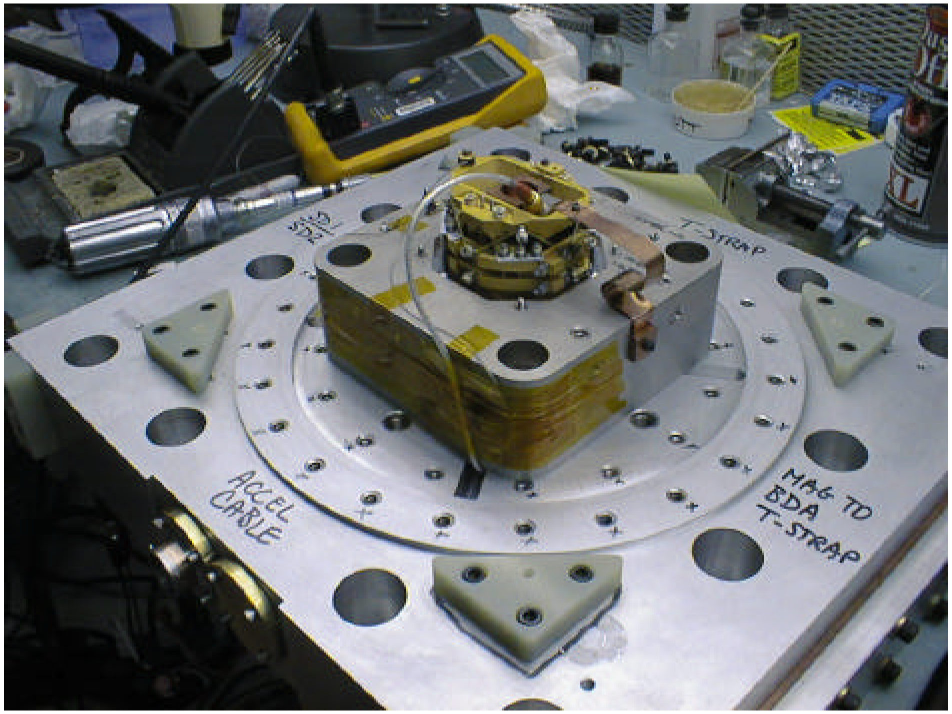
Compatible with BDA and JFET

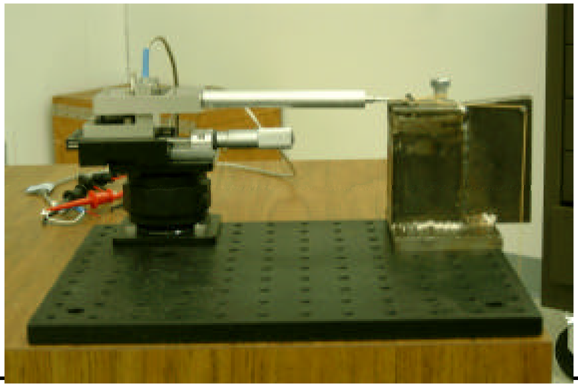
Status

Functional
Approved by Safety
Procedure and Certification needed

Peripherals

Tensionometer and metrology





The BoDAC's

Purpose

To Characterize Bolometer Performance

Description

Internal Optics and Filters
Cryogenics JFET/RF
3He/4He Closed cycle fridge
Warm Electronics
Lockin Amplifier
DAS

Status

Cryogenically Functional
3He/4He fridge operational
Optics and filters provided by Cardiff University, UK
JFET/RF and warm electronics in fabrication
Procedure and Certification needed

Beam Mapper

Purpose

To map the beam profile of the horns

Status

Design Phase

Picture avail. By CDR

Spectrometer

Purpose

To measure the spectral response of BoDAC

Description

Bruker IFS 120 HR Far IR Spectrometer

Operate from 10 to 4800 cm^{-1}

Continuous scanning

Status

On Loan to Glenn's Group in University of Colorado

Setup completed and ready for feedhorn testing

Picture available
by CDR

Documentation Schedule

Item	Document	% Complete	Completion Due Date
LN2 Vibration Test	Procedure	75%	Aug-01
	Certification	In Process	Sep-01
Thermal Cycling	Procedure	25%	Sep-01
	Certification	-	Dec-01
JFET Performance Testing	Procedure	-	Oct-01
	Certification	-	Nov-01
Bolometer Performance Testing	Procedure	25%	Oct-01
	Certification	In Process	Jan-02
Environmental Test Readiness Review	N/A	N/A	Nov-01
Performance Test Readiness Review	N/A	N/A	Jan-02

Hardware Schedule

Item	% Complete	Date Needed
BoDAC #1	100	Jul-01
3He/4He Fridge	75	Sep-01
Optics	80	Sep-01
Detector Mount	25	Oct-01
Cryocabling	50	Oct-01
JFETs	40	Oct-01
RF Filters	40	Oct-01
IR Filters	0	Sep-01
Warm electronics	60	Dec-01
Lockin amplifiers	90	Aug-01
Data Acquisition System	20	Dec-01
Software	0	Jan-01
Spectrometer	90	Nov-01
Beam Mapper	40	Sep-01
BDA and JFET simulators	10	Nov-01

Open Issues

- Schedule seems to have less slack than we would like for our test program

11.0
Mission Assurance Management

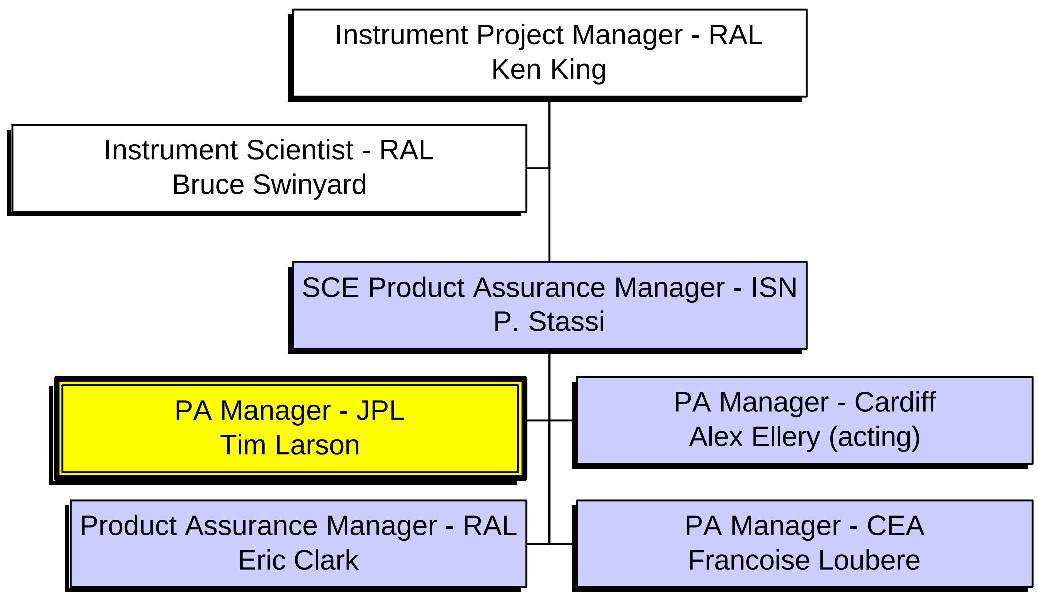
Gordon Barbay

Outline

- SPIRE Product Assurance Organizations
- JPL Mission Assurance Drivers
- Risk Management & Policy
- Mission Assurance Team
- Models & Implementation
- Mission Assurance Design Principles
- Mission Assurance Requirements & Documentation
- Mission Assurance Execution:
  - Systems Safety
  - Quality Assurance
  - Parts, Materials, Processes
  - Reliability Engineering
  - Environmental Engineering
  - Contamination Control
  - Problem/Failure Reporting
  - Configuration Management & Waivers

PA Organizational Interfaces

SPIRE PA Organization



Yellow = JPL Mission Assurance

Blue = JPL MA Interfaces

JPL Mission Assurance Drivers

- New, enabling technologies
  - New parts, materials, and processes
- Establishing "custom" reliability tests
  - Non-standard materials, processes
  - Cryogenic test & operating temperatures
- Multiple organizational interfaces
- Variations from European partners in established nomenclature (models, documentation)
- Transitions of technology development to flight hardware development

Risk Management

- The JPL Herschel/PLANCK project will:
    - 1. Plan and implement a disciplined approach to risk management throughout the project life cycle
    - 2. Support management decision-making by providing integrated risk assessments
    - 3. Communicate risk status to all project and appropriate NASA, JPL, and European Partners' management personnel
- The project risk policy is designed to first minimize risk (See Risk Policy).
- Mission Assurance program targets areas of risk for technologies and processes
    - Table identifies the SPIRE areas of risk and implications for mission assurance program at JPL.

Risk Policy

Herschel/Planck Project Risk Policy

Programmatic Objectives and Constraints

As a junior partner in a collaboration with Europe on the Herschel and Planck missions, JPL's objectives are to provide the European Space Agency (ESA) and the relevant instrument Principal Investigators (PIs) with specific contributions that benefit the overall science value of both missions and allow U.S. scientific participation in the resultant research efforts. The JPL effort is constrained by a funding profile determined by NASA headquarters. Within the risk policy and budget profile, JPL's goal is to maximize the performance contribution to both missions.

The Herschel and Planck missions are major scientific endeavors for ESA. Although both Herschel and Planck will be validating new technologies, they are not considered to be technology validation missions where significant risk-taking would be acceptable. Both missions must succeed in meeting their required science objectives.

Herschel/Planck Risk Policy

Minimizing risk to the overall mission is the highest priority. It is the goal of the Herschel/Planck project to eliminate the possibility that any single-point failure causes mission failure. This means that all items that are mission critical will have built-in redundancy, where this is possible (ex., Planck cryocooler). Where this is not possible (ex., Herschel telescope) special risk avoidance measures will be taken to minimize mission risk. Plans and status of this risk avoidance will be an important part of project reviews. Minimizing risk to mission performance is a second priority which will be addressed within schedule and budget limitations.

Risk Avoidance/ Risk Acceptance/ Risk Taking

When possible within the project constraints and the performance goals of the project, the emphasis shall be on risk avoidance rather than risk acceptance. When faced with a trade-off between risk acceptance and performance, risk acceptance can be considered as an acceptable alternative only when the risk being considered avoids placing the entire mission at significant risk as stated in the risk policy. Therefore some risks may be accepted with mitigation and justification. Such decisions will be made in collaboration with the appropriate European PI.

The JPL Herschel/Planck Project emphasizes risk avoidance by minimizing risk through:

- analysis and redesign
- alternative developments
- parallel developments
- appropriate margins

Where the JPL Herschel/Planck Project decides to accept risks, risk will be minimized by:

- developing contingency plans and margin management criteria
- exercising those plans
- allowing descope/reduction in mission return to trade against cost, schedule, and other resources

Some performance reduction options were exercised in Phase B, and any new options need to be identified and agreed upon (and will be listed on prioritization of performance list). Herschel/Planck may move risk from cost risk to performance risk, remaining within the performance requirements and agreements with ESA and the instrument PIs.

SPIRE Risk Management

Project Element	Technology/Process	Target Area	MA Actions
SPIRE	Bolometer Array technology	• Definition & implementation of qualification, assembly, test	• Qualification Plan D-19152 "SPIRE Bolometer Qualification Plan"
SPIRE	BDA thermal isolation/mechanical design	• Qualification	• Verification of thermal requirements & performance on Qual Model
SPIRE	JFET Module (Differential Amplifier Circuitry)	• Qualification	• Qualification Plan D-19153 "SPIRE JFET Module Qualification Plan"

JPL Mission Assurance Team

Mission Assurance Manager	Tim Larson
Quality Assurance	Donna Markley
System Safety	Karan L'Heureux
Reliability	Gordon Barbay
Environments:	Gordon Barbay with Peter Barrett
Dynamics	Peter Barrett, Terry Scharton, Dennis Kern
EMC	Al Whittlesey, Tom Larter
Thermal	Jim Fu, Henry Abakians
Space Radiation Environments	Martin Ratliff
Electronic Parts Engineering	Ed Erginsoy
Materials & Processes	Mike Knopp
Configuration Management	Charles Davis
Contamination Control	Glenn Aveni

Model Summary

	EBB	QM	PFM/FM	FS
HIFI		X	X	X
SPIRE		X	X	X
Sorption Cryocooler	X		X	
HFI		X	X	X

SPIRE has 5 qualification models, two of which will be flight spares

Key (see D-19155, section 2):

EBB = "Elegant" Breadboard (Fidelity between traditional Breadboard and Engineering Model)

QM = Qualification Model

PFM = Protoflight Model (Flight hardware for which there is no previous qualification heritage)

FM = Flight Model

FS = Flight Spare

Mission Assurance Requirements Flow

H/P PA Instrument Requirements

JPL SMA Best Engineering Practices

JPL
Safety & Mission Assurance (SMA)

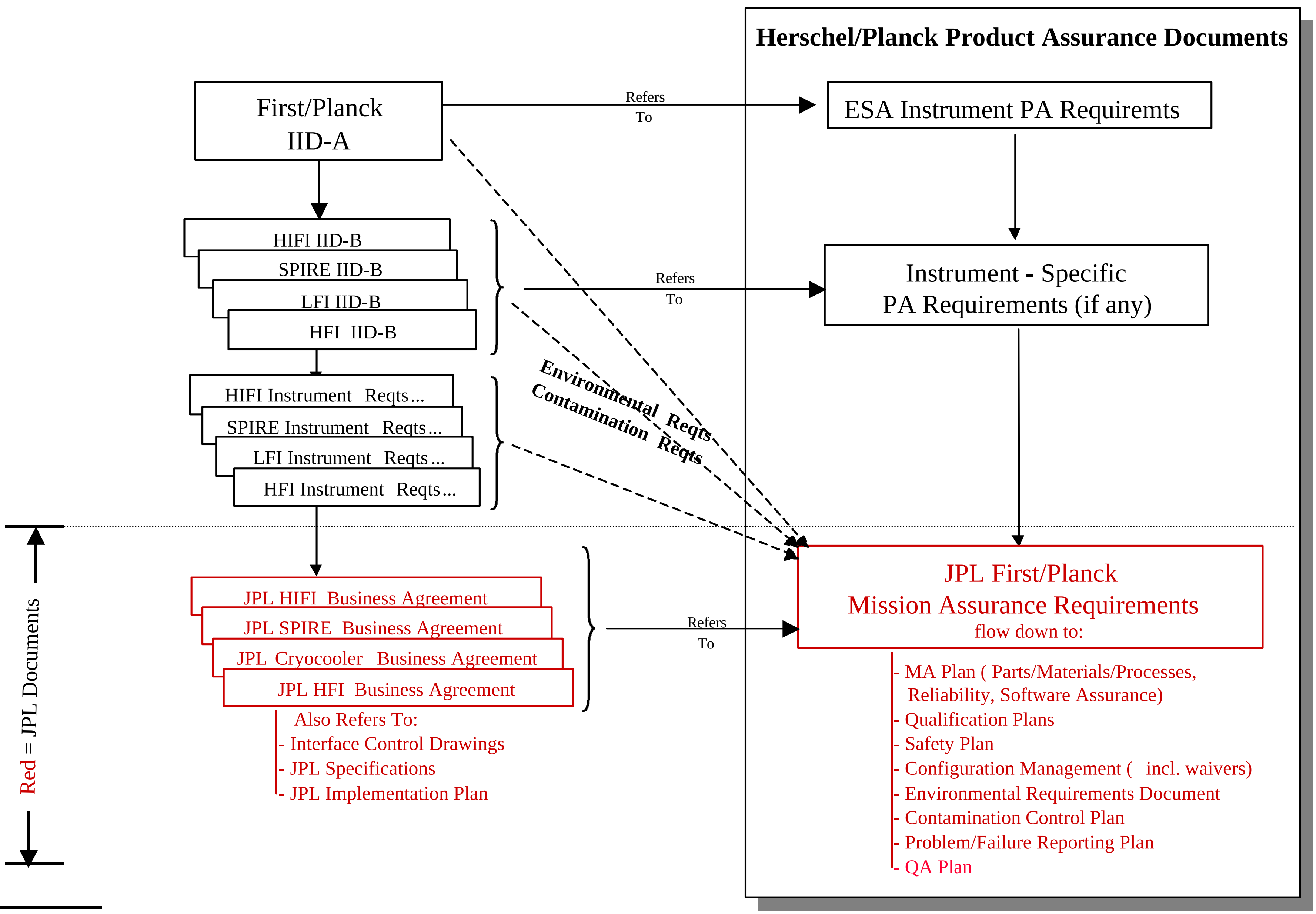
ESA Product Assurance

JPL Herschel/Planck SMA Requirements

Mission Assurance Design Principles

- Response to D-17868 "Design, V&V, and Ops Principles for Flight Systems" February 2001
  - Filtered for Mission Assurance-related principles
  - Each item dispositioned. See attachments.
  - No exceptions at this time (for Mission Assurance)

Product Assurance Documents



MA Documentation

Mission Assurance Requirements for the Herschel/Planck Mission	D-16642	RELEASED 1/01
Herschel/Planck Mission Assurance Plan (includes Parts/Materials/ Processes, Quality Assurance, Reliability)	D-16874	RELEASED 4/01
FIRST/Planck Safety Plan	D-16875	RELEASED 12/00
FIRST/Planck Risk Management Plan	D-16857	RELEASED 11/00
Herschel/Planck Configuration Management Plan (includes Waivers)	D-16873	RELEASED 1/01
FIRST/Planck Problem/Failure Reporting Plan	D-19151	RELEASED 10/00
Herschel/Planck Contamination Control Plan	D-19156	RELEASED 4/01
Herschel/Planck Quality Assurance Plan	D-19173	TBR August 2001
Herschel/Planck Environmental Requirements Document	D-19155	RELEASED 2/01
SPIRE Product Assurance Requirements Map	D-19164	TBR September 2001
SPIRE Bolometer Detector Assembly Qualification Plan	D-19152	RELEASED 7/01
SPIRE JFET Module Qualification Plan	D-19153	TBR August 2001

System Safety (1 of 2)

- Requirements & Implementation: Herschel/Planck Safety Plan (D-16875)
  - Meets requirements of:
    - JPL D-560 “JPL Standard for Systems Safety” applicable to hardware developed, integrated, or tested at JPL
    - RS-CSG-Ed.5 (0) Vol. 1 “CSG Safety Regulations (Payload Design)”
    - RS-CSG Ed. 5 (0) Vol. 2 “CSG Safety Regulations (Payload Preparation)”
  - Responsive to:
    - “Ariane 5 Users Manual” Issue 3, Rev 0
    - MSFC-HDBK-527
    - JSC 09604 “Materials Selection List for Space Hardware Systems”
    - NASA Technical Standards, where applicable
    - NFPA Regulations
    - National Electrical Code
    - Federal OSHA Regulations
    - Environmental Protection Agency Regulations

System Safety (2 of 2)

- Safety Challenges:
  - Cryogenics
  - Pressurized Tanks
  - No pyrotechnic devices, no ionizing radiation devices, no batteries, no propellants, no hazardous materials, no power during launch
- Safety Compliance Documentation: Hazard Analysis
- Preliminary Safety Survey of 183-215 Lab Complete
  - No issues, waiting for final equipment delivery & installation
- Certification of Qualification tests (Cold Vibration Test)

Quality Assurance (1 of 2)

- Requirements & Implementation:
  - Mission Assurance Requirements for Herschel/Planck (D-16642)
  - Quality Assurance Plan (D-19173)

- Scope:
  - Facilities Certification
  - Procurement Control
  - Manufacturing and Assembly control
  - Integration and Test control
  - Handling, Storage, Packaging, Marking, Labeling, Transportation Control
  - Acceptance and Delivery

Quality Assurance (2 of 2)

- MDL: Flight build preparations for detector arrays are near completion
  - Processes are documented (evaluated by J. Bock)
  - Procedures completed, in approval cycle and in PDMS
  - Process traveler completed and approved
  - Fabrication AIDS are approved
  - Facilities are certified
  - Personnel are certified and trained
- Fabrication and Test (Building 103):
  - QA is ready to support integration of detector array into BDA in Bldg. 103
    - Generation fabrication procedures and AIDS
    - Qualification units fabrication _____

Parts, Materials, Processes (1 of 5)

- Requirements & Implementation:
  - Mission Assurance Requirements for Herschel/Planck (D-16642)
  - Mission Assurance Plan for Herschel/Planck (D-16874)
- Requirements/Scope:
  - Approvals of required Parts, Materials, Processes
    - Review of M&P accomplished through Material Identification & Usage Lists (MIUL)
    - Review of electronic parts accomplished through approved parts lists
  - Prohibited materials, Alerts
  - Electronic parts MIL-STD-975M Grade 1 or 2 parts or equivalent
  - Derating per JPL Derating Guidelines (D-8545) for electronics
  - Radiation TID 20 Krad (includes RDM = 2), SEU LET = 37 MeV/cm^2, SEL LET = 75 MeV/cm^2
  - Lot Acceptance Test & Screen
  - Requirements flow down to suppliers

Parts, Materials, Processes (2 of 5)

- Requirements/Scope (continued):
  - Qualification Plans:
    - Qual Plans for new part types/high risk non-standard parts include manufacturer surveys, design & construction analysis, in-process inspection & test samples, lot qualification, destructive physical analysis, testing (performance, environmental, life), screening
    - Qual Plans for materials/processes not previously qualified for application include thermal vacuum, thermal cycling, radiation, stress corrosion, fracture mechanics

Parts, Materials, Processes (3 of 5)

- Safety & Mission Assurance working with PEMs concurrently for approval of parts, materials, processes
- Activities:
  - Preliminary MIUL for BDAs
    - Not all materials and processes identified
    - Final PMP lists expected by ________
  - Parts/Materials Selection
  - Qualification support
  - Procurement/procurement support
  - Stores, Radiation Test Facilities, Electronic Parts Evaluation Laboratory, Failure Analysis Laboratory

Parts, Materials, Processes (4 of 5)

PMP Status

- **M&P**
  - **Preliminary MIUL for BDA Complete**
    - **Working to identify remaining materials and processes**

- **EEE Parts - Two parts identified**
  - **U401 JFET – JPL approved part, being procured**
  - **Murata EMI chip filter – JPL unapproved part, going through element evaluation to class K**

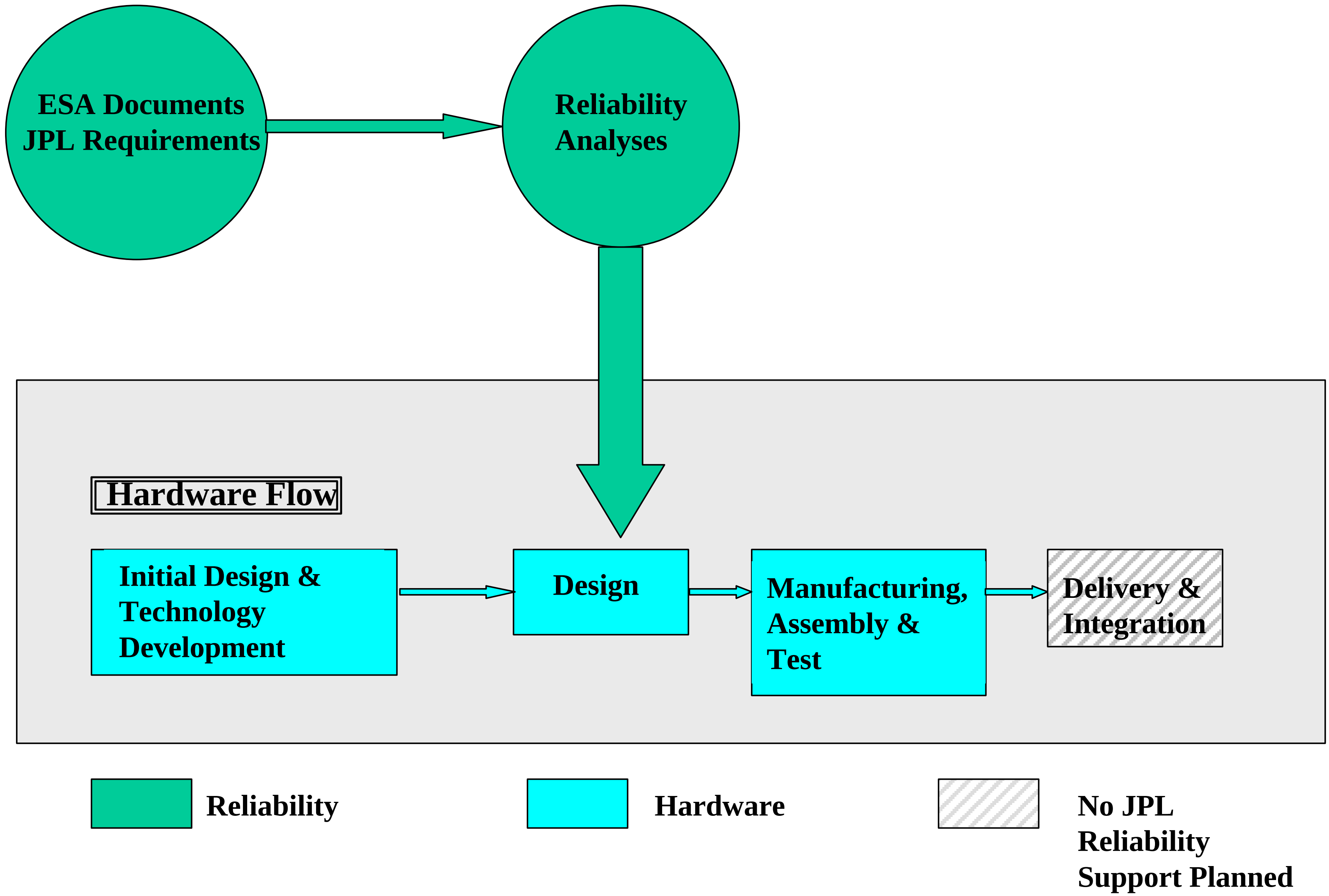
Parts, Materials, Processes (5 of 5)

- Specific Support - The Cognizant Engineer ensures the appropriate participation, including drawing approval, of engineering specialists:

Discipline	Contact
Cabling Engineering	Mark Hetzel (ASI), Mick Tickner
Contamination	Glenn Aveni
Electronic Packaging Engineering	Roy Packard, Charlie Kaczinski
Fabrication Engineering	Randy Fayner
Fasteners	Don Lewis
Materials & Processes	Mike Knopp
Mechanical Components	Mike Knopp
Structures & Dynamic Analysis	Mike O'Connell, Michelle Coleman, Peter Barrett
Temperature Control	Jim Fu, Henry Abakians
Radiation Control	Al Hoffman, Martin Ratliff
Electronic Parts	Ed Erginsoy, Parts Specialists
Connectors	Pat Dillon
PDMS (Drawing Control)	Charles Davis, Mike Stefanini
Shipping Containers	Mick Tickner

Reliability Engineering (1 of 5)

Reliability Analysis Requirements



Reliability Engineering (2 of 5)

Reliability Analyses Matrix

	FIRST/Planck JPL Hardware - Reliability Analysis						
ITEM	Parts Stress Analysis (PSA)	Worst Case Analysis (WCA)	Power Supply Transient Analysis	Sneak Circuit Analysis (SCA)	Failure Modes, Effects and Criticality Analysis (FMECA)	Fault Tree Analysis (FTA)	Ground Support Equipment (GSE) FMECA
Herschel							
HIFI	A	A	N	N	A	A	A
SPIRE	A	A	N	N	A	N	A

N = Analysis Not Required
A = Analysis Required

WCA, PSA FMECA completed July 2001
GSE FMECA TBD by September 2001

Reliability Engineering (3 of 5)

- Requirements & Implementation:
  - Mission Assurance Requirements for Herschel/Planck (D-16642)
- Detailed Requirements:
  - Assure flight hardware operation within specification over expected environments and conditions (including design margins)
  - During design process, perform:
    - Fault Tree Analysis and Failure Modes, Effects & Criticality Analysis
    - Parts Stress Analysis and Worst Case Analysis
    - Identification of single point failures and critical items
    - Infusion of Lessons Learned (preventive action) http://llis.nasa.gov

Reliability Engineering (4 of 5)

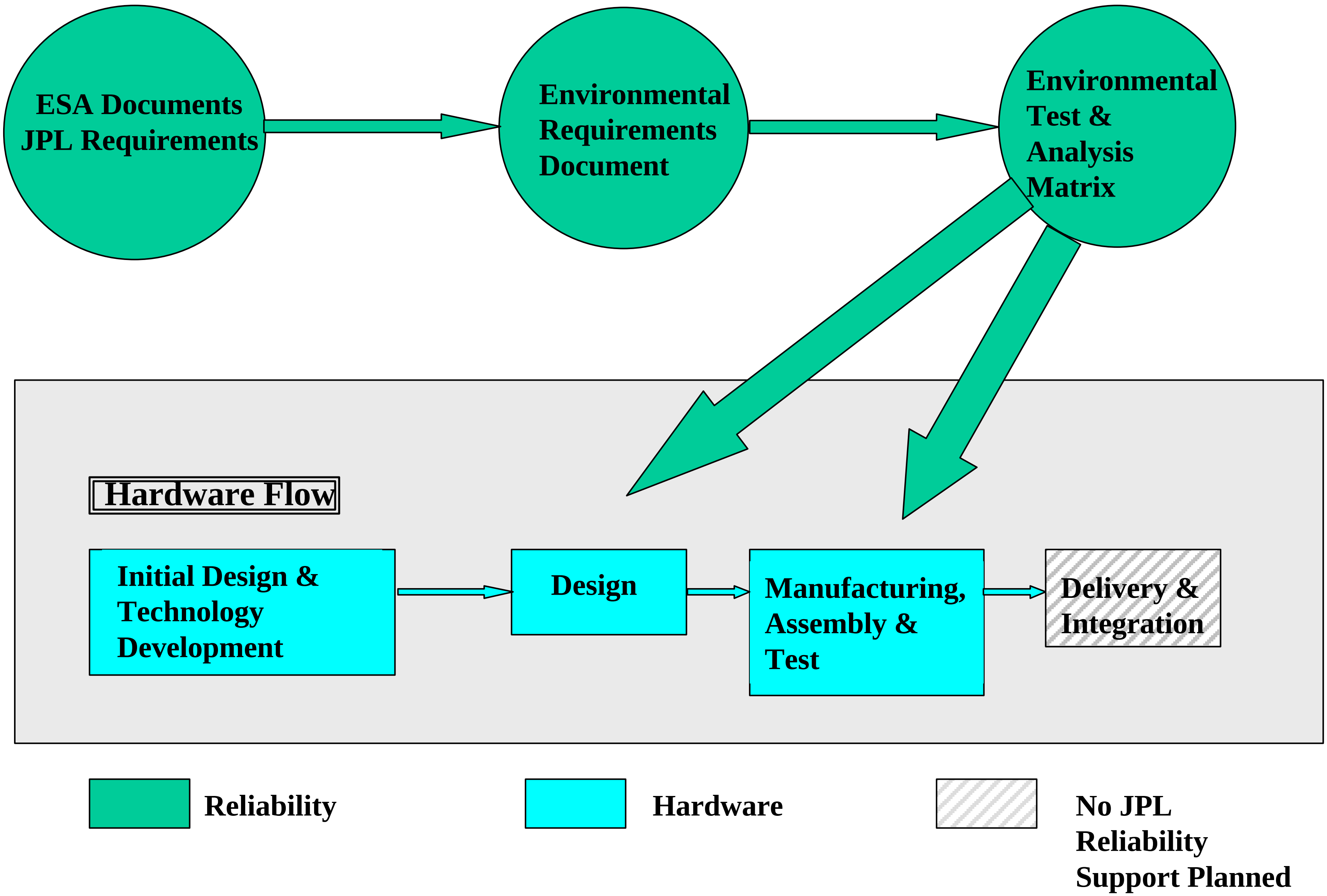
- Flight Electronics Operating Hours
  - Design Principles:
    - Unit Level prior to spacecraft integration minimum of 200 hours
    - System Level prior to launch minimum:
      - 1000 hours single string
      - 500 hours each side of redundant (with goal of 1000 hours)
  - Operating time measured by “youngest” replacement part
  - Requirement needs to be specified in Herschel/Planck MA requirements document (No ESA requirement at this time)

Reliability Engineering (5 of 5)

- Reliability Analyses Results:
  - Parts Stress & Worst Case Analysis
    - Insufficient data to assure EOM success
    - Plans to close issue
      - Acquire historical data
      - Explore feasibility of testing
      - Other avenues
  - FMECA Analysis
    - No discrepancies found
    - Possible shorts between cable harness wires issue
      - Add to FMECA analysis, if needed (August 2001)

Environmental Engineering (1 of 9)

Environmental Analyses and Test Requirements



Environmental Engineering (2 of 9)

Environmental Analyses Drivers

- **Dynamics**
  - **Ariane 5 Launch Vehicle**
- **Thermal**
  - **Multiple Thermal Environments**

•EMC/EMI

•Natural Space Environment

- **Using Standard Environments for L2 Orbit**

Environmental Engineering (3 of 9)

Environmental Test and Analysis Matrix - Part 1

			Static Load		Earth Handling			Dynamics			
	HARDWARE ITEM	Test Program Type	Static Loads	Quasi-static acceleration	Package Drop & Trans Vibration	Humidity	Explosive Atmosphere	Acoustic	Vibration - sine	Vibration - Random	Pyro. Shock/Simulated Drop Shock
	SPIRE (Jerry Lilienthal)										
	Qual Cold Electronics JFET Module	Q	A	A	Z	Z	Z	N	X	X	SD
	Proto Flt Cold Electronics JFET Module	PF	A	A	Z	Z	Z	N	X	X	N
	Flt Spare Cold Electronics JFET Module	FA	A	A	Z	Z	Z	N	X	X	N
	Qual Photometer Assembly	Q	A	A	Z	Z	Z	N	X	X	SD
	Flt Spare Photometer Assembly	PF	A	A	Z	Z	Z	N	X	X	N
	Proto Flt Photometer Assembly	FA	A	A	Z	Z	Z	N	X	X	N
	Qual Spectrometer Assembly	Q	A	A	Z	Z	Z	N	X	X	SD
	Proto Flt Spectrometer Assembly	PF	A	A	Z	Z	Z	N	X	X	N
	Flt Spare Spectrometer Assembly	FA	A	A	Z	Z	Z	N	X	X	N
SD =	Simulated Drop Shock										
C =	Cold Vibration Test (4 deg K)										
Z =	No Test or Analysis is Required if Approved Procedures are Followed and Acceptable Environmental Conditions are Maintained										
N =	Neither Test or Analysis Required										
H =	Test or Analysis Req at the Higher Level of Assembly or One Analysis Performed for The Group										
X =	Test Required										
A =	Analysis Required										

Environmental Engineering (4 of 9)

Environmental Test and Analysis Matrix - Part 2

		Thermal						Natural Space						
HARDWARE ITEM	Test Program Type	Contamination	Temp. ground handling	Thermal Shock	Launch Press Profile	Temp./ Atmosphere	Thermal Vac.	Ionizing Dose	Displacement Damage	Low Dose Rate	EUV	Single Event Effects	Solid Particles	Orbital Debris Generation
SPIRE (Jerry Lilienthal)			A	A	A			A	A	A	A	A	A	A
Qual Cold Electronics JFET Module	Q	Z	H	H	H	N	X	H	H	H	H	H	H	H
Proto Flt Cold Electronics JFET Module	PF	Z	H	H	H	N	X	H	H	H	H	H	H	H
Flt Spare Cold Electronics JFET Module	FA	Z	H	H	H	N	X	H	H	H	H	H	H	H
Qual Photometer Assembly	Q	Z	H	H	H	N	X	H	H	H	H	H	H	H
Flt Spare Photometer Assembly	PF	Z	H	H	H	N	X	H	H	H	H	H	H	H
Proto Flt Photometer Assembly	FA	Z	H	H	H	N	X	H	H	H	H	H	H	H
Qual Spectrometer Assembly	Q	Z	H	H	H	N	X	H	H	H	H	H	H	H
Proto Flt Spectrometer Assembly	PF	Z	H	H	H	N	X	H	H	H	H	H	H	H
Flt Spare Spectrometer Assembly	FA	Z	H	H	H	N	X	H	H	H	H	H	H	H

Environmental Engineering (5 of 9)

Environmental Test and Analysis Matrix - Part 3

HARDWARE ITEM	EMC						
	EMC Conducted susc. Note 3	EMC Radiared susc.	EMC Cond Emissions	EMC Radiated Emission	ESD Susceptibility	Magnetic	EMC Isolation
SPIRE (Jerry Lilienthal)							
Qual Cold Electronics JFET Module	H	H	H	H	H	H	X
Proto Flt Cold Electronics JFET Module	H	H	H	H	H	H	X
Flt Spare Cold Electronics JFET Module	H	H	H	H	H	H	X
Qual Photometer Assembly	H	H	H	H	H	H	X
Flt Spare Photometer Assembly	H	H	H	H	H	H	X
Proto Flt Photometer Assembly	H	H	H	H	H	H	X
Qual Spectrometer Assembly	H	H	H	H	H	H	X
Proto Flt Spectrometer Assembly	H	H	H	H	H	H	X
Flt Spare Spectrometer Assembly	H	H	H	H	H	H	X

Environmental Engineering (6 of 9)

- Requirements & Implementation:
  - Herschel/Planck Environmental Requirements Document (D-19155)
    - **JPL Requirement/Analysis Used Where No "flowdown" Requirement Specified**
    - **Resolution of variant requirements addressed as they are identified to JPL by the Instrument**
    - **Approach: Meet ERD requirements and assess hardware capability**

Environmental Engineering (7 of 9)
Environmental Testing

- Environmental Test Authorization & Summary (ETAS) Forms Document Tests on Flight Hardware
  - Documents Configuration, Specs, Approved Deviations, As-Tested Levels, & Results
  - Approved and Tracked by Environmental Requirements Engineer (ERE)
  - Used to Provide Documentation for Reviews
- Test Failures Reported and Tracked via P/FRs
- Any Re-testing Based on Need
  - Type and Levels Determined by CogE and ERE

Environmental Engineering (8 of 9)
ERD/ESA Specification Differences

- **ESA requirements derived from IIDA or IIDB**
- **No ESA Radiation Requirement (Environment Only)**
  - **ERD has JPL Derived Requirements**
- **Low Level Sine Sweep: ESA - .5g vs JPL - .25g**
  - **ESA Level Could Cause Excessive Response**
- **ESA High Level Sine Sweep Levels**
  - **Cause Excessive Shaker Displacement (5-20 Hz)**
  - **Potentially Damaging to Hardware (20-100 Hz)**
- **ESA Random Vibration Levels Below JPL Standard Workmanship Levels**

- **Working with European partners to resolve differences**

Environmental Engineering (9 of 9)
Vibration Test

- Vibration Test
  - Warm & Cold Test Performed on BDA EM
  - Warm test on JFET module in work
- Test Results
  - BDA Test Successful

Contamination Control

- Requirements & Implementation:
  - Herschel/Planck Contamination Control Plan (D-19156)
- Detailed Requirements:
  - Assembly, Handling, Test Facilities
    - Class 100,000 (ISO 14644-1 Class 8) cleanroom
    - Class 10 Microdevices Fabrication
- Certification of 183-215 Lab Awaiting Clean Bench Delivery
  - Delivery expected August 2001

Problem/Failure Reporting (1 of 2)

- Requirements & Implementation:
  - Mission Assurance Requirements for Herschel/Planck (D-16642)
  - FIRST/Planck Problem/Failure Reporting (D-19151)
- Non-conforming materials in-process dispositioned on Inspection Report, Non-conforming Materials Report, Destructive Physical Analysis Report
- Problems/unexpected behavior/anomalies reported in P/FR System
- If determined to have impact on European interface, can create NCR
- P/FR system is set up and ready to go

Problem/Failure Reporting (2 of 2)

Begin problem reporting at:

Hardware/ Software	Ground Support Equipment (GSE)	EBB/QM	Flight
Hardware	At GSE Acceptance Test before interface with qualification or flight hardware.	System Electronics: First application of power for performance test prior to assembly level qualification.	System Electronics: First application of power for performance test prior to assembly level flight H/W protoflight testing.
		Mechanical Devices: Starting with assembly level qualification.	Mechanical Devices: Starting with assembly level protoflight testing.
Software	At GSE Acceptance Test before interface with qualification or flight hardware.	Prior to integration.	Prior to integration.

Configuration Management (1 of 3)

- Requirements & Implementation:
  - Mission Assurance Requirements for Herschel/Planck (D-16642)
  - Herschel/Planck Configuration Management Plan (D-16873)
- Baselines, changes, controlled change decision-making process
- Scope includes, but not limited to:
  - Engineering data
  - Proposal data
  - Requirement data
  - Specification data
  - Design data
  - Fabrication or assembly data
  - Test or inspection data
  - Repair or rework data
  - Change or modification data
  - Configuration lists
  - Parts lists and Bills of Material
  - Documentation and drawing lists
  - Problem, failure or anomaly reports
  - Plans
  - Work Package Agreements
  - Interface Agreements/Commitments
  - Project/Programmatic Documentation

Configuration Management (2 of 3)

- Configuration Control Begins:
  - Documents/Drawings/Plans: First release
    - "Pre-release" control for drawings
  - QM and Flight Hardware: complete traceability
    - Lot traceability on procured items
    - Serial number traceability on built items
- Configuration Control Services
  - Project Data Management System: Drawings, Waivers, Engineering Change Requests, Project Documents, Master Control Document List, Project Archive
  - Project Library: Work Areas, Reviews, Presentations
  - PFOC: Problem/Failure Reporting System
  - QA: QA Records
  - DMIE: JPL Institutional Documents

Configuration Management (3 of 3)

- Waivers
  - ESA “Request for Waiver” for ESA-approved Requirements
  - JPL Waiver Form for JPL-approved requirements that do not impact post-delivery I&T, launch, operations

Mission Assurance

Backup Charts: Attachments

- Mission Assurance Design Principles Conformance Matrix

Mission Assurance Design Principles (1 of 8)

1.10	4	During development a list of potential credible single point failures shall be developed, maintained and reported at PMSR, PDR, CDR, ATLO START and Launch.	Will Comply. Will be documented during design analysis on "Critical Items and Single Point Failures" form.
1.10	5	The list of accepted potential single point failures shall be communicated to the flight operations team. Particular attention shall be given to those items where the risk mitigation plan requires flight operational actions.	Will Comply. Inputs will be to Instrument Teams for HIFI, HFI, SPIRE, to Spacecraft Systems/Ops Team for Telescope, and to both ? for Sorption Cryocooler.
1.12	1	The project shall plan early in the formulation phase for adequate safety and mission assurance activity, and shall identify the responsibilities of the participating organizations in tailored Safety and Mission Assurance plans. These plans shall define	Comply.
1.13	1a	- Mission Assurance and Independent Assessment	See D-16874 "FIRST/Planck Mission Assurance Plan"
1.13	1b	- System Safety	See D-16875 "FIRST/Planck Safety Plan"
1.13	1c	- Reviews	See Project Implementation Plan (PIP) section on Reviews.
1.13	1d	- Reliability Engineering	See D-16874 "FIRST/Planck Mission Assurance Plan"
1.13	1e	- Quality Assurance	See D-16874 "FIRST/Planck Mission Assurance Plan"
1.13	1f	- Electronic Parts Engineering	See D-16874 "FIRST/Planck Mission Assurance Plan"
1.13	1g	- Risk Management	See D-16857 "FIRST/Planck Risk Management Plan"
1.13	2	Assurance engineering shall be integrated and concurrent with the design activity throughout the project life cycle.	Comply. Started late due to technology development (appropriately) not including assurance engineering processes. Progressing at an acceptable rate. Still "catching up" on HFI and SPIRE.

Mission Assurance Design Principles (2 of 8)

No.	Item	Requirement	Disposition
1.13	1	The project shall plan early in the formulation phase for adequate safety and mission assurance activity, and shall identify the responsibilities of the participating organizations in tailored Safety and Mission Assurance plans. These plans shall define	Comply.
1.13	1a	- Mission Assurance and Independent Assessment	See D-16874 "FIRST/Planck Mission Assurance Plan"
1.13	1b	- System Safety	See D-16875 "FIRST/Planck Safety Plan"
1.13	1c	- Reviews	See Project Implementation Plan (PIP) section on Reviews.
1.13	1d	- Reliability Engineering	See D-16874 "FIRST/Planck Mission Assurance Plan"
1.13	1e	- Quality Assurance	See D-16874 "FIRST/Planck Mission Assurance Plan"
1.13	1f	- Electronic Parts Engineering	See D-16874 "FIRST/Planck Mission Assurance Plan"
1.13	1g	- Risk Management	See D-16857 "FIRST/Planck Risk Management Plan"
1.13	2	Assurance engineering shall be integrated and concurrent with the design activity throughout the project life cycle.	Comply. Started late due to technology development (appropriately) not including assurance engineering processes. Progressing at an acceptable rate. Still "catching up" on HFI and SPIRE.
1.13	3	Project quality assurance provisions shall be flowed down to all project acquisitions.	Will Comply. Telescope and HIFI LO contracts, and parts/ materials/processes procurements will include QA provisions.
1.13	3R	*Rationale: Proposals should reflect S&MA approach to customer, and assurance engineering can be involved in the earliest design decisions. Avoids redesign resulting from after-the-fact MA review, and resolves product quality issues as they arise. Commu*	(Rationale)
1.16	1	The design shall be reviewed early in the formulation process, and at appropriate points in the life-cycle, by the engineering team against the JPL/ NASA Lessons Learned data base, NASA/JPL Alerts, etc. Each item of potential applicability to the project	Will Comply. There are 805 Lessons Learned. Need to consolidate into what is applicable (some are). Make or Get LL to provide a selectable, dispositionable list. Alerts will be reviewed during parts/materials/processes approvals.
1.16	1R	*Rationale: Important "lessons" can be drawn from past events which have applicability beyond the original event, which can preclude recurrence of faults/failures, and enable early and cost-effective changes. Some examples of past troublesome areas are:*	(Rationale)

Mission Assurance Design Principles (3 of 8)

No.	Item	Requirement	Disposition
1.18	1	The project shall perform, with appropriate independent assessment support, a total mission risk assessment at inception of project, and as defined for reviews.	Will Comply As Applicable, at Project-Element Level and at Project Level. Peer Reviews and PDR are independent inputs to this assessment. Define GPMC's role in this.
1.18	1R	*Rationale : To ensure JPL and customers are informed of risk to program/project success, and to provide independent assessment back to project to enable possible mitigation approaches outside the project's sphere of influence.*	(Rationale)
1.18	2	These assessments shall specifically identify and address risks to project and program objectives.	Will Comply. Determine how documented.
1.18	3	Risk assessments shall specifically include margin assessment as one of the risk metrics.	Will Comply As Applicable.
1.19	3	Particular attention should be given to Red Flag PFRs/unverified failures and ISAs. (new)	Will Comply.
1.19	3R	*Rationale: Identifies incompatibilities between previous usage and current mission requirements.*	(Rationale)
1.19	1	A tailored closed loop problem failure reporting (PFR) system shall be implemented. Strategy, specific approach, and timing for instituting PFRs shall be documented. The JPL electronic problem log/PFR System shall be used.	Will Comply. Need to coordinate with COI.
1.19	1R	*Rationale: Uniformity of describing and reporting problems, and consistent reference capability enables cross-project understanding of risks and implications of the issues.*	(Rationale)
1.19	2	A process that utilizes a concurrent cognizant project team (Project Manager for Red Flag PFRs) shall be established to close problems in a timely and confident manner. Red Flag PFRs or unverified failures shall be compiled and forwarded to the flight op	Will Comply.
1.19	2R	*Rationale: To make the flight team aware of those pre-launch problems that may be a significant threat to flight operations activities. (new)*	(Rationale)
1.27	3	To enable use of engineering or prototype models as flight spares, appropriate actions shall be taken to ensure hardware safety, reliability, and functionality.	Will Comply.

Mission Assurance Design Principles (4 of 8)

No.	Item	Requirement	Disposition
1.31	1	Orbital debris safety considerations shall be addressed during the project formulation phase and during the implementation phase.	Will Comply.
1.31	2	Orbital debris from launch vehicles, spacecraft, instruments or components thereof (e.g., launch vehicle 2nd or 3rd stage, instrument covers) shall be limited, as much as practical, by employing prudent design and flight operations techniques, as appropri	Comply.
1.31	3	The design and flight operations shall employ debris-limiting options (e.g., propellant depletion burns, cover release inhibits) considering normal and off-normal operations, and certain anomalous events (e.g., explosions, breakups, or collision with othe	Not Applicable. Ask Peter Barrett how to document this.
1.31	4	Identification of orbital debris sources, potential hazards and a debris-limiting assessment shall be presented at the SRR. Functional design implementation shall be reviewed at the PDR and finalized at the CDR. (new)	Not Applicable. JPL hardware has no orbital debris sources.
1.31	4R	*Rationale: Limit the proliferation of debris that may be a safety threat to personnel or space vehicles (current and future) generated by orbital debris. (new)*	(Rationale)
			-
2.8B	5	The design shall keep piece-part silicon junction temperatures less than 110°C (assuming a mounting surface temperature of 70°C) for the planned circuit design and packaging scheme. Higher junction temperatures may be considered where risk is shown to be	Will Comply via worst-case analyses.
2.8B	7	Optics, detectors and other unique hardware shall be designed for allowable flight temperature limits extended by -15°C and +20°C and margins may be tailored to specific application based on required operating temperature ranges of sensitive elements.	Will Comply. See D- 19155 "FIRST/Planck Environmental Requirements Document"
2.8C	8	Electronic hardware design shall be capable of surviving power on-off temperature cycling and/or solar exposure cycling of three times the number of worst-case expected mission cycles with worst-case flight temperature excursions. Prior to having a missi	Will Comply As Applicable. Ask Brad's team do we address this in ERD (how).
2.8C	9	Mechanical hardware design thermal cycling profile shall be tailored for the specific application.	Will Comply.
2.8C	10	Flight hardware thermal cycling shall be minimized to preclude the risk of damage.	Will Comply.
2.8C	10R	*Rationale: Thermal cycling has been implicated as a major contributor to faults/problems.*	(Rationale)

Mission Assurance Design Principles (5 of 8)

No.	Item	Requirement	Disposition
2.21	2	The Design shall be assessed for robustness through a program of analyses tailored from the Reliability Analysis Handbook Guidelines (JPL D-5703) or Contractor/Partners equivalent, including Part Parameter Data from available databases, and Derating Guide	Will Comply. Need to determine if this should be in MA Plan (Reliability Section) or in Qual Plans (to be written).
2.21	2	- Worst-case circuit analysis or Voltage-Temperature- Frequency margin testing - to demonstrate performance margin.	-
2.21	2	- Failure mode effects functional analysis (FMEA) at the system/subsystem functional block diagram and interface levels - identifies potential critical single failure points.	-
2.21	2	- System interface circuit, functional, and fault analyses (mechanical, thermal, etc.) - demonstrate that faults in one subsystem/system will not propagate or functionally degrade other subsystems.	-
2.21	2	- Failure Modes Effects/ Criticality Analyses (FMECAs) are generally applied to electronics and electronic functional interfaces, and Fault Tree Analyses (FTAs) to devices and mechanisms).	-
2.21	2	- Parts stress analyses - verify margins.	-

Mission Assurance Design Principles (6 of 8)

No.	Item	Requirement	Disposition
2.22A	0	General	-
2.22A	1	Appropriate derating of parts shall be incorporated in electronics design.	Will Comply. Qualification Plans? need to identify derating approach for custom devices.
2.22A	2	The availability and cost/risk effectiveness of grade-one parts shall be considered before COTS parts become the design baseline.	Will Comply.
2.22A	3	An early design parts list review shall be performed against documented requirements to:	Will Comply. "Catching up" with HFI and SPIRE.
2.22A	3a	- identify long-lead time parts.	-
2.22A	3b	- assess radiation dose, latch up and Single Event Effects (SEE) capability/compatibility.	-
2.22A	3c	- minimize the number of different part types.	-
2.22A	3d	- provide parts vendor assessment information.	-
2.22A	3e	- assure all known parts issues are identified and closed early.	-
2.22A	3f	- benefit from Parts Engineering/independent assessments and knowledge from other missions.	-
2.22A	3g	- provide data to project risk data base.	-
2.22A	3h	- cost-effective match between design and parts capabilities.	-
2.22A	4	The root cause of electronic parts failures shall be determined.	Will Comply.
2.22A	4R	*Rationale: Avoids repeating same or related failure, and develops effective and efficient corrective action that addresses underlying cause.*	(Rationale)

Mission Assurance Design Principles (7 of 8)

No.	Item	Requirement	Disposition
2.25	1	System Safety analyses, inspections and tests, and required reports, shall be performed according to the guidelines and requirements of JPL Standard for System Safety (D-560). These include:	Will Comply.
2.25	1a	- A preliminary hazard analysis- in support of preparation of System Safety Plan	-
2.25	1b	- A Safety Compliance Data Package	-
2.25	1c	- Safety tests and/or inspections, and Facility and operational Safety Surveys	-
2.26	1	Environmental design assessments and verification tests shall be performed to verify the design against the specified environment. These shall be performed at the unit, and system level, considering the requirements and guidelines of JPL D-14040, “Proces	Will Comply As Applicable. See D-19155 "FIRST/Planck Environmental Requirements Document"
2.26	1a	Analyses - Single Event Effects (SEE), micrometeoroid, pressure profile, magnetic fields, etc.	-
2.26	1b	Unit-level Qual random vibration, pyro, thermal, EMC, and Acceptance random vibration and thermal	-
2.26	1c	System-level/ Protoflight random vibration and/or acoustic, pyro shock, thermal vacuum, EMC	-
2.27	1	A minimum power-on operating time shall be established for all electronics as follows:	See below.
2.27	2	Unit Level prior to spacecraft integration minimum of 200 hours	Will Comply. Current requirement states 100 hours pre-delivery, plus 500 hours pre-launch. Need to re-word requirement for clarity, and application to deliveries (assembly versus subsystem).
2.27	3	System Level prior to launch minimum of 300 hours (Goal 1000 hours)	TBD. Does ESA have op hrs reqt?

Mission Assurance Design Principles (8 of 8)

No.	Item	Requirement	Disposition
2.28	1	JPL source QA provisions shall be provided for critical processes/products and strategically applied to high risk suppliers.	Will Comply.
2.28	2	Analyses, inspections, and/or tests shall be performed to ensure that the as-built product is consistent with the as-designed Baseline Configuration.	Will Comply.
2.28	3	Quality assurance provisions, as defined in the Project QA Plan, shall be implemented throughout the ATLO process. Such provisions may include:	Will Comply. Applicable to the extent of JPL ATLO responsibilities.
2.28	3a	- Work proactively in the safety and contamination control activity to ensure hardware integrity.	Note: assure shipping/handling documents include these.
2.28	3b	- Provide configuration support for test and flight software.	-
2.28	3c	- Assure that project documentation requirements are met.	-
2.28	3d	- Conduct a physical verification of all hardware - to ensure that it meets the workmanship, CM and other project requirements.	-
2.28	3e	- Witness Critical operations.	-
2.28	3f	- Maintain spacecraft/instrument configuration log.	-
2.28	3g	- Remain an integral part of the SRCR/HRCR process.	Note: need to assure HRCRs are in Reviews Plan (PIP).
PLES			-
3.3	1	First-time, in-flight events/activities, particularly mission critical or irreversible events shall receive special development attention (e.g., analyzing what ifs, reviewing Red Flag PFRs, unverified failures/ISAs, identifying need for additional testing	Will Comply.

12.0
Implementation Plan

Gerald Lilienthal

Implementation Plan

BDA Structure

- Parallel implementation for CQM hardware
  - If CQM design acceptable (0.12 g^2/Hz TBD) then:
    - Fabricate STM
    - EM modification to accommodate higher loads
    - Test new EM while CQM hardware is on order
  - If a higher level is required (>0.12 g^2/Hz TBD) then:
    - Fabricate STM
    - EM modification to accommodate higher loads
    - Test with higher denier kevlar
    - Negotiate new system resources
    - Fabricate CQM hardware
    - Negotiate schedule and budget revisions

BDA Components

- Bolometers – Go ahead with fabrication
- Kapton Cable
  - Complete and test EM2 cable, then fabricate CQM
- Load Resistors and Backshorts – Go ahead with fabrication
- Horns – Go ahead with delivery of photometer horns; await data and then start fab of spectrometer horns
- Packaging process
  - EM BDA to be packaged and tested with EM hardware
  - Process review to take place prior to CQM build

Implementation Plan

JFET Assemblies

- Complete and test EM JFET membranes for performance
- Begin fabrication of STM and CQM hardware
- Qualify assembly processes on EM modules and EM membranes

Implementation Plan

RF Filters

- Await tests on the EM JFET modules prior to fabrication

Implementation Plan

Cables

- Harness definition document is nearly complete
- Routing design of cables has not started at MSSL
- Fabricate and qualify cables at manufacturer prior to drop shipment to RAL – Delivery could be negotiated if there are budget or schedule problems

Testing Program

- Design of test facilities is completed
- Definition of test program completed
  - Qual Plan signed off
  - Test Plan nearly complete
  - Test procedures to be written
- Test Readiness Review scheduled prior to CQM testing

13.0
RFA Summary

Jamie Bock

Responses to 2000 Peer Review

Programmatic and technical comments from last year's review were presented and responded to at the Confirmation Readiness Review (7/2000) as follows

We collected 36 technical RFAs from the review panel

25 Accepted
11 were taken on an Advisory basis
0 Rejected

We continue to value your input

Programmatic Replies to Peer Review

1. Documentation of requirements, interfaces, deliverables.

Action: Completion of business agreement.

2. Bound scope of technology development.

Action: Current performance levels are adopted as specifications; design values incorporate margin.

3. Better define testing interfaces with European partners.

Action: a. JPL delivers directly to RAL, 3 months later. QMW personnel participate in detector testing at JPL.

b. JPL verifies performance of CEA warm electronics.

4. Better define interface of JFET modules.

Action: JFET enclosure fabricated in Europe, resulting in simple ICD.

5. Tailor schedule and deliverables to match budget profile.

Action: CQM deliverables limited to 2 array assemblies.

6. Workforce limitations.

Action: Increasing workforce, first at MDL.

SPIRE REVIEW BOARD RFAs (1)

#	Description	Disp.	Response
1	Develop understanding of Kevlar stress as a function of temperature and creep as a function of time. (HM)	Accept	Unit was designed based on published contraction and creep data.
2	Negotiate reduction in deliverables from 15 units to 10. (GS)	Accept	Baseline is 2 CQM BDA units, 5 PFM units and 3 new FSM units, refurbished from CQM units.
3	Increase 500 g mass allocation for Bolometer Assemblies to ~600g with mass margin. (GS)	Accept	Done.
4	Assess number of total JFET modules available vs. cost, mitigated against risk of possible failures during integration. (GS)	Accept	Baseline is FSM JFET units are the CQM JFET units.
5	Get hard numbers for limits on required max heat loads at all stages; try to increase power budget for the arrays from 10 microwatts to 20 microwatts. (MD)	Advisory	Impact of additional heat load raises operating temp. Dissipation spec defined as 15 uW pending systems study.

SPIRE REVIEW BOARD RFAs (2)

#	Description	Disp.	Response
6	Is there a well understood definition of time constant? What about the 2-T model applied to spiders? Which definition holds? (MD)	Accept.	Time constant is defined as drop in optical response by 0.7.
7	Is there a spec on the Beam Asymetry and the Width Scatter across the plane? Get these into the agreements. (MD)	Advisory.	Specification on feedhorn beams (BDA-FUN-10, 11 single-mode/multi mode). This is a specification on optics.
8	Get a better definition of final requirements for FPA motion and internal resonances. (MD)	Accept.	Done. Requirement reflected in BDA-TEC-04, BDA-FUN-04
9	Define responsibilities for light leaks into the focal plane. (PR)	Accept.	MSSL is responsible for baffling of 2-K and 4-K boxes.
10	Develop a spec on the RF attenuation of the 2K heat strap penetration.	Accept	Spec to be less than BDA-STR-03.

SPIRE REVIEW BOARD RFAs (3)

#	Description	Disp.	Response
11	Improve the feedhorn efficiency testing by making a cryogenic black body the same diameter as the Lyot Stop. (PR)	Advisory.	We measure total efficiency and beam patterns.
12	Consider use of weak spring in place of PTFE and multiple turns on pulleys in place of glue. (PR)	Advisory.	Determine need based on test of EM unit, but can be accommodated.
13	Investigate the issues of heat dissipation in Kevlar during shake, temperature stability of Kevlar and the issue of fatigue. Utilize quantitative measurements of resonance damping. (PR)	Advisory.	Address kevlar fatigue via vibration tests on prototype unit. Unit has already survived preliminary vibration test.
14	Investigate the issue of focal plane shift during shake; first with full tension, then with reduced tension strands. (PR)	Accept.	Will implement.
15	Design for minimum number of interfaces to reduce effects of uncertainty in boundary resistance. Consider use of distributed one dimensional heat flow single pole filter of a suitable magnetic alloy as used on Benoit refrigerator. (PR)	Accept.	Will reduce number of interfaces. Investigating passive filtering. Will measure temperature gradients in array assembly.

SPIRE REVIEW BOARD RFAs (4)

#	Description	Disp.	Response
16	Establish a more structured approach and document the deliverables (in addition to the hardware) between organizations. (SK)	Accept.	Defined in business agreement.
17	Document the contamination requirements and investigate the suitability of thermal grease for their application. (SK)	Accept.	Any application of grease must be consistent with contamination specifications.
18	Investigate an applicable specification (similar to MIL-461) for EMC/EMI requirements and discuss with SPIRE Instrument Scientist (SK) Make part of BA. (GR)	Accept.	Specifications are listed in sub-systems specification document. Levels are still TBD.
19	Establish and document the qualification plan to address all aspects of performance, test, radiation, manufacturing, process, etc. (SK)	Accept.	All test and assembly procedures will be written and documented prior to CQM testing.
20	Investigate the effects of radiation on the JFETs and document the results to meet environmental requirements. Utilize resident expertise at JPL for radiation effects.	Accept.	We concur.

SPIRE REVIEW BOARD RFAs (5)

#	Description	Disp.	Response
21	Develop a complete qualification plan to verify mission life and radiation performance. (SK)	Accept.	We concur.
22	Consider doing away with corrugations due to their limited efficiency improvement. Determine if multi-mode smooth bands are adequate using HFSS and a larger entrance hole. (GR)	Accept.	We concur.
23	Use electronic parts acceptable for flight to ESA/CEA. Prepare a list of critical parts and negotiate selections. (GR)	Accept.	Readout prototype developed at CIT will use ESA qualifiable parts.
24	Define the whole train and quantify how the alignment of optics contributes to offsets. (GR)	Advisory.	Optical tolerance budget defined in optics SSSD (document #) and optical alignment plan (document #).
25	Conduct a literature search of thermal conductivity of greases and joints. Look at Kittel paper. (MD)	Advisory.	Design needs to minimize effects of interfaces.

SPIRE REVIEW BOARD RFAs (6)

#	Description	Disp.	Response
26	Use Cobalt 60 source to simulate cosmic ray hits and to calibrate time constant of detectors instead of taking photometer to an accelerator. (MD)	Advisory.	We take this under advisement.
27	Investigate the use of stacked washers for the corrugated feeds. Look at Dragone's work at Bell Labs and Paul Goldsmith's book. (MD)	Advisory.	We take this under advisement.
28	Simulate, with HFSS, the use of a choke at the bolometer/horn interface to stop leakage out the sides of the cavity. (MD)	Advisory.	We take this under advisement.
29	Determine if the 25 micron alignment requirement can be reduced, given the pixel size. (RR)	Accept.	Specification reduced to 125 um.
30	Run a launch vibration test with before and after alignment measurements. (RR)	Accept.	We concur. In process.

SPIRE REVIEW BOARD RFAs (7)

#	Description	Disp.	Response
31	Carefully analyze the tension cord design for slipping past the rollers, its damping, heating and alignment performance. (RR)	Accept.	We agree and are conducting vibration tests on prototype.
32	Try to converge quickly on the development of all key requirements needed for important decisions. (RR)	Accept.	Developed in business agreement and sub-system specification.
33	Test Kevlar straps early and often at LN and room temperature. Test to destruction to determine margins. Develop cheap metrology for tests. (PR)	Accept.	We agree and are conducting vibration tests on prototype.
34	Corrugated horns, although enthusiastically endorsed in the UK, are high risk, higher cost, and more difficult to inspect than smooth horns. They are unlikely to approach theoretical performance as closely as smooth horns. Consider their use only where there is a substantial >10% theoretical advantage. (PR)	Accept.	We concur.
35	Establish a spec on the fridge. Determine what your (Delta T)/T temperature attenuation requirement will be. Is the thermal shunt better?	Accept.	Specification on fridge in BDA-HCO 01, 02, and 03. Investigating passive solutions.

SPIRE REVIEW BOARD RFAs (8)

#	Description	Disp.	Response
36	Fabricate test blocks of horns with both corrugated and smooth feeds to save time. (MD)	Advisory.	Prototyping of horns will be completed before CQM delivery.
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14.0
Summary/Objectives

Gerald Lilienthal

Charter

- Evaluate the readiness of the SPIRE Detector Subsystem to proceed into CQM fabrication, assembly and test
  - Previous concerns and deficiencies considered and resolved
  - Requirements flowdown from instrument
    - Requirements traceability and compliance matrix
    - Documentation of requirements and interfaces
  - Detailed design is adequate stable and well documented
    - Detailed design responds to requirements
    - Tradeoffs understood
    - Demonstration of technology
    - Configuration control
    - Implementation documentation is adequate (AIDS, Process Sheets, Travellers)
    - Manufacturing process design
    - GSE design and certification of test equipment
    - Integration and test plans
    - Reliability analysis and qualification plans
    - Delivery, handling and shipping plans
  - Product assurance plans are adequate
  - Risks understood and plans exist for managing them

Success Criteria

- Designs and processes meet requirements and are sufficiently defined and documented to proceed with development within the risk policy of the project
- Plans for resolving remaining problems are consistent with available resources and risk policy
- Test approach and test product status is thorough and acceptable with verifying compliance with the requirements
- Technology has been demonstrated by test and correlated to the analyses

Recommendations

- All interfaces should be frozen by September, 2001 (ICD's should be signed off)
- Vibration levels for the BDAs should be set to the BDA capability or the instrument must accept the risk
- Comment on the benefit of coordination between IPAC and the SPIRE instrument team
- Comment on potential descopes to our program if they are necessary