SPIRE (SAp) Monthly Report – August 2001 Date: 30/8/01

Work Package: **DRCU** SPIRE-SAP-REP-000859 1. Subsystem Progress Since Project Inception Documentation Management Plan. Available. PA Plan Available. DRCU Dev. Plan Available. **DRCU** Specification Available. DPU/DRCU ICD Available. DRCU/FPU ICD Available. **DCU** QM1 Board Design completed, fabrication process started. **SCU** Draft Specification and preliminary design available. Draft DPU/SCU ICD issued. Draft QM1 schedule issued (shows negative margin) PSU Standard Power Supply will be used for QM1. Works on final specification Call for tender process started (Call for Application completed) Preliminary design available, has to be reworked due to the new PSU I/F. DRCU Box Specification available. **FPU Simulator** Preliminary development started. 2. Subsystem Progress This Month F.Pinsard on mission at JPL from 23/7 to 2/8 attended the BDA CDR. DCU Design completed, Board layout (SAp) almost completed, QM1 Part procurement (JPL) started. - LIA board: Cutt off freq. of the BFP modified, Broader supply track required. – BIAS: OK. – DAQ+IF: New distribution for ADC and Offset agreed, investigation on possible use of the FPGA dowload I/F. SCU Not a lot due to vacation period. **PSU** Progress on Specification writing.

Equipment end parts procurement started.			
3. Problem Areas	Remedial Actions		
FMECA outcome impact	A priori not much on the boards but modification on LIA		
	board channel distribution could have to be done (mainly		
	impact on LIA harness distribution)		
Concerns about actual JPL efforts put on DCU	Actually nothing to become alarmed but a note will be issued		
EM/QM1 development.	by SAp to specify/clarify the various issues.		
SCU QM1 negative margin (1.5 month)	The overall development schedule will be reworked.		
Project Control resource missing	Bids received, Selection ongoing		
A Fusingsuing Activities			

# 4. Engineering Activities

**DRCU Box** 

**FPU Simulator** 

### 5. Design Changes

➤ No major design change expected but LIA harness distribution should have to be modified (system issue)

#### 6. PA/QA Activities

> FMECA preliminary result.

# 7. Subsystem Management Issues

- Missing resource: Still no Project Controller on board.
- > DCU QM1 development schedule slip but there is still margins.

None

Breadboard design started.

SCU QM1 development

# 8. Actions Requiring Immediate Attention

> see Problem Areas section.

## 9. Status of Previous Actions

#### 10. Activities Yet to be Achieved

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11. Milestones		Status
xx/xx/01	DCU + PSU DDR	Date not yet frozen
17/09/01	DCU EM/QM1 fabricated at JPL	To be postponed
30/11/01	DCU EM/QM1 tested at JPL	To be postponed
03/12/01	DCU EM/QM1 delivered to SAp by JPL	To be postponed
03/12/01	Bolometer Test Facility delivery to SAp by JPL	To be postponed
01/12/02	DRCU & WIH QM1 delivery to RAL	On schedule
01/12/02	FPU Simulator delivery to RAL	On schedule
01/06/03	DRCU QM2 delivery to RAL	On schedule
02/07/03	WE CDR	On schedule
16/03/04	DRCU & WIH FM delivery to RAL	On schedule
10/01/05	DRCU & WIH FS (spare boards) del. to RAL	On schedule
13. Schedule Changes		
None		