DRCU Operation - MCU & SCU

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DCU operations (1)

- Before operation (bolometer data acquisition and data frame transfer to the DPU via the High Speed Interface) DPU have to initialize DCU H/W: after a power on all the registers are reseted.
- **List of parameters to be loaded:**
  - **Photometer BIAS module configuration**
    - Sine bias generator frequency divider [64;511]
      - *Set_photo_bias_freq{div}*
    - Demodulation phase for P250 bolometers,
    - Demodulation phase for P350 bolometers,
    - Demodulation phase for P500 bolometers,
    - Demodulation *phase for T/C (temperature control) bolometers,*
      - *Set_photo_demod_ph{channel id,phase}*

DCU operations (2)

- *Bias generator mode (Run/Stop/Test values)*
  - *Set_photo_bias_mode{mode}*
- *Sine Output Amplitude attenuation for P250 bolometers,*
- *Sine Output Amplitude attenuation for P350 bolometers,*
- *Sine Output Amplitude Attenuation for P500 bolometers,*
- *Sine Output Amplitude Attenuation for T/C bolometers,*
  - *Set_photo_bias_ampl{channel id,att}*
- *JFET source biasing Vss1 to Vss6 for P250 bolometers,*
- *JFET source biasing Vss1 to Vss4 for P350 bolometers,*
- *JFET source biasing Vss1 to Vss2 for P500 bolometers,*
  - *Set_photo_JFET_Vss{channel id,voltage}*
- *JFET heater current*
  - *Set_photo_heater_pwr{current}*

DCU operations (3)

- ***Corresponding configuration sequence:***

  - *Set_photo_bias_mode{Stop}*
  - *Set_photo_bias_freq{photo_divider}*
  - *Set_photo_bias_ampl{0,ampl_p250}*
  - *…*
  - *Set_photo_bias_ampl{3,ampl_pT/C}*
  - *Set_photo_demod_ph{0,phase_p250}*
  - *…*
  - *Set_photo_demod_ph{3,phase_T/C}*
  - *Set_photo_JFET_Vss{0,vss}*
  - *…*
  - *Set_photo_JFET_Vss{11,vss}*
  - *Set_photo_bias_mode{Run}*

DCU operations (4)

- ***Remarks:***

  - Photometer Bias configuration sequence corresponds to **23** successive low level commands;
  - Set_heater_current is not in the sequence (info from JPL).
  - Set_photo_bias_mode{test_value} is implemented for on ground testing only.

DCU operations (5)

- **Photometer DAQ_I/F module configuration**

  - Sampling frequency divider (derived from BIAS frequency)
  - Number of frame to be transferred to DPU (0 to 16 or continuous)
    - *Set_photo_frame_mode{div,frame_number}*
  - Offset setting and acquisition mode (do nothing, automatic settings, acquisition, acquisition test)
    - *Set_photo_offset{mode}*
  - Frame type setting(Array Subset, Full Array, Test Pattern, Offset table)
    - *Set_photo_data_mode{mode,subset_id}*

DCU operations (6)

– ***Corresponding configuration sequence:***

- Set_photo_offset{automatic}
  - Comment DCU computes offset table
- Set_photo_offset{acquisition test}
- Set_photo_data_mode{offset}
- Set_photo_frame_mode{samp_div,1}
  - Comment: DCU send a data frame containing previously computed offset table
  - Data transfer stops after 1 frame
- Set_photo_offset{acquisition}
- Set_photo_data_mode{mode} (i.e.: mode = full array)
- Set_photo_frame_mode{samp_div,frame number}

DCU operations (6)

- ***Remarks:***

  - Photometer DAQ_I/F configuration sequence corresponds to **7** successive low level commands.
  - Photometer complete configuration sequence corresponds to 30 successive low level commands.

DCU operations (7)

- **Spectrometer BIAS module configuration**

  - Sine bias generator frequency divider [64;511]
    - *Set_spectro_bias_freq{div}*
  - Demodulation phase for SSW bolometers,
  - Demodulation phase for SLW bolometers,
    - *Set_spectro_demod_ph{channel id,phase}*
  - *Bias generator mode (Run/Stop/Test values)*
    - *Set_spectro_bias_mode{mode}*
  - *Sine Output Amplitude attenuation for SSW bolometers,*
  - *Sine Output Amplitude attenuation for SLW bolometers,*
    - *Set_spectro_bias_ampl{channel id,att}*

DCU operations (8)

- **Spectrometer BIAS module configuration**
  - *JFET source biasing Vss1 to Vss2 for SSW bolometers,*
  - *JFET source biasing Vss1 for LSW bolometers,*
    - *Set_spectro_JFET_Vss{channel id,voltage}*
  - *JFET heater current*
    - *Set_spectro_heater_pwr{current}*

DCU operations (9)

- **Spectrometer DAQ_I/F module configuration**

  - Sampling frequency divider (derived from BIAS frequency)
  - Number of frame to be transferred to DPU (0 to 16 or continuous)
    - *Set_spectro_frame_mode{div,frame_number}*
  - Offset setting and acquisition mode (do nothing, automatic settings, acquisition, acquisition test)
    - *Set_spectro_offset{mode}*
  - Frame type setting(Array Subset, Full Array, Test Pattern, Offset table)
    - *Set_spectro_data_mode{mode,subset_id}*

DCU operations (9)

- ***Corresponding configuration sequences:***

  - *Set_photo_bias_mode{Stop}*
  - *See photometer configuration BIAS & DAQ_I/F sequences*
  - *…*

- ***Remarks:***

  - Spectrometer DAQ_I/F configuration sequence corresponds to **17** successive low level commands.

DCU operations (10)

- ***Others commands …***
  - *All the Set_… commands have a corresponding Get_… commands (to re-read registers)*
  - *Get_hk_channel is a read only command for WE housekeeping acquisition*
  - *Reset_time_counter is a broadcast write only command for sub-system synchronization*

SCU operations (1)

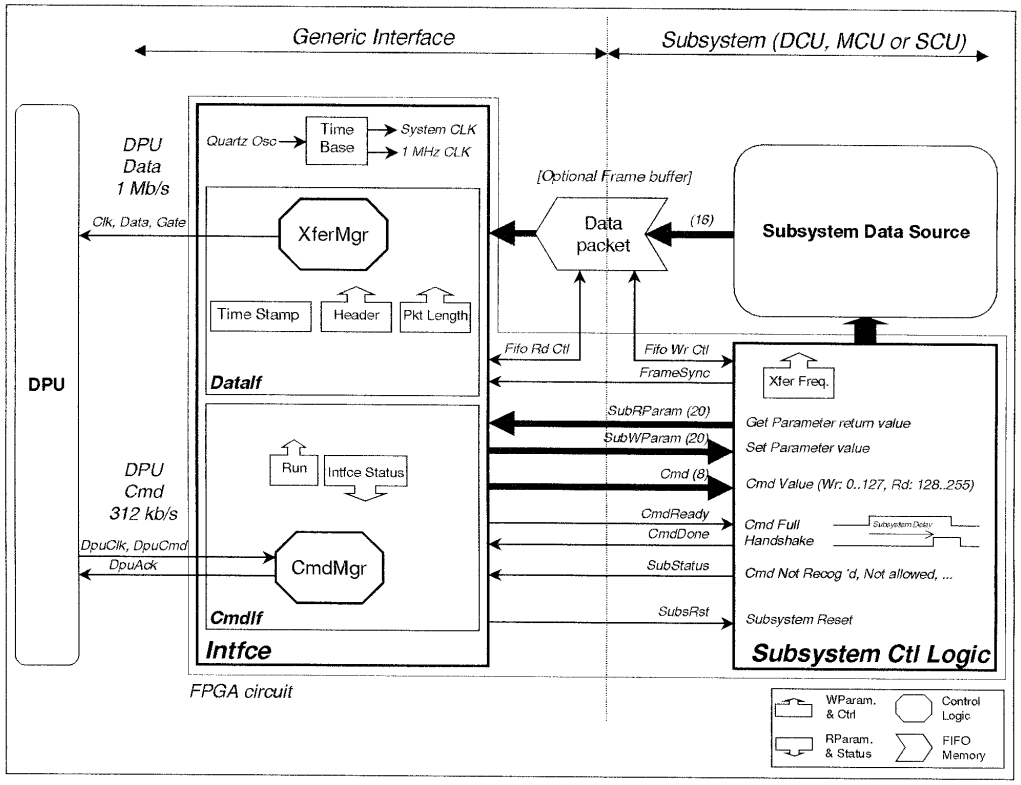
- Before operation DPU have to initialize SCU H/W: after a power on all the registers are reseted.
- **List of parameters to be loaded:**
  - **TEMP module configuration**
    - Thermometer switching on/off
      - *Set_therm_on/off{on/off vector}*
  - **CAL_COOL_HK module configuration**
    - Calibrator current
      - *Set_calibrator_current{channel id, current value}*
    - Heater current
      - *Set_heater_current{channel id, current value}*

SCU operations (2)

- **DISTRIB module configuration**
  - Sub-system switching on/off
    - *Set_S/S_on/off{on/off vector}*
- **DAQ_I/F module configuration**
  - Sampling frequency divider
  - Number of frame to be transferred to DPU (0 to 16 or continuous)
    - *Set_SCU_frame_mode{div,frame_number}*
  - Frame type setting(Normal, Test Pattern)
    - *Set_SCU_data_mode{mode}*

DPU I/F
General considerations (1)

– *DPU I/F block diagram:*



DPU I/F
General considerations (2)

- *Design is implemented into a FPGA along with the subsystem control logic.*
- *VHDL code will be distributed to DCU, MCU & SCU design teams.*
- *Optionally support for a FIFO data buffer between the interface logic & the subsystem data source.*
- *Data transfer rate is controlled by the subsystem logic ("FrameSync" signal).*