FIRST/SPIRE

Comparative assessment of different architectures for warm electronics

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	Function	Name	Date	Visa
Prepared by	Product Assurance	F.LOUBERE		
Prepared by				
Verified by				
Approved by				

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1. Purpose of the study

The aim of the study is to :

- get an assessment on the reliability of the warm electronic of SPIRE instrument, in order to achieve the architecture with the best reliability/complexity compromise solution,
- Evaluate the opportunity to cross strap or not DRCU and DPU.

1.1. Context and limitations of the study

For the moment, no allocations of reliability and availability have been given to the warm electronic from for the whole instrument. Therefore, the study is limited to the comparison of different options on the architecture.

The DPU is common with 2 others instruments. It is defined to be full hard redundant. As no details on the internal architecture are available, study will be limited to the interface with the DRCU

Some reliability simulations are performed on analogic chains, only on CEA detectors option.

This document shows the first trend of the results. Additional simulations and detailed studies will be performed later, based upon :

- Additional information changing hypothesis of the present simulations,
- Results of detectors selection and associated electronic,
- Progress of design and knowledge about different items.

1.2. Hypothesis

The study has been performed on the following hypothesis :

- Length of mission = 5 years
- Calibrations sources and Beam Steering Mirror failure modes are not taken into account (no information available for the moment)
- Reliability of telescope considered = 1 during the whole mission (supposing it's mechanical item)
- Reliability of the cooler = 1 during the whole mission (no information available. A failure of the cooler leads to lose the mission)
- Photometer and spectrometer do not operate simultaneously. Mission is considered successful whether the photometer or the spectrometer is operating : simulations are performed separately on the photometer, then on the spectrometer, considering that each operates 100% of the time during the 5 years mission.

2. Reliability assessments

2.1. Method

1. Building reliability bloc diagrams of the different functional modules of the system,
2. Reliability assessment of each functional bloc (empirical from the estimated reliability value of the parts implementing the function),
3. Simulation of different architecture possible, by using a serial/parallel model (all simulations performed with tool Supercab).

2.2. Simulations performed

The system has been divided into 3 parts, for witch different possibilities of architecture have been evaluated :

- Digital processing chain
  - DRCU digital part
    - Cold redundancy,
    - Partial cross strapping
    - Full cross strapping
  - DPU
    Simulations on the DRCU/DPU interface
    - Cold redundancy between DRCU and DPU,
    - Cross strapping between DRCU and DPU
- Detectors and analogic chain

2.3. Functional blocs reliability assessment

Module	fit
Detectors and analogic chain	
Detectors + BAU	120/line
ASP	140
Detectors power supply	50
Digital processing chain	
Photometer array controller analogic part (switch) (= Ph C A	100
Photometer array controller digital part (FPGA + RAM) (= Ph C B)	300
Spectrometer array controller analogic part(switch) (= SP C A)	100
Spectrometer array controller digital part (FPGA + RAM) (= Sp C B)	300
BSM controller	500
FTS controller	500
Cooler controller	500
DRCU Ctrl	1000
DRCU DC/DC	500
DRCU I/F	300
DPU	1000

3. Results summary

The following tables indicate the reliability assessments regarding different configurations. All the details can be found in annex.

Reliability of DRCU

Internal configuration of DRCU	Reliability Spectrometer chain	Reliability Photometer chain
Cold redundancy	0,983	0,989
Partial cross strapping	0,987	0,992
Full cross strapping	0,989	0,994

Reliability of DRCU and DPU

Configuration DRCU/DPU	Reliability Spectrometer chain	Reliability Photometer chain
Cold redundancy DRCU/DPU	0,977	0,982
Cross strapping DRCU / DPU *	0,977	0,983

*A single point failure comes out with cross strapped configuration

Reliability of detectors and analogic chain

Analogic chain	Reliability Spectrometer chain	Reliability Photometer chain
lost 4 rows no converter no array	0,971	0,784
lost 4 rows OR 1 converter AND 1 array	0,991	0,824
lost 4 rows OR 1 converter OR 1 array	0,995	0,832

4. Conclusions

The digital part of DRCU and DPU is intrinsically reliable, whatever the redundancies are. (cold or cross strapped).
Cross strapping between DRCU and DPU does not improve significantly reliability, but introduces a single point failure. Therefore, that cross strapped architecture must not be chosen.

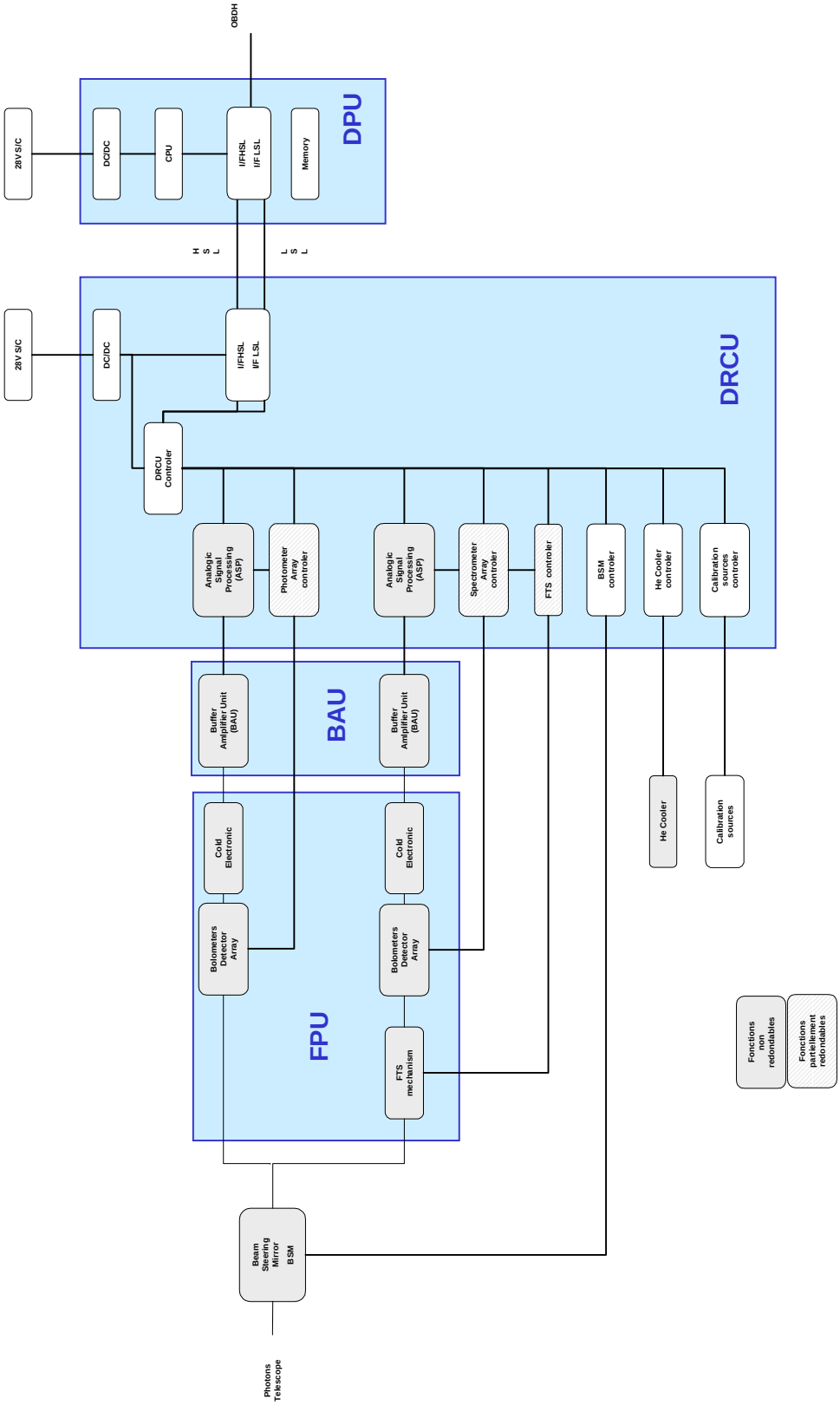
Internal cross strapping of DRCU does not seem to be interesting in a first approach. If this configuration is considered, more detailed investigation should be performed, taking into account effects of commutation on reliability.

Simulation results on detection and analogic chain are not significant, due to lack of information about what can be considered as a success for the mission. The hypothesis taken might not be very realistic from that point of view.
Nevertheless, a conclusion can be made :

- The reliability of the whole chain is fully dependant on the reliability of the analogic chain of the photometer,
- Precision must be obtained on mission profile in order to perform additional estimations :
  - ⇨ Share of operating time between photo and spectrometer,
  - ⇨ Success of mission ; how many rows is it acceptable to loose,
  - ⇨ ...

Annexe 1. Inputs

Annexe 1.1. General synopsis



General description of each functional module and their implementation (as seen for the moment)

Annexe 1.2. Focal Plane Unit (FPU)

Annexe 1.2.1. Detectors

2 bolometers arrays for the spectrometer
16 bolometers arrays for the photometer

1 row of matrix = 1sampling line (corresponding to 16 pixels)

Annexe 1.2.2. Cold electronic

Operates at à 2K – analogic signals amplification and multiplexing

Annexe 1.3. Buffer Amplifier Unit (BAU)

For each line, amplification is implemented by :

- 2 operational amp.
- 5 R
- 16 solders

Annexe 1.4. DRCU

Annexe 1.4.1. DRCU controller

Function of control and command of DRCU. Data acquisition

DRCU controller will be implemented with SPARC ERC 32 board

Annexe 1.4.2. DC/DC

Parts not yet defined

Annexe 1.4.3. I/F

- 1 FPGA
- 3 drivers (for HSL)
- 1 driver and 1 receiver (for LSL)

Annexe 1.4.4. Analogic signal processing (ASP)

256 + 32 =288 lines to be converted
for each line :

- 4 operational amp.
- 10 R and C
- 1 converter for 8 lines

Annexe 1.4.5. Photometer array controller (PhC)

Function of control and drive of the detectors. Analogic part (detectors side) non redundant, digital part (DRCU controller side) redundant

- 1 FPGA
- 1 memory
- 9 analogic switch

Annexe 1.4.6. Spectrometer array controller (Sp C)

Function of control and drive of the detectors. Analogic part (detectors side) non redundant, digital part (DRCU controller side) redundant

- 1 FPGA
- 1 memory
- 9 analogic switch

Annexe 1.4.7. FTS controller (FTS C)

Function of control command of the mechanism.
Redundancy scheme in the mechanism not available for the moment : 1 or 2 input lines from FTS mechanism ?
We suppose the implementation of function inside DRCU will require

- 1 FPGA
- 1 memory
- control command electronic (to be detailed)

Annexe 1.4.8. BSM controller (BSM C)

Function of control command of the mechanism.
We suppose the mechanism has a nominal and a redundant line as inputs on the BSM controller.
We suppose the implementation of function inside DRCU will require

- 1 FPGA
- 1 memory
- control command electronic (to be detailed)

Annexe 1.4.9. Calibration source controller

Function of polarisation for 2 sources, one for the spectrometer and one for the photometer.

Function will be implemented by :

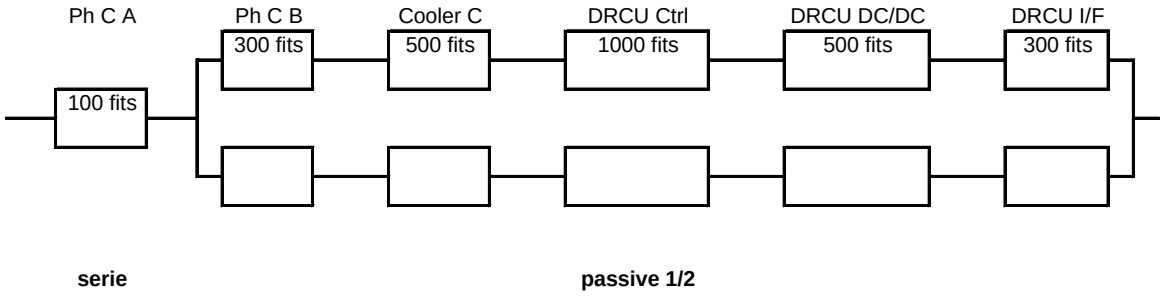
- 1 A/D C
- 1 operational amp.
- R

Annexe 1.4.10. Cooler controller

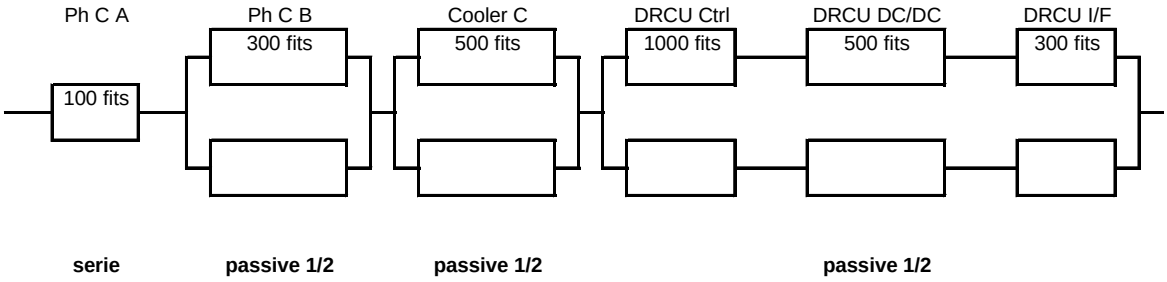
Function of control command of the mechanism, to be detailed.

Annexe 2. Photometer - Reliability assessment DRCU digital part

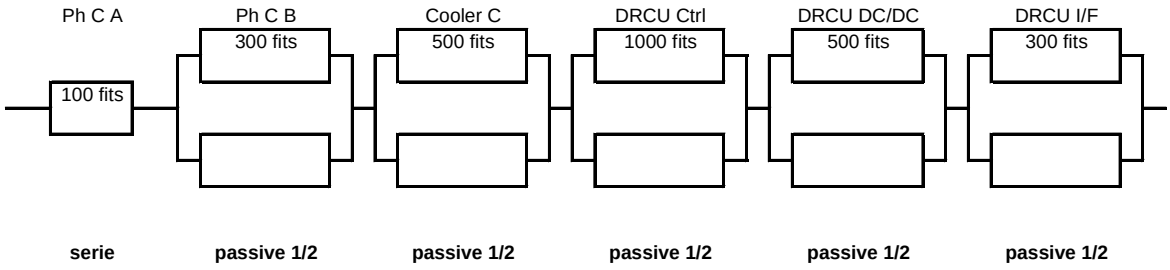
Annexe 2.1. Cold redundancy



Annexe 2.2. Partial cross strapping



Annexe 2.3. Full cross strapping



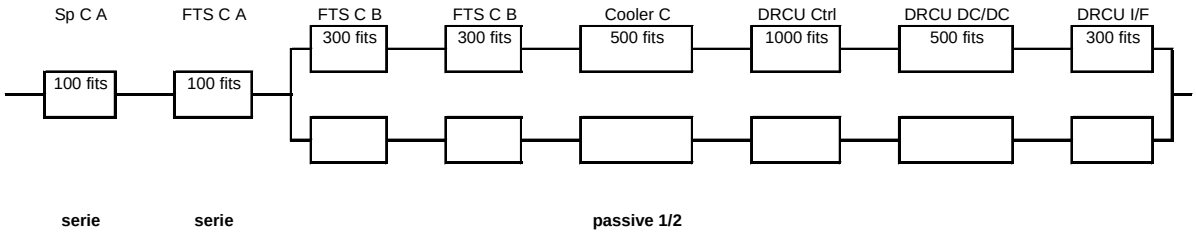
Annexe 2.4. Simulation results

Configuration	Reliability
Cold redundancy	0,989069
Partial cross strapping	0,992057
Full cross strapping	0,993907

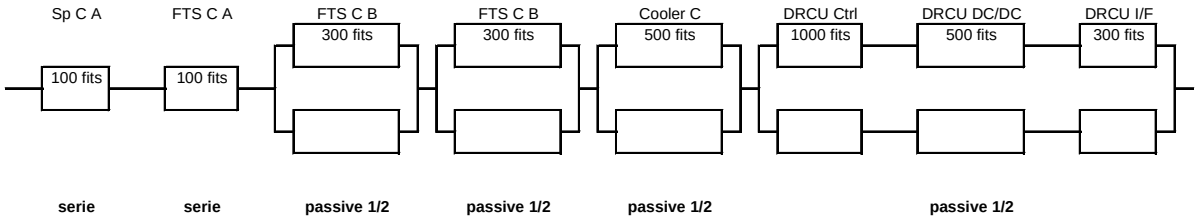
Cross strapping between DRCU and DPU does not improve significantly reliability.
This assessment does not include loss of reliability due to commutation system in cross strapped configuration.

Annexe 3. Spectrometer - Reliability assessment DRCU digital part

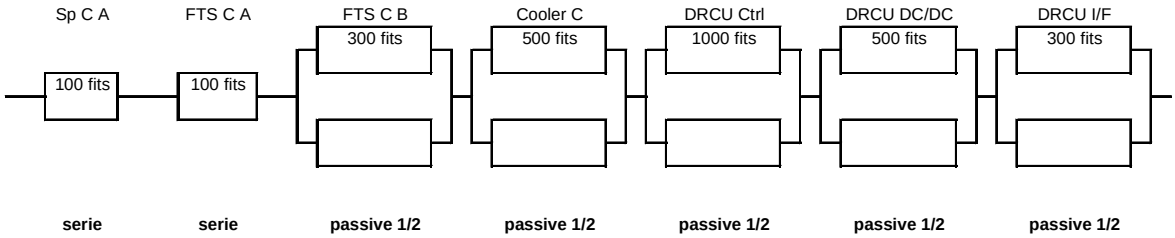
Annexe 3.1. Cold redundancy



Annexe 3.2. Partial cross strapping



Annexe 3.3. Full cross strapping



Annexe 3.4. Simulation results

Configuration	Reliability
Cold redundancy	0,983226
Partial cross strapping	0,987628
Full cross strapping	0,989470

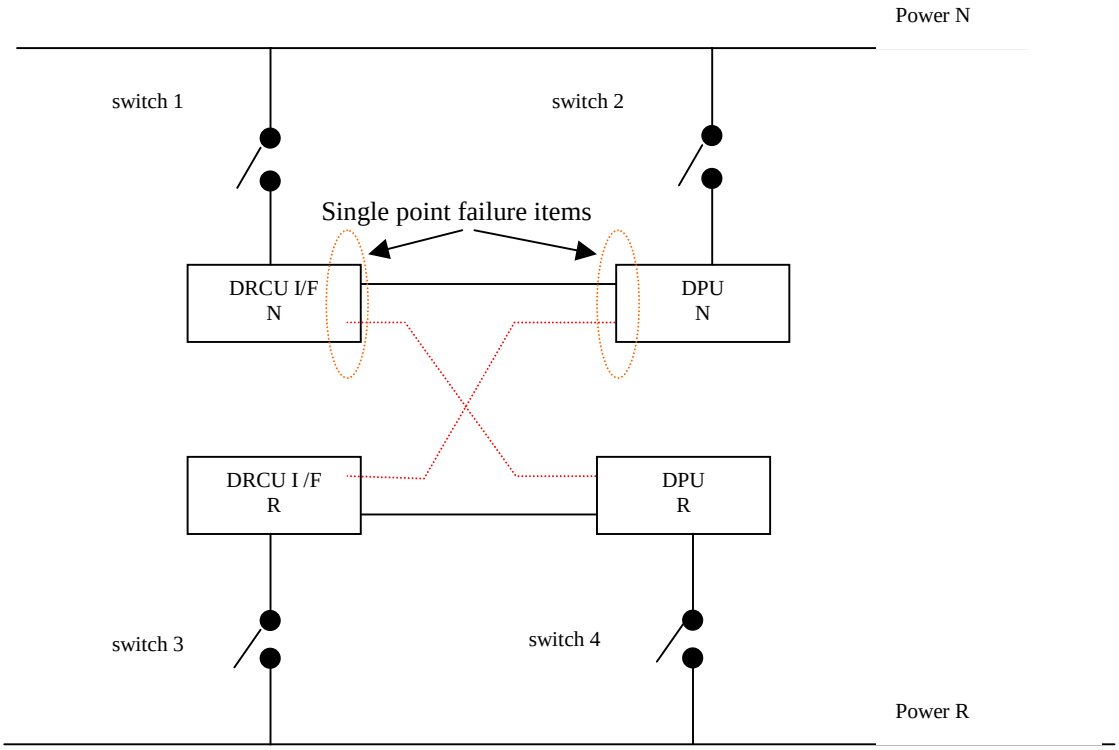
Cross strapping between DRCU and DPU does not improve significantly reliability.
This assessment does not include loss of reliability due to commutation system in cross strapped configuration.

Annexe 4. Reliability assessment DRCU digital part /DPU

Commutation from main to redundant is based in implemented by switches (estimated reliability 50 fit).

Annexe 4.1. Interface electric architecture hypothesis :

Simple (plain line)and cross strapped (doted line)



Annexe 4.2. Failure modes of cold redundancy architecture

Initial status : Switch 1 ON, Switch 2 ON, DRCU N ON, DPU N ON

Scenario 1 : failure on DRCU N
Switch on whole R chain : Switch 1 and 2 OFF and Switch 3 and 4 ON

Scenario 2 : failure on DPU N
Switch on whole R chain : Switch 1 and 2 OFF and Switch 3 and 4 ON

Failure propagation : in case of failure on DRCU I/F N (short circuit to GND) possible risk of propagation of failure to DPU N. In this case, **a whole functional chain is lost**.
The risk can be reduced by design means.

Annexe 4.3. Failure modes of cross strapped architecture

This architecture introduces additional parts and links.

M and R power supplies must be active simultaneously.

Initial status : Switch 1 ON, Switch 2 ON, DRCU N ON, DPU N ON

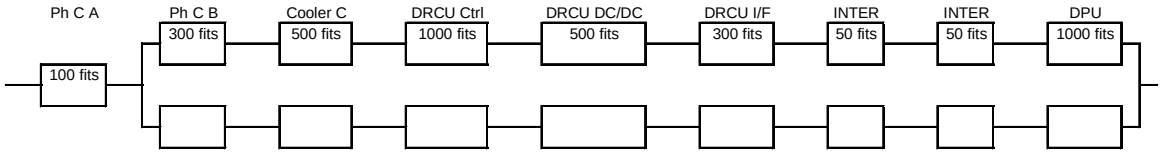
Scenario 2 : failure on DPU N
switch OFF 1, switch ON 3

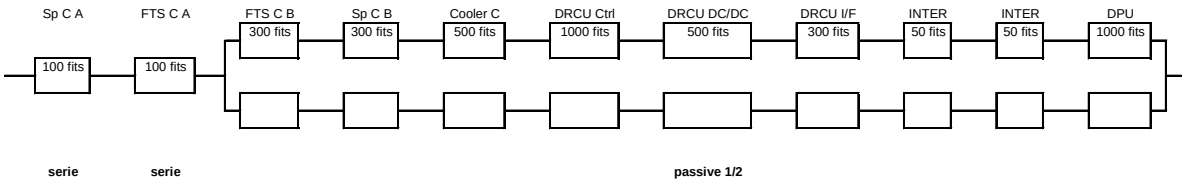
Scenario 2 : failure on DPU N
switch 2 OFF, switch ON 4

Single Point Failure : in case of failure on DRCU I/F N (short circuit to GND) possible risk of propagation of failure to DPU N and DPU R. In this case, there is a **risk to loose both chains**.
The risk can be reduced by design means.
Simulation includes a functional block : I/F PPU = 100 fit

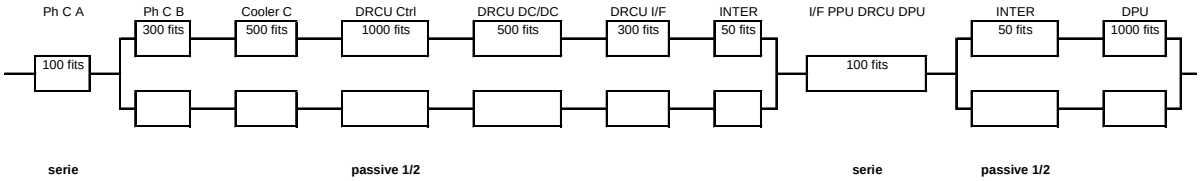
Annexe 4.4. Simulation results

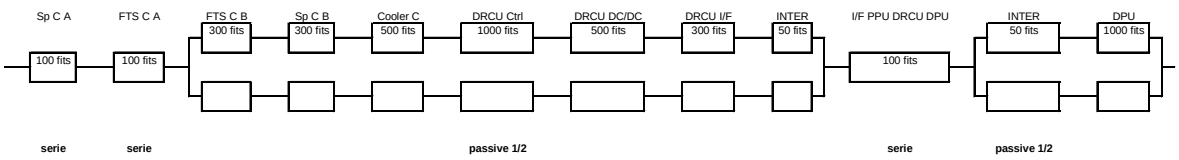
- Cold redundancy between DRCU and DPU





- Cross strapped architecture between DRCU and DPU





Configuration	Spectrometer	Photometer
Cold redundancy DRCU/DPU	0,976461	0,982780
DRCU internal cold redundancy, DRCU / DPU cross strapped	0,977560	0,983394

Annexe 4.5. Conclusion

Cross strapping between DRCU and DPU does not improve significantly reliability, but introduces a single point failure.

Annexe 5. Photometer : detection and analogic processing chain reliability

Annexe 5.1. Hypothesis

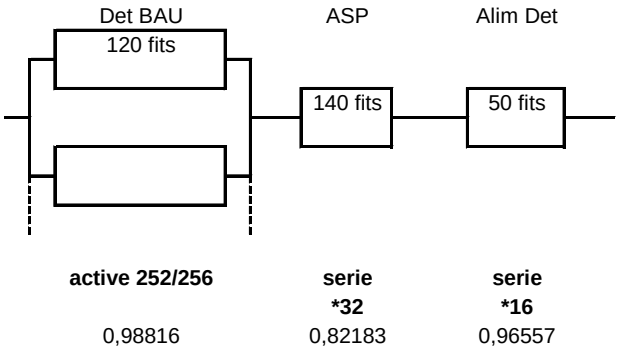
- Each array is 16 sampling lines ; one sampling line is 16 pixels
- 16 arrays : 16 x 16= 256 sampling line
- power supply of each line is independent
- 1 converter for 8 lines (= 32 converters for 256 lines), each converter dedicated to 8 consecutive lines

- Estimated failure rates :
- 1 sampling line = 120 fit
- 1 converter (and passives) = 140 fit
- 1 array = 50 fit (power supply failure)

Annexe 5.2. Simulation results

Simulations are performed regarding 'acceptable' losses during the mission. These simulations would be updated with additional information on accepted losses (when available)

1st simulation : allowed loss of : sampling lines – no converter – no array



Type	Det + BAU	ASP	Power supply	Total
loss of 0 sampling lines	0,260	0,821	0,965	0,206
loss of 1 sampling line	0,611	0,821	0,965	0,485
loss of 2 sampling lines	0,847	0,821	0,965	0,672
loss of 3 sampling lines	0,953	0,821	0,965	0,756
loss of 4 sampling lines	0,988	0,821	0,965	0,784

Comments :
- In the case of a few lines lost, reliability of the chain is dependant to the one of the detectors.
- In the case of a more numerous lost of lines, reliability of the chain is dependent to the one of the converter

2nd simulation : allowed loss of : sampling lines – one converter – no array

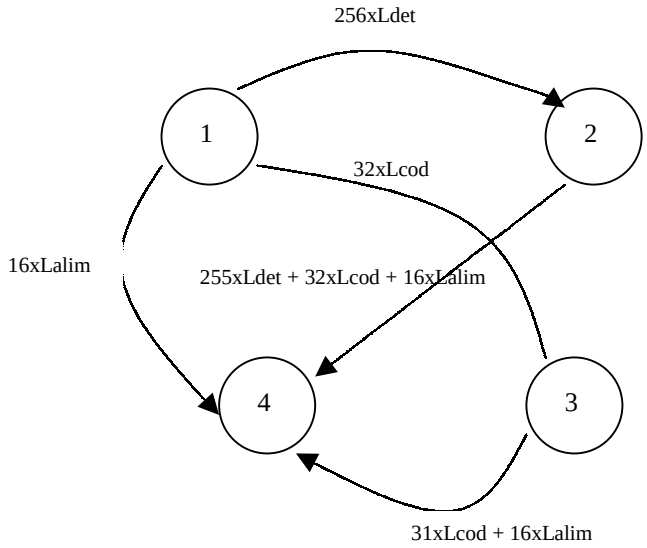
Description of different configurations by a Markov diagram

Case 1 : lost of 1 line OR 1 converter AND 0 array

System status :

1 System OK
2 lost of one line
3 lost of one converter (8 lines lost)
4 system lost

Status diagram :



Result :

	MAT :	1	2	3	4
Syst OK	1	-	256*Ldet	32*Lcod	16*Lalim
Perte d'une voie	2		-		255*Ldet+32*Lcod+16*Lalim
Perte 1 codeur	3			-	31*Lcod+16*Lalim
Perte Système	4				-
	INIT :	1	0	0	0
	ETATS :	1	1	1	0

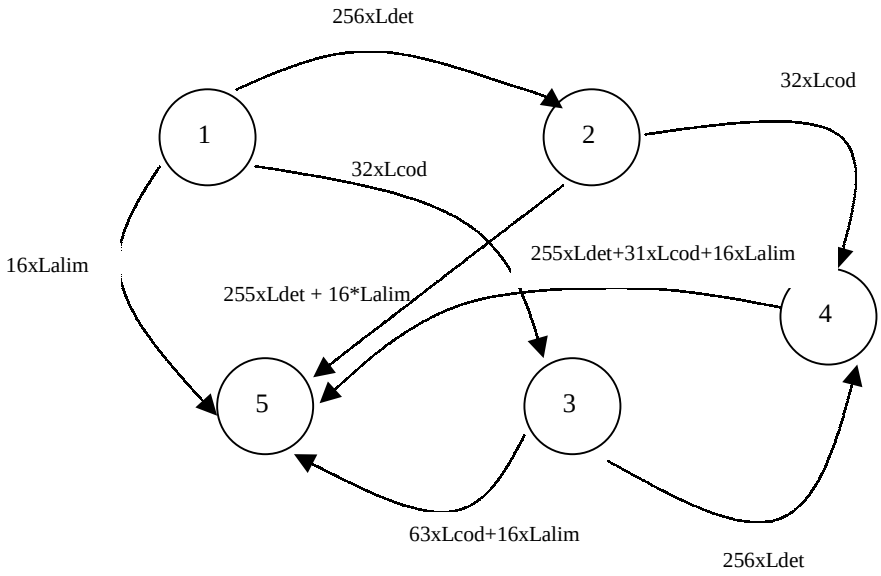
P(t=5years) = 0,571

Case 2 : lost of 1 line AND 1 converter AND 0 array

System status :

1 System OK
2 lost of one line
3 lost of one converter (8 lines lost)
4 lost of 1 line + 1 converter
5 system lost

Status diagram :



Results

	MAT :	1	2	3	4	5
Syst OK	1	-	256*Ldet	32*Lcod		16*Lalim
Perte d'une voie	2		-		32*Lcod	255*Ldet+16*Lalim
Perte 1 codeur	3			-	256*Ldet	31*Lcod+16*Lalim
Perte 1 voie + 1 codeur	4				-	255*Ldet+31*Lcod+16*Lalim
Perte Système	5					-
	INIT :	1	0	0	0	0
	ETATS :	1	1	1	1	0

P(t=5ans) = 0,580

Case 3 : lost of 2 lines OR 1 converter AND 0 array

System status :

1 System OK
2 lost of one line
3 lost of 2 lines
4 lost of one converter (8 lines lost)
5 system lost

Status diagram :

	MAT :	1	2	3	4	5
Syst OK	1	-	256*Ldet		32*Lcod	16*Lalim
Perte d'une voie	2		-	255*Ldet		32*Lcod+16*Lalim
Perte 2 voies	3			-		254*Ldet+32*Lcod+16*Lalim
Perte 1 codeur	4				-	256*Ldet+31*Lcod+16*Lalim
Perte Système	5					-
	INIT :	1	0	0	0	0
	ETATS :	1	1	1	1	0

P(t=5ans) = 0,713

Case 4 : lost of 3 lines OR 1 converter AND 0 array

P(t=5ans) = 0,796

Case 5 : lost of 4 lines OR 1 converter AND 0 array

	MAT :	1	2	3	4	5	6	7
Syst OK	1	-	256*Ldet				32*Lcod	16*Lalim
Perte d'une voie	2		-	255*Ldet				32*Lcod+16*Lalim
Perte 2 voies	3			-	254*Ldet			32*Lcod+16*Lalim
Perte 3 voies	4				-	253*Ldet		32*Lcod+16*Lalim
Perte 4 voies	5					-		252*Ldet+32*Lcod+16*Lalim
Perte 1 codeur	6						-	256*Ldet+31*Lcod+16*Lalim
Perte Système	7							-
	INIT :	1	0	0	0	0	0	0
	ETATS :	1	1	1	1	1	1	0

P(t=5ans) = 0,824

3rd simulation : allowed loss of : sampling lines – one converter – one array

loss of 4 lines OR one converter OR one array

	MAT :	1	2	3	4	5	6	7	8
Syst OK	1	-	256*Ldet				32*Lcod	16*Lalim	
Perte d'une voie	2		-	255*Ldet					32*Lcod+16*Lalim
Perte 2 voies	3			-	254*Ldet				32*Lcod+16*Lalim
Perte 3 voies	4				-	253*Ldet			32*Lcod+16*Lalim
Perte 4 voies	5					-			252*Ldet+32*Lcod+16*Lalim
Perte 1 codeur	6						-		256*Ldet+31*Lcod+16*Lalim
Perte 1 matrice	7							-	256*Ldet+32*Lcod+15*Lalim
Perte Système	8								-
	INIT :	1	0	0	0	0	0	0	0
	ETATS :	1	1	1	1	1	1	1	0

P(t=5ans) = 0,832

Annexe 5.3. Conclusions

Configuration	Reliability
lost : 4 lines – no converter – no array	0,784
lost : 4 lines OR 1 converter AND no array	0,824
lost : 4 lines OR 1 converter OR 1array	0,832

Depending on the definition of the degraded modes, reliability can reach a level comparable to the one of the digital chain.

Annexe 6. Spectrometer : detection and analogic processing chain reliability

Annexe 6.1. Hypothesis

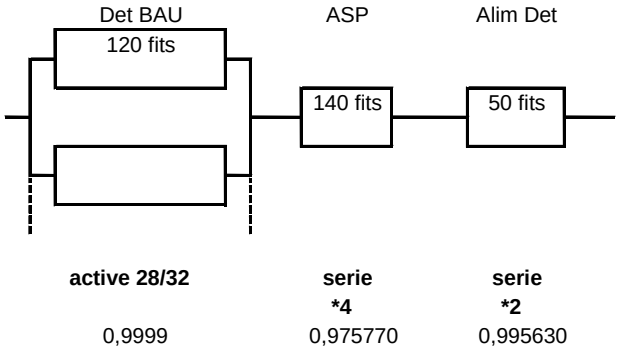
- Each array is 16 sampling lines ; one sampling line is 16 pixels
- 2 arrays : 2 x 16= 32 sampling line
- power supply of each line is independent
- 1 converter for 8 lines (= 4 converters for 32 lines), each converter dedicated to 8 consecutive lines

- Estimated failure rates :
- 1 sampling line = 120 fit
- 1 converter (and passives) = 140 fit
- 1 array = 50 fit (power supply failure)

Annexe 6.2. Simulation results

Simulations are performed regarding 'acceptable' losses during the mission. These simulations would be updated with additional information on accepted losses (when available)

1st simulation : allowed loss of : sampling lines – no converter – no array



Type	Det + BAU	ASP	Power supply	Total
loss of 0 sampling lines	0,8451915	0,97577037	0,99562958	0,821109
loss of 1 sampling line	0,9877202	0,97577037	0,99562958	0,959576
loss of 2 sampling lines	0,9993623	0,97577037	0,99562958	0,970886
loss of 3 sampling lines	0,9999759	0,97577037	0,99562958	0,971482
loss of 4 sampling lines	0,9999993	0,97577037	0,99562958	0,971505

2nd simulation : allowed loss of : sampling lines – one converter – no array

Description of different configurations by a Markov diagram

Case 1 : lost of 1 line OR 1 converter AND 0 array

System status :

1 System OK
2 lost of one line
3 lost of one converter (8 lines lost)
4 system lost

Status diagram :

	MAT :	1	2	3	4
Syst OK	1	-	32*Ldet	4*Lcod	2*Lalim
Perte d'une voie	2		-		31*Ldet+4*Lcod+2*Lalim
Perte 1 codeur	3			-	3*Lcod+2*Lalim
Perte Système	4				-
	INIT :	1	0	0	0
	ETATS :	1	1	1	0

P(t=5ans) = 0,9815

Case 2 : lost of 1 line AND 1 converter AND 0 array

System status :

1 System OK
2 lost of one line
5 lost of one converter (8 lines lost)
6 lost of 1 line + 1 converter
5 system lost

	MAT :	1	2	3	4	5
Syst OK	1	-	32*Ldet	4*Lcod		2*Lalim
Perte d'une voie	2		-		4*Lcod	31*Ldet+2*Lalim
Perte 1 codeur	3			-	32*Ldet	3*Lcod+2*Lalim
Perte 1 voie + 1 codeur	4				-	31*Ldet+3*Lcod+2*Lalim
Perte Système	5					-
	INIT :	1	0	0	0	0
	ETATS :	1	1	1	1	0

P(t=5ans) = 0,9831

Case 3 : lost of 2 lines OR 1 converter AND 0 array

System status :

1 System OK
4 lost of one line
5 lost of 2 lines
4 lost of one converter (8 lines lost)
5 system lost

	MAT :	1	2	3	4	5
Syst OK	1	-	32*Ldet		4*Lcod	2*Lalim
Perte d'une voie	2		-	31*Ldet		4*Lcod+2*Lalim
Perte 2 voies	3			-		30*Ldet+4*Lcod+2*Lalim
Perte 1 codeur	4				-	32*Ldet+3*Lcod+2*Lalim
Perte Système	5					-
	INIT :	1	0	0	0	0
	ETATS :	1	1	1	1	0

P(t=5ans) = 0,9910

Case 4 : lost of 3 lines OR 1 converter AND 0 array

	MAT :	1	2	3	4	5	6
Syst OK	1	-	32*Ldet			4*Lcod	2*Lalim
Perte d'une voie	2		-	31*Ldet			4*Lcod+2*Lalim
Perte 2 voies	3			-	30*Ldet		4*Lcod+2*Lalim
Perte 3 voie	4				-		29*Ldet+4*Lcod+2*Lalim
Perte 1 codeur	5					-	32*Ldet+3*Lcod+2*Lalim
Perte Système	6						-
	INIT :	1	0	0	0	0	0
	ETATS :	1	1	1	1	1	0

P(t=5ans) = 0,9916

Case 5 : lost of 4 lines OR 1 converter AND 0 array

	MAT :	1	2	3	4	5	6	7
Syst OK	1	-	32*Ldet				4*Lcod	2*Lalim
Perte d'une voie	2		-	31*Ldet				4*Lcod+2*Lalim
Perte 2 voies	3			-	30*Ldet			4*Lcod+2*Lalim
Perte 3 voies	4				-	29*Ldet		4*Lcod+2*Lalim
Perte 4 voies	5					-		28*Ldet+4*Lcod+2*Lalim
Perte 1 codeur	6						-	32*Ldet+3*Lcod+2*Lalim
Perte Système	7							-
	INIT :	1	0	0	0	0	0	0
	ETATS :	1	1	1	1	1	1	0

P(t=5ans) = 0,9917

3rd simulation : allowed loss of : sampling lines – one converter – one array

loss of 4 lines OR one converter OR one array

	MAT :	1	2	3	4	5	6	7	8
Syst OK	1	-	32*Ldet				4*Lcod	2*Lalim	
Perte d'une voie	2		-	31*Ldet					4*Lcod+2*Lalim
Perte 2 voies	3			-	30*Ldet				4*Lcod+2*Lalim
Perte 3 voies	4				-	29*Ldet			4*Lcod+2*Lalim
Perte 4 voies	5					-			28*Ldet+4*Lcod+2*Lalim
Perte 1 codeur	6						-		32*Ldet+3*Lcod+2*Lalim
Perte 1 matrice	7							-	32*Ldet+4*Lcod+1*Lalim
Perte Système	8								-
	INIT :	1	0	0	0	0	0	0	0
	ETATS :	1	1	1	1	1	1	1	0

P(t=5ans) = 0,9953

Annexe 6.3. Conclusions

Configuration	Reliability
lost : 4 lines – no converter – no array	0,9715
lost : 4 lines OR 1 converter AND no array	0,9917
lost : 4 lines OR 1 converter OR 1array	0,9953

Reliability is already acceptable in the 1st case (4 lines lost).