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LIST OF ACRONYMS

AD#	Applicable Document number #
ASI	Agenzia Spaziale Italiana
ATP	Authorization to proceed
CGS	Carlo Gavazzi Space SpA
CNR	Consiglio Nazionale delle Ricerche
CPP	Coordinated Part Procurement
DPU	Data Processing Unit
EDAC	Error Detector And Corrector
DPR	Dual Port Ram
EEPROM	Electrically Erasable Programmable Read Only Memory
EM	Engineering Model
EPROM	Erasable Programmable Read Only Memory
EQM	Engineering Qualification Model
FIRST	Far Infra-Red and Sub-millimeter Telescope
FM	Flight Model
FPGA	Field Programmable Gate Array
FS	Flight Spare
FSDL	Fast Science Data Link
HIFI	Heterodyne Instrument for First
IFSI	Istituto per la Fisica dello Spazio Interplanetario
I/F	Interface
LSL	Low Speed Link
OBDH	On Board Data Handling
PA	Product Assurance
PACS	Photoconductor Array Camera and Spectrometer
PCB	Printed Circuit Board
PROM	Programmable Read Only Memory
PL	Payload
RAM	Random Access Memory

RD#	Reference Document number #
SEU	Single Event Upset
S/C	Spacecraft
SPIRE	Spectral and Photometric Imaging Receiver

1 SCOPE

The aim of the present document is to define the specifications of the CPU board to be used in the Data Processing Units, developed in the framework of the First program.

2 APPLICABLE DOCUMENTS

[AD1]: CNR.IFSI.2000TR01 "Documento di Specifiche Tecniche per il Contratto delle Data Processing Units del Satellite First dell'ESA" IFSI (Issue: 1 - 15/09/2000)

[AD2]: Technical proposal CGS (Ref. S9-030 November 99)

[AD3]: "Allegato Tecnico al Contratto ASI"

3 REFERENCE DOCUMENTS

[RD1]: Radiation Tolerant 32/40-BIT IEEE Floating Point DSP Microprocessor Data Book Temic REV E October 05, 1998

4 BOARD CHARACTERISTICS

The CPU board is based on the TEMIC TSC21020 DSP. The main characteristics of the board are the following:

- ✓ DSP TSC21020 clocked @20MHz, 50ns instruction cycle time
- ✓ 20 MIPS 66MFlops (peak) of instruction rate
- ✓ 512K x 48bit (3MByte) program memory (0 Wait States operation)
- ✓ 512K x 32bit (2MByte) data memory (0 Wait States operation)
- ✓ 256K x 32bit (1MByte) EEPROM memory
- ✓ 32K x 8bit PROM based bootloader that automatically stores the boot program in program memory
- ✓ Internal watchdog for monitoring of software execution (disabled via jumper)
- ✓ Custom parallel data bus with 24 bit address and 32bit data
- ✓ Interrupt manager, totally configurable, with 6 available interrupt lines
- ✓ 32bit programmable interval timer (1μs of resolution)
- ✓ Three IEEE1355 interfaces up to 100MHz, (50% of the time machine for the transferring) with 1K x 32bit DPR buffer and RS422 standard outputs
- ✓ JTAG plug for the on board software debugging (EM version only)
- ✓ AMP connector for test purpose (EM version only)

5 MECHANICAL CONSTRAINTS

The CPU function is implemented through two Printed Circuit Boards named:

- ✓ Main board
- ✓ STD Mezzanine board
- ✓ an additional I/F mezzanine can be mounted for custom interface applications

The mechanical constraints of the two boards are shown in the Table 1 and Table 2 while the weight of the overall CPU function is specified in the Table 3

Main board size:	Double Euro (160mm x 233.35mm)
Overall thickness:	28 mm (6mm solder side, 20mm comp. side, 2 mm PCB max)
Card retainers:	Calmark series 260
Board connectors (connection to back plane):	90°, male, DIN41612 type
Board connectors (connection to mezzanines):	AMP 536280-2

Table 1 Main board constraints

STD Mezzanine size:	TBD
STD Mezzanine connectors:	AMP 536279-2
STD Mechanical fastening:	Fixation on main board and stiffening bar with six screws

Table 2 STD mezzanine board constraints

Overall weight (max):	600g (TBC)

Table 3 CPU board weight

Due to critical allocation of the components on the board, components are mounted on both sides of the PCB.

6 ENVIRONMENTAL CONSTRAINTS AND POWER SUPPLY

The constraints are summarised in the following tables:

Operating temperature:	-30 ÷ +55 °C
Non operating temperature:	-50 ÷ +85 °C
Total dose:	≤ 10 Krad
SEU rate:	≤ 1 error/year

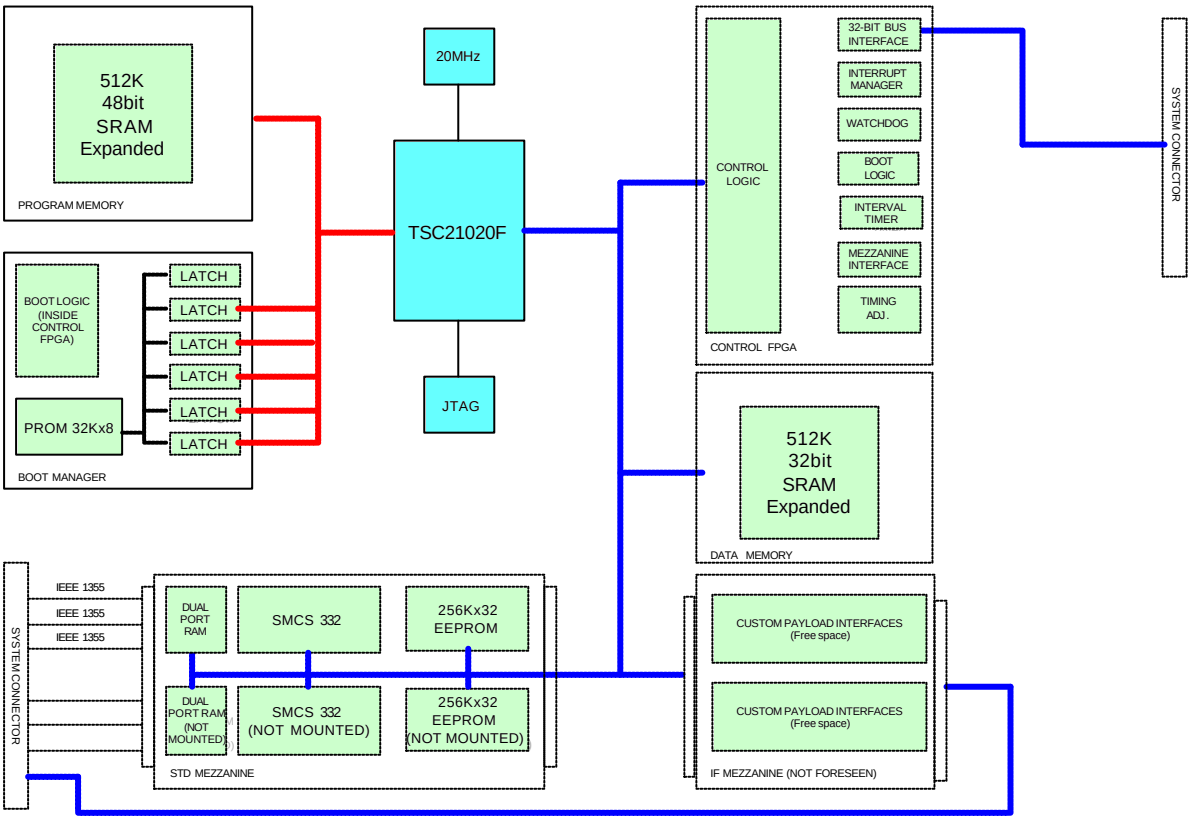
Table 4 Environmental constraints

Power supply:	5V +/- 0.5V
Maximum continuous supply current	1.5A
Peak current:	2A

Table 5 Power supply

7 FUNCTIONAL DESCRIPTION

The block diagram of the CPU board is shown in the Picture 1



Picture 1 CPU board block diagram

In the next paragraphs each block will be described in detail.

7.1 Processor

The CPU is a Temic TSC21020F clocked @20MHz. The clock is generated by an integrated oscillator and distributed through low skew clock distributors. The other clocks (showed in the Picture 7) are obtained by successive divisions from 20 MHz.

The processor works as 32-bit fixed point format.

7.1.1 INTERRUPTS

DSP IRQ #	Peripheral
0	Interrupt manager (see paragraph 7.4.1)
1	IEEE1355 dual port ram
2	Not Used
3	Not used (highest priority)

Table 6 DSP interrupt table

The interrupt 0 must be configured as level in any case. The four interrupts can be read in the IRPTL register (1=asserted).

The ISR are 8-instruction wide and are mapped in memory according to the following table:

IRQ#	PM Address
0	0x000040
1	0x000038
2	0x000030
3	0x000028

Table 7 Addresses of the interrupt service routines

In order to avoid that high level interrupts are not detected during the execution of an ISR related to a lower level IRQ, the interrupt-nesting mode of the DSP should be activated setting the bit 11 of the MODE1 register.

7.2 Program Memory

A description of the DSP program memory mapping and characteristics of the data memory bench are presented in the next three paragraphs.

7.2.1 PROGRAM MEMORY MAP

In the program memory only the SRAM is present, mapped according to the following table:

Range	Bank	Peripheral
0x000000-0x07FFFF	0	Program Memory (512KWord 48-bit wide)

Table 8 Program Memory map

The most significant digits are not decoded by hardware. Their value is set in the bank registers. The table reflects the default configuration:

- PMBANK=0x800000.

Changing the values of this register will reflect on the memory map. Consequently if there isn't any particular reason to have different bank sizes these registers should be left as they are at power-up.

7.2.2 WAIT STATES

The wait states for the Program Memory **must be set by software when the program starts execution**. The PMWAIT register must be set as follows:

	Number of WS	Bits to set	WS Mode	Bits to set
Bank0	0x0	4-2	Both int & ext (0x02)	1-0
Bank1	0x0	9-7	Both int & ext (0x02)	6-5
	PMWAIT=0x00000042			

Table 9 Program memory: setting of wait state numbers and modes

7.2.3 PROGRAM MEMORY BENCH

The program memory is formed by six 512Kx8bit SRAM memory chips. The access time of such chips shall be ≤35ns to allow 0 wait states operation. For the program memory bench the global capacity is given by 512x1024x48bit=25.165.824 bit. The SEU requirement is a probability ≤ 1 error/year in RAM; taking into account the manufacturer data of 10^{-11} errors/(bit day) for geosynchronous orbit, the probability of a

SEU event (due to a heavy ion impact), is equal to 0.1 error/year. Since this figure is less than the maximum requested no EDACs are foreseen.

7.3 Data Memory

A description of the DSP data memory mapping and characteristics of the data memory bench are presented in the next three paragraphs.

7.3.1 MEMORY MAPPING

In the data memory are mapped all the peripherals connected to the CPU, according to the following table

Range	Bank	Peripheral
0x00000000-0x0007FFFF	0	Data Memory (512KWord 32-bit wide)
0x20000000-0x3FFFFFFF	1	IF Mezzanine (not used)
0x40000000-0x400003FF	2	IEEE1355 interface (1K X32-bit wide)
0x80000000-0x8003FFFF	3	EEPROM (256Kx32-bit wide)
0x81000000-0x81FFFFFF	3	Interval timer
0x82000000-0x82FFFFFF	3	Watchdog
0x83000000-0x83FFFFFF	3	Interrupt manager
0x84000000-0x84FFFFFF	3	SMCS332 configuration registers
0x88000000-0x8FFFFFFF	3	32-bit Bus Interface

Table 10 Data Memory map

The most significant digit is not decoded by hardware. Its value is set in the bank registers. The table reflects the default configuration:

- DMBANK1=0x20000000
- DMBANK2=0x40000000
- DMBANK3=0x80000000.

Changing the values of these registers will reflect on the memory map. Consequently if there isn't any particular reason to have different bank sizes these registers should be left as they are at power-up.

7.3.2 WAIT STATES

The wait states for the Data Memory **must be set by software when the program starts execution**. The DMWAIT register must be set as follows:

	Number of WS	Bits to set	WS Mode	Bits to set
Bank0	0x00	4-2	Internal SW (0x01)	1-0
Bank1	0x02	9-7	Both int & ext (0x02)	6-5
Bank2	0x00	14-12	Internal SW (0x01)	11-10
Bank3	0x01	19-17	Both int & ext (0x02)	16-15
	DMWAIT=0x00030541			

Table 11 Data Memory: setting of wait state numbers and modes

7.3.3 DATA MEMORY BENCH

Since the processor works at 32-bit fixed point mode-operation, the lowest 8-bits of the data bus won't be used; the memory bench shall be mapped in D8-D39 data bus space.

The data memory is formed by four 512Kx8bit SRAM memory chips (32 bit parallelism), mapped on the lowest memory space of the address bus. The access time of such chips shall be ≤35ns to allow 0 wait states operation. For what concern the SEU rate, the same program memory concept can be applied and no EDACs are necessary.

7.4 Control FPGA

The control FPGA is implemented with a rad-hard Actel RH1280 (TBC).

The block performs the following functions:

- ✓ bus control and bus management
- ✓ local peripheral timing adjustment
- ✓ mezzanine interface
- ✓ boot logic

- ✓ interrupt manager
- ✓ watchdog
- ✓ interval timer

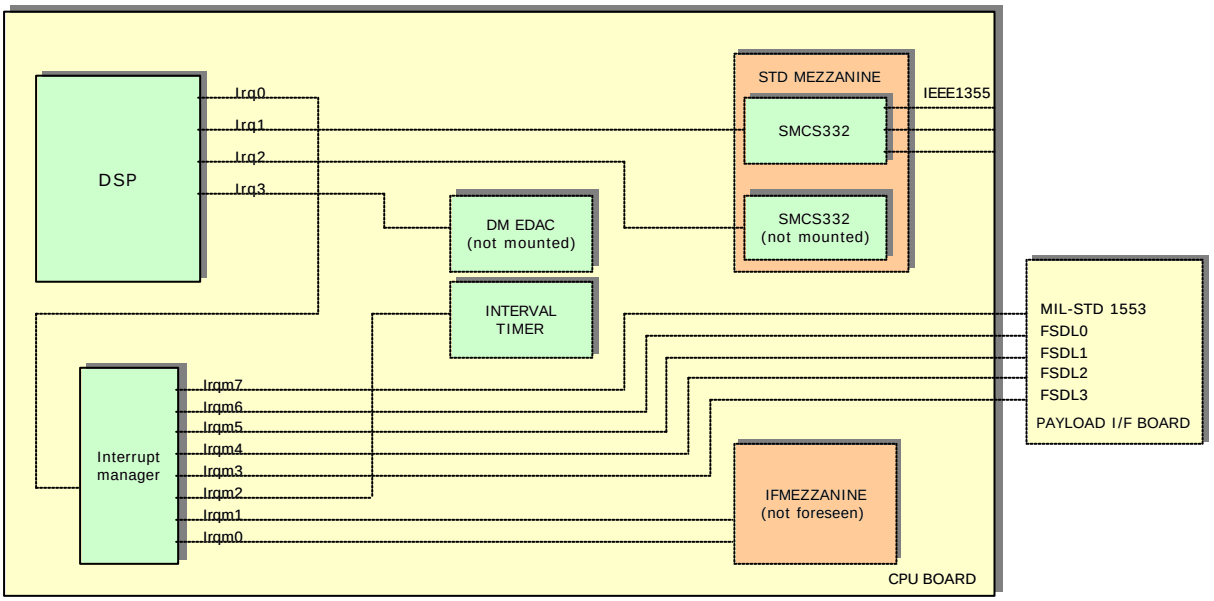
In the next paragraphs the main sections will be discussed.

7.4.1 INTERRUPT MANAGER

The interrupt manager expands the overall number of interrupts adding 8 more interrupt lines to the 4 native of the DSP. The dashed interrupts IRQ2, IRQ3 IRQM0, IRQM1 are reserved!

This peripheral is mapped as a set of registers starting at the base address specified in the DM map and is connected to the interrupt 0 of the CPU.

The interrupts are connected to this peripheral as follows in the Picture 2 and in the Table 12:



Picture 2 Interrupts distribution

IRQM#	Peripheral
0	IF Mezzanine (not used, kept low)
1	IF Mezzanine (not used, kept low)
2	Interval timer

IRQM#	Peripheral
3	Bus interface (FSDL 0)
4	Bus interface (FSDL 1)
5	Bus interface (FSDL 2)
6	Bus interface (FSDL 3)
7	Bus interface (MIL-STD 1553)

Table 12 Meaning of the eight added interrupts

The programmer must set the interface at startup so that each interrupt is configured with the correct polarity.

The meaning of the registers is explained in the following table along with the corresponding location in memory (*=default).

DM Address	Register	Type
BASE+0x00	IRQ level register (0=high*, 1=low)	R/W
BASE+0x01	IRQ type register (0=edge*, 1=level)	R/W
BASE+0x02	IRQ mask register (0=masked*, 1=active)	R/W
BASE+0x03	IRQ acknowledge register (0=ignored, 1=acknowledge)	W
BASE+0x03	IRQ vector register (0=no interrupt, 1=interrupt pending)	R

Table 13 Interrupt manager registers

The interrupt service routine related to DSP IRQ0 must read the vector register to know which peripheral requested an interrupt, then perform the operations related to the interrupt and write the acknowledge register setting at 1 the bits corresponding to the interrupts to acknowledge.

The registers are 8-bit wide, mapped on the bits 15-8 of the data memory. For each register the link between the interrupt number and the bit number is shown in the following table:

IRQM#	Bit
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7

Table 14 Correspondence bit position-irqm#

All the bits of the registers are set to 0 at power-up.

7.4.2 WATCHDOG & RESET

The watchdog timer is mapped on the data memory starting from the base address specified in the data memory map. The unit is visible by software as two registers, whose meaning is shown in the following table:

DM Address	Register	Type
BASE+0x00	Watchdog delay register	R/W
BASE+0x01	Watchdog trigger register	W

Table 15 Watchdog registers

Both registers are 16-bit wide, mapped on bits D23-D8 of the data memory bus. The delay between two triggers can be programmed writing the first 3 bits (w0, w1, w2) in the delay register, according to the table hereafter. The programmer must keep in mind that, after each power on reset, **only one writing is allowed in this register to prevent unwanted watchdog interval reprogramming due to software failures! Further writings shall have no effect.**

The fourth bit of the watchdog delay register causes the reset of the remote peripherals, connected to the parallel bus. By asserting (high) this flag, the \SYSRESETOUT output line of the board shall be asserted, to propagate the reset on the bus; a successive de-asserting (low) of the flag causes the de-asserting of the output line. Pay attention that the CPU board will not be reset by this flag, nevertheless a software reset of the board will be possible simply avoiding the trigger of the watchdog.

Value	Delay
0	13.36s (default)
1	208.75ms
2	417.5ms
3	835ms
4	1.67s
5	3.34s
6	6.68s
7	Watchdog disabled (test only)

Table 16: Watchdog delays

Hereafter the semantic of the watchdog delay register is presented:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used	Not used	**RESET**	**W2**	**W1**	**W0**

Table 17: watchdog delay register

The watchdog is triggered writing the value 0x5A6C (hex) on the trigger register. If the programmed time expires without triggering the Watchdog, the CPU is reset.

An hardware jumper shall disable the watchdog circuit.

7.4.3 INTERVAL TIMER

A programmable 32 bit binary interval timer is implemented in the FPGA and it is visible in the data memory space as a set of three registers:

- ✓ control register with a start stop/stop bit and IRQ enable/disable bit
- ✓ loading register for the setting of the programmable value
- ✓ read-back register for the counting monitoring

The counter is clocked @1MHz allowing 1µs of timing resolution.

An edge-mode interrupt is generated whenever the programmed time is elapsed (see Table 12).

7.5 EEPROM Block

The EEPROM block contains the program to execute. It is formed by a single 256Kx32bit (32-bit parallelism) EEPROM. The 32 bits shall be mapped in the bits D8-D39 of the DSP data bus. For unwanted writings on the EEPROM, it can be software protected in single frames (JEDEC standard algorithm).

The transfer of the program from this module to the program memory and the reconstruction of the 48-bit words from the 8-bit code, shall be performed by software resident in PROM and loaded in program memory after the power-on.

7.6 Boot PROM

The boot PROM contains the primary bootloader. It is made by a single 32Kx8bit PROM. Jumpers make possible to insert a differently sized PROM (up to 32Kx8bit). This PROM is fully controlled by the boot section of the control FPGA and is not visible to the software during normal operation. Other drivers contained in PROM are described in the "Software Architectural Design".

7.7 Bus Interface

The internal bus is directly derived from the DSP data bus (see [RD1]); it is composed by the following lines:

- ✓ 24 address lines
- ✓ 32 data lines
- ✓ 5 interrupt lines (programmable)
- ✓ 8 chip select lines (actives low)
- ✓ 1 read line (active low)
- ✓ 1 write line (active low)
- ✓ 1 system clock (20MHz)
- ✓ 1 asynchronous reset line (active low)

On this bus are mapped all the external peripherals. The DSP decodes eight chip select, agree with the following table:

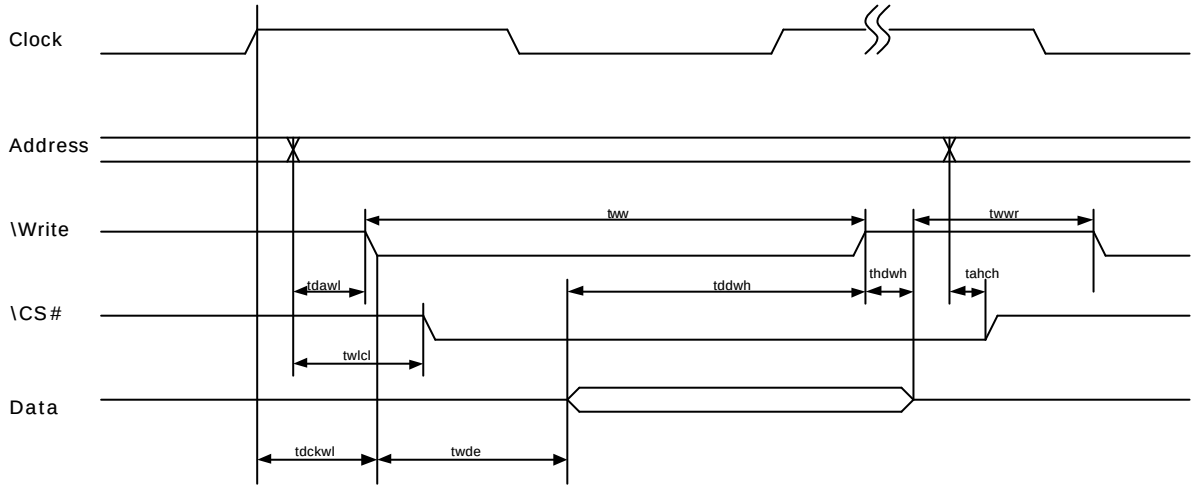
\CS	Address range
0	0x88000000-0x88FFFFFF
1	0x89000000-0x89FFFFFF
2	0x8A000000-0x8AFFFFFF
3	0x8B000000-0x8BFFFFFF
4	0x8C000000-0x8CFFFFFF

\CS	Address range
5	0x8D000000-0x8DFFFFFF
6	0x8E000000-0x8EFFFFFF
7	0x8F000000-0x8FFFFFFF

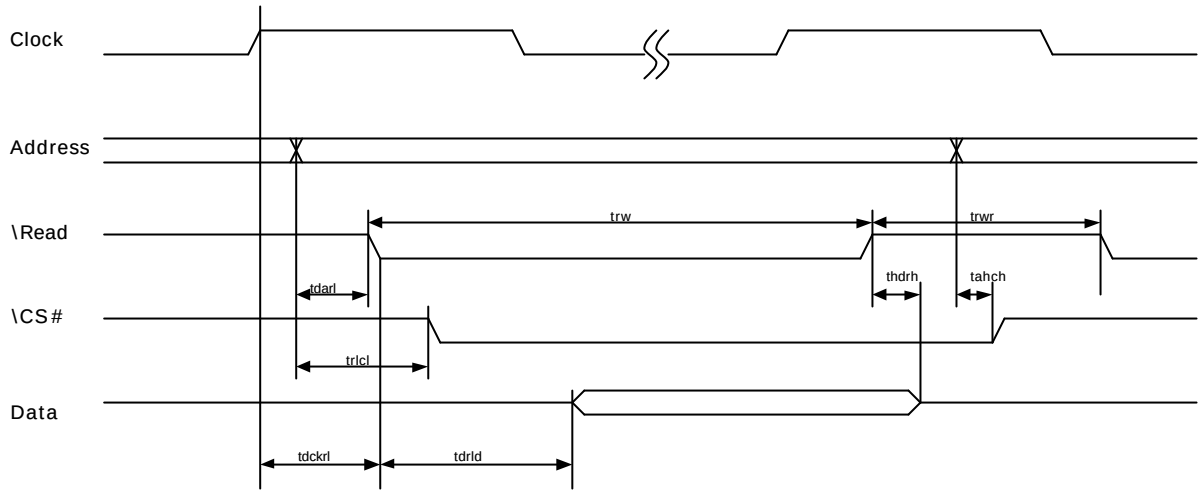
Table 18: chip select address range

The timing of the bus is compliant to the 21020 read and write timing with 1 W/S (TBC) for the devices addressed by CS0÷CS6; the last one has 6 hardware W/S (TBC) to address slow peripherals. The 32 bits shall be mapped in the bits D8-D39 of the DSP data bus.

The Picture 3 and Picture 4 show respectively, the write and read cycles for the peripherals on the bus space whereas the Table 19 reports the timing values.



Picture 3 Bus write cycle



Picture 4 Bus read cycle

Parameter	Min	Max	Unit
tdawl	14 (TBC)		ns
twlcl		17 (TBC)	ns
tdckwl	20 (TBC)	30 (TBC)	ns
twde	0 (TBC)		ns
tww	26 (TBC)		ns
tddwh	19 (TBC)		ns
thdwh	50 (TBC)		ns
tahch		17 (TBC)	ns
twwr	17 (TBC)		ns
tdarl	11 (TBC)		ns
trlcl		17 (TBC)	ns
tdckrl	20 (TBC)	30 (TBC)	ns
tdrld		21(TBC)	ns
trw	76 (TBC)		ns
thdrh	-4 (TBC)		ns
trwr	17 (TBC)		ns

Table 19 Bus timings

In case of successive accesses to the same memory area (same chip select), the \CS lines remain asserted until a different memory area is addressed; this means that is not mandatory to have chip select signal edges on a bus cycle.

7.8 IEEE 1355 Interface

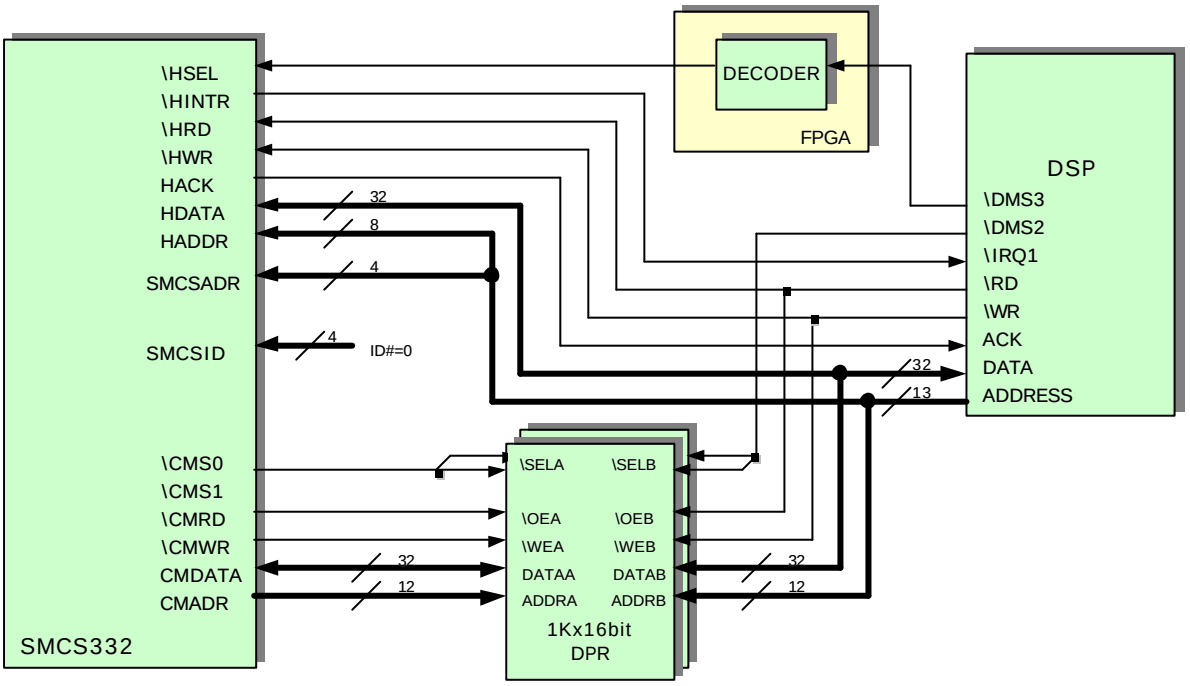
The STD mezzanine contains three IEEE1355 serial links; they are realised with a single chip named SMCS332. Each link is composed by four signals: data-in, strobe-in,

data-out, strobe-out; the signals are in RS422 electrical standard format. A dual port ram (4Kx32-bit) is foreseen to minimise the CPU intervention.

To optimise the data exchange between the DSP and the SMCS, the data are 32-bit deep, consequently the SMCS data bus, must be configured via software in 32 bit-parallelism mode.

The configuration registers of the SMCS are mapped in the bank 3 of the data memory space; to adapt the timing cycle of the SMCS, the DSP uses the acknowledge line to add hardware W/S.

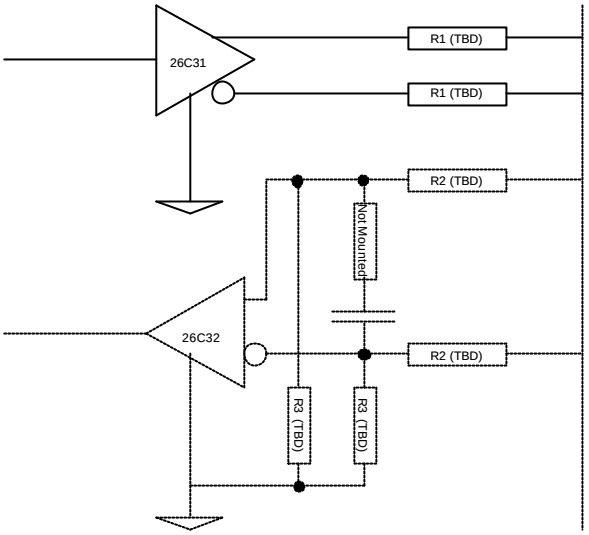
The DPR is addressed directly by the bank 2 to maximise the transfer speed.



Picture 5 IEEE1355 interface stage

7.8.1 ELECTRICAL INTERFACE

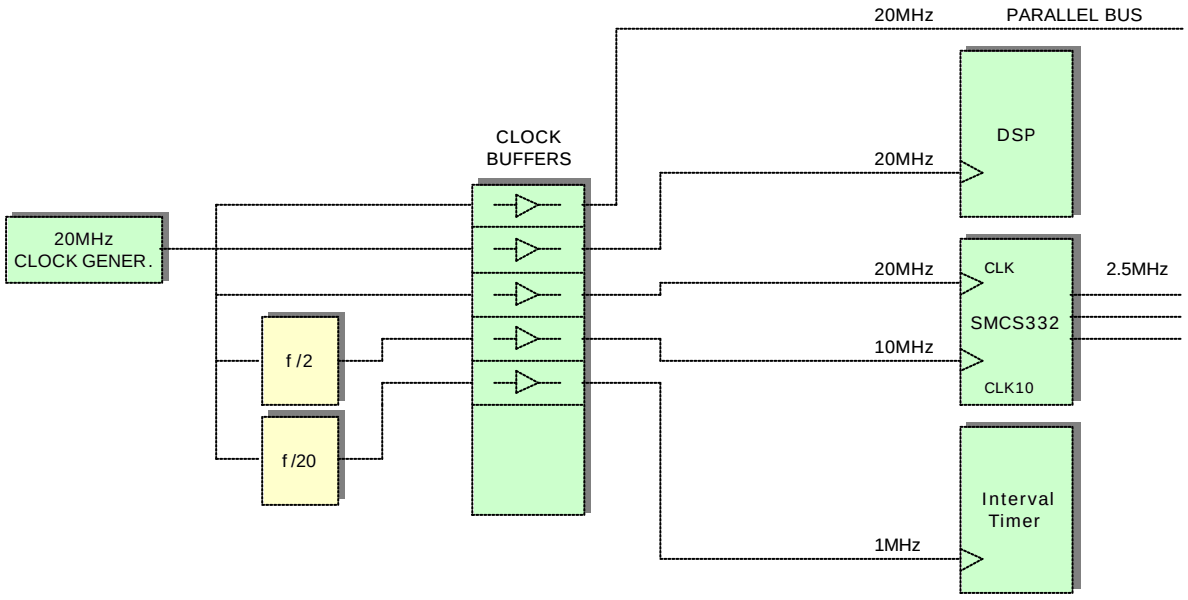
As mentioned above, the IEEE1355 links shall be in RS422 electrical standard format. The interfaces employ balanced differential line drivers and receivers, type 26C31, 26C32 to provide good common mode rejection and reasonable isolation characteristics. In the Picture 6 are shown the driving and receiving networks:



Picture 6: RS422 electrical interface

The parasitic capacitance of the 26C32 input lines (to ground) shall be <20pF, this restricts the length of the PCB traces between the input resistors and the 26C32 inputs.

7.9 Clocks Generation and Distribution



Picture 7 Clock generation and distribution

An oscillator generates the 20MHz clock (maximum frequency clock) for the DSP and the bus interface; the other clocks are generated by some FPGA blocks by successive divisions. In particular, the 10MHz and 1 MHz clocks, are obtained dividing the original clock respectively by 2 and by 20. The clocks are distributed by means of clock buffers.

7.10Latchup Protection

Due to the high level of latchup immunity of the selected components (>100MeV/mg cm^2), no latchup protection is implemented on CPU board. Anyway, different supply sections are foreseen on the board itself to increase flexibility of the current protection philosophy of the system. Actually, all the power supply sections are joined on the motherboard to supply the CPU board with a single power line.

8 PERFORMANCES

The CPU board performances are the following:

- ✓ computational machine at 20 MIPS 66MFlops (peak)
- ✓ 20MHz system clock
- ✓ automatic HW bootloader for boot program storing in program memory
- ✓ 32-bit interval timer, 1µs resolution
- ✓ 32-bit parallel system bus <110ns transfer time (TBC)
- ✓ eight CS lines (active low) for the addressing of the other peripherals of the bus
- ✓ three IEEE1355 serial interfaces up to 100Mbit/s (50% of the time machine for the transferring) in RS422 electrical standard interfaces
- ✓ programmable watchdog with settable intervals from 417.5ms to 13.36s
- ✓ interrupt manager, totally configurable, with 6 available interrupt lines

9 PIN FUNCTION

The pin function of the CPU board is shown in the Table 20 and Table 21.

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+5VD	33	+5VD	65	+5VD
2	+VEEPROM	34	+VFPGA (RTC)	66	+VDSP
3	D0	35	D1	67	D2
4	D3	36	D4	68	D5
5	D6	37	D7	69	D8
6	D9	38	D10	70	D11
7	D12	39	D13	71	D14
8	D15	40	D16	72	D17
9	D18	41	D19	73	D20
10	D21	42	D22	74	D23
11	D24	43	D25	75	D26
12	D27	44	D28	76	D29
13	D30	45	D31	77	\WR
14	A0	46	A1	78	A2
15	A3	47	A4	79	A5
16	A6	48	A7	80	A8
17	DGND	49	SACK	81	DGND
18	A9	50	A10	82	A11
19	A12	51	A13	83	A14
20	A15	52	A16	84	A17
21	A18	53	A19	85	A20
22	A21	54	A22	86	A23
23	\CS0	55	\CS1	87	\CS2
24	\CS3	56	\CS4	88	\CS5
25	\CS6	57	\CS7	89	\RD
26	IRQM3	58	IRQM4	90	IRQM5
27	IRQM6	59	IRQM7	91	SYSCLK
28	RESERVED	60	\SYSRESETOUT	92	SYSCLK
29	RESERVED	61	RESERVED	93	RESERVED
30	AGND	62	AGND	94	AGND
31	RESERVED	63	RESERVED	95	RESERVED
32	DGND	64	DGND	96	DGND

Table 20 CPU board: P1 pin function

Pin #	Signal	Pin #	Signal	Pin #	Signal
1	+5VD	33	+VIFMEZZ	65	+5VD
2	L0DI+	34	L1DI+	66	L2DI+
3	L0DI-	35	L1DI-	67	L2DI-
4	L0SI+	36	L1SI+	68	L2SI+
5	L0SI-	37	L1SI-	69	L2SI-
6	L0DO+	38	L1DO+	70	L2DO+
7	L0DO-	39	L1DO-	71	L2DO-
8	L0SO+	40	L1SO+	72	L2SO+
9	L0SO-	41	L1SO-	73	L2SO-
10	RESERVED	42	RESERVED	74	RESERVED
11	RESERVED	43	RESERVED	75	RESERVED
12	RESERVED	44	RESERVED	76	RESERVED
13	RESERVED	45	RESERVED	77	RESERVED
14	RESERVED	46	RESERVED	78	RESERVED
15	RESERVED	47	RESERVED	79	RESERVED
16	RESERVED	48	RESERVED	80	RESERVED
17	RESERVED	49	RESERVED	81	RESERVED
18	RESERVED	50	RESERVED	82	RESERVED
19	RESERVED	51	RESERVED	83	RESERVED
20	RESERVED	52	RESERVED	84	RESERVED
21	RESERVED	53	RESERVED	85	RESERVED
22	RESERVED	54	RESERVED	86	RESERVED
23	RESERVED	52	RESERVED	84	RESERVED
24	RESERVED	53	RESERVED	85	RESERVED
25	RESERVED	54	RESERVED	86	RESERVED
26	RESERVED	58	RESERVED	90	RESERVED
27	RESERVED	59	RESERVED	91	RESERVED
28	RESERVED	60	RESERVED	92	NOT USED
29	NOT USED	61	NOT USED	93	NOT USED
30	RESERVED	62	RESERVED	94	RESERVED
31	RESERVED	63	FLAG0	95	FLAG1
32	DGND	64	DGND	96	DGND

Table 21 Cpu board: P2 pin function