

CLRC
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## DCU Redundancy/Cryoharness

This is the memorandum that I promised last week to be consideresd prior to our video-conference. I hope I'm sending it to the relevant people this time rather than the world who got the original E-mail due to finger trouble!

Figure 1 shows the configuration for bolometer bias and JFET voltage supplies at IIDR. This takes a functional block approach because showing everything semi-physically becomes like the overall block diagram and is quite complicated. For instance, the detector a.c. biases enter the JFET PCBs from the correct back-harness direction, whereas the JFET voltage supplies are drawn as entering from the side farther from the BDAs although we all know that they are actually routed in the same back-harness as the a.c. biases. The radiometric signal functions are omitted for clarity. The filter units associated with the bolometer non-radiometric signal wires are similarly omitted.

Because of the much discussed criticality w.r.t. power dissipation and noise performance, each JFET membrane PCB has its own power supply with adjustable setting, as confirmed by the numbers of functions just presented at the IIDR. Thus the photometer has 12 twenty four channel JFET membrane PCBs. To relate this a little to the physical, they are housed in 6 two compartment JFET modules as delineated in purple. The spectrometer has 3 PCBs in one and a half modules. The two systems are electrically isolated. The JFET membrane PCBs condition bolometer pixels that are located as detector planes in BDAs, shown ringed in purple down the l,h,s. of the figure. Each membrane PCB feeds an a.c. bias to its pixels as shown.

All the functional arrows represent a $+/$ - pair. Because ISO experience says that cryoharness is the least reliable part of the system, two cryoharness wires are used for each of the + and - to confer robustness against a single cryoharness wire breakage, making 4 contacts and 4 wires per functional arrow. [In fact they leave the JFET modules as two wires and split into 4 in the back-harness / bolometer filter units that I have omitted from the figure]. Some contacts are also needed for ground wires and heaters, but they have been also omitted to keep things simple.

Each BDA has an associated a.c. bias module with adjustable amplitude and frequency, to permit optimum operation of that BDA. An a.c. bias is used to avoid 1/f noise and galvanic offsets. A sine-wave bias is applied to measure the bolometer's impedance. A bias frequency should be sufficiently high that a bolometer does not significantly follow it as a driven power/temperature cycle, which would modulate the working point. However, the highest appropriate frequency is constrained by stray capacitance, including that due to harness, which starts to attenuate the signals sourced via the high impedance detectors.

The whole cryogenic bolometer system is non-redundant when considered in the sense that Spire has Prime and Redundant sided electronics, either of which can be used to nominally identical effect. The same applies for warm analogue DCU lock-in amplifiers that handle the bolometer radiometric signals.

For a long time electronics block diagrams and documents have shown the DCU to have Prime and Redundant analogue bolometer bias and JFET voltage supplies. Redundant units are represented in the figure by shadowed blocks. Prime functional links are shown in red and redundant ones in orange. The
unpowered sections and their associated harness remain connected to the powered side, with joints indicated by the blue patches on the diagram. I have queried this several times, not least as I am unaware of a formal requirement for any part of the bolometer analogue system to be redundant. It complicates grounding, and having some of the analogue DCU [which needs specialist quiet supplies] running redundantly and some non-redundantly must also complicate the FCU power supply and filtering configuration.

However, there were more major matters to work through (some remaining so) and I waited for this information to become apparent. The only reply I had received about leaving unpowered items connnected was one from Viktor who also seemed to be querying whether the configuration was in fact optimum. However the major problem that I had already noted and circulated in the Harness Document is that whilst the Spectrometer wiring just fitted down the cryoharness with a bit of a squeeze on the JFET heater wires, the Photometer wires did not. The need to fit down harness is represented diagrammatically by the ovals around the functional arrows. I did not find this matter answered in documents provided for the IIDR or in Presentations.

I therefore discussed the situation with Frederic Pinsard, and mentioned putting the Prime / Redundant joints at the warm end as shown in figure 2, probably as a little inelegant Y adaptor, to solve my perceived cryoharness problem. Such an approach would mean that double-pinned functions from the JFET Membrane PCBs would pass as $1: 1$ wires through the r.f. filters (that I have omitted from the figures) to cryoharness pins, rather than needing to divide into two somewhere. Frederic did not suggest that the problem had already been solved because I was looking at things incorrectly, he only expressed a wish to avoid DCU I/F changes. The configuration in figure 2 results in no such DCU changes at all. I appreciate that JPL knew nothing of this specific proposal re. the harness, but I note that it came to Jean-Louis " to our utmost surprise"!
[I have previously been happy to say that all bolometer system wires are minimum stainless gauge and only carry signals. In fact with 48 JFETs in 24 pairs in a JFET Membrane PCB, and each passing a maximum of $100 \mu \mathrm{~A}$, the rating should be 5 mA (for one wire if one should be able to break without causing a failure). This is not insignificant for cryoharness. Further, we need the test and flight harness to match well to avoid radiometric calibration differences due to small V+ and V-changes. This is the more important because of Spire's philosophy of carrying "stable" reference points taken with the shutter-closed between instrument and CVV test configurations without requiring the shutter to provide a precision quantifiable radiance.]

Consider the possible simplification shown in figure 3. Bruce had already noted that because of the small fraction of Spire that fails if one JFET membrane power supply were to malfunction, we would almost certainly not take the risk of swapping the whole instrument Prime to Redundant just for such a failure. So the redundancy would probably be redundant! I somewhat simplistically took the view that standard electronics are extremely unlikely to fail, and Spire already has multiplexors and ADCs as major single point bolometer system degradations, so why not remove the redundant units in question To my mind the configuration has a certain elegance. It also removes unpowered items hanging on sensitive bias and supply lines. Another factor is that if any of the analogue parts of the bolometer are prime/redundant, all ground radiometric calibration must be done fully and properly on both sides of the instrument. Note that figure 3 is only a possible simplification.

Finally. consider figure 4, a suggestion from Bruce (that I have worked through somewhat) in which the redundant JFET supplies are deleted, but all 8 a.c. bias generators remain and are permanently powered as non-redundant. This has the evident advantage of making the instrument degradation in the event of a bias generator failure much more palatable. The damage caused by a single bias generator failure is limited to one or two JFET Membrane PCBs, and only in the case of the SLW does a whole detector drop out. The system is still able to provide Prime and Redundant temperature control thermistor conditioning, actually hot redundant, if this is needed to fit in with Prime/Redundant FCU and DCU systems.

In figures 1-4 the harness wiring for the photometer supplies/biases amounts to $32,16,16$ and 20 functions respectively. After adding heaters, grounds, etc., all but the first can be fitted through a 100way. However, I will now defer working through the details until after we have all agreed on the principles.

For noise control we clearly only want one frequency present at one phase in each BDA, which means that if the figure 4 configuration were to be adopted the common frequency generators shown on the r.h.s. become other examples of items with wide failure consequences, having just the same impacts of those of the bias generators in figure 3 !

There is one further move towards elegance that should be considered. There can be two identical looking JFET type modules for the Spectrometer and 7 for the Photometer if in the Spectrometer one of the JFET Membrane PCBs were to have no membrane/aperture and just tracks across this area, and two identical items were used in the Photometer. This would match $4 \times 25$ way MDMs on each module to 100 way CVV connects all across the bolometer cryoharness, require Berend's frames to only hold shape of unit faceplate, fully use the half unused JFET module in the Spectrometer, etc.. I hope we can adopt this and no-one will rule it out because it's making filters with 25 way connectors instead of the decreed 37 ways (we keep the 37 ways in non-bolometer filters mounted in the FPU). Hopefully with the signal channel 25ways now as in the harness spec. a well structured 51way MDM the other end of the modified JFET module would permit a flat ribbon configuration for the back-harness without non-interleaved function conductors or other PCB adjustments. I attach a possible system block diagram for this scenario.

Now, as has been logically pointed out, such configurations can only properly assessed in the light of an overall coherent Prime/Redundant design, noting where single point failures exist. Two reviews ago I started into a discussion about making DRCU functions individually switchable between Prime and Redundant and was told that the subject has been fully assessed, and that Spire was fine with simple overall Prime and Redundant instrument electronics. Please could the author get Judy to post this in the Design Description folder on Livelink so that all of us who wish to take part in the forthcoming teleconference on the subject can have read it beforehand to see the criteria by which just a part of the DCU analogue section is presently redundant.

Maybe engineering judgement is at least as relevant as formal FMECAs statistics, i.e. failures in high build-standard one-off equipment are far more likely to be common by design/batch to all similar items than random! Hence the importance of radical peer assessment.

It will be evident from the above that having come into the project late I still need to catch up on the design tradeoffs that have gone into the DCU and maybe never appeared as formal project documents*. This is a much wider ranging matter than a description of the present design. I have recently included a top down timing philosophy in the IID-B ch5 considered from the S/C control and command I/F. However, looking "up" at the timing from the bottom of the system, frequencies and synchronisation are clearly major factors. Let me suppose that we want to use all the performance of the 4 msec spectrometer and 12 msec photometer time-constant detectors. Settling to $4 \tau$, which is still imprecise by Spire S/N standards, will require 14 or 48 msec respectively, corresponding to maximum rates at which fairly independent radiometric signals can be meaningfully be measured of 71 and 20.8 Hz . respectively. To scale the other way and minimise bias-driven modulation would require nominal bias frequencies of 1.1 KHz and 332 Hz . I therefore reckon that when $60-300 \mathrm{~Hz}$ bias is specified people must be happy to have the bolometers driven in temperature by their own readout bias.

Since we have a smoothed and digitised system, rather than one with a bandwidth limit and formal integration, one supposes oversampling to avoid aliasing, e,g. maybe 32 Hz . sampling on a 12 Hz . bandwidth. So why for instance for the photometer is the detector bandwidth being degraded from 20.8 Hz . not to 12 Hz . but to 5 Hz .(4Pole). Not least, this will give an $800 \mathrm{msec} 4 \tau$ signal settling time, instead of 48 msec !

Whatever the precise frequency of the post PSD filters, I would suppose that no sensible filtering can adequately remove the PSD ripple such as to permit asynchronous sampling and so, for any given channel, the smoothed post PSD signal needs to be sampled with a fixed phase lock to whole cycles of the bias modulation period. [Whole cycles not half cycles because of possible significant second harmonic content in the bolometer signals that cannot be pre-filtered prior to the PSD]. Also, we need confirmation that the information given at the last detector meeting is correct, namely that the ADC picks up each sample 8 times to reduce its own input noise and that (excluding the offset switching bits) the documented 16bits are output from the DCU to the DPU, not 19.

I note that there are 6 A-D convertors but, unless I'm mistaken, instead of the channels going to them being grouped as the six bias generators, they are grouped in numerically symmetric trees. This seems inconsistent with having adjustable frequency to optimise detector performance, given that each BDA characteristic, associated with a bias generator, has different resistance and capacitance. Surely optimum performance requires separate frequencies. Have I got something wrong?

This is all leading to the point, as already stated, of needing to couple the complete DCU/bolometer system block diagram together in detail in order to consider the need any for redundancy of particular
elements. The we can detail how to couple them together and power/command the system. Possibly the redundancy trade-off document I've mentioned above does all this, but if not maybe Christophe has some internal notes that need circulating.

So, can everyone stick in ideas and information, even of the "you obviously did not read my e-mail of $\mathrm{xx} / \mathrm{xx} / 89$ " type, and then an optimist would hope that the same best way forward will be clear to everyone before the video conference.

Best regards
John

* I suppose I ought to really come clean, go right back to basics, and ask where I can find how Spire did the trade-off to arrive at a system that does a very large amount of multiplexor switching just at the time when all the signals are required to be most stable to input $\mathrm{nV} / \mathrm{sqrt}(\mathrm{Hz}$.$) levels? Why for instance, with$ only $16-32 \mathrm{~Hz}$ sampling, does the front-end analogue part not finish in 16 -channel wide ASICs that have alternate timeslot double dual slope integrators per pixel, integrating rather than smoothing over numbers of bias cycles, using the reverse integrators' counts of a clock at thresholds? Such results which can be taken away from a buffer comparatively slowly.


Figure 2
LFET BIAS/SUPPLY CONFIGURATION


Figure 3
POSSIBLE SIMPLIFICATION to IFET BIAS/ SUPPLY CONFIGURATION



