Herschel

SPIRE

DPU Interface Control Document

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Document Status Sheet:

Document Title: Herschel- SPIRE DPU Interface Control Document			
Issue	**Revision**	**Date**	**Reason for Change**
Draft 1		22/11/2000	First draft
Draft 2		5/12/2000	Low speed I/F timing
1.0		2/4/2001	
	1	11/02/2002	Updating
	2	10/02/2003	Updating
	3	13/02/2003	Updating
	4	24/03/2003	Updating for IHDR

Document Change Record:

Document Title: Herschel- SPIRE DPU Interface Control Document	
DOCUMENT REFERENCE NUMBER: SPIRE-IFS-PRJ-000650	
Document Issue/Revision Number: 1.4	
Section	**Reason For Change**
3.3	S/C connectors and pin functions
4.2	Low speed I/F protocol and timing definition
3.1	Updated box dimensions
3.2.2	Updated power consumption estimates
5	Added
6	Added
	ISSUE 1.1
	Updated the Applicable Documents table
3.1	Box interface control drawing added
3.2.3	Synch. Signal removed
3.3	Removed the synch. Signals from connectors J03, J04, J05, J06
4.2	Updated T2min to –30 Ns
7	Updated signal name for Low Speed Clock: LCLK_DCU… And for High Speed Clock: HCLK_DCU….
7	Low Speed Clock Shield added on pin 1 of connectors J07 to J12
	ISSUE 1.2
4.2	Updated table
4.3	Updated Table
	ISSUE 1.3
4.3	Updated Table
	ISSUE 1.4
4	DPU/ICU mass Breakdown added
5	DPU/ICU Power Breakdown added
10.1 to 10.6	Added TX Shield at pin 14

Applicable documents

Document Reference	Name	Reference
AD1	Herschel/Planck Instrument Interface Document Part A	PT-IID-A-04624
AD2	Herschel/Planck Instrument Interface Document Part B Instrument “SPIRE”	PT-HIFI-02125
AD3	SPIRE Instrument Requirements Document	SPIRE-RAL-PRJ-000034
AD4	Operating Modes of the SPIRE Instrument	SPIRE-RAL-PRJ-000---
AD5	SPIRE Data ICD	SPIRE-RAL-DOC-001078

Reference documents

Document Reference	Title	Reference
RD1	ESA PS-ICD	
RD2	SPIRE DPU Subsystem Specification Document	SPIRE-IFS-PRJ-000462
RD3	DRCU Interface Control Document	Sap-SPIRE-Cca-25-00
RD4	MCU Design Description	LAM/ELE/SPI/000619

Acronyms

CDMS	Central Data Management System
CDMU	Central and Data Management Unit
CNR	Consiglio Nazionale delle Ricerche
CPU	Control Processing Unit
DCU	Detector Control Unit
DPU	Digital Processing Unit
DRU	Detector Readout Unit
DSP	Digital Signal Processor
EGSE	Electronic Ground Support Equipment
ESA	European Space Agency
FIRST	Far InfraRed and Submillimeter Telescope
HK	HouseKeeping
HW	HardWare
ICD	Interface Control Document
ICU	Instrument Control Unit
I/F	Interface
IFSI	Istituto di Fisica dello Spazio Interplanetario
MCU	Mechanism Control Unit
NA	Not Applicable
OBS	On-Board Software
PDU	Power Distribution Unit
S/C	Spacecraft
S/S	Subsystem
SPIRE	Spectral and Photometric Imaging REceiver
SPU	Signal Processing Unit
SR	Software Requirement
SSD	Software Specification Document
SVVP	Software Verification and Validation Plan
SW	SoftWare
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TC	Telecommand
TM	Telemetry

Table of contents

1 Scope of the document

This document describes the interfaces of the SPIRE Digital Processing Unit with the Herschel spacecraft (S/C), the Instrument Control Unit (ICU) and the Detector Readout Unit (DRU)
The following block diagram shows the simplified overall layout of SPIRE and the interfaces described in this document.

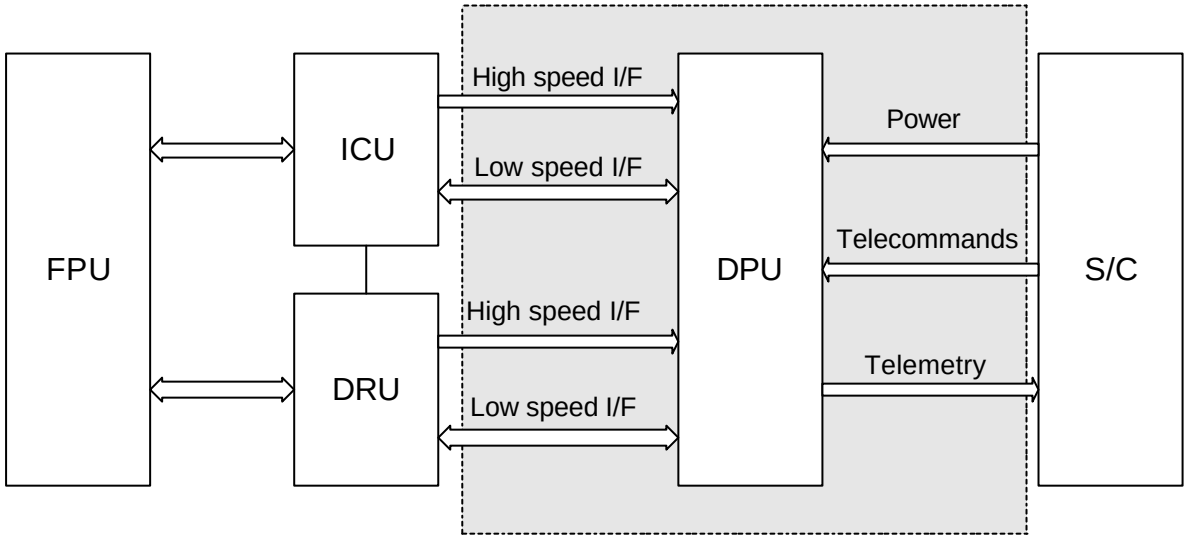


Figure 1-1 SPIRE DPU interfaces schematic view

2 Description of DPU subsystem

The DPU is based on a 20 MHz clock TEMIC TSC21020 Digital Signal Processing (DSP) developed by Analogue Devices and implemented for flight use by TEMIC.
The DSP implements Harvard architecture, i.e. the data bus (32 bit) and the programme bus (48 bit) are completely separated, so increasing the execution speed.
The program area is implemented with PROMs, EEPROMs and RAM. The PROM stores the initial boot loader and emergency recovery modules. The instrument program is stored in EEPROMs and copied in RAM at run time for execution. Program area may be used as data memory.
The DPU includes a free running (about 131 kHz) DC/DC converter to supply the internal circuitry.

2.1 Overall DPU block diagram

The following diagram shows the main DPU blocks, the electrical interfaces and the memory dimensions.

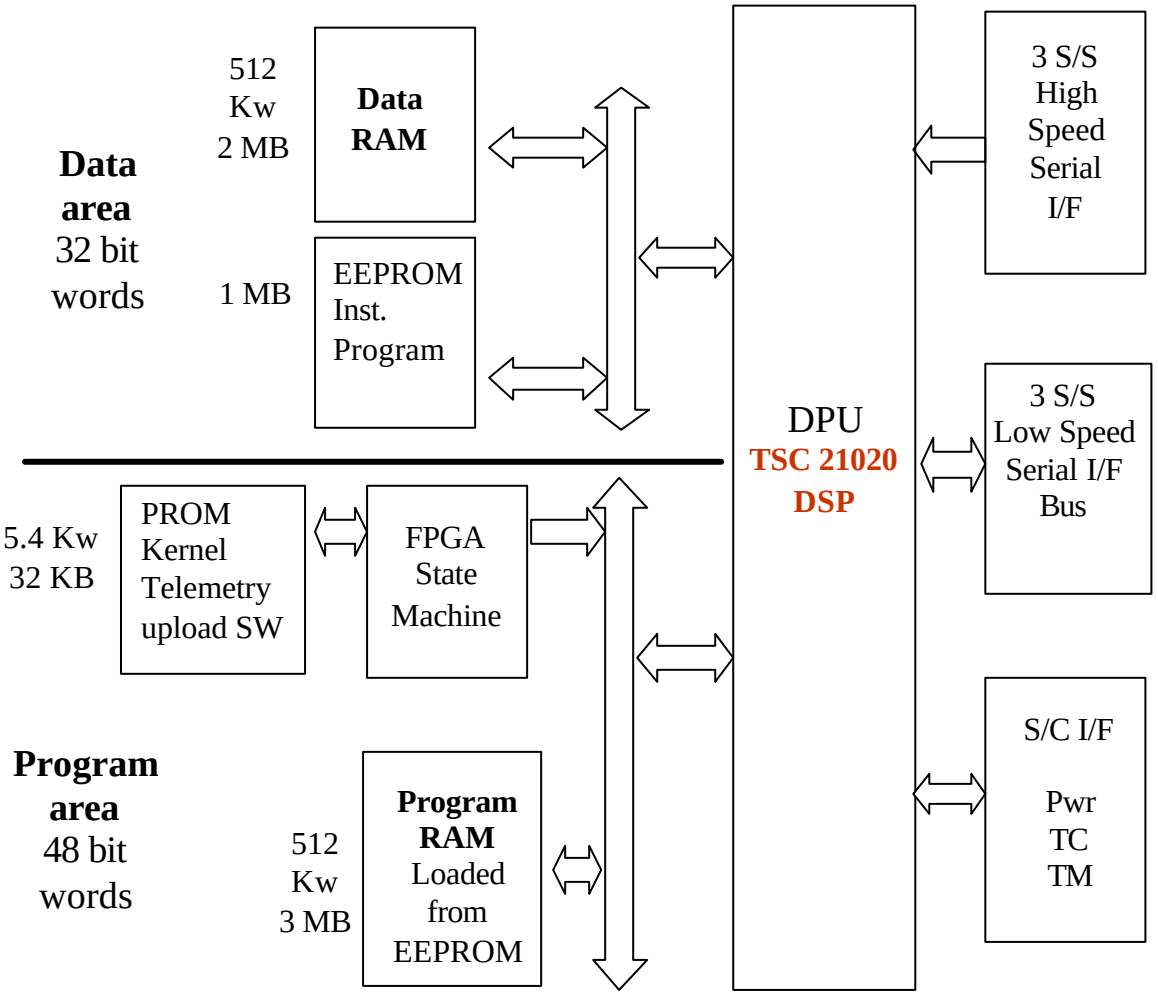


Figure 2-1 DPU CPU memory organisation

2.2 Redundancy concept

The top level DPU redundancy concept is shown in the following diagram:

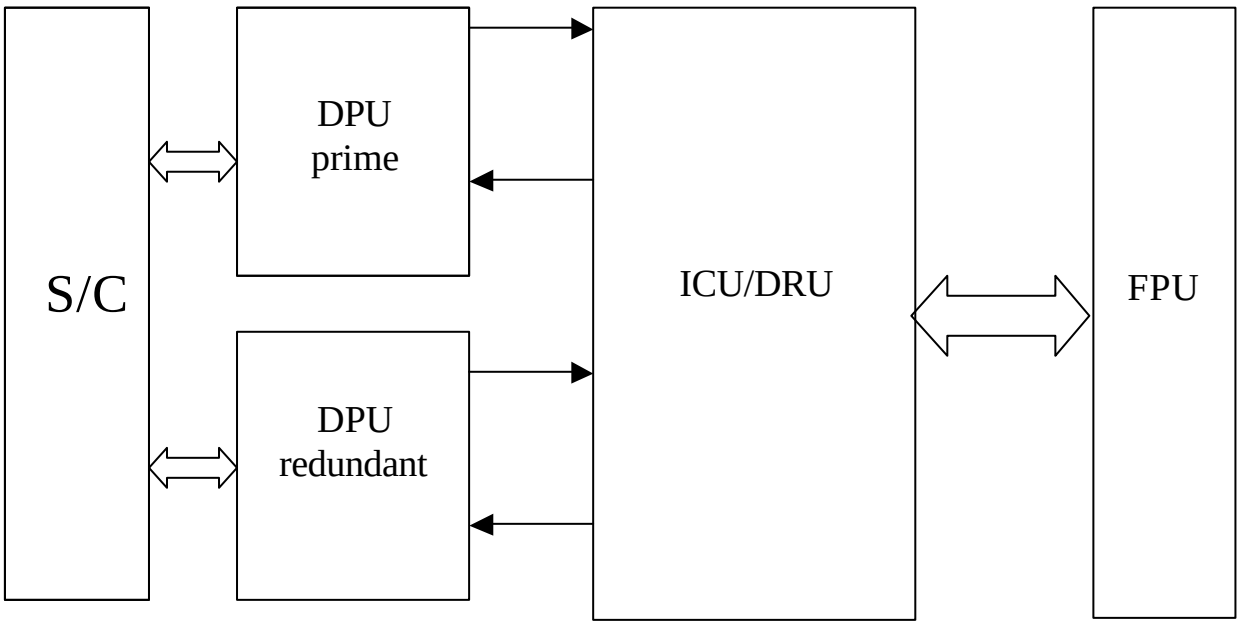


Figure 2-2 DPU redundancy concept

The DPU box contains two complete units in cold redundancy states. The S/C prime/redundant 28V power bus controls the switching between the two units.
As a consequence, the DPU interfaces with both S/C and S/S are doubled.

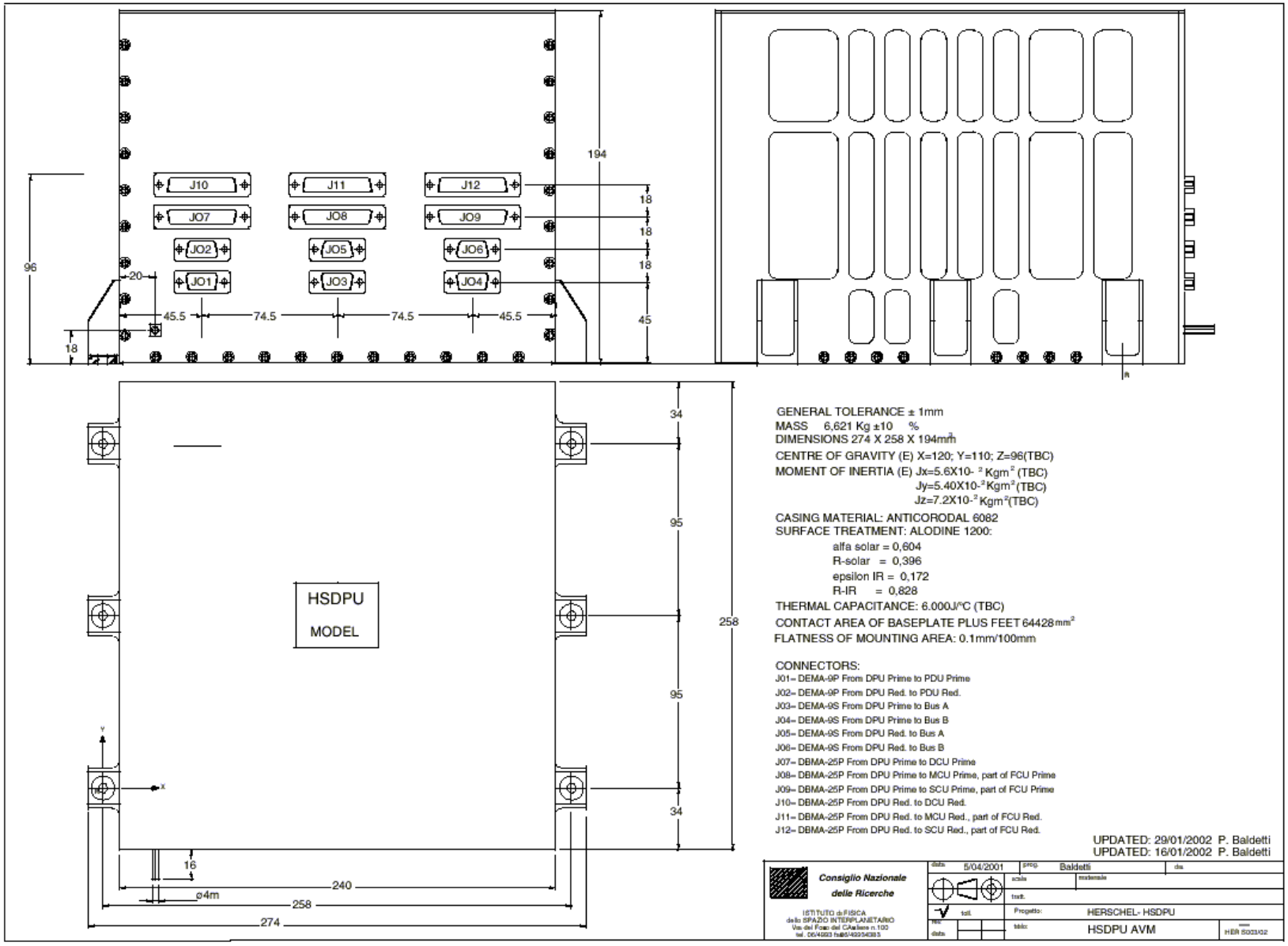
3 DPU - Spacecraft interfaces

3.1 Mechanical I/F

The prime and redundant DPUs are included in the same mechanical box whose dimensions are:

274x258x194 mm including the feet
240x258x194 mm without the feet

The box interfaces mechanically with the S/C with 6 feet.
In the following figure the mechanical interface control drawing is shown.


J10
J11
J12
JO7
JO8
JO9
JO2
JO5
JO6
JO1
JO3
JO4
194
96
20
45.5
74.5
74.5
45.5
18
18
18
18
45
HSDPU
MODEL
34
95
95
34
258
16
240
ø4m
258
274
GENERAL TOLERANCE ± 1mm
MASS 6,621 Kg ±10 %
DIMENSIONS 274 X 258 X 194mm
CENTRE OF GRAVITY (E) X=120; Y=110; Z=96(TBC)
MOMENT OF INERTIA (E) Jx=5.6X10-2 Kgm2 (TBC)
Jy=5.40X10-2Kgm2(TBC)
Jz=7.2X10-2Kgm2(TBC)
CASING MATERIAL: ANTICORODAL 6082
SURFACE TREATMENT: ALODINE 1200:
alfa solar = 0,604
R-solar = 0,396
epsilon IR = 0,172
R-IR = 0,828
THERMAL CAPACITANCE: 6.000J/°C (TBC)
CONTACT AREA OF BASEPLATE PLUS FEET 64428mm2
FLATNESS OF MOUNTING AREA: 0.1mm/100mm
CONNECTORS:
J01= DEMA-9P From DPU Prime to PDU Prime
J02= DEMA-9P From DPU Red. to PDU Red.
J03= DEMA-9S From DPU Prime to Bus A
J04= DEMA-9S From DPU Prime to Bus B
J05= DEMA-9S From DPU Red. to Bus A
J06= DEMA-9S From DPU Red. to Bus B
J07= DBMA-25P From DPU Prime to DCU Prime
J08= DBMA-25P From DPU Prime to MCU Prime, part of FCU Prime
J09= DBMA-25P From DPU Prime to SCU Prime, part of FCU Prime
J10= DBMA-25P From DPU Red. to DCU Red.
J11= DBMA-25P From DPU Red. to MCU Red., part of FCU Red.
J12= DBMA-25P From DPU Red. to SCU Red., part of FCU Red.
UPDATED: 29/01/2002 P. Baldetti
UPDATED: 16/01/2002 P. Baldetti
Consiglio Nazionale delle Ricerche
ISTITUTO di FISICA dello SPAZIO INTERPLANETARIO
data 5/04/2001
proj. Baldetti
Progetto: HERSCHEL- HSDPU
HSDPU AVM
HER 503302

4 DPU/ICU Mass Breakdown

4.1 Boards

BOARD	PACS (g)	HIFI (g)	SPIRE (g)
CPU (2 of)	960	960	960
I/F Board (2 of)	640	640	640
DC/DC (2 of)	1200	1580	1200
Motherboard	520	520	520
SUBTOTAL	**3320**	**3700**	**3320**

4.2 Box

Box Component	Weight (g)
Base-Plate	1071
Front Wall	230
Front Wall Connectors(delta: Estimated)	150
Back Wall	230
Lateral Walls (2 of)	988
Cover	368
SUBTOTAL	**3037**

4.3 Other Components

Component	Weight (g)
Screws etc. (E)	100
Cabling (E)	300
Conformal Coating (60g/Board: E)	420
SUBTOTAL	**820**

4.4 Total Weights

The weights are inferred from the actual AVM measurements.
We can assume the total to be within + - 200 g.

Component	PACS (g)	HIFI (g)	SPIRE (g)
Boards	3320	3700	3320
Box	3037	3037	3037
Other	820	820	820
TOTAL	**7177**	**7557**	**7177**

4.5 Electrical I/F

4.5.1 Telemetry and Telecommand

The DPU interfaces with the S/C TM and TC subsystems (CDMS) with a redundant couple of wires implementing the MIL-STD 1553 B in the long stub configuration (transformers coupling). Each DPU section (prime and redundant) is connected to both prime and redundant bus lines, as shown in Fig 3.2

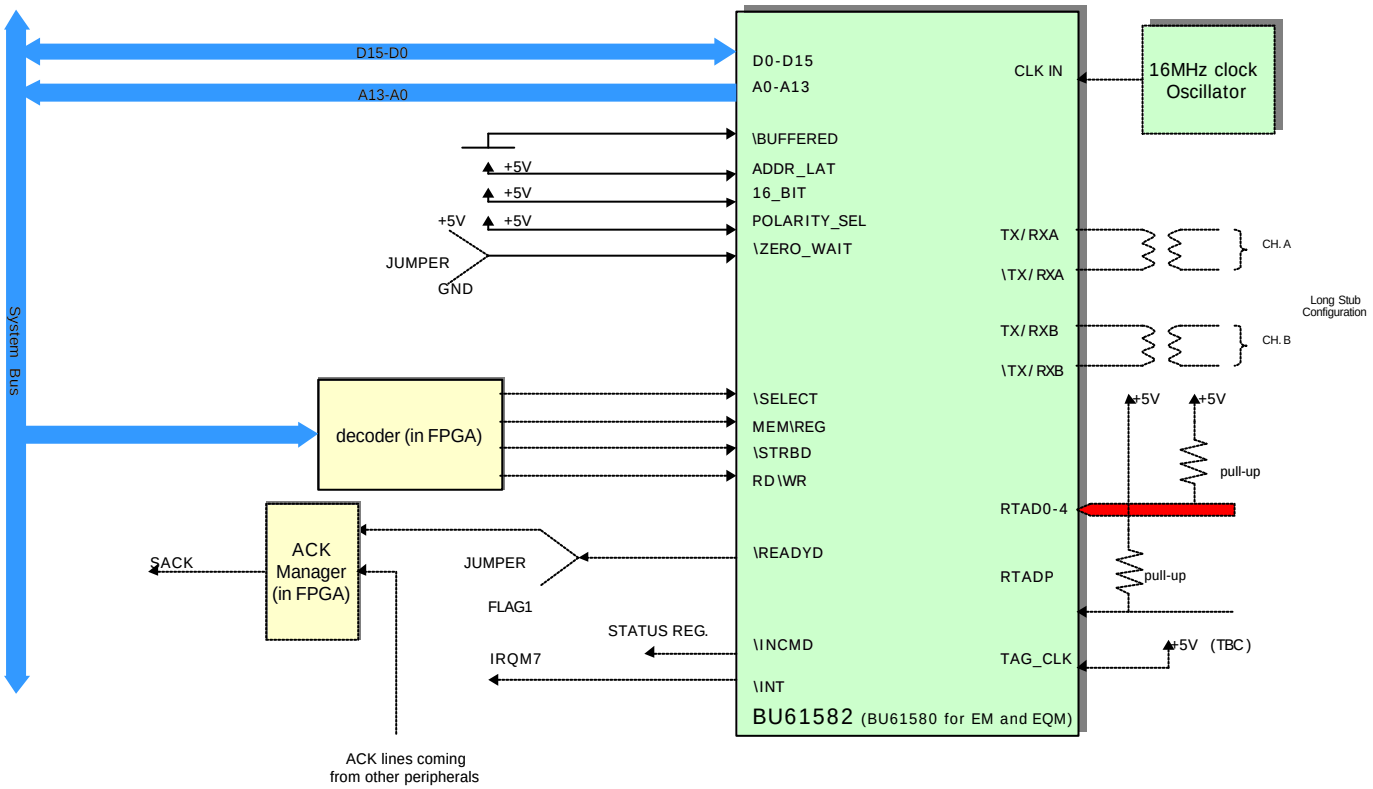


Figure 4-1 Detailed DPU Spacecraft interface

The nominal bit rate is 100 Kbps with a burst mode of 300 Kbps (TBC).

5 DPU/ICU Power

5.1.1 Introduction

The following sections are intended to provide the power budget of the DPU/ICU for the three instruments HIFI, PACS and SPIRE, part of a section will be dedicated to the HIFI FCU subsystem that is powered by a DC/DC converter resident in the ICU.

The DPU/ICU gets the power trough the 28 V wire redundant power lines, separated for DPU/ICU DC/DC converter prime and DC/DC converter redundant. A S/C command decides which DPU/ICU is operated with the other in cold stand-by mode.

The power indicated is mostly drained by CMOS digital integrated circuits for which the power consumption is a function of the switching frequency. For most of the components, then, and especially for the most power hungry ones, the exact power consumption will not be known that after the full software is working, especially the software related to the fast serial data acquisition from the subsystems.

It is recalled that the DPU/ICU box will contain two complete units and that the only common board is the motherboard, where in any case all signals of the two units are completely separated. It is also recalled that all the boards will be designed and manufactured by CGS under a contract CGS-ASI.

Each unit will consist (besides the single motherboard) of:

- CPU board
- Interface board
- DC/DC Converter board.

It is also recalled that, in the case of HIFI, one DC/DC converter board will contain two DC/DC converters: one converter for the ICU and one converter for the FCU. In the other cases, i.e. for SPIRE and PACS the nominal (or prime) DC/DC converter board and the redundant DC/DC converter board will host only the converter for the DPU.

5.2 Power breakdown

5.2.1 CPU board power breakdown

In the following table the CPU board power breakdown is shown.

HSO/FIRST-DPU: CPU Board Power Budget [Watt]								
Item	**+5V & 2.5V**		**+15V**		**-15V**		**Duty cycle %**	**Power Supply**
	Nominal	**Peak**	**Nominal**	**Peak**	**Nominal**	**Peak**	**Nominal**	**Nominal**
DSP	1,5	2	0	0	0	0	100	**1,5**
DPR	2	3,2	0	0	0	0	10	**0,2**
TSS901	0,6	1	0	0	0	0	10	**0,06**
SRAM @1MHz	6	6	0	0	0	0	80	**4,8**
EEPROM	0,1	0,5	0	0	0	0	100	**0,1**
Glue logic	1	1	0	0	0	0	80	**0,8**
FPGA	0,125	0,25	0	0	0	0	100	**0,125**
Total	**11,32**	**13,95**	**0**	**0**	**0**	**0**		**7,58**

The power budget is strongly depending on the duty cycle of the various components, but the final power figure can be considered close to the actual one, approaching 7.6 W at the secondary power lines.

5.2.2 Interface board power breakdown

In the following table the interface board power breakdown is shown.

HSO/FIRST-DPU: PL I/F Board [Watt]								
Item	**+5V**		**+15V**		**-15V**		**Duty cycle %**	**Power Supply**
	Nomin.	**Peak**	**Nomin.**	**Peak**	**Nomin.**	**Peak**	**Nomin.**	**Nomin.**
BU61582	0,7	1,2			3,45	3,825	100	**4,15**
FIFO	0,09	9,9					100	**0,09**
RS422 Receiv.	0,3	0,4					80	**0,24**
RS422 Transm.	0,9	1					80	**0,72**
Analog Section	0,15	0,2	0,111	0,181	0,33	0,535	40	**0,23**
Glue logic DC	1	1					80	**0,8**
Glue logic AC	0,4	0,6					80	**0,32**
FPGA	0,125	0,25					100	**0,125**
	3,66	**18,15**	**0,111**	**0,181**	**3,78**	**4,36**		**6,67**

The power budget is strongly depending on the duty cycle of the various components, and the final power figure can not be considered close to the actual one (with the exception of PACS, as explained later on), as the duty cycle of various components in not well defined yet and it is very much depending on the FIFO use, i.e. the data gathering on the fast serial links from the subsystems to the DPU.

It is to put in evidence that the FIFO are present only in HIFI and SPIRE that have the same monodirectional fast serial links, while in the case of PACS the serial links among the various subsystems are according to the MIL-STD 1355 DS-DE. In the PACS case this standard high speed serial circuit is implemented by a special chip (TSS901) whose peak power drain is 1 W and it is located in the CPU board.

In strict terms, as this chip is not used (and not mounted!) in the case of SPIRE and HIFI, the estimated 0.06 W can be taken out from the CPU power breakdown for these two instruments.

5.2.3 Power losses breakdown

In the next table the estimated power losses are shown for the various DC/DC converter components. These power losses ca be considered close to the actual ones and hence the 70% efficiency of the DC/DC converters will be likely achieved.

Item	Voltage	Current	Rect losses	Switching losses	Postregulation losses	Control losses	Total losses	Power	Efficiency
Main bus	28			1,47			1,47		70,4%
Out 1	5	3,00	2,40				2,40	15,00	
Out 2	15	0,15	0,12		0,45		0,57	2,25	
Out 3	15	0,15	0,12		0,45		0,57	2,25	
Startup	12	0,02				0,56	0,56		
Self supply	15	0,10				1,50	1,50		
Snubber				0,74			0,74		
Transformer				0,39			0,39		
HIFI option									
Main bus	28			1,47			1,47		70,7%
Out 1 reg	5	0,20	0,16		0,40		0,56	1,00	
Out 2 reg	16	0,50	0,40		1,00		1,40	8,00	
Out 3 reg	16	0,50	0,40		1,00		1,40	8,00	
Out 1	8	0,05	0,04		0,15		0,19	0,40	
Out 2	18	0,08	0,06		0,24		0,30	1,44	
Out 3	18	0,08	0,06		0,24		0,30	1,44	
Self supply	15	0,10				1,50	1,50		
Snubber				0,74			0,74		
Transformer				0,41			0,41		

Main bus switching losses = primary mos
Snubber switching losses = primary snubber
Transformer switching losses = 98% of delivered power
Posregulation losses = 2V (1834); 3V (LM117)

5.2.4 Total power budget

In the following table all the figures are shown leading to the overall power budget for the three instruments.

	Power1 (W)	Power2 (W)	Total (W)
PACS DPU	14.2	20.3	**25.4**
SPIRE DPU	14.2	20.3	**25.4**
HIFI ICU	14.2	20.3	**25.4**
HIFI FCU	23.8	34	**42.5**

Power1 : the power drained on the secondary power lines.

Power2: the power drained on the primary power lines (+ - 28 V) including a DC/DC converter efficiency of 70%.

Total: The total power including a contingency of 25%.

5.2.5 DC/DC Synchronisation

Each DPU DC/DC converter is free running at 131 kHz + - 10% via an internally generated synchronisation signal.

6 Connectors and pin functions

From the prime DPU there will be 3 Cannon DEMA 9 ways connectors respectively to prime CDMS "A", prime CDMS "B" and prime PDU. The same will apply to the redundant DPU so that a total of 6 connectors and 6 cables will be used to electrically connect the DPU to the spacecraft.

6.1.1 DPU to PDU Prime Power Bus

Unit DPU
Connector ID J01
Connector type DEMA9P
Connector name TO PDU_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	28_V_P		AWG26	PDU P		
3						
4	PWR_RET_P		AWG26	PDU P		
5						
6						
7	28_V_P		AWG26	PDU P		
8						
9	PWR_RET_P		AWG26	PDU P		

6.1.2 DPU-Prime to CDMS-Prime 1553B Bus A

Unit DPU
Connector ID J03
Connector type DEMA9S
Connector name FM P_CMDS_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	Bus + A		AWG26	CDMS P		
3						
4						
5						
6	Bus - A		AWG26	CDMS P		

7						
8						
9						

6.1.3 DPU-Prime to CDMS- Prime 1553B Bus B

Unit DPU
Connector ID J04
Connector type DEMA9S
Connector name FM R_CMDS_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	Bus + B		AWG26	CDMS P		
3						
4						
5						
6	Bus - B		AWG26	CDMS P		
7						
8						
9						

6.1.4 DPU to PDU Redundant Power Bus

Unit DPU
Connector ID J02
Connector type DEMA9P
Connector name TO PDU_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	28_V_R		AWG26	PDU R		
3						
4	PWR_RET_R		AWG26	PDU R		
5						
6						
7	28_V_R		AWG26	PDU R		
8						
9	PWR_RET_R		AWG26	PDU R		

6.1.5 DPU-Redundant to CDMS-Redundant Bus A

Unit DPU
Connector ID J05
Connector type DEMA9S
Connector name FM P_CMDS_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	Bus + A		AWG26	CDMS R		
3						
4						
5						
6	Bus - A		AWG26	CDMS R		
7						
8						
9						

6.1.6 DPU-Redundant to CDMS-Redundant Bus B

Unit DPU
Connector ID J06
Connector type DEMA9S
Connector name FM R_CMDS_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	Bus + B		AWG26	CDMS R		
3						
4						
5						
6	Bus - B		AWG26	CDMS R		
7						
8						
9						

7 DPU - Subsystems interfaces

7.1 General Information

The DPU interacts with the subsystems via dedicated low speed bidirectional and high speed mono-directional serial interfaces.
The two physical subsystem units are logically divided into three independent units each connected to the DPU with one high speed and one low speed interface.
Both the DPU and the S/S (interfaces) are fully redundant, so that the total number of serial interfaces is 12.

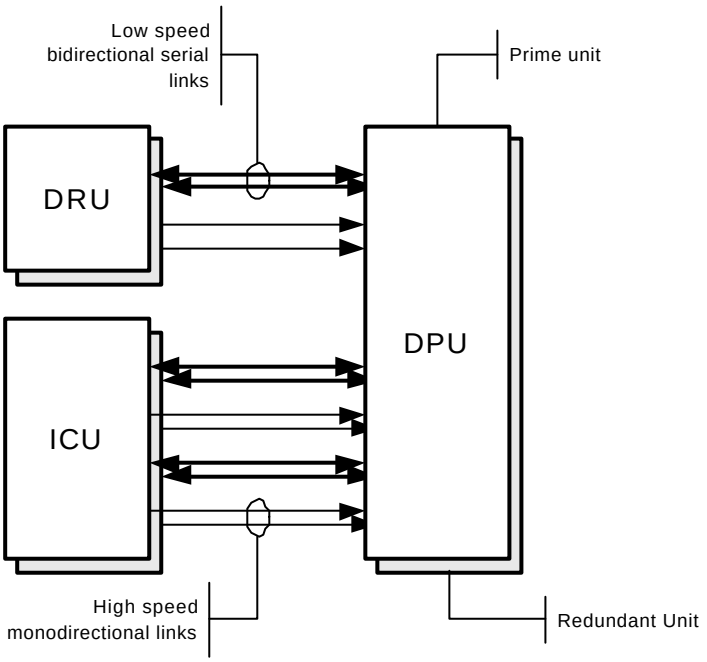


Figure 7-1 DPU - Subsystems Interfaces schematic view

All interfaces adopt the balanced line drivers and receivers as shown in figure 4-2.

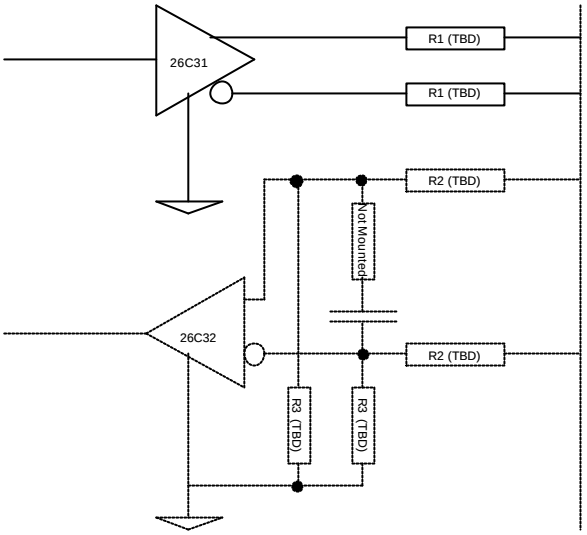


Figure 7-2 Balanced line drivers and receivers

7.2 Low Speed Interface

The low speed bidirectional I/F is organized as a bus with the DPU acting as controller so that all data transactions with the subsystem are initiated by DPU.
The low speed interface protocol is shown in figure 4-3.

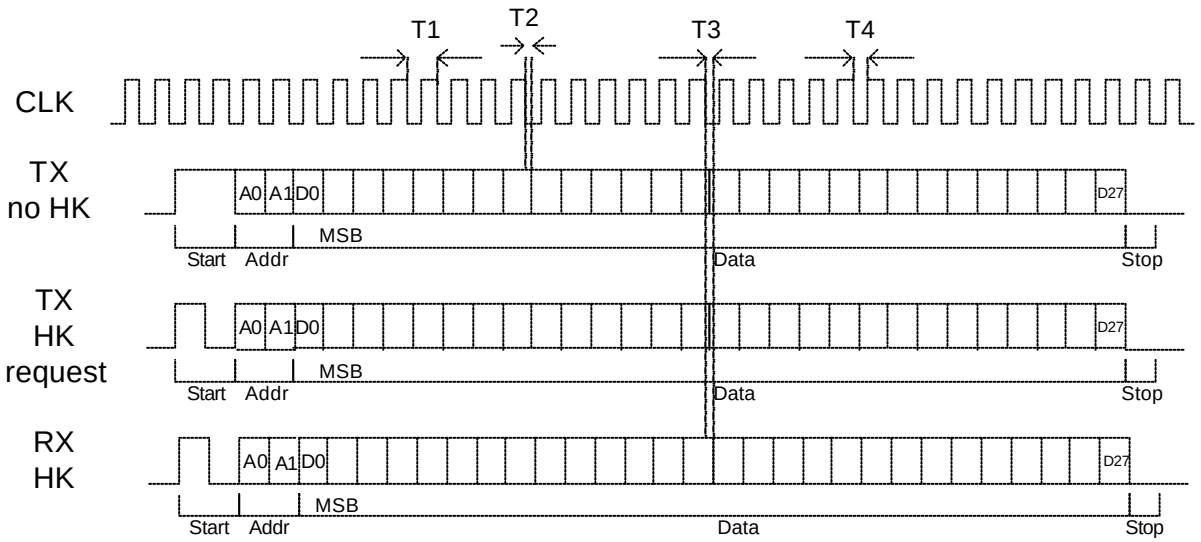


Figure 7-3 Low speed interface protocol

With reference to the figure, the tolerances on the indicated time parameters are:

Parameter	Min. Value	Max. Value	Unit

T1	3.17	3.23	µs
T2	-30 nS	0.7	µs
T3	0	1.2	µs
T4	1.53	1.66	µs

Commands sent by the DPU via the TX lines are always received by all the subsystems, the address field of the command word selecting the relevant unit. One address is reserved as a broadcast command. The subsystem addressing is made according to the following table:

A0	A1	Subsystem
0	0	DCU
0	1	MCU
1	0	SCU
1	1	Broadcast

The DPU can send both commands and/or HK requests as signalled by the second start bit of the command word. When requested, the subsystems will send responses via the RX line.

A command is made of 2 start bits, 2 address bits, 28 data bits and 1 stop bit.
A HK request is issued by setting the second start bit according to the following table:

Start0	Start1	HK
1	1	No
1	0	Yes

The HK response will have the same form of the requesting command, the address field indicating the originating subsystem.

The command word data field can be subdivided in every way, the baseline is shown in the following table:

From	To	Description
D0	D7	Command identifier
D8	D27	Command parameters

As the selection of the input RX channel is done by the sub-unit address field of the last TX command sent, no command can be sent to a different sub-unit until the last HK RX corresponding to the last command sent is received. Figure 4-4 shows the transmission reception sequence.

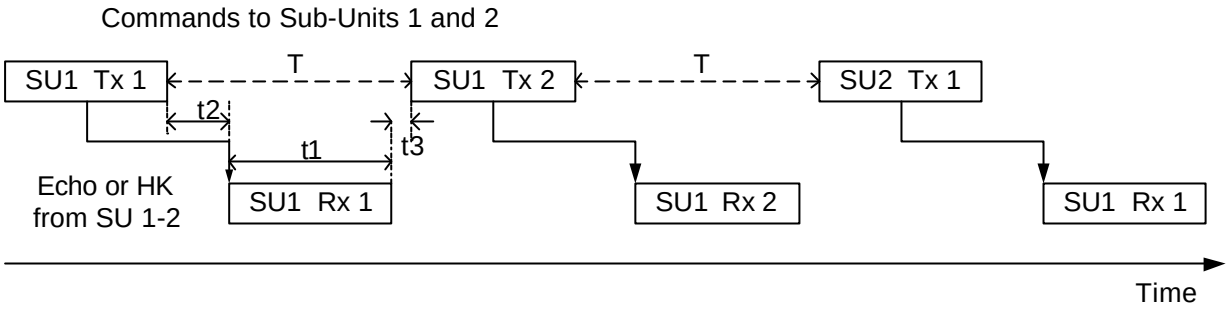


Figure 7-4 Low speed interface – transmission reception protocol

In order to avoid system lock a 2 ms timeout **TO** is defined. In any case, a new HK request cancels the previous request whether already sent or not.

The following table shows the timing requirements with and without HK request.

Parameter	**Min value [us]**	**Max value [us]**	**Description**
TO	2000	2500	Time-Out
t1	101	104	Command word length
t2	6.4	500 TBC [RD3]	HK response time
t3	10	NA	Time to next command
T	10	NA	No HK request
T	Minimum value between (t1+t2+t3) and TO		With HK request

The DPU side of the low speed I/F is shown in figure 4-5. The DPU originated clock line has a fixed frequency of 312.5 kHz. The clock signal generated by DPU is distributed to all subsystems and can be used for synchronisation purposes, after a dedicated broadcast command is issued (see section 4.4).

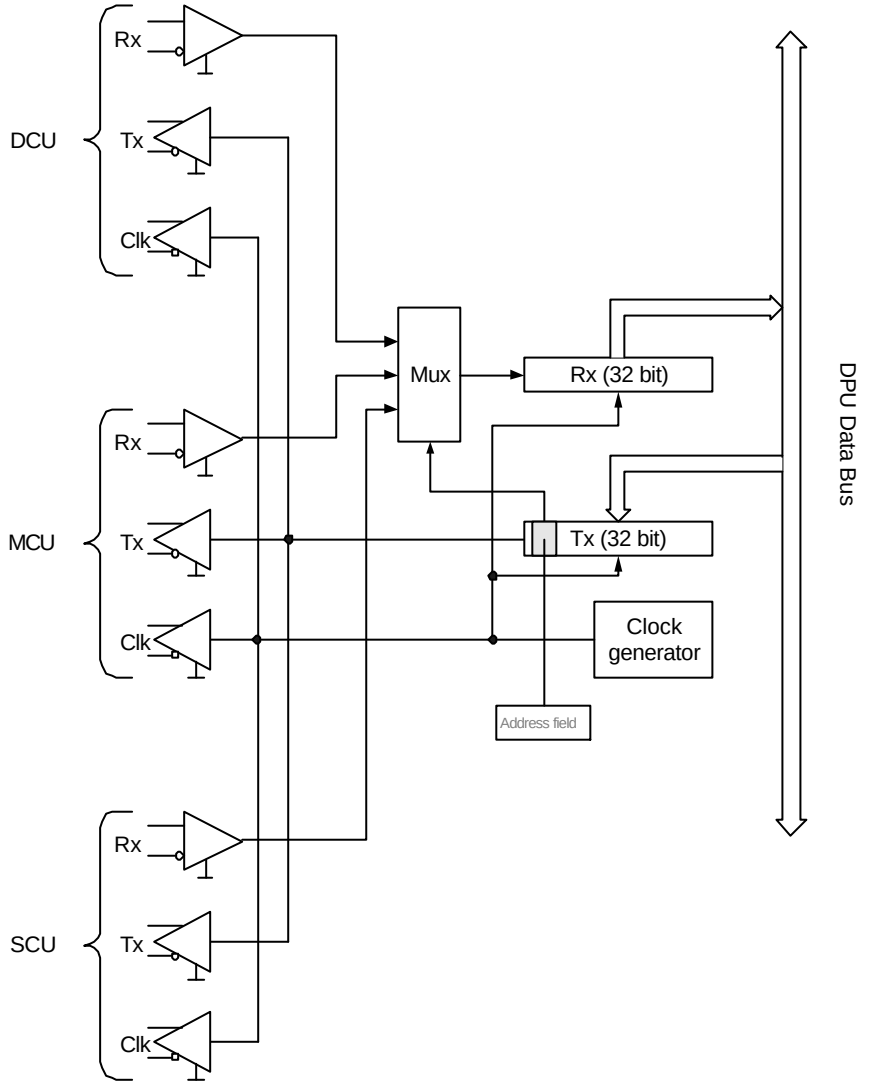


Figure 7-5 Detailed bi-directional low speed interface

The detailed subsystems commands lists are reported in sections 5 and 6.

7.3 High Speed Interface

The high speed data link (science data link) is made by three monodirectional fast synchronous serial input interfaces, each of which with 8 KW 16 bits FIFO. The FIFOs half full signal generates an interrupt on the DSP. Three independent interfaces are required since simultaneous data transfer can occur.
The high speed I/F will transfer data from ICU/DRU sub-units to DPU as 16 bit words using a clock up to 2.5 MHz (baseline 1 MHz). Being the interface unidirectional, all signals are generated by ICU/DRU.

The DPU side of the 3 high speed I/F is shown in the following figure:

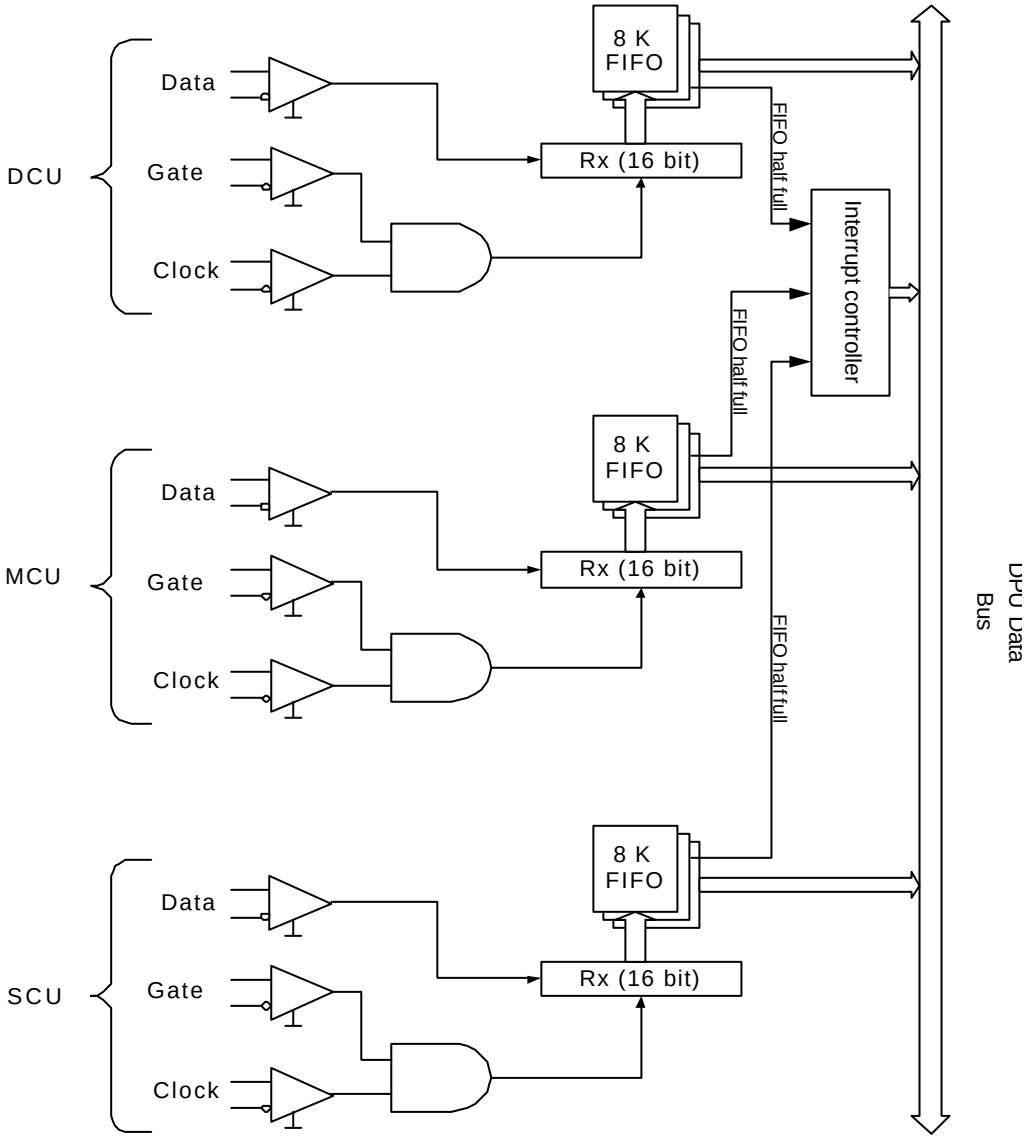


Figure 4-6 Detailed monodirectional high speed interface

The clock, gate and data signals coming from the subsystems are as in figure 4-7.

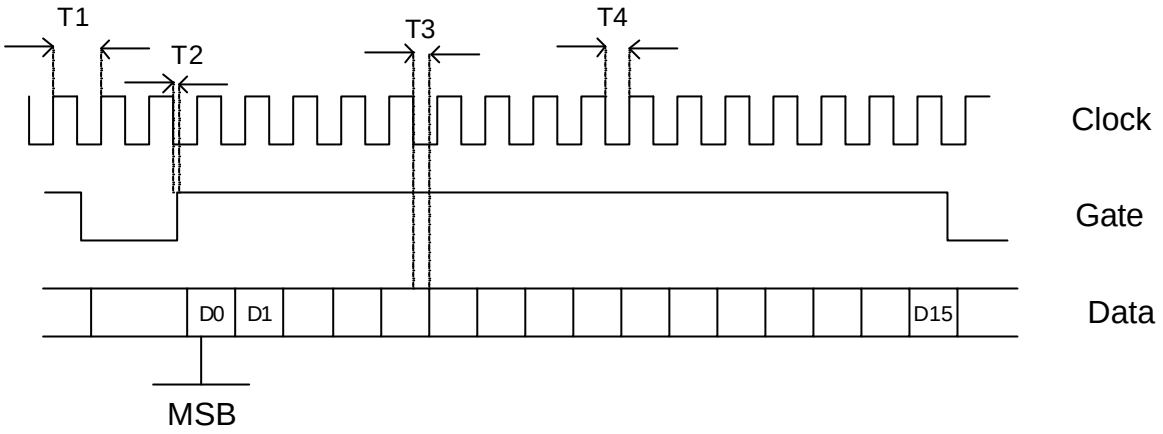


Figure 7-7 High speed interface protocol

Signal lines are defined as in figure. The tolerances on the indicated time parameters are:

Parameter	Min. Value	Max. Value	Unit
T1	400	1010	ns
T2	-30	T4-130	ns
T3	-30	T4-130	ns
T4	(T1)/2 – 10%	(T1)/2 + 10%	ns

The SPIRE clock frequency is 1 MHz.

7.4 DRU/ICU data

The SPIRE telemetry parameters can be split into two types:

1. **Science Parameters**: detector data plus those data required to process the detector data.
2. **Housekeeping parameters**: data required to monitor the configuration and health and safety status of the instrument.

Housekeeping parameters are provided on the *Low Speed RX* data line from DRU and ICU to the DPU in response to a HK request . Each request will return one or more data values within a 32 bit word. 28 bits are available for data.
The DPU will request the housekeeping data from the DRU/ICU subsystems at regular intervals (1sec typical) and place them, along with the DPU parameters into a single housekeeping TM packet. There will be a single instance of each housekeeping parameter in a housekeeping TM packet. In the case of a value being invalid, the OBS will set a flag in the Housekeeping indicating this.

Science parameters are provided on the *High Speed data lines* from DRU and ICU to the DPU following a request for data issued on the Low Speed data line. The science information is provided in the form of frames containing a fixed set of science parameters.

The number of frame types per subsystems is:

- DCU: 10 (test pattern, all photometric arrays, both spectrometer arrays, 5* one detector array, 2 others TBD)
- SCU: 2 (test pattern, all data)
- MCU: 2 (test pattern, delta time + 2 other channels (selectable))

The number of acquisition rates available will be limited to 3 for the MCU and 4 for the DCU and SCU

Each frame is composed of :
- a header word (16bits);
- a frame time (TBD bits – see later)
- a number of data words;
- a check word (16bits)

Both word and frame definitions are subsystem dependent and will be described in sections 5 and 6 (TBW).

The DPU will copy the science data frames into a telemetry packet (including the check word). It will also check the header and the check word with the data in the frame and, if check fails, it will take action to re-synchronize with the data stream (TBC).

7.5 Data acquisition Timing

Each DRU/ICU subsystem maintains its own counter driven by the 312.5 kHz clock provided by the DPU on the low speed interface. Thus the counters remain in synchronization at all times and can provide the time to an accuracy of ~3 microseconds.

The counters are reset to 0 by a command from the DPU, which is broadcast to all three subsystems at the same time. Thus the counters should be identical (provided the reset pulse is generated from the received command in the three subsystems in a time that is identical, within <~3 microseconds).
The time taken to reset the counters after the DPU issues the command is not critical, as this is used only to provide a link to the absolute time maintained by the DPU (received from the S/C). The accuracy of this time value is 1000 microsec.
The counters are used to mark each frame with the elapsed time since the last reset command.

Because the frames from the FTS are generated asynchronously with the detector data frames, it is not possible to include data from different subsystems into a single TM packet. The DPU will therefore generate separately:

1. DCU science packets;
2. MCU science packets;
3. SCU science packets;
4. DPU science packets (TBC)

Each TM packet will contain, in addition to the standard header information and the data frames the absolute DPU time of the last counter reset command.

8 Low Speed Data I/F Protocol

8.1 Command Word

At any time after completion of a previous command/response exchange the DPU can send command words to the DRCU subsystems on the CMD line.
The 32-bit command word is divided into 5 fields as defined bellow:

- a 2-bit sync pattern : see table 5.1-a for details
- a 2-bit sub-unit address : see table 5.1-b for details
- a 8-bit command or command + parameter address : see table 5.1-c for details
- a 20-bit parameter when applicable*

*: filled with zero if the command does not require any parameter.

These 4 fields are concatenated as follow to form the 32-bits word:

Figure 5.1-a - Command Word Field Structure

SYN1 - SYN0 : sync. pattern
SSA1 - SSA0 : subsystem address
CID7 to CID0 : command identifier
PAR19 to PAR0 : command parameter*
*: filled with zero if no used

Note : • MSB is transmitted first
• SYN1 = MSB
• PAR0 = LSB

SYN1	SYN0	Response
1	0	Yes
1	1	No

Table 5.1-b - Sync Pattern definition

SSA1	SSA0	Subsystem Name
0	0	DCU
0	1	MCU
1	0	SCU
1	1	Broadcast Command

Table 5.1-c - Subsystem address allocation

CID7	CID6 to CID0
0	command code (0 of 127)
1	parameter address (0 of 127)

Table 5.1-d - Command Identifier Structure

Note: the subsystems do not include any command buffering. If a subsystem is enabled to any reason to execute a command it will reply with a negative acknowledge and the last command is definitively lost.

8.2 Response Word

The response line (HK) enables command verification and DRCU sub-system housekeeping parameters reading by the DPU.

When a "set_parameter" command is received the subsystem responds to the DPU by transferring a command acknowledge word (positive or negative) on the response line. The positive acknowledgement is required for further command transfer after specific critical commands. When a "get_parameter" command is received the subsystem responds to the DPU by transferring the requested housekeeping parameter(s). (Housekeeping parameter polling is running typically at 1Hz).

The sub-system shall respond (leading bit of the response word) within a maximum delay of tbd clock periods (t2– see §4.2). The DPU S/W shall include a time-out in order to recover from a lack of response and then report the anomaly.

The 32-bit command response is divided into 3 fields, which are:

- a 2-bit sync pattern (SYN0 & SYN1),
- a 8-bit command or parameter address echo (CID7 to CID0),
- a 20-bit parameter (PAR19 to PAR0) or acknowledge code.

These 3 fields are concatenated as follow to form the 32-bits word:

SYN1-SYN0	00	CID7 to CID0	PAR19 to PAR0

If the subsystem address corresponds to the broadcast address the subsystems do not generate any response word to avoid collision at the DPU end.

A "negative" acknowledge (specific parameter field) may result from the following reasons:

- DRCU or DRCU subsystem is off
- A transmission error occurred: receiver does not recognise command identifier
- A command is not allowed in a specific subsystem status (e.g. modification of FTS scan length when mechanism is scanning

8.3 Command list

8.3.1 DCU specific command list

Command Name	Command Code	Arguments	Range List	Command verification
Set_photo_bias_freq		Channel id. Frequency divider	NA 64 to 511	?
Set_spectro_bias_freq		Channel id. Frequency divider	NA 64 to 511	?
Set_photo_bias_ampl		Channel id. Sine amplitude	0 to 3 0 to 255	?
Set_spectro_bias_ampl		Channel id. Sine amplitude	0 to 1 0 to 255	?
Set_photo_JFET_Vss		Channel id. Vss voltage	0 to 11 0 to 255	?
Set_spectro_JFET_Vss		Channel id. Vss voltage	0 to 2 0 to 255	?
Set_photo_JFET_pwr		On/Off word	See note x	?
Set_spectro_JFET_pwr		On/Off word	See note xx	?
Set_photo_heater_pwr		Channel id. On/off	NA	
Set_photo_heater_pwr		Channel id. On/off	NA	
Set_spectro_heater_pwr		Channel id. On/off	NA	
Set_photo_offset		Channel id. Offset value	0 to 287 0 to 7	
Set_spectro_offset		Channel id. Offset value	0 to 71 0 to 7	
Set_data_mode		Mode: 0 to 9	Test Pattern Photo. Offset Spectro. Offset Photo. Bolo. Spectro. Bolo. Photo. PLW Photo. PMW Photo. PSW Spectro. SLW Spectro. SSW	?
Set_multiple_frames		Nber of frames Frame Rate Divider	1 to 255 0 for continuous 1 to 255	
Command Name	Command Code	Arguments	Range List	Command verification
Start_multiple_frames		Start / Stop		

Get_single_frame		NA		
Get_hk_channel		Channel id.	See AD2	
Reset_time_counter		NA	Broadcast cmd	

Note x: on/off word bit allocation is defined as follows: TBW

Note xx: on/off word bit allocation is defined as follows: TBW

8.3.2 MCU specific command list

Command Name	Command Code	Arguments	Comment	Command verification
Set_scan_length		Scan length	B0 to B21	?
Set_scan_speed		Scan Speed	B0 to B21 0: position mode	?
Set_SMEC_mode		Mode	Open loop Closed loop w encode Closed loop w back EMF	?
Start_SMEC		Start / Stop	Start: B0 = 1 Stop: BO = 0	?
Set_SMEC_position		Position from home	?	
Set_data_mode		Mode Data Selection	Jiggle / SMEC	?
Get_hk_channel		Channel	Scan length Scan speed Scan mean period SMEC Mode SMEC Position SMEC temp. MAC temp. …	
Reset_time_counter		NA	Broadcast cmd	

8.3.3 SCU specific command list

Command Name	Command Code	Arguments	Comment	Command verification
Set_calibrator_current		Channel id. Current	Photometer Spectro. Flood Spectro. Point 0 to 255	
Set_heater_current		Channel id. Current	SP HS1 HS2 FPU 0 to 255	
Set_therm_on/off		On/Off word	See note xxx	
Set_S/S_pwr_on/off		On/Off word	See note xxxx	
Set_multiple_frames		Nber of frames Frame Rate	1 to 256 0 for continuous 1 to 256	
Start_multiple_frames		Start / Stop		
Get_single_frame		NA		
Get_housekeeping		Channel id.	See AD2	
Reset_time_counter		NA	Broadcast cmd	

Note xxx: on/off word bit allocation is defined as follows:

Bit weigh	Thermometer channel

Note xxxx: on/off word bit allocation is defined as follows:

Bit weigh	S/S
7 (MSB)	DCU_LIA_P
6	DCU_LIA_S
5	DCU_DAQ
4	DCU_BIAS_P
3	DCU_BIAS_S
2	MCU_MAC
1	MCU_SMEC
0 (LSB)	MCU_BSM

8.4 Constraints on the command sequencing

The purpose of this chapter is to give constraints related to the command sequencing when applicable. Depending of the status of a sub-system following a low-level command, the next command may have to be delayed in order to give chance to the subsystem to execute the command. A typical example corresponds to a cryo-cooler recycling after sending the SP pump heating command. In that case the DPU shall wait before sending the next command the necessarily time to the sorption pump to reach 40 K.

TBW

8.5 Typical commanding scenario

This scenario is given as an example only.

Action	DCU Status	Data Transfer
DCU power-on	DCU default	T3 @ 16 Hz
Set_Bias_amplitude	Configuration	
Set_Bias_Frequency	“	
…		
…		
Start_multiple_frame(stop)	DCU configurated	No data
Set_data_mode(photometer)		
Set_multiple_frames(4,16Hz)		
Start_multiple_frame(start)	“Observing”	T4 @ 16 Hz
…		

Asynchronously with those commands, the DPU will send regularly requests (typically @ 1 Hz - 1 per 1 or 2 parameters) for housekeeping parameters. It will also send the “Set_heater_current” command at the same rate order to achieve FPU temperature stabilisation.

9 High Speed Data I/F Protocol

9.1 General Information

The Data Interface is dedicated to data transfer from subsystem to DPU. Three independent “Data Interface” are required allowing simultaneous DRCU data transfer.
This interface is unidirectional: data are transferred from the DRCU sub-units to the DPU acquisition electronics. Fixed data packets are defined according to sub-unit operating mode.
This data packet contents both scientific data (i.e. bolometer signal) and/or housekeeping parameters.

9.2 Overall Interface Diagram

The Command Interface diagram is given in figure 6.2. Prime and Redundant interfaces are shown.

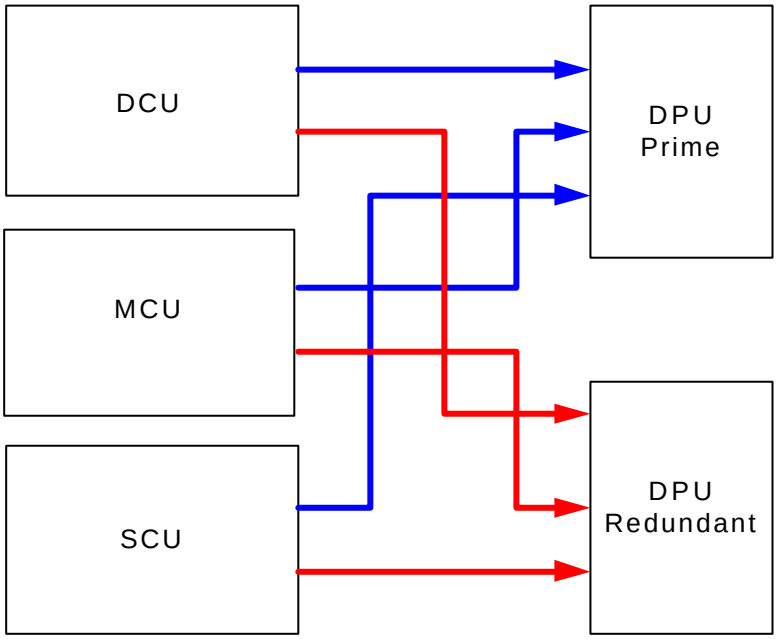


Figure 6.2-a

9.3 Word definition

Word definition is subsystem dependent. Data are currently 16-bit encoded and correspond to bolometer signal, mechanisms motion parameters, instrument temperature and all other housekeeping channels.
In order to deal with the latch-up effect of the analogue to digital converters, which cause the generation of wrong data until the converter recovers full performances, a specific "invalid" data identifier is defined. This avoids the DRCU to transfer unpredictable packet length following a cosmic ray impact on the converter and later on-ground misanalysis.

These data words are defined as follow:

DAT15 to DAT0

Figure 6.3-a - Data Word Definition

DAT15 to DAT0: data

Note: • MSB (DAT15) is transmitted first

9.4 Frame Definition

Data frame length and structure are defined regarding the DRCU sub-unit and its mode of operation. The sub-systems data structures are encapsulated into a common frame structure as described bellow.

The frame is composed of:
- a header word
- a frame time
- a number of data words
- a data structure
- a check word

9.4.1 Header

The "header" field is a 16-bit word placed at the head of the frame. Along with the "length" field and the check word it allows data consistency checking. In case the check fails the DPU takes action to re-synchronize with the data stream. The "header" is itself composed of the following elementary fields:

- header pattern: 1 byte / AA hexadecimal
- ADC latch-up flags: 6 bits /
- 2 spare bits

The purpose of the ADC latch-up flag word is to keep track of an analog to digital converter latch-up event, which affects the integrity of the digitized data. When a flag or more is set the related

data of the current frame have to be discarded during on-ground data processing.
The number significant of flags depends on the data interface mode: 6 corresponding to the "Photo. Full Array" mode. See table above for details

DCU Configuration	FST	# of flags
Photo. Array Subset	T1	1
Spectro. Array Subset	T1	1
Photo. Full Array	T2	6
Spectro. Full Array	T2	2
Test Pattern	T3	0
Photo. Offset table	T2	0
Spectro offset table	T2	0

9.4.2 Frame time

The "frame time" field follows the "header". It is a 32-bit word filled with the contents of the subsystem "time tag" counters. In order to keep data frame synchronization for the 3 subsystems this counter is driving by a single clock signal and reset by a broadcast command. The clock is derived from the CLK line of the Command interface and the resolution is then 3.2 µs. The full range of the counter is then above 13740 s (229 min); this means the DPU have to sent the reset command at least every 229 min in order to keep synchronization between the 3 DRCU sub-systems.
The subsystem time counter shall be effectively reset within 10 (TBC) µs from the command reception and with a maximum skew between subsystems of 3 µs.

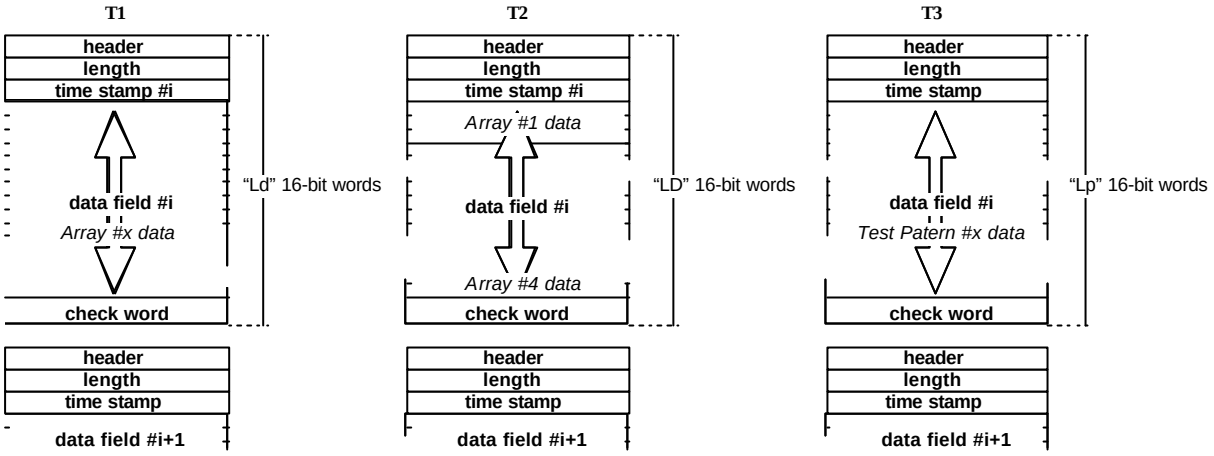
9.4.3 Length

The "length" field (16 bits) follows the "frame time" field. It indicates the number of 16-bit words of the frame (including all the fields). Along with the "header" and "check word" fields this field allows frame consistency checking by the receiver unit.

9.4.4 Data structure

9.4.4.1 DCU Frames Definition

The four frame structures of the DCU are defined as follows:



The following cross table shows the corresponding Frame Structure Type for each DCU configuration status:

DCU Configuration	FST	Length
Photo. Array Subset	T1	See Note
Spectro. Array Subset	T1	See Note
Photo. Full Array	T2	301
Spectro. Full Array	T2	69
Test Pattern	T3	301
Photo. Offset table	T2	301
Spectro. Offset table	T2	69

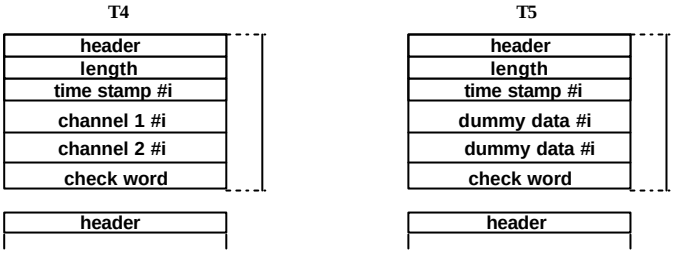
Remind: the DCU data interface configuration is configured by means of the "Set_Data_Mode" command.
Note: Frame length depends on the detector selected subset (Band 1 2 or 3 for photometer and band 1 or 2 for spectrometer).

For the T2 frame length it assumed:

- the photometer is composed of 288 bolometers
- the spectrometer is composed of 56 bolometers
- along ith the imaging bolometers we transfer 8 thermometry bolometers

9.4.4.2 MCU Frame Definition

The two frame structures of the MCU are defined as follows:

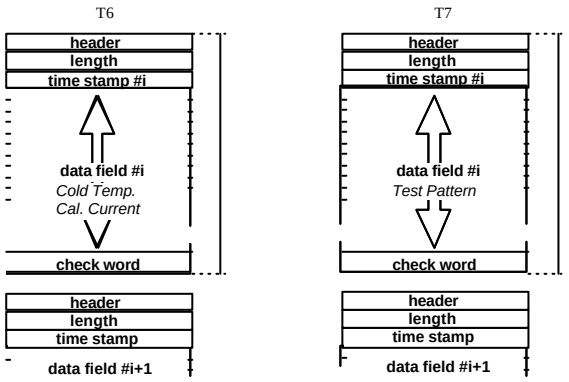


The following cross table shows the corresponding Frame Structure Type for each MCU configuration status:

Configuration Status	FST	Length
Nominal	T4	6
Spectrometer	T5	6

9.4.4.3 SCU Frame Definition

The two frame structures of the SCU are defined as follows:



The following cross table shows the corresponding Frame Structure Type for each SCU configuration status:

Configuration Status	FST	Length
Nominal	T6	
Test Pattern	T7	

9.4.5 Check word

The “check” word ends the data frame. Along with the “header” and “length” field it allows frame consistency checking.

9.5 Test pattern

The purpose of this mode is to generate variable and predictable digital data for test and verification activities. Instead of transmitting a fixed pattern it implements a pseudo random generator.

10 Connectors and pin functions

From the prime DPU there will be 3 Cannon DBMA25P connectors respectively to DCU, MCU and SCU, carrying both low speed and high speed interfaces signals.
The same will apply for the redounded DPU so that a total of 6 connectors and a total of 6 cables will be used to interconnect the subsystems. The connectors and cables pin function are defined in the following tables.

10.1 DPU to DCU - Prime

Unit DPU
Connector ID J07
Connector type DBMA25P
Connector name TO DCU_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	LCLK_DCU_SHD					
2	LCLK_DCU_P+		AWG26	DRU		
3	TX_DCU_P+		AWG26	DRU		
4	RX_DCU_P+		AWG26	DRU		
5	RX_SHD					
6						
7						
8	HCLK_DCU_P+		AWG26	DRU		
9	HCLK_SHD					
10	DAT_DCU_P+		AWG26	DRU		
11	GAT_DCU_P+		AWG26	DRU		
12	GAT_SHD					
13						
14	TX_DCU_SHD					
15	LCLK_DCU_P-		AWG26	DRU		
16	TX_DCU_P-		AWG26	DRU		
17	RX_DCU_P-		AWG26	DRU		
18						
19						
20						
21	HCLK_DCU_P-		AWG26	DRU		
22	DAT_DCU_P-		AWG26	DRU		
23	DAT_SHD					
24	GAT_DCU_P-		AWG26	DRU		
25						

10.2 DPU to MCU - Prime

Unit DPU
Connector ID J08
Connector type DBMA25P
Connector name TO MCU_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	LCLK_MCU_SHD					
2	LCLK_MCU_P+		AWG26	ICU	J08	
3	TX_MCU_P+		AWG26	ICU	J08	
4	RX_MCU_P+		AWG26	ICU	J08	
5	RX_SHD					
6						
7						
8	HCLK_MCU_P+		AWG26	ICU	J08	
9	HCLK_SHD					
10	DAT_MCU_P+		AWG26	ICU	J08	
11	GAT_MCU_P+		AWG26	ICU	J08	
12	GAT_SHD					
13						
14	TX_MCU_SHD					
15	LCLK_MCU_P-		AWG26	ICU	J08	
16	TX_MCU_P-		AWG26	ICU	J08	
17	RX_MCU_P-		AWG26	ICU	J08	
18						
19						
20						
21	HCLK_MCU_P-		AWG26	ICU	J08	
22	DAT_MCU_P-		AWG26	ICU	J08	
23	DAT_SHD					
24	GAT_MCU_P-		AWG26	ICU	J08	
25						

10.3 DPU to SCU - Prime

Unit DPU
Connector ID J09
Connector type DBMA25P
Connector name TO SCU_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	LCLK_SCU_SHD					
2	LCLK_SCU_P+		AWG26	ICU		
3	TX_SCU_P+		AWG26	ICU		
4	RX_SCU_P+		AWG26	ICU		
5	RX_SHD					
6						
7						
8	HCLK_SCU_P+		AWG26	ICU		
9	HCLK_SHD					
10	DAT_SCU_P+		AWG26	ICU		
11	GAT_SCU_P+		AWG26	ICU		
12	GAT_SHD					
13						
14	TX_SCU_SHD					
15	LCLK_SCU_P-		AWG26	ICU		
16	TX_SCU_P-		AWG26	ICU		
17	RX_SCU_P-		AWG26	ICU		
18						
19						
20						
21	HCLK_SCU_P-		AWG26	ICU		
22	DAT_SCU_P-		AWG26	ICU		
23	DAT_SHD					
24	GAT_SCU_P-		AWG26	ICU		
25						

10.4 DPU to DCU - Redundant

Unit DPU
Connector ID J10
Connector type DBMA25P
Connector name TO DCU_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	LCLK_DCU_SHD					
2	LCLK_DCU_P+		AWG26	DRU		
3	TX_DCU_P+		AWG26	DRU		
4	RX_DCU_P+		AWG26	DRU		
5	RX_SHD					
6						
7						
8	HCLK_DCU_P+		AWG26	DRU		
9	HCLK_SHD					
10	DAT_DCU_P+		AWG26	DRU		
11	GAT_DCU_P+		AWG26	DRU		
12	GAT_SHD					
13						
14	TX_DCU_SHD					
15	LCLK_DCU_P-		AWG26	DRU		
16	TX_DCU_P-		AWG26	DRU		
17	RX_DCU_P-		AWG26	DRU		
18						
19						
20						
21	HCLK_DCU_P-		AWG26	DRU		
22	DAT_DCU_P-		AWG26	DRU		
23	DAT_SHD					
24	GAT_DCU_P-		AWG26	DRU		
25						

10.5 DPU to MCU - Redundant

Unit DPU
Connector ID J11
Connector type DBMA25P
Connector name TO MCU_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	LCLK_MCU_SHD					
2	LCLK_MCU_P+		AWG26	ICU		
3	TX_MCU_P+		AWG26	ICU		
4	RX_MCU_P+		AWG26	ICU		
5	RX_SHD					
6						
7						
8	HCLK_MCU_P+		AWG26	ICU		
9	HCLK_SHD					
10	DAT_MCU_P+		AWG26	ICU		
11	GAT_MCU_P+		AWG26	ICU		
12	GAT_SHD					
13						
14	TX_MCU_SHD					
15	LCLK_MCU_P-		AWG26	ICU		
16	TX_MCU_P-		AWG26	ICU		
17	RX_MCU_P-		AWG26	ICU		
18						
19						
20						
21	HCLK_MCU_P-		AWG26	ICU		
22	DAT_MCU_P-		AWG26	ICU		
23	DAT_SHD					
24	GAT_MCU_P-		AWG26	ICU		
25						

10.6 DPU to SCU - Redundant

Unit DPU
Connector ID J12
Connector type DBMA25P
Connector name TO SCU_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	LCLK_SCU_SHD					
2	LCLK_SCU_P+		AWG26	ICU		
3	TX_SCU_P+		AWG26	ICU		
4	RX_SCU_P+		AWG26	ICU		
5	RX_SHD					
6						
7						
8	HCLK_SCU_P+		AWG26	ICU		
9	HCLK_SHD					
10	DAT_SCU_P+		AWG26	ICU		
11	GAT_SCU_P+		AWG26	ICU		
12	GAT_SHD					
13						
14	TX_SCU_SHD					
15	LCLK_SCU_P-		AWG26	ICU		
16	TX_SCU_P-		AWG26	ICU		
17	RX_SCU_P-		AWG26	ICU		
18						
19						
20						
21	HCLK_SCU_P-		AWG26	ICU		
22	DAT_SCU_P-		AWG26	ICU		
23	DAT_SHD					
24	GAT_SCU_P-		AWG26	ICU		
25						