Mechanism Control Unit

Design Description

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Acronyms

AD	Applicable Document
AVM	Avionics Model
BOL	Begin Of Life
BSM	Beam Steering Mirror
CQM	Cryogenic Qualification Model
EGSE	Electrical Ground Support Equipment
EOL	End of Life
ESA	European Space Agency
FIRST	Far Infra Red and Sub-millimeter Telescope
FM	Flight Model
FPU	Focal Plane Unit
FTS	Fourier Transform Spectrometer
FTSE	FTS warm Electronics
FTSP	FTS Preamplifier for the position encoder signals
H/K	House Keeping
H/W	Hardware
I/F	Interface
LAM	Laboratoire Astrophysique de Marseille
MAC	Multi Axes Controller
MCU	Mechanism Control Unit
N/A	Not Applicable
RAL	Rutherford Appleton Laboratory
RD	Reference Document
ROE	Royal Observatory of Edinburgh
S/C	Spacecraft
SM	Spare Model
SMEC	Spectrograph MEChanism
S/W	Software
TBC	To Be Confirmed
TBD	To Be Define
TBW	To Be Written
TC	Tele-Command
TM	TeleMetry
WE	Warm Electronics

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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

The purpose of this document is to describe the electronics design for the control and monitoring of the HERSCHEL/SPIRE FTS scan mechanism (**SMEC**) associated with the Beam Steering Mirror mechanism (**BSM**) control.
The control electronics unit of the 2 mechanical subsystems is called **MCU (Motorization Control Unit).**

The **MCU** is part of the **DRCU** and has electrical (Main Power Supplies) and mechanical (Electronics Cabinet) interfaces with it.

1.2 APPLICABLE AND REFERENCE DOCUMENTS

1.2.1 Applicable documents

AD1	Operating Modes for the SPIRE Instrument (SPIRE-RAL-DOC-000320)
AD2	FIRST/Planck Packet Structure Interface Control Document (SCI-PT-IF-07527)
AD3	Spire Spectrometer Mirror Mechanism Subsystem Specification (SPIRE-LAM-PRJ-000460)
AD4	FIRST / Planck Instrument Interface Document Part B (SCI-PT-IIDB/SPIRE-02124)
AD5	DRCU Electrical Interface Control Document (SAp-SPIRE-CCa-24-00)
AD6	SPIRE Instrument Requirements Specification (IRD) (SPIRE-RAL-PRJ-000034)
AD7	DPU Interface Control Document SPIRE-IFS-PRJ-000650 2 April 2001 Issue 1.0

1.2.2 Reference documents

RD1	Beam Steering Mirror Control Software Requirements (Spire-ATC-Draft)
RD2	Beam Steering Mirror Warm Electronics (Spire-ATC-Draft)
RD3	Beam Steering Mirror Electronics Electrical Interface (Spire-ATC-Draft)

2 SYSTEM OVERVIEW

The **MCU** is dedicated to the control and monitoring of the following 3 axis of the SPIRE instrument:

- the Spectrometer Mechanism (**SMEC**). The control is typically based on a scan at a configurable speed, but can be set-up on the basis of a step position control in case of the step and integrate mode of the instrument.
- the **Chopper** and **Jiggle** axis of the Beam Steering Mirror subsystem . The control is a position step control pattern.

The control of the 3 axis is performed by a 21020 DSP on the basis of trajectory generators and digital PID controllers associated with filtering for notching of mechanism modes. The control parameters are put in memory for configuration purpose by mean of a command line (bi-directional 32 bit/330 kHz synchronous serial line) connected with the DPU. The software shall be based on a master scheduler on the principle of time sharing without the use of a specific multitask kernel. The tasks to be performed shall be called on a software interrupt generated by the inner DSP timer. The software interrupt defines the global sampling time (i.e. the computation cycle) of the DSP tasks @ a programmable rate between 100 us min and 300 us max[1] . At each cycle the following tasks are performed :

- the SMEC control loop task
- the chopper control loop task,
- the jiggle control loop task,
- the communication with the command line and other various internal DSP tasks,
- telemetry packet concatenation and transmission to high rate serial link

2.1 GENERAL ARCHITECTURE

The MCU control electronics includes:

- 2 MAC Boards (prime and redundant): common digital control board including:
  - 1 **21020** DSP
  - 3 DACs for SMECm and BSMm motor control,
  - 1 multiplexed (16 channels) 16 bits ADC for SMEC and BSM analogue signal acquisitions,
  - 8 logical inputs
  - 12 logical outputs.
  - 1 54SX32S ACTEL FPGA for:
    - the bus control for interface with DACs, multiplexed ADC, digital inputs and outputs, and the optical encoder counting and logic. The encoder pulses generated by the encoder electronics are entering an Encoder Unit Interface (Bus control FPGA function) for pulses counting and crude position determination. The incremental position count is done in the FPGA for in order to verify the trajectory controlled by the DSP and acts the role of a watchdog. Furthermore, the Encoder Unit Interface includes error signals generation for whatever problem occurs during the trajectory (limits reached, etc...). If one on the logical signal is high, the DSP is interrupted and put in safe configuration.

    - the communication with DPU high and low rate serial links.

[1] The value of the main servo sampling rate shall depend on the final software load and functions to be performed. In the case of SMEC control, the arctangent computation and potentially the non-linear spline correction increase the software load to an amount which is not completely defined yet.

- 2 SMEC Boards (prime and redundant): analogue electronics for the power amplification of the actuators and acquisition electronics for sensors pre-amplification and conditioning of the SMEC subsystem

- 1 BSM Board: analogue electronics for the power amplification of the actuators and acquisition electronics for sensors pre-amplification and conditioning of both prime and redundant BSM subsystems.

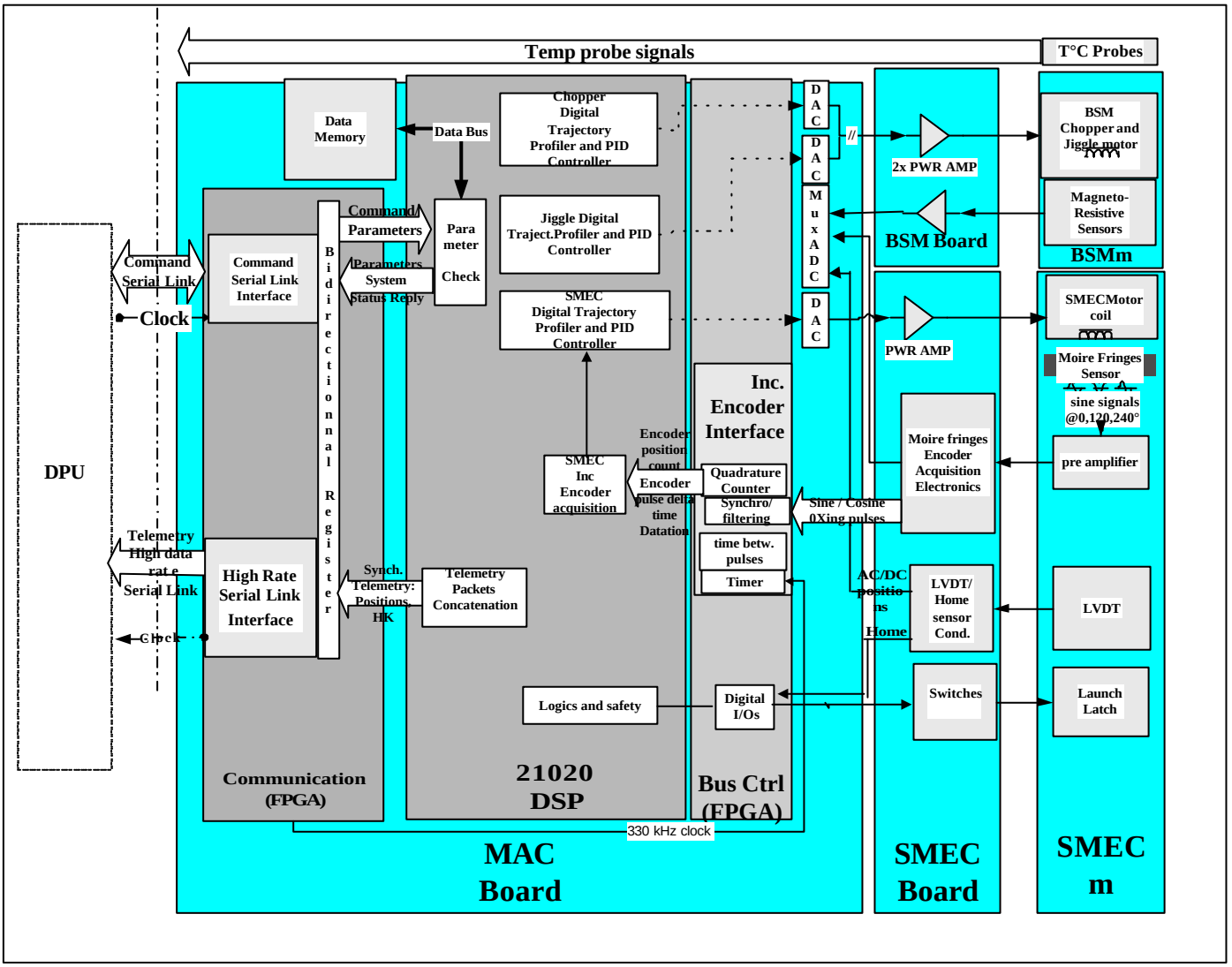

Figure 1: MCU architecture

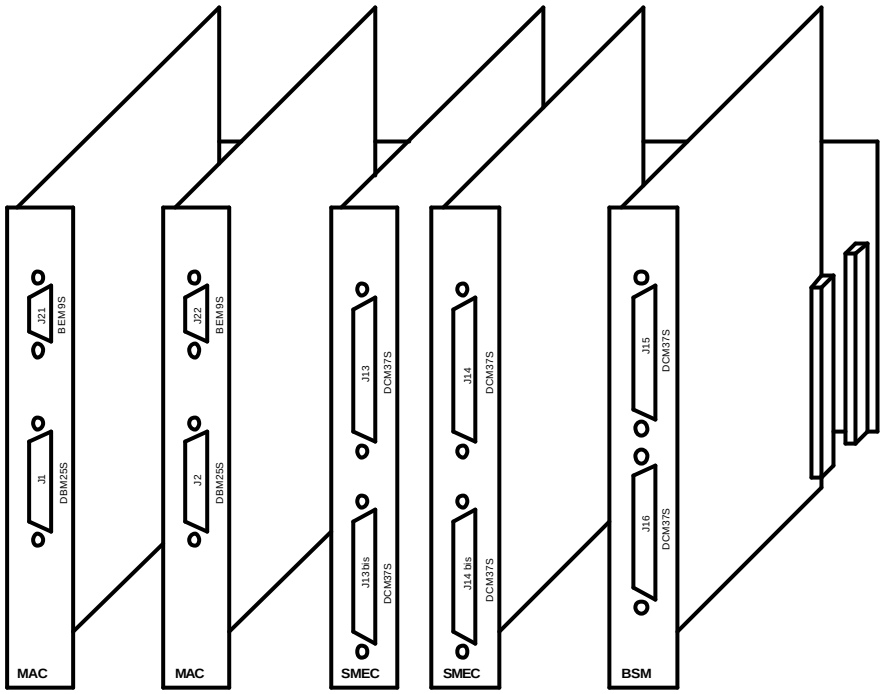

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Figure 2: MCU boards overview

- Dimensions of the MAC, SMEC and BSM boards are 220 x 223 mm² (TBC).
- The two MAC boards, SMEC boards and BSM board are plugged on the same mother board.

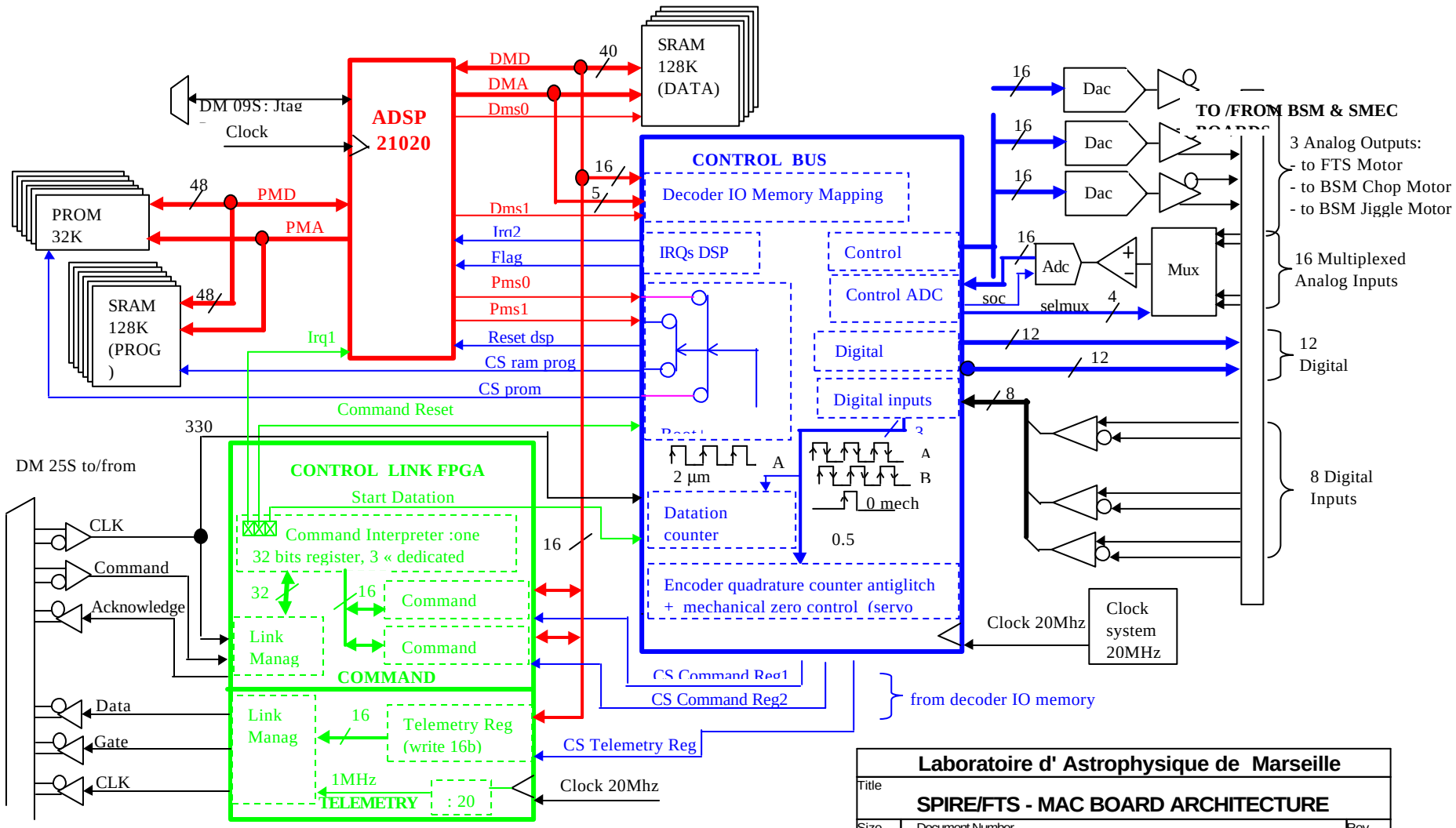

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Figure 3: MAC Board Architecture

2.2 SMEC AXIS CONTROL

The SMEC axis is controlled by a digital PID with a position ramp reference to insure a scan with configurable length and speed. The scan may be single with a fly-back at the end or a double scan (single and return) with the same common speed and stroke.

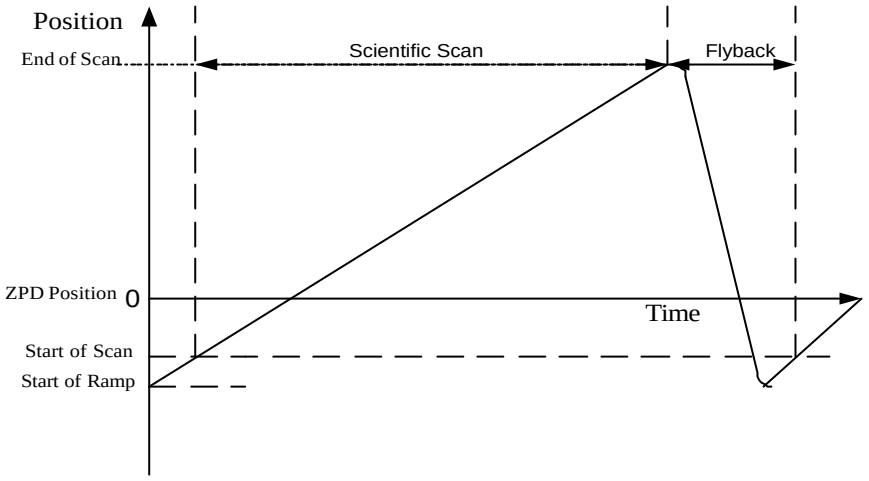


Figure 4: SMEC Scan characteristics

Scan characteristic	Requirement	Comment
Scan length	- 0.3 cm min to 3.2 cm max	Programmable length Value referred to the home position
Scientific Scan Length resolution	0.5 µm	based on a 16 bits parameter reference
Speed range	0 – 1mm/s	The value 0 means that the servo can be controlled in position steps.
Nominal scan speed	500 µm/s	The nominal speed is the basis for velocity stability requirements
Stability of the velocity scan	(10 µm/s rms).	on the basis of a filtered velocity fluctuation in the band 0.03-25 Hz
Fly-back duration	(less than 10% of the scientific scan)	including acceleration phase

Table 1 : SMEC scan specifications

2.2.1 SMEC Home position acquisition

The home position is delivered by the null differential signal provided by a +/- 0.1 inch useful stroke length LVDT. The home digital signal pulse resets the optical encoder counter in the bus control FPGA.

2.2.2 Limits positions

There is no specific sensor for limits. A dedicated mechanical stop reference for metrology is foreseen on SMEC mechanism.

After the initialisation of the incremental encoder counter, the limits shall be defined by software.

Before initialisation of the incremental encoder counter, the limits can be found by a dedicated motion up to mechanical stop, or by the LVDT absolute position signal when the mechanism is within its range.

2.2.3 Optical Encoder Position Acquisition

The position is determined from the summation of a crude and a fine position computation.
The fine position is calculated on the basis of the 3 sine optical encoder signals after pre-amplification, conditioning to be read directly by the DSP via a multiplexed 16 bits ADC for arctangent calculation.
The crude position is determined by an encoder counter register located in the Bus control FPGA incremented by TTL zero crossing signals of sine and cosine value every 2 µm encoder cycle . Since that, the sampling time of the DSP does not depend on velocity. Furthermore, the arc tangent computation of the position is dedicated for a fine and continuous position control, avoiding speed jitter that should be generated by encoder pulses if these signals enters directly in the control loop. The number of sine/cosine samples is given by :

$$N = \text{Sine period} / (\text{Speed} * t_{sampling}), \text{ with Sine period} = 2\ \mu m$$

2.2.4 Optical encoder LED control

Because of the possible decay of flux emitted by the optical encoder LED due to ageing, 8 possible current levels can be set by the MAC board through the digital I/O port (3bits encoding).

2.2.5 Degraded mode control using the LVDT

In case of optical encoder malfunction, the control loop may use the absolute position provided by the LVDT. The LVDT signals acquisition is done on the SMEC Board and digitised by a 16 bits multiplexed ADC converter. The useful range of the LVDT measurement with nominal linearity is +/- 2.54mm but shall be extended at twice this length with poorer linearity performance. Furthermore, an AC coupling of LVDT measurement permits to get a 0.1 um rms accuracy.

2.2.6 Degraded mode control using the motor back emf

In case of optical malfunction, the control loop uses the LVDT for short range as described above. For a complete SMEC mechanism travel, the control shall work in a degraded mode using the motor back emf information and/or open loop parameters according to the mechanism stiffness law. The back emf permits a velocity control of the mechanism only.

2.2.7 SMEC telemetry

In order to reconstruct the interferometer signal, the detector readout data must be concatenated with position sampling data. There is no absolute time tag in the SMEC Control System, but an extra signal on the timer of the MAC Bus control FPGA is implemented from the 330kHz command line clock.
For this purpose, the SMEC control electronics provides the time elapsed between encoder pulses corresponding to, for example, 6 µm displacement (i.e.3 encoder engraving wave of 2 µm), by mean of a timer triggered by an external clock provided by the synchronous command serial line.
This is done by the Bus control FPGA on the basis of a zero crossing of one sine encoder signal. These data are then read by the DSP, formatted and delivered to telemetry high data rate serial link.
The value of the number of encoder cycles is programmable with a minimum value of 2 microns corresponding to the zero crossing of an elementary sine wave of the moiré fringe optical encoder

Position data characteristic	As designed specification (Initial Requirement)	Comment
Position data sampling	2 µm (5 µm)	Provides a time count every encoder engraving of 2 µm Initial requirement based on the mini scientific wave length (200 um) divided by : - 4 (interferometer arm ratio) x - 5 (position data over sampling for calibration)
Position data accuracy	0.01 µm (0.1 µm)	Resolution given by the optical encoder after systematic non linearity correction
Position data synchronisation	time count start between pulse triggered by external	allows to reconstruct the trajectory starting from a reference start signal to be synchronised with start of detector samples

	signal	

Table 2 : SMEC delta time positions specifications

2.3 BSM CONTROL

The BSM is used to steer the optical beam of the SPIRE photometer channel over the detector arrays. The beam steering mirror will be used to perform jiggle mapping (to produce fully sampled images for feedhorn arrays, and to improve image quality) and perform chopping (to remove background and background variations and perform fine pointing corrections). This peaking up mode will be used to quickly ensure that point sources are well centred on individual detectors

The BSM comprises a flat mirror which is mounted on a two axis pivot system. This pivot system allows precise angular motion of the mirror over a small range of angular travel in two orthogonal axes. Electrical actuators are used to provide motion of the mirror. Magneto-resistive sensors are used to measure the mirror position to allow control of the mirror position. Control of each axis is done by a digital conventional PID (3-term) controller - with corrections for cross-coupling between axes- in the MAC Board.

The BSM is controlled via software running on the DSP. The BSM software controls the position of the two BSM axes in response to external commands from the host software (DPU). Each axis can move independently. Typicaly, a step command waveform is assumed, and above a certain amplitude (10% of peak), it is profiled to produce a sinusoidal acceleration demand.
The movement with respect to time is profiled via stored parameters to give a minimum energy, minimum noise position change, particularly for step commands.In general the movements are repetitions of the same position/time profile. The BSM is slaved to the input demands at all times, so to perform a repetitive chop pattern the host processor has to issue a succession of position demands at the relevant times. For example, to perform a 2 Hz chop between BSM positions p1 and p2, the following chop axis demand sequence and timing is required. The command update rate (Ts) must always be >= 0.1 mS . Other waveforms, such as triangular, can be approximated by a succession of incremental step demands, however the resolution will always be dependant on the update rate.
In addition, in the event of measured behaviour resulting in a fault diagnosis, some system backup procedures are available. Diagnosis of excessive position errors and analysis of recorded transient behaviour during operation can result in modifications to the control system by uploading different parameters.

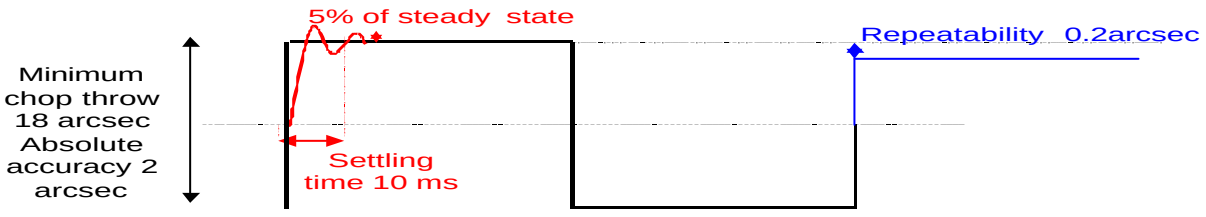


Figure 5: BSM chop control specification

3 LIST OF PROCESS SIGNALS CONNECTED TO THE MAC BOARD

The MAC board including the DSP and the FPGA shall have the following interface signals with the analogue electronics :

3.1 DACS ANALOGUE OUTPUTS (3)

Outp	Name	To board	Use
1	VOUT_DAC1	SMEC	FTS mirror actuation
2	VOUT_DAC2	BSM	chopper actuator
3	VOUT_DAC3	BSM	jiggle actuator

3.2 MULTIPLEXED ANALOGUE INPUTS (GOING TO ADCS AND DSP) (16)

Input	Name	From board	Use
1	ANALOG_IN_0	SMEC	position encoder sine
2	ANALOG_IN_1	SMEC	position encoder 120° sine
3	ANALOG_IN_2	SMEC	position encoder 240° sine
4	ANALOG_IN_3	SMEC	LVDT signal (AC)
5	ANALOG_IN_4	SMEC	LVDT signal A (DC)
6	ANALOG_IN_5	SMEC	LVDT signal B (DC)
7	ANALOG_IN_6	SMEC	motor back emf value
8	ANALOG_IN_7	SMEC	motor current value
9	ANALOG_IN_8	BSM	chopper position # 1
10	ANALOG_IN_9	BSM	chopper position # 2
11	ANALOG_IN_10	BSM	jiggle position # 1
12	ANALOG_IN_11	BSM	jiggle position # 2
13	ANALOG_IN_12	BSM	chopper motor back emf
14	ANALOG_IN_13	BSM	jiggle motor back emf
15	ANALOG_IN_14	BSM	chopper motor current value
16	ANALOG_IN_15	BSM	jiggle motor current value

3.3 DIGITAL INPUTS (GOING TO DSP) (8)

Input	Name	From board	Use	Remarks
1	DIG_IN_0	SMEC	position encoder A signal	
2	DIG_IN_1	SMEC	position encoder B signal	
3	DIG_IN_2	SMEC	launch latch # 1 status	engaged/ disengaged
4	DIG_IN_3	SMEC	launch latch # 2 status	
5	DIG_IN_4	SMEC	mechanical zero position	
6	DIG_IN_5	BSM	launch latch # 1 status	(ch & jig)
7	DIG_IN_6			
8	DIG_IN_7			

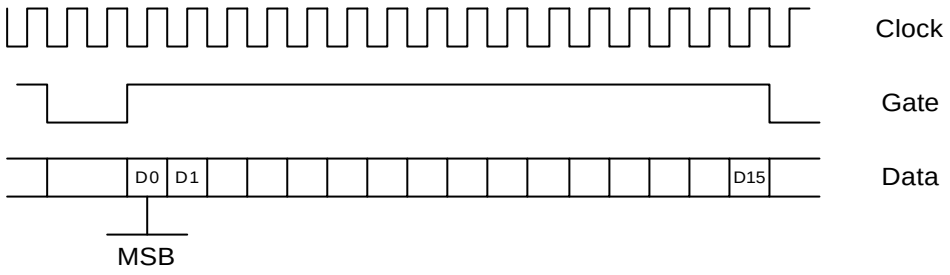
3.4 DIGITAL OUTPUTS (12)

Input	Name	From board	Use	Remarks
1	DIG_OUT_0	SMEC	launch latch command	
2	DIG_OUT_1	SMEC	launch latch eng/diseng select	
3	DIG_OUT_2	SMEC	LVDT power supply On	
4	DIG_OUT_3	SMEC	position encoder Led power supply bit # 0	also command of preamp power supply
5	DIG_OUT_4	SMEC	position encoder Led power supply bit # 1	also command of preamp power supply
6	DIG_OUT_5	SMEC	position encoder Led power supply bit # 2	also command of preamp power supply
7	DIG_OUT_6	SMEC	launch latch #1/#2 select	
8	DIG_OUT_7	BSM	launch latch command	
9	DIG_OUT_8	BSM	launch latch eng/diseng select	
10	DIG_OUT_9	BSM	chopper position sensor power supply On	
11	DIG_OUT_10	BSM	jiggle position sensor power supply On	
12	DIG_OUT_11			

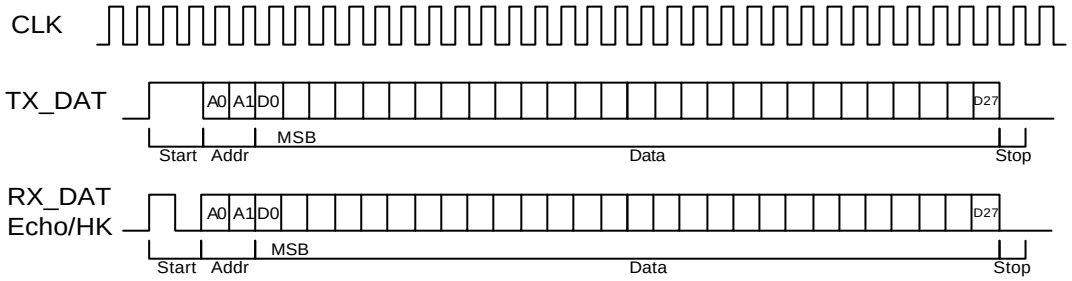
4 I/F WITH DPU (COMMUNICATION AND TELEMETRY)

The MCU communication with DPU shall be done through 2 serial lines :

- Low rate command interface link @330 kbits, based on 32 Bits word for commanding and H/K monitoring.
- High rate telemetry interface link 1Mbits, based on 16 bits for large amount of data



High speed interface protocol



FSDPU/FSDRCU Low Speed Interface protocol

4.1 LOW RATE COMMAND INTERFACE

This link is based on a Master/Slave relationship between DPU and MAC. By mean of a FPGA dedicated to serial interface, the commands and parameters are decoded and put in 2 registers to be read by the 21020 DSP. There is a systematic reply to DPU for each command.
The MCU shall receive from the DPU a 32 bits word for each command. The 32 bits word shall include (i) subsystem id (ii) 12 bits for command type (e.g. set scan_length), (iii) 16bits for the parameter itself. When a command from DPU is received by CONTROL LINK FPGA, the 32 bits are unserialised (by Link Management) and put in the Command Interpreter 32 bits register only if the command concerns the MAC subsystem . Command Interpreter reacts according 2 ways:
1) there is a “reset command” or a “start datation counter command”: so, DSP is not concerned and CONTROL LINK FPGA set one the 2 dedicated bits for CONTROL BUS FPGA (that executes the command), then put a 32 bits word acknowledge into Link Management that serialises and sends it to DPU.
2) in the most of cases, it’s a SET or GET command, Command Interpreter loads two 16 bits registers (Command Reg1, Command Reg2) and interrupts DSP (IRQ1). In the interrupt routine, DSP reads the two registers to build 32 bits command (that contains a parameter address and its value if it’s a “set parameter”), and sets or gets the concerned parameter in its memory (variables table). Then, DSP writes the acknowledge into Command Reg1 and Command Reg2 and returns to its main servo control

task (according to the new value parameter if it's a "set parameter"). Then, the Command Interpreter reads the 32 bits acknowledge and gives it to the Link Management to serialise it to DPU.
For every command, a handshake is done with DPU, so that only one command can be sent at one time until the parameter of the control shall be taken into account. Since the DSP is interrupted by a command, the maximum delay for a command to be taken into account is:
100µs for un serialise + 500ns interrupt routine + 100µs for serialise acknowledge ≅ 200µs

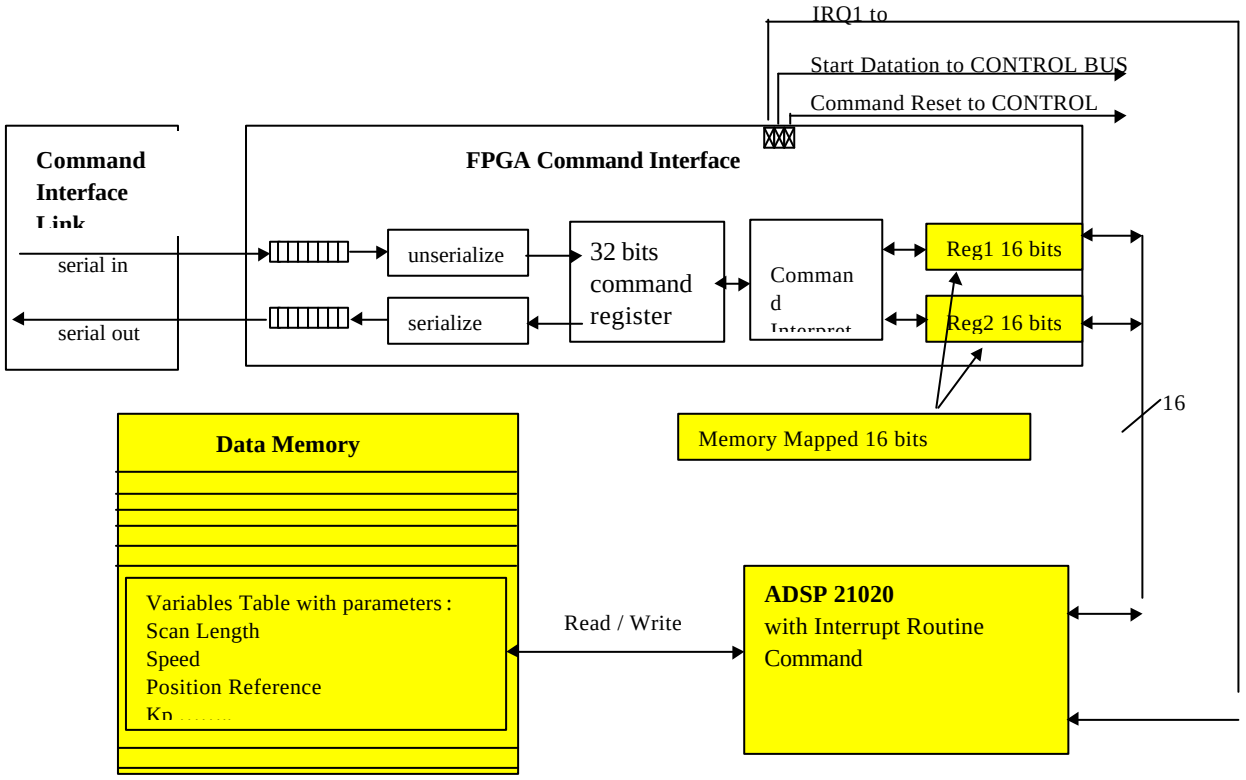


Figure 6: Command line and DSP link principles

4.2 MONITORING, H/K AND TELEMETRY FUNCTION

The MCU shall provide 2 types of monitoring data for the 3 axis:

- H/K,
- telemetry.

4.2.1 H/K Data

The HK data consist of the readout of single variable read by the command line @ a low rate (1 second typically and defined by the DPU). The H/K variables readout is made on the basis of a 'get_parameter' command with a reply within the DSP master scheduler time sampling rate added with the transmission delay. The complete overall delay is about 200 us.
Typically, the H/K variables may be all possible variables set-up or computed by the DSP, e.g.:

- mean SMEC scan speed
- SMEC control status
- SMEC encoder status
- Chopper mean position
- Jiggle mean position
- Etc …

See the complete set of commands to have the list of all available H/K variables

4.2.2 Telemetry data

The telemetry data consists of data frames transmitted to the DPU by the high speed 16 bits 1MHz synchronous serial line.

4.2.2.1 DATA FRAMES FORMAT

The MCU telemetry data frame structures follows the following template :

Length
Frame ID
Frame Time (32 bits)
Data
Checksum

Where:

Length:	Total number of (16 bit) words in the frame, including Length
Frame ID:	Frame type identifier: Note: Each Frame type is allocated to a different Science Telemetry Packet Subtype and SID for transmission to the ground
Frame Time:	Time that the frame was generated by the DRCU Unit
Checksum :	Exclusive OR of all words (TBC). This value is checked by the DPU and a flag set in the DPU telemetry if there is an error.

Data: Determined by Frame ID

All words are 16 bits unless indicated otherwise

Shaded words are removed by the DPU before packing into a science telemetry packet

The MCU shall send 6 data frame types :

TM Packet Subtype, SID (hex)	Frame Type	Frame ID (hex)
2,10	SMEC Scan	10
2,11	SMEC Step	11
2,12	Chop	12
2,13	Jiggle	13
3,14	Trace	14
3,15	Test Pattern	15

4.2.2.2 SMEC SCAN FRAME (10)

This telemetry data packet includes the SMEC time count between two encoder N micron positions (N is a configurable value between 2 and 26 microns by step of 2 microns) synchronized with an external clock signal provided by the command line clock. The LVDT absolute position is as well provided for comparison.

Zero Crossing Delta Time (32 bits)
Crossing Count
Mean Velocity
DC LVDT

4.2.2.3 SMEC STEP FRAME (11)

This telemetry packet is sent if the SMEC mechanism is controlled by position steps instead of a constant velocity.

SMEC Position
Position Error
AC LVDT
DC LVDT

4.2.2.4 CHOP FRAME(12)

This telemetry packet includes the chopper position at a dedicated sampling time programmed in the DSP.

Time (32 bits)

Chop Position
Chop Error Signal

4.2.2.5 JIGGLE FRAME (13)

This telemetry packet includes the jiggle position at a dedicated sampling time programmed in the DSP.

Time (32 bits)
Jiggle Position
Jiggle Error Signal

4.2.2.6 TRACE FRAME (14)

The trace data is a buffer in the DSP data memory which is a long data acquisition. The number of trace variables, the sampling time, the length of the data buffer are programmable. This buffer can be read off-line, i.e. when the DPU sends a dedicated command for each data sample.

Typically, the trace data mode shall be used for the scanning of large number of samples @ high sampling rate for engineering purpose.

Sample Time (32 bits)
Parameter#1
Parameter#2
Parameter#3
Parameter#4
Parameter#5
Parameter#6

4.2.2.7 TEST PATTERN (15)

This is a specific frame for communication tests. The exact contents is TBD.

4.3 SYNCHRONIZATION WITH DPU

The measurement of the delta time elapsed between 2 or more encoder zero crossing starts on the receipt of a specific synchronisation signal. This synchronisation signal resets the internal timer of the delta time count in the Bus Control FPGA. This function is implemented to allow synchronisation with detector data frames acquisitions. Since that the first delta time value provided to telemetry is representative of the time delay between the synchronisation signal provided by the DPU and the first optical encoder pulse of the scientific scan. The delta time counter is incremented by the Low Speed Serial link clock set to 330 kHz. The counter range is defined to 32 bits.

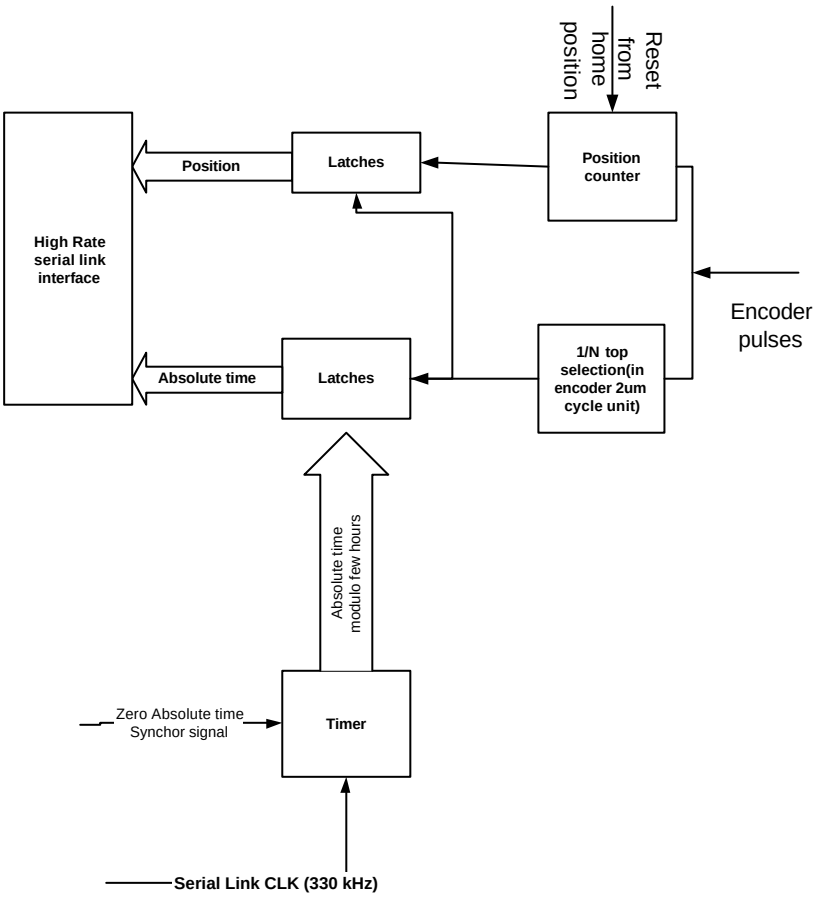


Figure 7 : Principle of position sampling timer synchronisation with DRCU

5 MAC OPERATION

The MAC Board may be operated by a set of commands according to the following table.

Mode #	Mode Name	Action	Possible Next Mode	On Command
0	Off	The set of boards is not powered. No function available	On	Power On
1	On	The set of boards (main or redundant) board is powered .	Off	Power Off
1.0	Booting	• The software is initialised after reset. • The software is downloaded from Prom memory to SRam memory	Downloaded	MAC Reset On
1.1	Downloaded	• The communication is available. • The status of the system is available. • Waiting for commands • Goes initially to Open loop mode	Booting	MACReset On **'ResetMAC'**
1.1.0	Open Loop	• Waiting for Advanced Configuration Commands (Control gains,etc ...) • Goes initially to open loop standby	Close Loop	'**CloseLoop**'
1.1.1	Close Loop	• nominal control loop mode using a digital PID controller at 300 µs sampling rate • Goes initially to Stand By mode	Open Loop	**'OpenLoop'**
1.1.1.0	CLoop Stand By	Waiting for motion configuration: (Scan Length, etc..)	Motion init	**'Init Motion'**
1.1.1.1	CLoop Motion Init	Searching for limits and diagnostics	Ready	End of Motion initialization
1.1.1.2	CLoop Ready	Waiting for motion commands and configuration	Scan	'**StartMotion'**
1.1.1.3	CLoop Scan	Motion underway: scan for the SMEC, chopping and jiggling for BSM	Ready	End of Motion '**StopMotion**' **'ResetMotion**

5.1 COMMAND TYPES

There are typically three types of commands :

- **Set Command** : the parameter is put in the DSP memory for immediate or delayed execution
- **Get Command** : the dedicated parameter in memory can be read by the DPU
- **Immediate Command:** Reset Command or Start Datation Counter

5.2 BUFFERED COMMANDS AND PARAMETERS

Some parameters set by a Set Command should not take immediate effect on the control. These parameters are called **buffered parameters**. They are taken into account when a specific **Start** command is sent. This is useful for a configuration set definition such as the scan speed and length

before a validation of the configuration. The buffered parameters relates to the motion trajectory, control loop and telemetry configuration set up parameters.

5.3 COMMAND LIST

The complete list of parameters associated with the Set or Get command is listed in the document " **MCU /DCU Command List ICD"**

6 MAC SOFTWARE DESIGN

6.1 21020 DSP SOFTWARE PRINCIPLES

The DSP software is in 21020 assembly language without the use of a specific off-the-shelf real time operating kernel. The assembly language is chosen because Analog Devices provides directly specific libraries to produce PID, filtering, arctangent computation with a high efficiency and readability. For this reason C coding is not foreseen since the software shall be simple, dedicated to pure signal processing (ie realisation of IIR Filters with product/summation operations) without complex command interpreting nor complex mode of operations.
Code uploading in the DSP is not foreseen, the DSP being only used for control, in substitution of analogue electronics, with very poor load regarding communication / command interpreter. Code uploading would imply a very heavy software management task.

6.1.1 ITs

The main tasks to be performed are called by a Master scheduler which is a routine interrupted by a software interrupt generated by the inner timer of the DSP.
Mainly, the software does not use other interrupt, excepted for the following functions :

- watchdog interrupt to recover from a loss of control of the DSP,
- interrupt (IRQ1) on a received command from DPU.
- interrupt (IRQ0) on each SMEC incremental encoder pulse for position counting (TBC)

6.1.2 Watchdog mechanism

A Watchdog mechanism is implemented between Control Bus FPGA and DSP to monitor the DSP behaviour. This counter is incremented on the basis of the Control Bus FPGA internal clock.
If the DSP does not ensure the counter reset, the FPGA automatically resets the DSP.

6.1.3 Reset

The reset of the DSP shall be activated on the following events :

- no watchdog signal
- specific command line word (reset command from DPU)

We can also implement in soft a time out between two commands, that shall detect a potential loss of the command line, so DSP must be in a "reset state", but this reset state doesn't involve a hard reset.
Hard Reset DSP is monitored by Control Bus FPGA (that contains Watchdog and receives the dedicated bit Command Reset). Reset DSP is performed in two steps:
Step 1: Control bus FPGA maintains reset line of DSP active, connects Pms0 and Pms1 lines to respectively PROM chip select and SRAM chip select. Then, it releases reset line so DSP jump at 0x00 0008 address of bank 0 program memory, i.e. 0x00 0008 PROM memory address. At this

address, DSP shall perform a boot program, that verifies RAM memory integrity, and loads all the instructions in the RAM memory. After this, DSP send a word to Control Bus FPGA to signify that it has completed this step 1

Step 2: Control bus FPGA again maintains reset line of DSP active, but now connects Pms0 and Pms1 lines to respectively SRAM chip select and PROM chip select. Then, it releases reset line so DSP jump at 0x00 0008 address of bank 0 program memory, i.e. 0x00 0008 SRAM memory address (SRAM now contains the program that has been loaded during step 1, that performs servo control and all DSP operations).

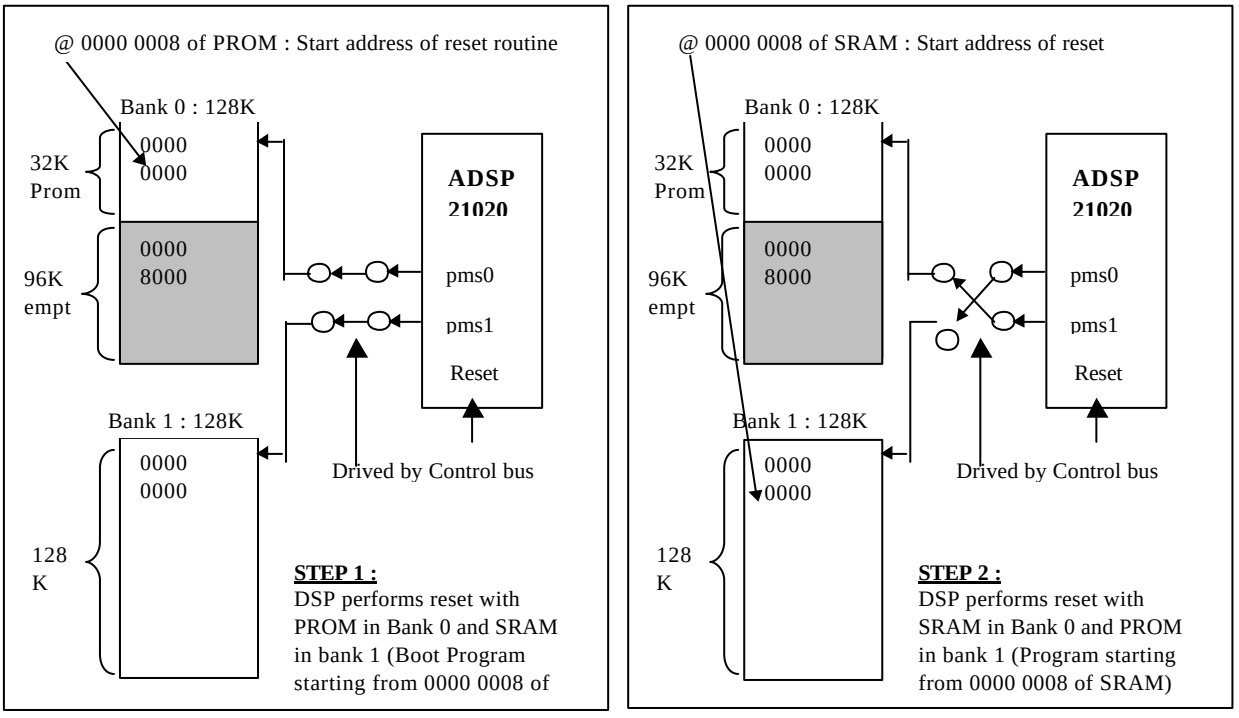


Figure 8: Mapping Program Memory of DSP during Reset sequence

6.1.4 Motion in safe configuration

In case of problem detected by the control (position error greater that a threshold value, loss of encoder pulses, etc ...), the software shall immediately open the axis control loop and force dac to 0 volt. A redundancy in the fault condition shall be implemented to detect possible memory latch-up. In case of ram memory partial destruction, an other mapping may be specified.

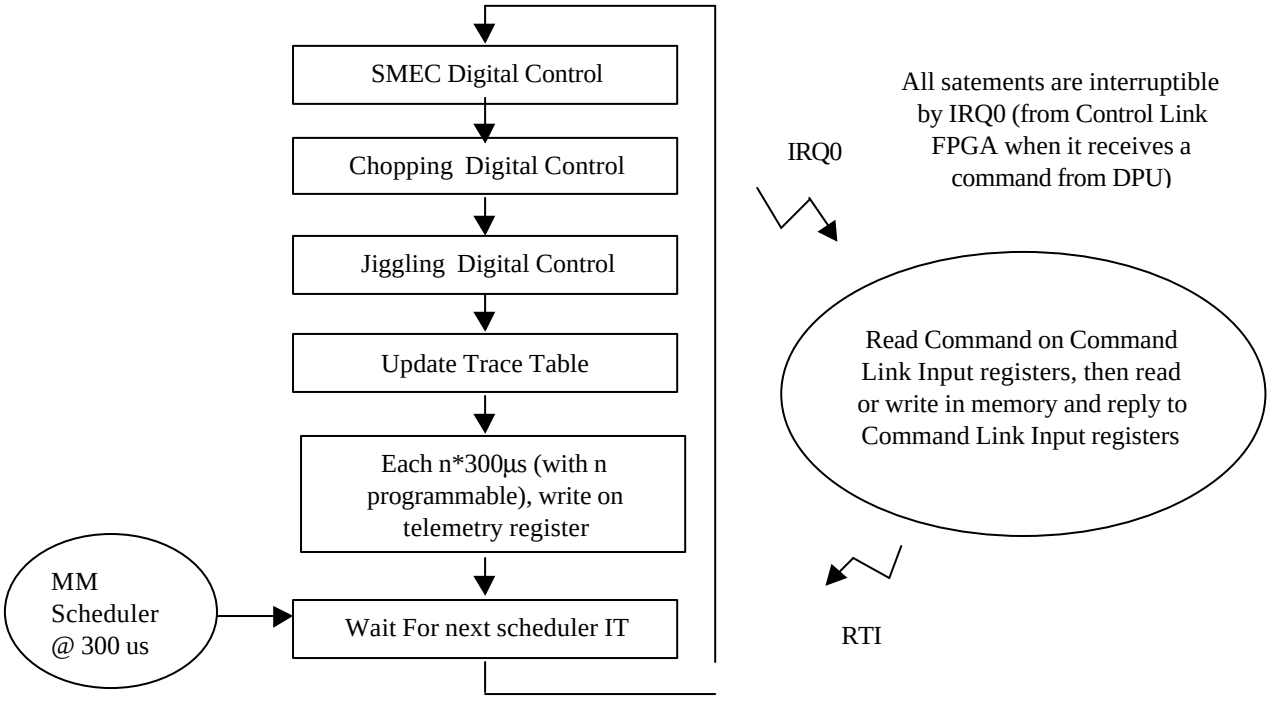
6.2 MAC SOFTWARE ARCHITECTURE

The software is designed to be as simple as possible. For this purpose, there is an only task running every time defined by the digital servo sampling time parameter. The digital servo sampling time is defined by the MMS (Mac Master Scheduler).

6.2.1 MAC Master Scheduler (MMS)

The principle of the MMS is the management of the main cycle to be performed in the MAC DSP.
The main cycle is set by default to 300 us (TBC), but is configurable.
The MMS uses the internal clock of the DSP , incrementing an internal counter set to deliver an interrupt every main cycle interrupt signal triggering the start of the main task.

6.2.2 MAC Main task



6.2.3 SMEC and BSM axis Control Algorithms

- Read Digital I/O (Home, Launch Lock)
- Compute control status
- Compute servo loop

6.2.4 SMEC Servo Loop algorithm

- Step 1 : read sinus and cosinus (1 DSP cycle = 50 ns)
- Step 2 : read cosinus (1 DSP cycle = 50 ns)
- Step 3 : filtering sinus (T1 = 40 DSP cycles = 2 µs)
- Step 4 : filtering cosinus (T1=40 DSP cycles = 2 µs)
- Step 5 : compute arctangent (T2 = 120 DSP cycles = 6 µs)
- Step 6: compute current trajectory,that is the same that a speed filtering (T1=40 DSP cycles=2 µs)
- Step 7 : compute current error and "do something" if error > max error (T3=40 DSP cycles=2 µs)
- Step 8 : with error, compute output DAC for FTS motor amplifier (T4 = 80 DSP cycles = 4 µs)
- Step 9 : write output DAC (1 DSP cycle = 50 ns)

T1, T2 are roughly given and are to be exactly defined.
T3,T4 and T6 are estimated with Analog Device application notes, for example the number of cycles for a FIR Filter is given by : **number of cycles = 7 + number of taps used for filtering.**
Another example is the compute of **PID in 10 cycles** (ref : DSP-Based Motor Controller Seminar of Analog Devices)
These numbers don't include error test , overflow… so we must reserve about 20 cycles for this.
The compute of **Arctangent** is given for **82 cycles** maximum from Analog Devices (ref ADSP-21000 Family Application Handbook), but we must reserve about 40 cycles for overflow and error tests.
So, the total timing for execute step 1 to 11 can be estimated to about 17 µs.

6.2.5 BSM Chopping axis Servo loop

Nota : the BSM software is specified in the Reference Document RD1 Beam Steering Mirror Control Software Requirements (Spire-ATC-Draft)

- Step 1: set analog multiplexer to BSM chop position magneto-resistive sensor (1 DSP cycle = 50ns)
- Step 2: wait 300 ns (analog mux transition time)
- Step 3: write Start of Conversion to ADC (1 DSP cycle = 50 ns)
- Step 4: wait 15 µs (ADC conversion time)
- Step 5: read position (1 DSP cycle = 50 ns)
- Step 6: compute position filter (T1 = 40 DSP cycles = 2 µs)
- Step 7: compute current error and "do something" if error>max error (T2 = 40 DSP cycles = 2 µs)
- Step 8: with error, compute output DAC for BSM Chopping axis (T3 = 40 DSP cycles = 2 µs)
- Step 9: write output DAC (1 DSP cycle = 50 ns)

So, the total timing for execute step 1 to 9 can be estimated to about 7 µs.
The steps are exactly similar to the previous task.

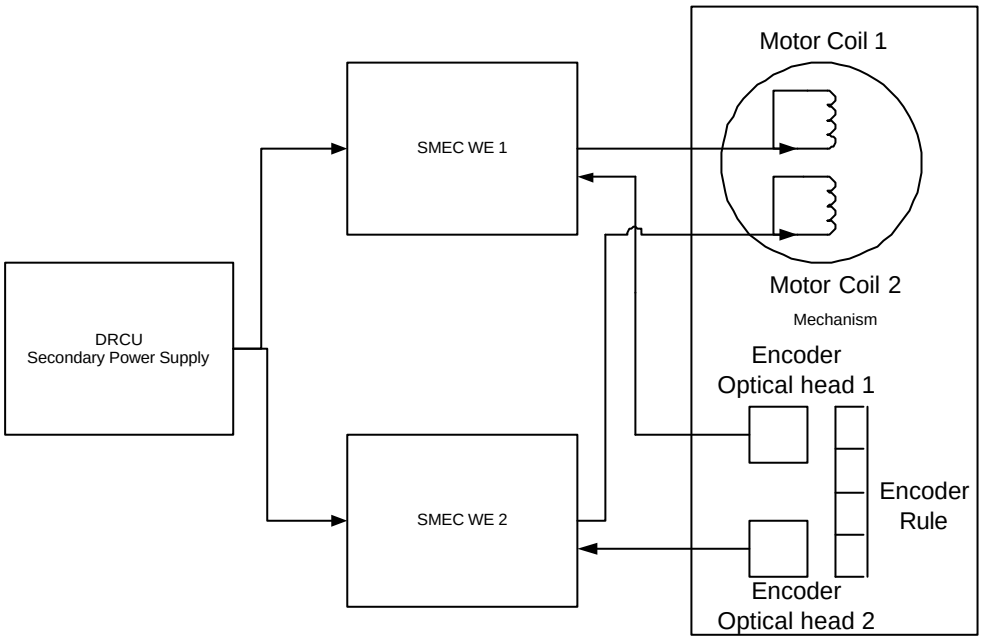
7 REDUNDANCY

The SMEC Control electronics consists of 2 independent sets of boards without cross switching. The related reliability is expressed by :

WE1.M1.OE1 + WE2.M2.OE2

Wei : FTS electronics board
Mi : motor coil
Oei : optical encoder and LVDT

Note : the solution with cross switching of the components would imply non reliable complexity and single point failure with the following reliability layout : ***(WE1+WE2).(M1+M2).(OE1+OE2).Ics with*** Ics : Necessary Interface for cross switching



For BSM see related documentation of BSM design data package.

8 LIMITATION OF FAILURE PROPAGATION

See Failure Mode and Evaluation of Criticality analysis report

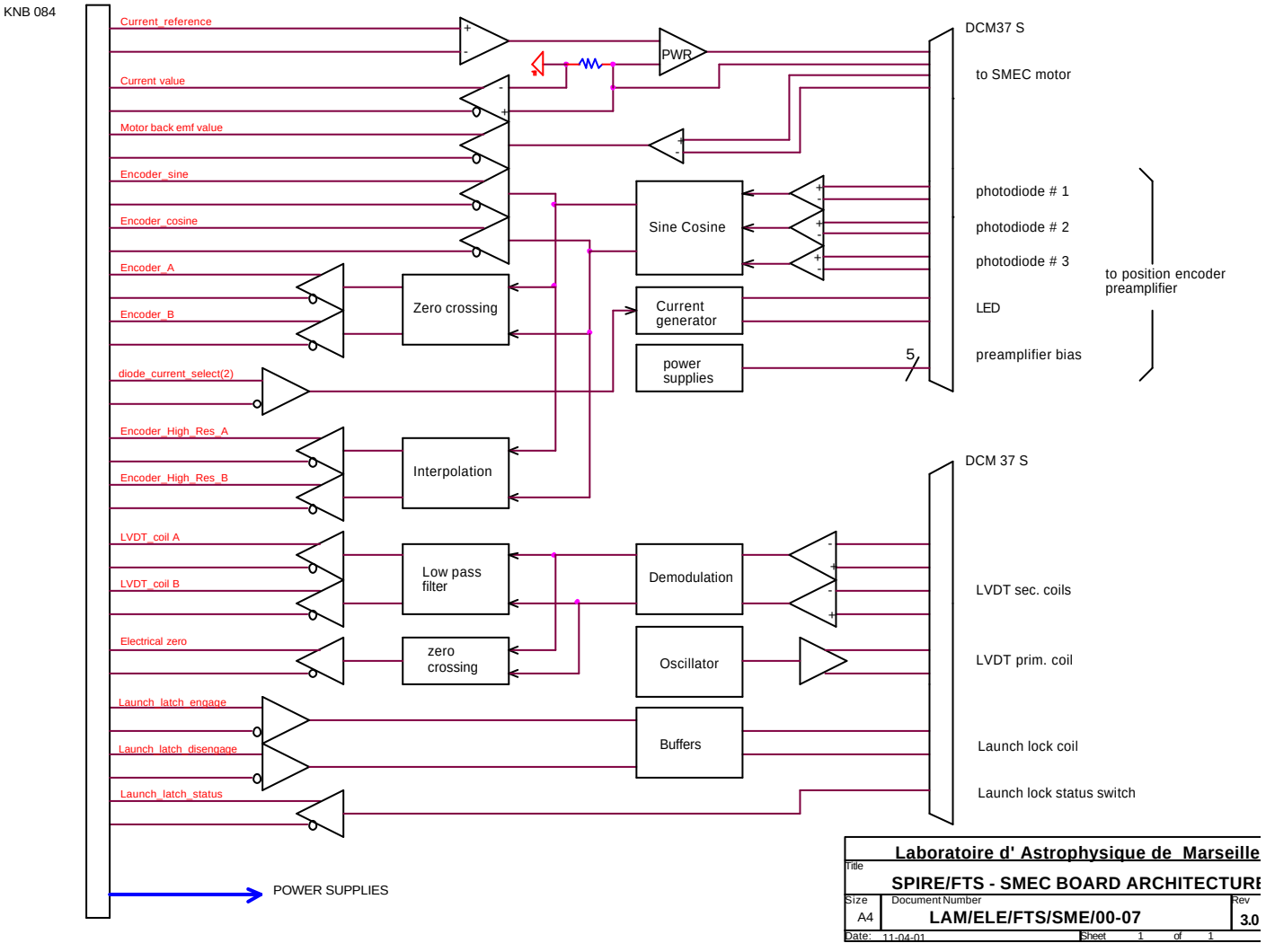
9 MCU ELECTRONICS DESIGN

This Section is intended to describe the features and the architecture of the Subsystem dedicated electronics (i.e. electronics circuitry and interconnection including complex circuits like FPGAs and/or dedicated micro-controllers.

9.1.1 SMEC Board

The SMEC Board is a 220x223 mm2 card including all analog electronics interfacing the SMEC Subsystem. It includes:

- the motor amplifier
- the optical encoder acquisition
- the LVDT conditioner
- the launch lock drivers



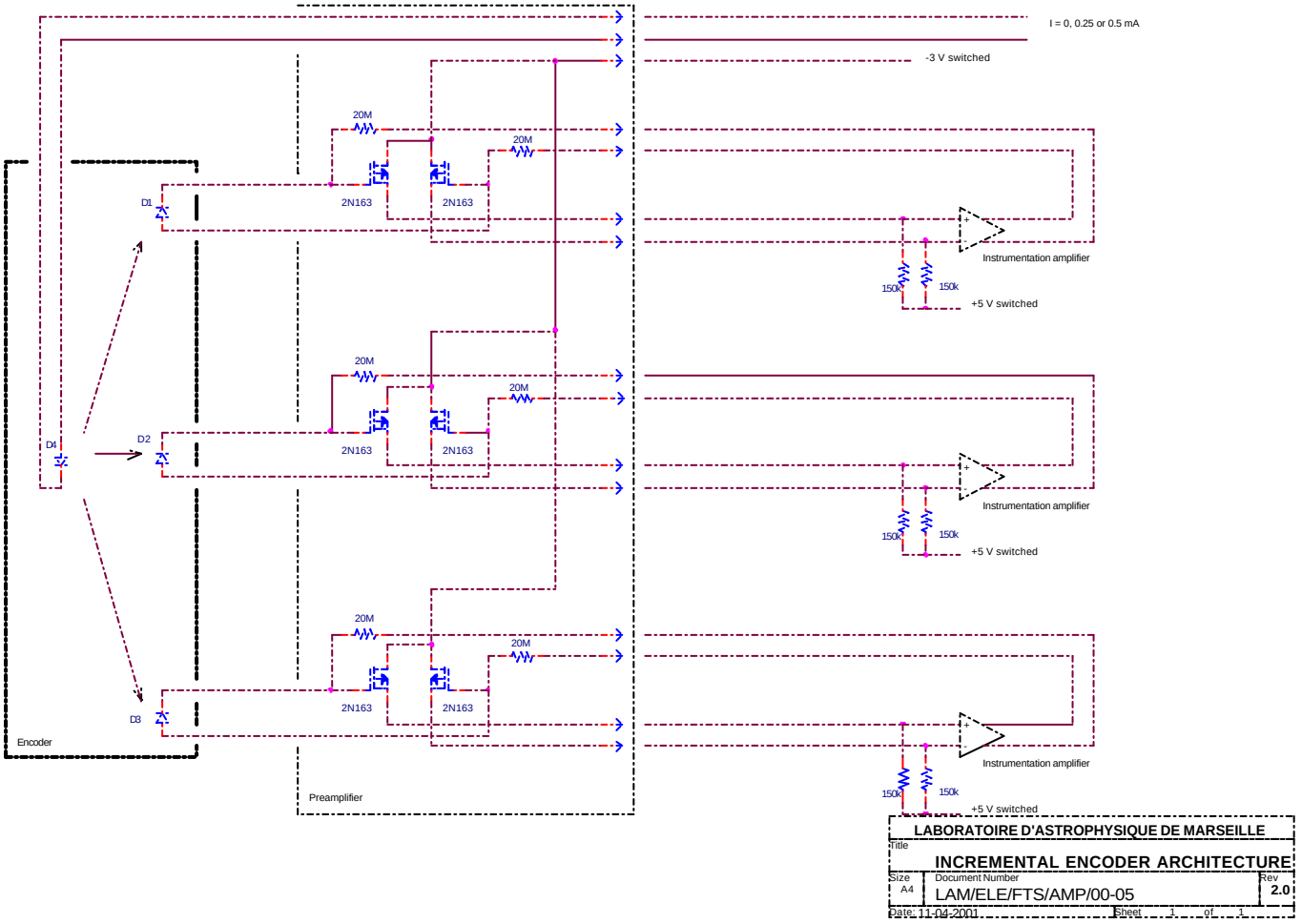
9.1.1.1 MOTOR POWER AMPLIFIER

The Power Amp is based on bipolar transistors (complementary pairs of 2N5153/2N5154) providing a gain of 10 mA/V with a bandwidth of 3.3 kHz.

9.1.2 Optical Encoder Preamplifier

The preamplifier box include the two preamplifiers for main and redundant channels. It is located in the SMEC mechanism, near the position encoder heads.

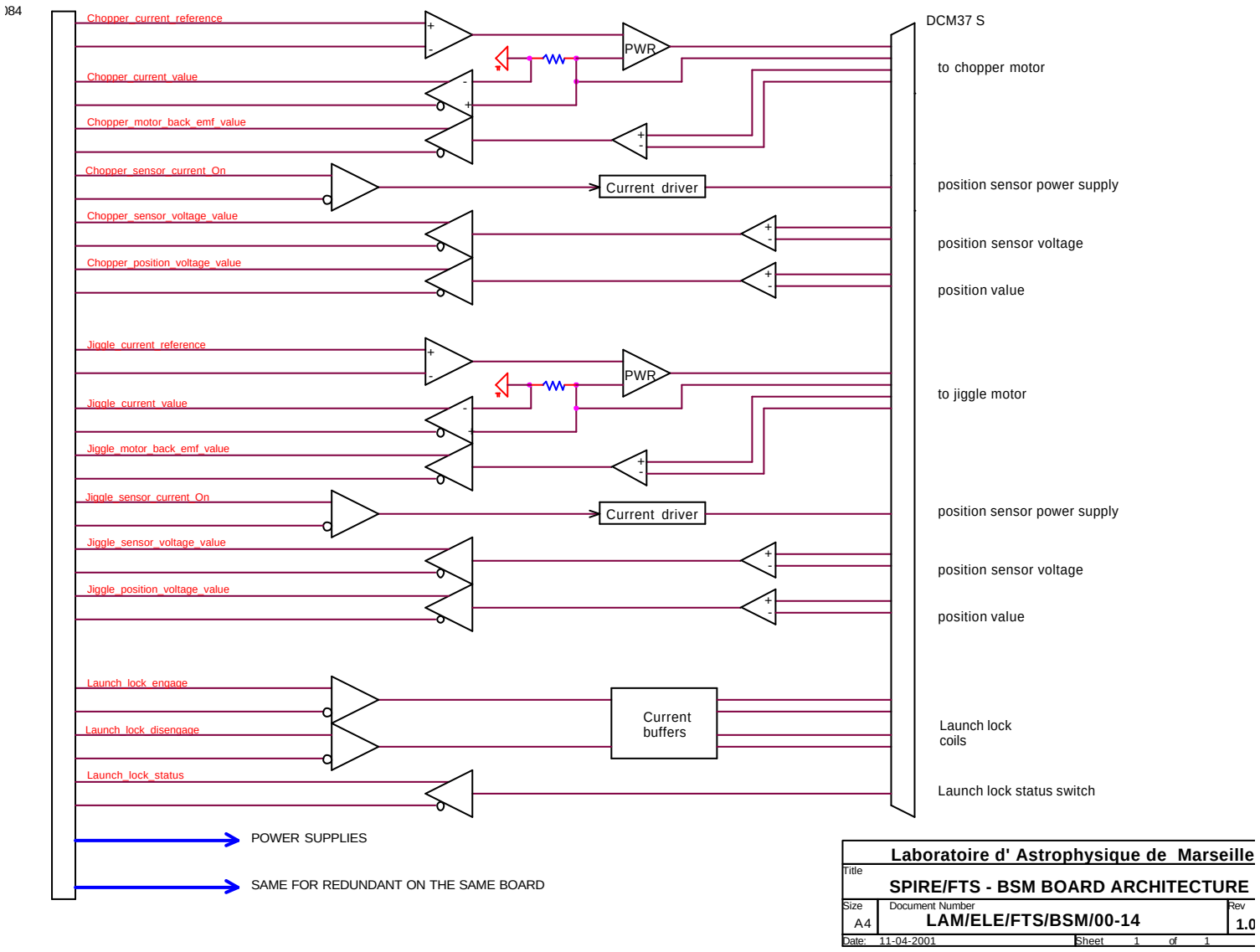
- The preamplifier board includes the two preamplifiers for main and redundant channels. It is located in the SMEC mechanism, near the position encoder heads.
- 6 x 3N163 PChannel Mosfet + 6 redundant
- Total dissipation for preamp < 500 uW
- Total dissipation for encoder head < 1 mW



9.1.3 BSM Board

Position sensor read-out :
Bridge circuit with switchable DC bias,
Instrumentation Amplifier eg A524,
Multiplexer and 16 bit A/D converter eg 7805ALPRP (SEi)

Motor drive:
Complimentary bipolar transistor pair eg 2N 5153/4
Motor Current Measurement:
series resistor and connection to A/D converter



9.2 POWER DISSIPATION

Subsystem	Voltage	Average power (TBC)	Peak power / time (TBC)	Average / peak current	Remarks
MAC board DSP and logic	+ 5 V	8000 mW (TBC)	13500 mW (TBC) t = 100 ms (TBC)	1.6 A / 2.7 A (TBC)	• power peak happens during DSP boot
MAC board analogue & data converters	± 13 V	1500 mW	1500 mW	65 mA (+13v) 50ma (-13v)	
SMEC board analogue electronics	± 13 V	3000 mW (TBC)	3000 mW (TBC)	115 mA	
SMEC board PWR Amplifier	± 15 V (TBC)	500 mW on + 15V and 500 mW on - 15V	3000 mW	33 mA 100 mA max (TBC)	• motor harness resistance less than 20 ohms
BSM board analogue electronics	± 13 V	1500 mW (TBC)	1700 mW (TBC)	60 mA	
BSM board PWR Amplifier	± 15 V (TBC)	500 mW on + 15V or 500 mW on - 15V (TBC)	1500 mW on + 15V or 1500 mW on -15V t < 10 ms	40 mA (TBC)	• motor harness resistance less than 200 ohms • power peak happens during acceleration of the mirror.
TOTAL		**15500 mW**	**22450 mW (TBC)**		• power peaks on SMEC and MAC boards are never at the same time.

9.3 POWER SUPPLY

Power Supplies which are needed are:

- 5V for DSP and logics
- +/-13V for analogue electronics excluding PWR Amplifiers
- +/-15V for BSM and SMEC Power amplifiers

Two complete sets of these above power lines are needed (main power lines & redundant power lines).
Encoder preamplifier boards (M & R) are powered by SMEC board.
All the electrical components in the SMEC mechanism are powered by the SMEC board.
All the electrical components in the BSM mechanism are powered by the BSM board.

The requirements for the PWR supply are included in the document “MCU Flight Model Interconnection List ‘’

9.4 GROUNDING SCHEME.

The main specifications for the grounding are:

- The analog grounds not connected @ MCU level
- Analog/Digital grounds connected @ ADC level
- Analog ground not connected to mechanics

See ‘ MCU Grounding Scheme’ document for detailed drawing of grounding (doc ref.LAM/ELE/SPI/011012)

9.5 COMPONENT LIST.

See the EEE part list for the complete set of components (doc ref LAM/ELE/FTS/QUA/000201).