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Summary :

   This document describes the photometer/spectrometer bolometers simulator specifications, the 0.3K cooler simulator specifications and the thermometry simulator specifications for DCU/SCU tests.

CEA - DSM/DAPNIA/**SIG**

FPU simulator specifications for DCU/SCU tests

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Acronyms and Key words

CEA	Commissariat à l'énergie atomique
CQM	Cryogenic Qualification Model
DAPNIA	Département d'Astrophysique, de physique des Particules, de physique Nucléaire et de l'Instrumentation Associée
DCU	Detector Control Unit
DSM	Direction des sciences de la matière
DUT	Device under test
DRCU	Detector Readout & Control Unit
EMC	Electromagnetic compatibility
FIRST	Far Infrared and Submillimetre Telescope
FPU	Focal plan unit
I/F	Interface
I/O	Input / Output
IR	Infra red
JFET	Junction Field Effect Transistor
LIA	Lock-in Amplifier
LTU	Local test unit
QM1	Qualification Model 1
RAL	Rutherford Appleton Laboratory
SBCC	Simulator name for SPIRE, bolometers, cryogenic and calibrators
SCU	Subsystem Control Unit
S/C	Spacecraft
SAP	Service d'Astrophysique
SIG	Service d'instrumentation générale
TBC	To be confirmed
TBD	To be defined

Table of contents

1 Introduction

1.1 Scope

This document describes the FPU simulator specifications for DCU/SCU tests relevant to its design and development. The purpose of this specification is to describe the main capabilities and features of the simulator.

It is organised with a top-down approach whereby general descriptions precede the more detailed specifications. The first section describes the FPU and gives a simulator overview. The subsequent sections cover electrical, software and mechanical requirements for the FPU simulator.

1.2 Objectives

The FPU simulator is a subsystem belonging to a test bench, it is an assembly of instrumentation modules. It has two functions:

- It generates patterns to simulate the FPU bolometers arrays of the spectrometer or the photometer.
- It simulates partially the 0.3 K cryo-cooler, the calibrators and other elements connected with the SCU.
- It measures signals coming from the DCU and SCU.

The objectives are to specify:

- The hardware instrumentation functions of the simulator.
- The software for the simulator control. It concerns the data packaging relative to patterns/measurements, and the interface with other test bench subsystems.
- The mechanical packaging of the simulator.

Those specifications are intended to serve the needs of simulator and test bench developers.

1.3 Applicable documents

AD1	DRCU Subsystem specification	SAp-SPIRE-CCa-25-00
AD2	FIRST/SPIRE Electrical system design	SAp-SPIRE-CCa-26-00
AD3	-	-

1.1 Reference documents

RD1	-	-
RD2	-	-

2 General description

2.1 SPIRE instrument overview

An overview of SPIRE electrical systems configuration is depicted in **Figure 1**.

The FPU performs scientific measurements, for example it includes: bolometer detectors for scientific observations, a cryogenic subsystem to cool the detectors at 0.3 K, black-bodies to calibrate detectors, and temperature probes for control purposes.

DCU and SCU are electronic modules dedicated to analog signal processing and FPU controls/commands. Those 2 modules belong to the DRCU.

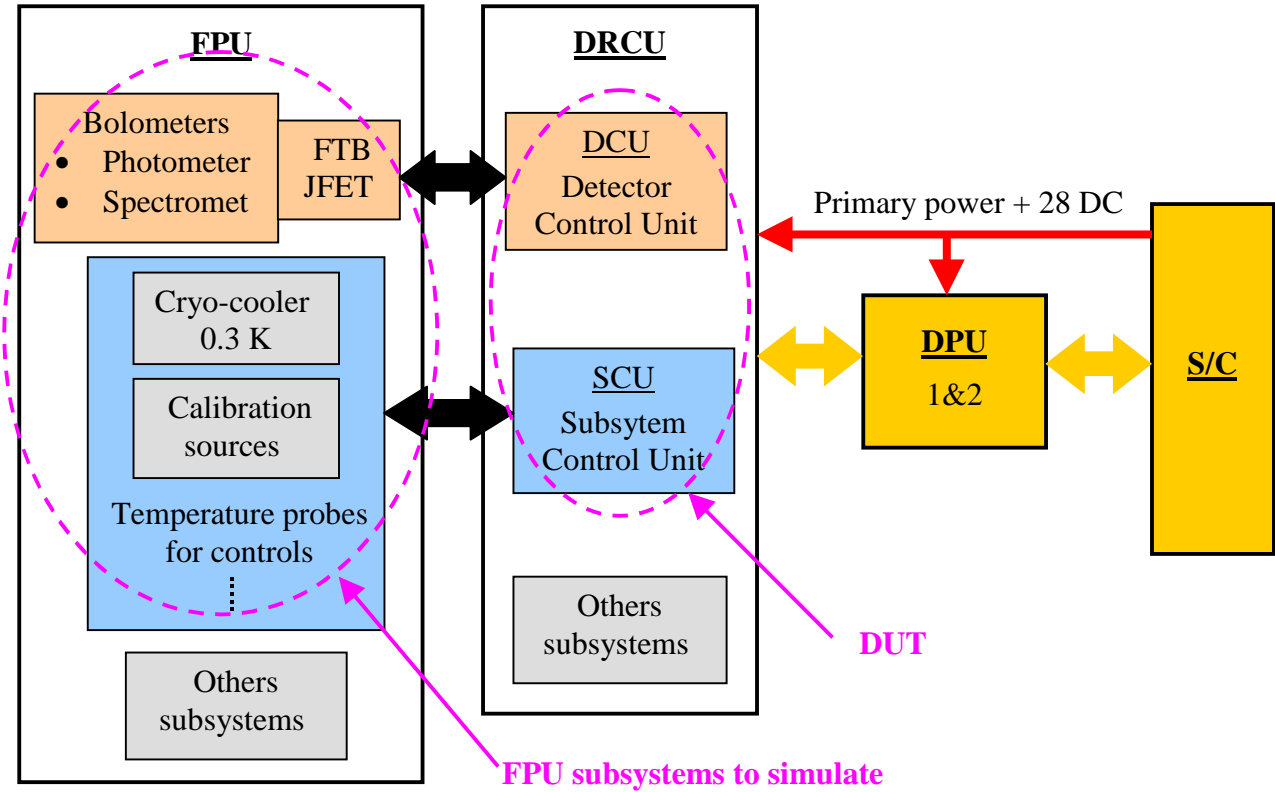The DPU supervises general tasks and the interface with the S/C.

Figure 1: *FPU subsystems to simulate DCU/SCU tests*

2.2 Simulator overview

2.2.1 Main simulator functions

The different SPIRE systems must be controlled and tested. This document is about a simulator which is a test equipment for:

- Simulating the FPU subsystems behaviours that are connected with DCU/SCU.
- Measuring bias, temperature probes power supplies and command signals that are coming from DRCU.

The simulator is named SBCC for the words <u>S</u>PIRE, <u>b</u>olometer, <u>c</u>alibrator, <u>c</u>ryogenic.

More precisely, the SBCC simulator includes the following functions:

- Behavioural simulation of the spectrometer bolometers.
- Behavioural simulation of the photometer bolometers.
- Behavioural simulation of the thermometer bolometers.
- Simulation of the heaters and the temperature probes used by the 0.3 K cryogenic sorption cooler.
- Measurements of the bias for the bolometers, the calibrator and the temperature probes.
- Measurements of the JFET box power supplies.

2.2.2 Simulator and test bench

SBCC simulator is a test bench subsystem as it is depicted in **Figure 2**.

SBCC includes three subsystems:

- A computer and a software which are the supervisor.
- The core that comprises instrumentation dedicated to simulation and control measurements.
- An electrical I/F to connect the simulator with the DUT.

The DUT is the SCU/DCU subsystems.

The LTU is the instrumentation instead of the DPU.

The way the test bench could work can be summarised as follows:.

- A input file defined by the LTU side is download into the core simulator through the computer. When the simulator is configured, a ready signal is set.
- An enable signal controls the beginning /end of the test.
- SBCC generates analog signals according to the input file.
- When the simulator generates or receives hardware triggers, control measurements are done and save in output files.

Warning: this description is only given as an example to define a general working principle.

Figure 2 : *Test bench hardware configuration*

3 Simulator specifications

3.1 General specifications

The goal of SBCC simulator design is the SCU&DCU functional test. SBCC simulates only the FPU interface behaviour, without link between each part. There is no need to reach the actual performances of those subsystems.

SBCC will be used by DCU/SCU designers when they assemble the electronic modules..

SBCC will be used by the RAL and the ESA.

Two SBCC simulators will be build.

3.2 Simulator hardware specifications

3.2.1 Generalities

Figure 3 describes the SPIRE FPU subsystems to simulate and gives an overview of DCU/SCU main modules. Those subsystems are:

- The three bolometers arrays from the photometer detector.
- The two bolometers arrays from the spectrometer detector.
- The bolometer arrays from the thermometry detector.
- The 2 temperature stabilization heaters
- The 19 temperature probes (CERNOX) for the thermometry. They are 10 primes and 9 redundant temperature probes.
- The electrical elements of the cooler. Those elements are 4 temperature probes (CERNOX) and 3 heaters (2 gas switch and 1 charcoal pump). The nominal group is doubled with a redundant one.
- The black bodies for the calibrator. There are 2×2 black bodies for the spectrometer (prime and redundant), and 2×1 black bodies for the photometer (prime and redundant).

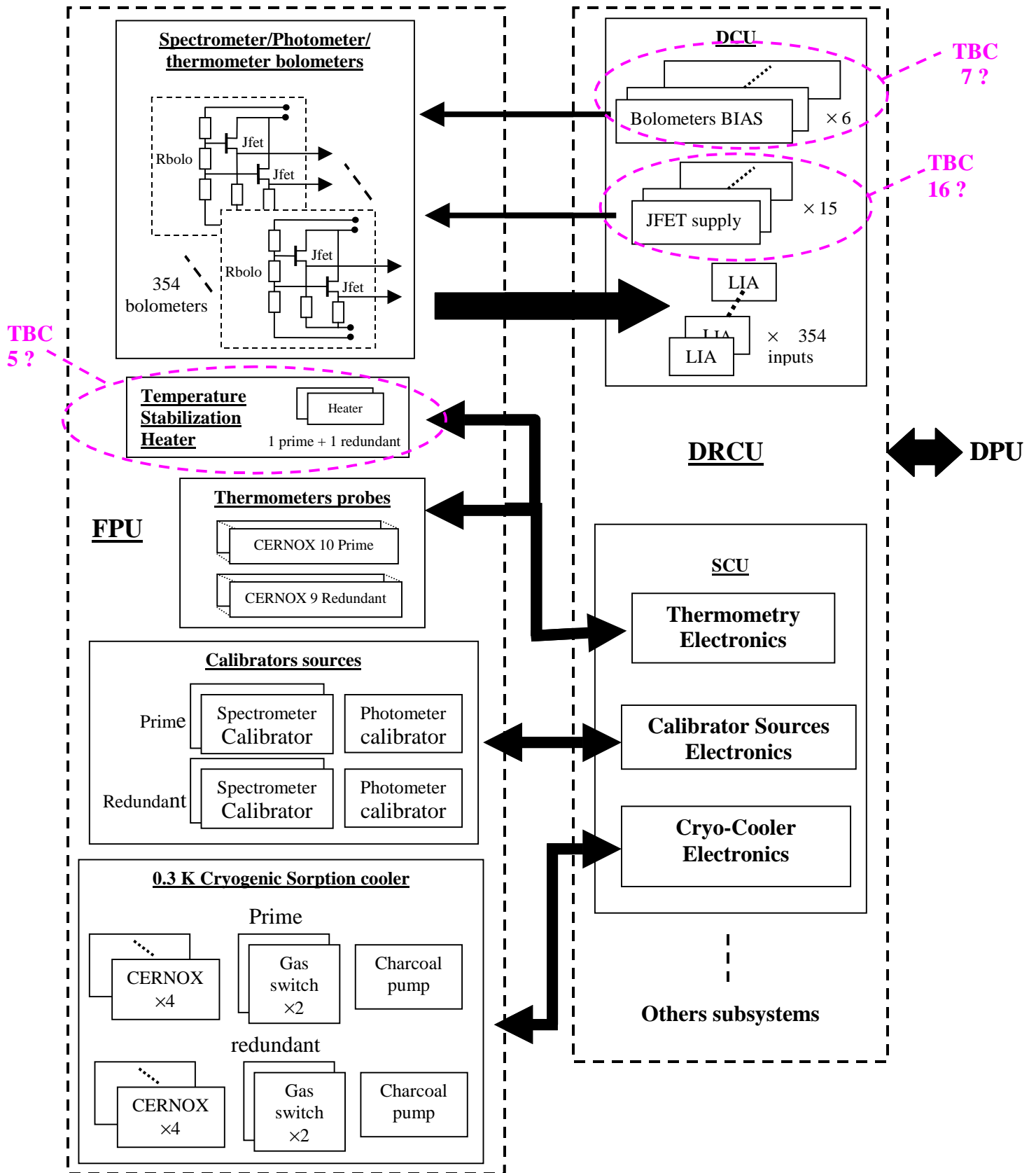The following subsections are going to specify those subsystems for the simulation.

Figure 3 : DRCU block diagram

3.2.2   Bolometers/JFET simulation and control measurements

3.2.2.1   Bolometers arrays and JFET descriptions

To understand what the simulator has to do, a description of the bolometers is needed. A synoptic of the bolometers organisation is depicted in **Figure 4**, there are:

- The **P250** array including 144 bolometers which belongs to the Photometer. The spectrum sensitivity is around 250nm.
- The **P350** array including 93 bolometers which belongs to the Photometer. The spectrum sensitivity is around 500nm.
- The **P500** array including 48 bolometers which belongs to the Photometer. The spectrum sensitivity is around 250nm.
- The **T/C** array including 3 bolometers. This group is for thermometric applications, it is included in the photometer.
- The **SSW** array including 42 bolometers which belongs to the Spectrometer. It is sensitive to the IR waves at high frequencies.
- The **SLW** array including 24 bolometers which belongs to the Spectrometer. It is sensitive to the IR waves at low frequencies.

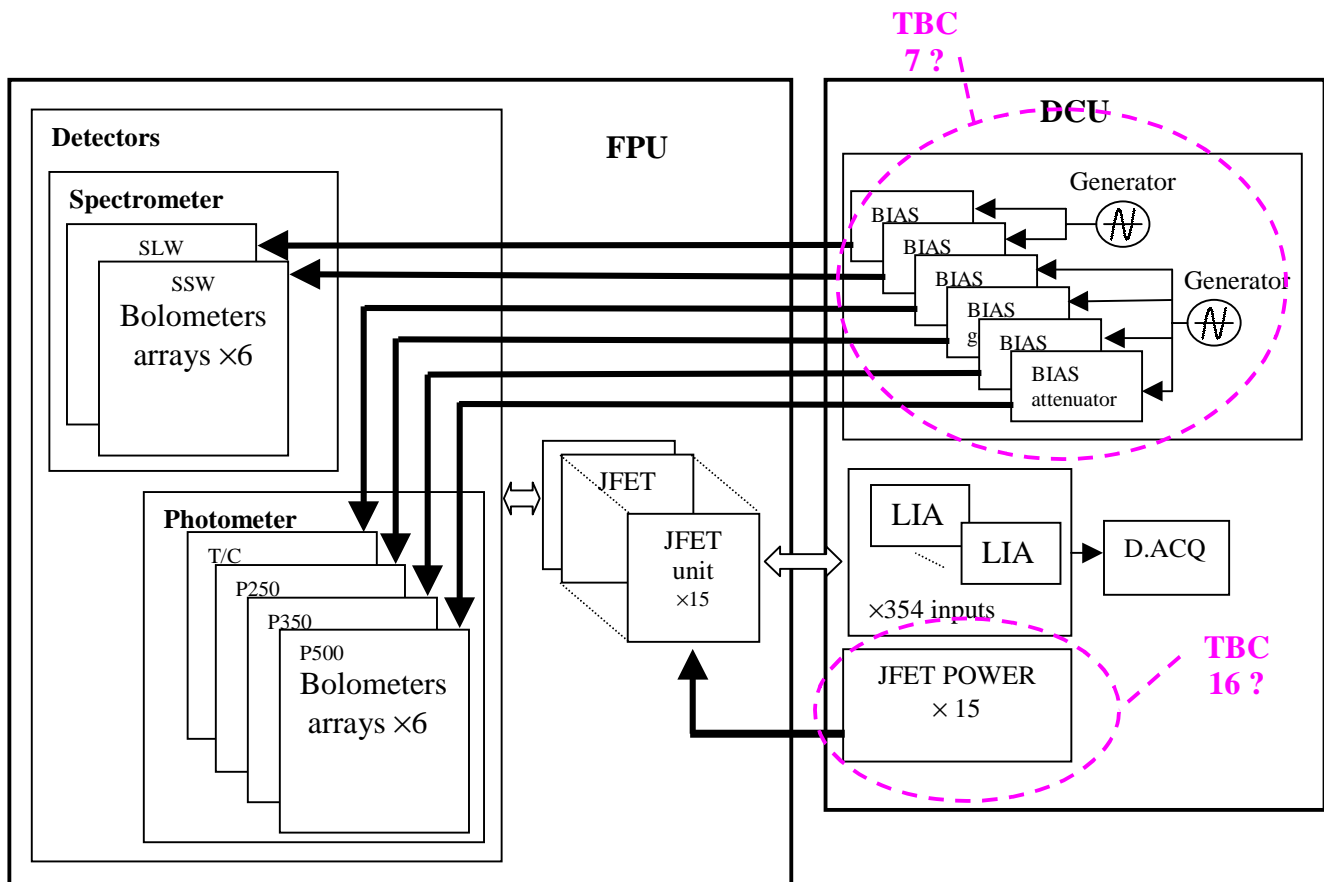The bolometers total number is 354.

Figure 4: *Bolometers arrays overview*

After the 354 bolometers, there are 15 JFET units (TBC). One unit includes 24 JFET differentials buffers (6 JFET are not used in the SSW). One bolometer is connected to a JFET buffer, its output goes toward a LIA input.

The DCU provides 15 (16 ? TBC) power supply for the JFET box and 6 (7 ? TBC) bias for the bolometers arrays.

The detail view of one of the 354 bolomoter analog channels is represented **Figure 5**. A bias generator provides a balanced sinusoidal signal for the bolometer. The bolometer resistor variations between TBD min and 5 MΩ generates a modulated signal toward the JFET buffer. This signal is demodulated by the LIA. The JFET buffer is supplied by adustable +4V/- 5V DC voltages (TBC).
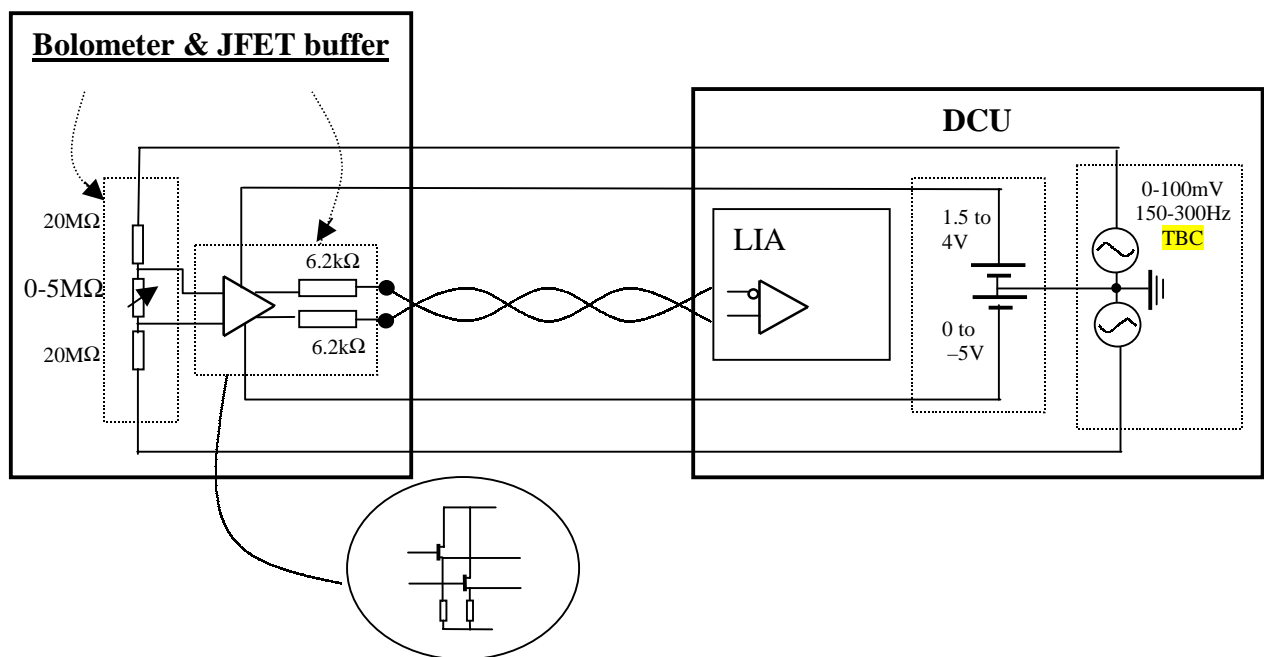

Figure 5: *View of bolometer readout with equivalents schemes*

3.2.2.2 *Bolometers/JFET simulation*

SBCC simulates the behaviour of the photometer and thermometer (288 bolometers) or the spectrometer (66 bolometers). To do so:

- Fixed resistors are connected to the sinusoidal bias signals to simulate the bolometers arrays loads.
- Fixed resistors are connected to the JFET power supply signals to simulate the JFET units loads
- SBCC generates 288 analog differential datas for the photometer/thermometer or 66 analog differential datas for the spectrometer. The datas sets to generate are defined in a input file (see subsection 3.3) which is loaded in the simulator. A new set of 288 or 66 datas is output automatically every 1 second or when the trigger NB is detected

(maximum speed 100Hz). Two different bolometer pictures can be generated alternatively by this way.

The simulation of the resistors for the bias or power supply is discussed in the subsections 3.2.2.3 about the bolometers/JFET measurements.

The simulator electrical model for one bolometer is represented **Figure 6**.
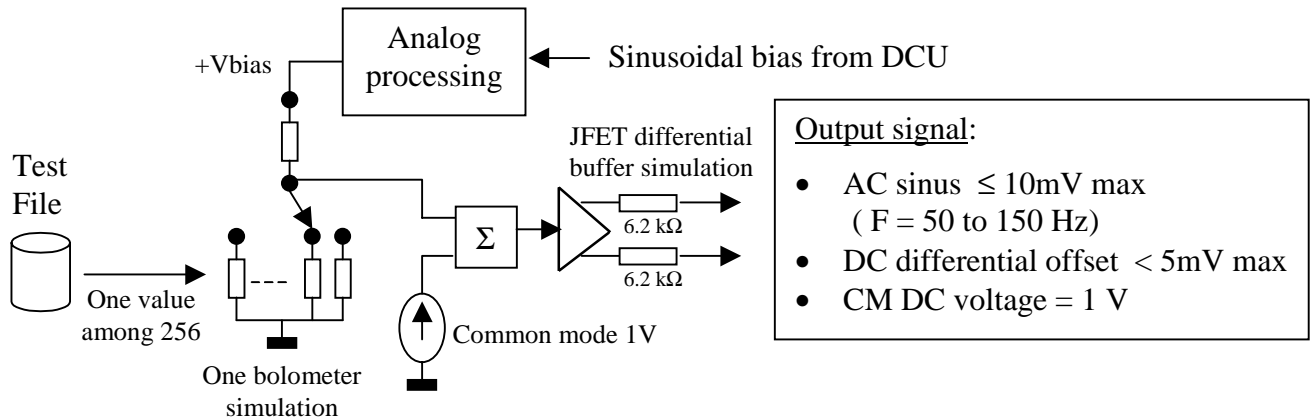

Figure 5: *Bolometer electrical model to simulate*

For each bolometer, SBCC can choose one resistor among 256 values. The set of 256 resistors is fixed and the same for all the bolometers. The resistors choices to output are defined in the input file.

3.2.2.3   Bolometers/JFET measurements

The simulator has to measure:

- The frequency and amplitude of the sinusoide for the bolometers biasing.
- The DC power supply for the JFET units.

All those measurements are done on the load resistors which simulate the bolometers arrays or the JFET units. There are repeated every 1 second.

3.2.2.3.1   Bolometers bias measurements

There are six bias for six bolometers arrays. The aim of the measure is to check the 6 (7 ? TBC) bias working with actual resistors loads.

The main characteristic of the bias signals to measure are:

- Balanced sinusoidal signal.
- Amplitude between 0 and 200 mV for the photometer and the spectrometer.
- Amplitude between 0 and 500 mV for the T/C.
- Frequency between 50 and 150 Hz

The table below gives the load resistors values of the 6 bolomoters arrays.

Array	Number of bolometers	Indicative load resistor (TBC)
P250	144	276 kΩ (= 40 MΩ / 144)
P350	93	430 kΩ (= 40 MΩ / 93)
P500	48	832 kΩ (= 40 MΩ / 48)
T/C	3	13333 kΩ (= 40 MΩ / 48)
S-SW	42	952 kΩ (= 40 MΩ / 42)
S-LW	24	1666 kΩ (= 40 MΩ / 24)

The frequency measurements are done with a 5% accuracy and the magnitude measurements are done with a 1% accuracy.. They are converted into 8 bits numerical datas.

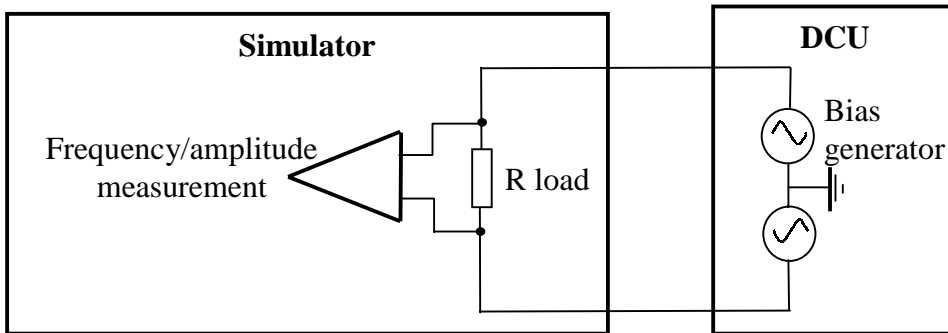A synoptic of the measurement principle is depicted **Figure 7**.

Figure 7: *Bolometers bias measurements*

3.2.2.3.2 JFET bias measurements

There are fifteen (16 ? TBC) +4V/-5V power supply generators for fifteen JFET units. The aim of the measure is to check the 15 power supplies working with actual 1 kΩ resistors loads. This lead to 30 voltage measurements.

The main characteristic of the power supplies to measure are:

- Nominal voltage = +1.5V to + 4V for Vdd and 0V to -5V for Vss
- Nominal current = 4.5 mA for Vdd /Vss (Maximal current = 5 mA for Vdd /Vss)

A synoptic of the measurement principle is depicted **Figure 8**. The realised measurements are Vdd and Vss. There are converted into two 8 bits numerical datas.
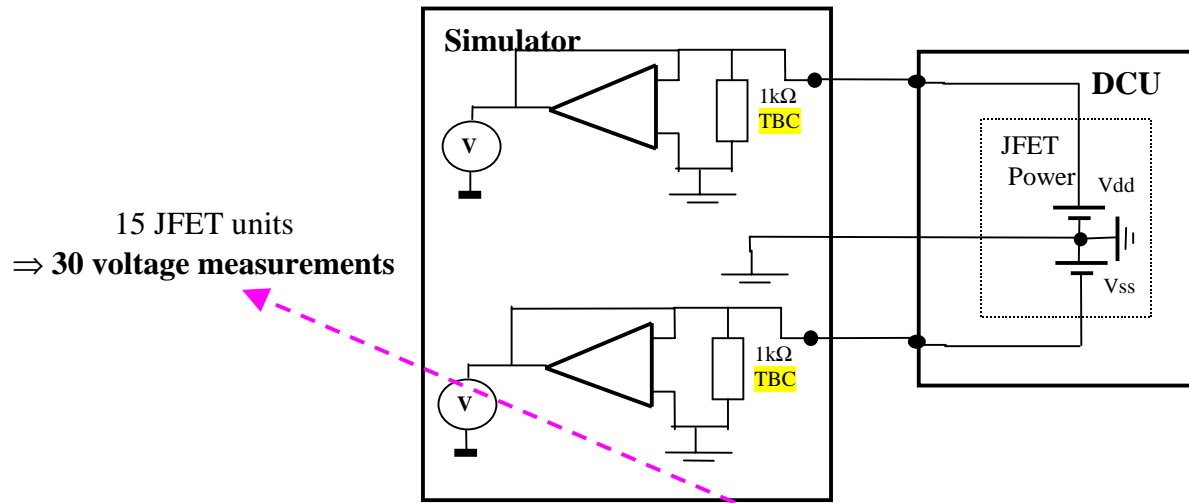
Figure 8: *JFET power supply measurements (**TBC**)*

3.2.3 *Cooler simulation and control measurements*

SBCC simulates the behaviours of the cooler electrical elements. There are:

- 6 temperature probes CERNOX (3 primes and 3 redundants) supplied by 1 µA DC currents. One temperature probe is a resistor equipped with 2 supplies and 2 measurements wires. The resistor is not grounded. The resistor value changes with the temperature, this information is controlled with a voltage measurement. A temperature probe is simulated by 4 fixed resistors which are selectable, their values are TBD for each kind of probe.

- 2 temperature probes CERNOX (1 prime and 1 redundant) supplied by a 100 nA (TBC) sinusoidal current – frequency = TBD. Those 2 temperatures probes are the same than the 6 previous ones. Their values are TBD.

- 4 gas switch and 2 charcoal pump (3 primes and 3 redundants). Those 6 elements are heaters. A heater is a fixed $400\,\Omega$ resistor supplied by a 0/35 mA DC current for a charcoal pump and a 0/1.6 mA (TBC) DC current for a gas switch. A resistor is not grounded.

SBCC measures :

- The bias currents for the 6 DC temperature probes and 6 elements heaters. The measurements are converted into 8 bits numerical datas.
- The amplitude voltages for the 2 AC temperature probes. A measurement is converted into 8 bits numerical datas.
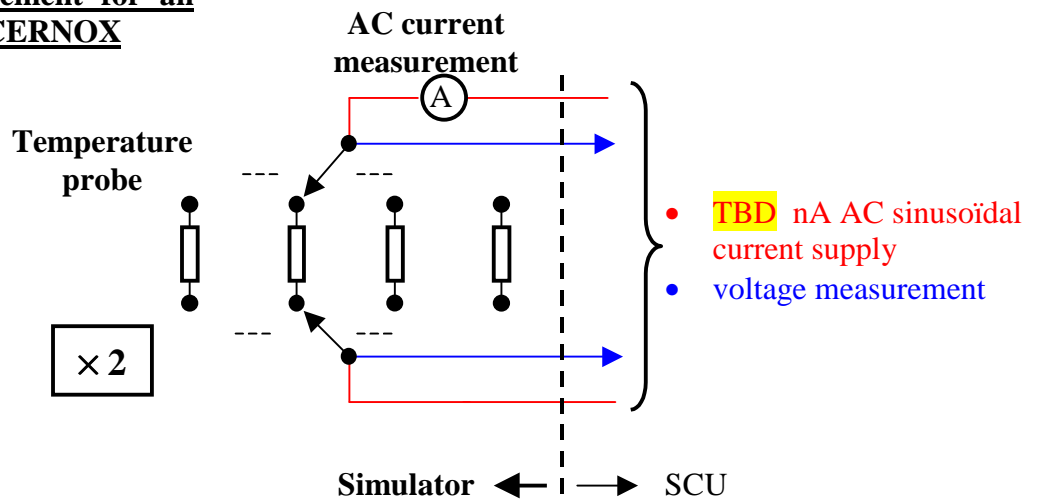
Those measurements are done every 1 second

The simulations and measurements of the cooler electrical elements are depicted in **Figure 9**.

Simulation and measurement for DC a temperature probe CERNOX
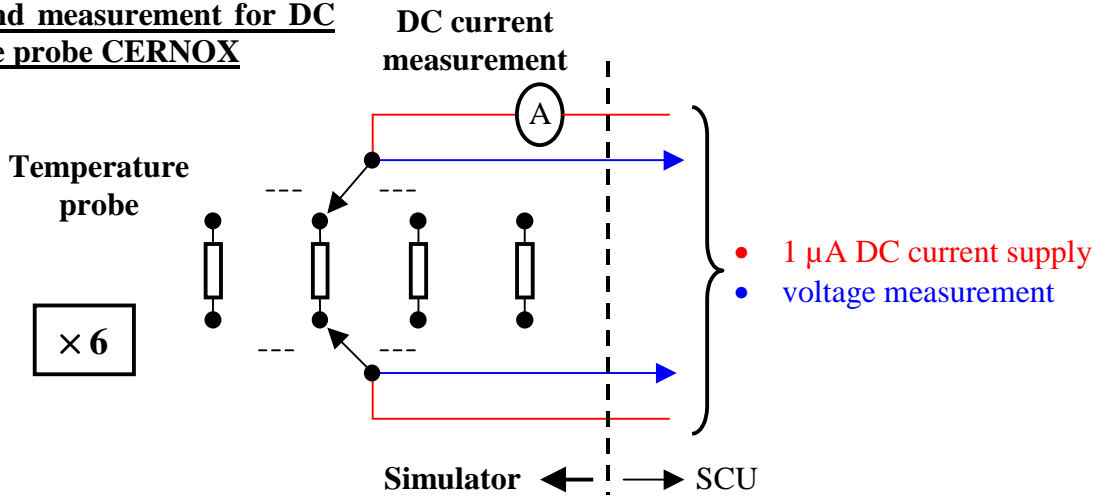
Simulation and measurement for an AC temperature probe CERNOX

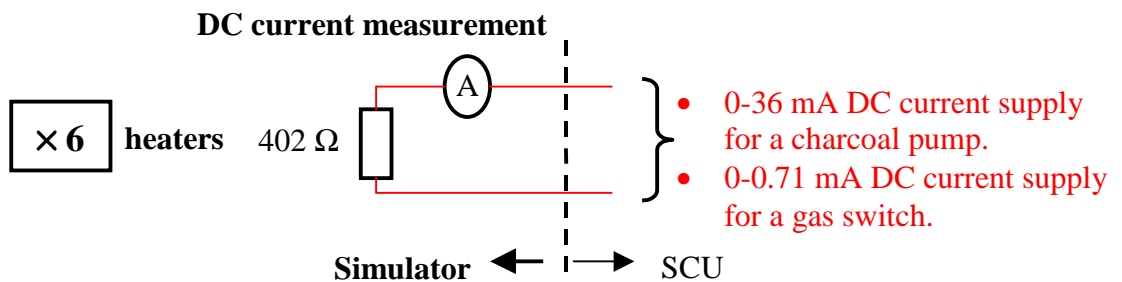**Simulation and measurement for a heater**

Figure 9: *Cooler electrical elements synoptic*

3.2.4   Calibrator simulation and control measurement

The simulators for the calibrators are split in two parts as it is represented **Figure 10**.

The first part gathers the 4 black bodies heaters for the spectrometer. A heater is a 1 kΩ to 10 kΩ (TBC) resistor which is supplied with a 0 to 1mA DC current (adjustable by a 8 bits DAC). The resistor is not grounded and is connected with a 4 wires technique.

The second part gathers the 2 black bodies heaters for the photometer. A heater is a 1 kΩ to 10 kΩ (TBC) resistor which is supplied with a 0 to1mA DC current (adjustable by a 8 bits DAC). This current can change at the frequency of 5 Hz max. The resistor is not grounded and is connected with a 4 wires technique.

SBCC has to measure:

- The DC bias currents for the 4 spectrometers black bodies. The measurements are converted into 8 bits numerical datas.
- The DC bias currents amplitudes for the 2 photometers black bodies. An amplitude measurement is converted into a 8 bits numerical data.. A particular trigger can order this measurement in slave mode (maximum speed: 5Hz).

Those measurements are done every 1 second (TBC) in nominal condition.

Simulation and measurement for spectrometer black bodies
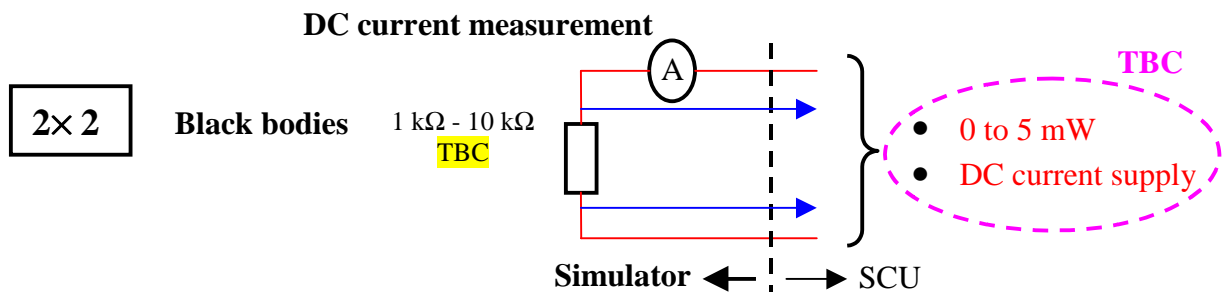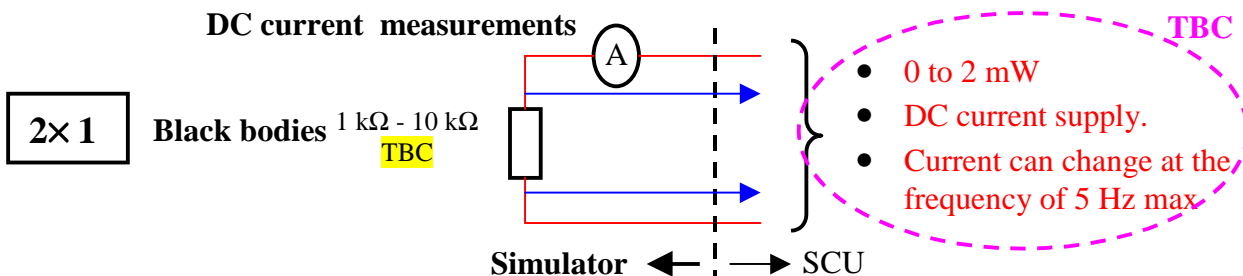

Simulation and measurement for photometer

Figure 10: *Calibrators electrical elements synoptic*

3.2.5 *Thermometry simulation and control measurements*

SBCC simulates the behaviour of CERNOX temperature probes which are used for thermometry applications in the FPU. The temperature probes for the cooler are not included in the thermometry – see cooler subsection.

There are 19 DC CERNOX temperature probes : 10 primes and 9 redundants. Those temperatures probes are the same as the ones describe for the cooler. Their values are TBD. One probe is supplied by a TBD µA DC currents.

SBCC measures the DC current for each temperature probe. A amplitude measurement is converted into 8 bits numerical datas. Those measurements are done every 1 second (TBC).

Figure 11 describes the simulations and measurements of one DC CERNOX temperature probe.

Simulation and measurement for DC temperature probes CERNOX
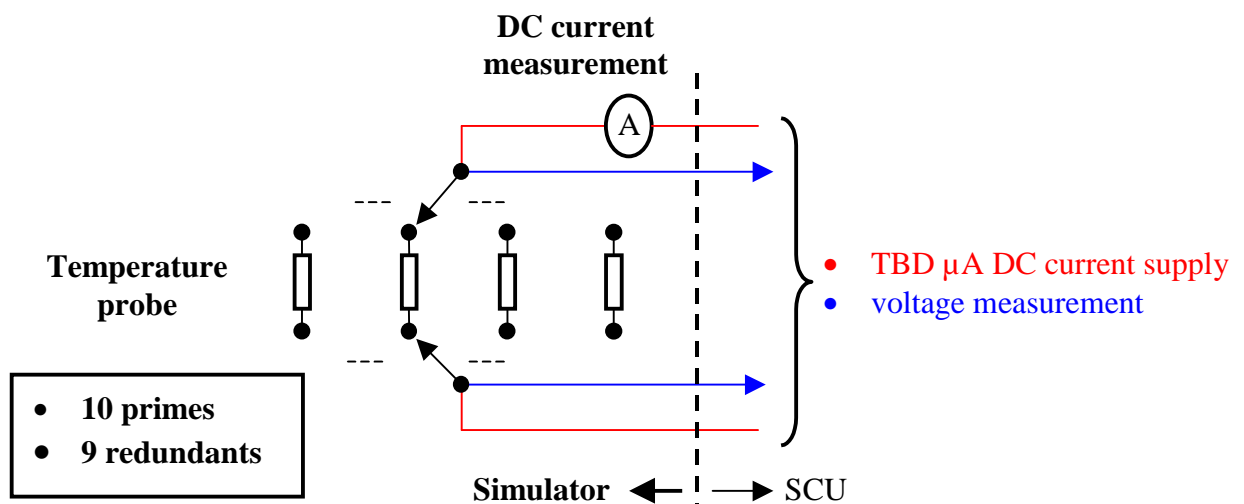
Figure 11: *Thermometry electrical elements synoptic*

3.2.6 *JFET hearters*

SBCC simulates the behaviour of 2 (5 ? TBC) resistors heaters for the JFET (1 prime + 1 redundant). The resistors are supplied by DC currents, the resistor are not grounded.

SBCC measures the DC current for each temperature probe. A amplitude measurement is converted into 8 bits numerical datas. Those measurements are done every 1 second (TBC).

Figure 12 describes the simulations and measurements of one JFET heater.

Simulation and measurement for JFET heaters

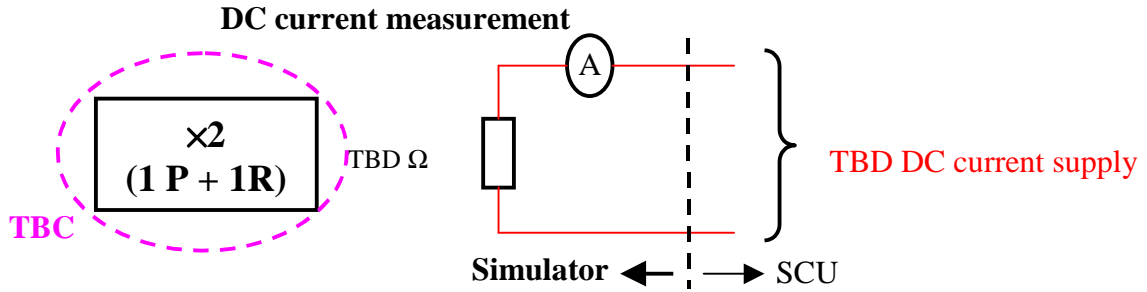**DC current measurement**

Figure 12: *Electrical JFET heater synoptic*

3.3 Simulator software and working specifications

3.3.1 Generalities

The simulator includes a PC computer with a software which supervises SBCC work. SBCC simulator is depicted in **Figure 13**.

The main software features can be summarised in four points:

1. The software is developed with LABVIEW. The operating system is WINDOWS 98 (TBC).
2. The user's software interface allows to configure the two SBCC working modes. Those two modes are the stand alone and slave modes.
3. The datas about the generated signals with SBCC are defined in an input file.
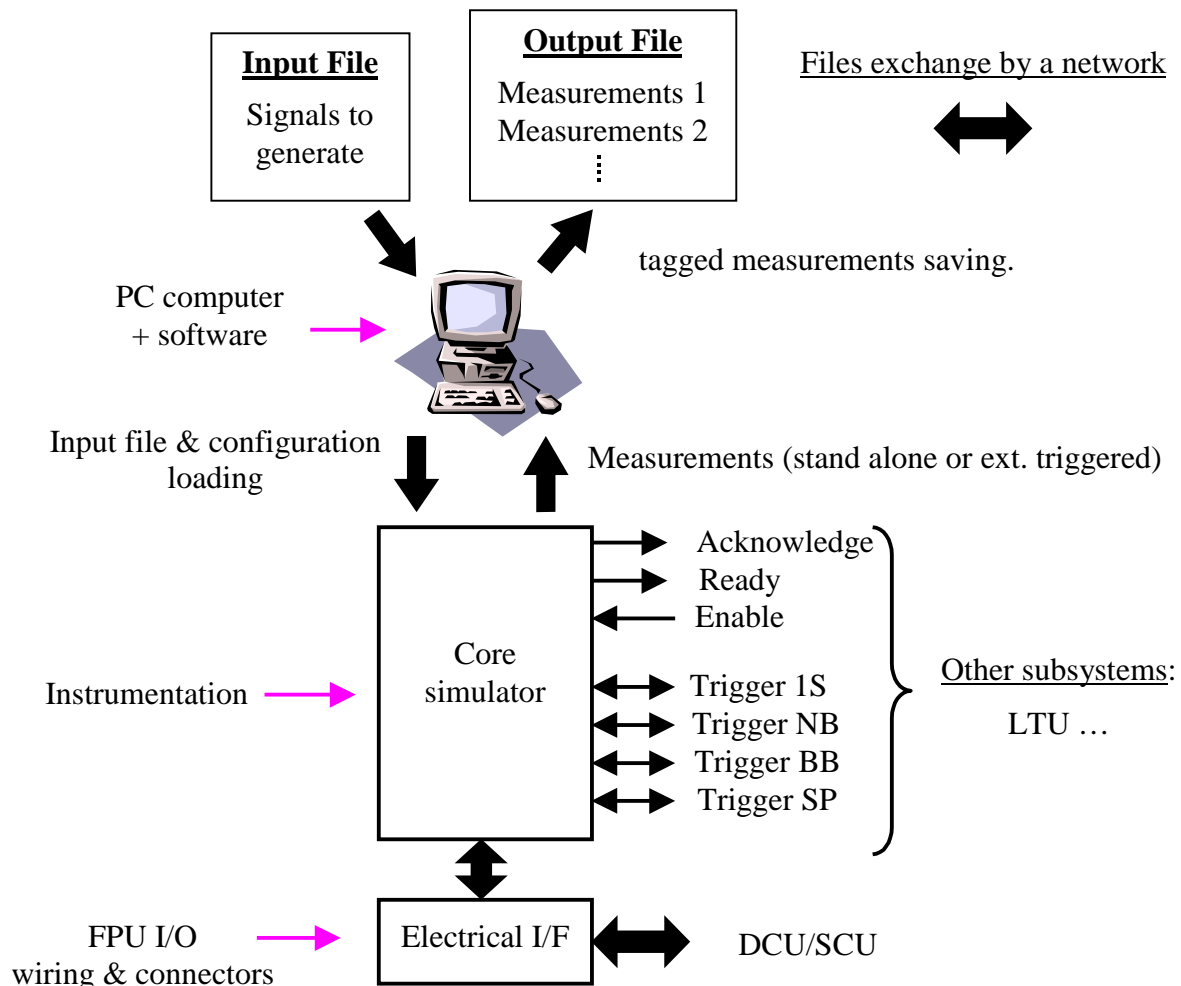4. The measurements done by SBCC are saved in an output file.

Figure 13: *SBCC simulator and software*

3.3.2   The program

The program runs on a PC (the supervisor of the simulator).

The program allows to set up the simulator core. That means you can download datas from the input file to the simulator core and assert a ready signal.

You can chose with this software between two functional mode : stand alone or slave modes. A user's software interface includes several windows which allow the simulator configuration. It allows also the visualisation of the measurements done by the simulator when they are saved in a output file.

During a nominal test sequence, the programs gets measurements from the simulator core every on second. They are saved in an output file, and an acknowledge pulse is generated.

3.3.2.1   Stand alone mode

The simulated bolometers signals and the measurements begin after a software start command or an enable hardware signal when the ready is set.

In this mode, the simulator doesn't care about the test bench. The measurements and the simulated bolometers signals are periodically refreshed :

- The trigger1S is generated every one second to do "one second measurements". When measurements are done and saved, an acknowledge pulse is generated.
- The triggerBB is generated when a new black body measurement is done. In stand alone mode, triggerBB equals trigger1S, black body measurements are part of "one second measurements".
- The triggerNB is generated when new bolometers signals are set.

The trigger SP is a spare signal.

3.3.2.2   Slave mode

The simulated bolometers signals and the measurements begin after the ready signal an enable hardware signal.

When the simulator receives a triggerNB or a software command, it set new bolometers signals according to the input file.

When the simulator receives a trigger1S, it performs measurements "one second measurements". When measurements are done and saved, an acknowledge pulse is generated.

When the simulator receives a triggerBB, it performs black bodies measurements. When measurements are done and saved, an acknowledge pulse is generated. TriggerBB has the priority on trigger1S.

The trigger SP is a spare signal.

3.3.3   The Input file

The Input file is an ASCII file which contains data to simulate such as impedance value of each bolometers or group of bolometers (TBD), impedance value of temperature probes …You also choose between the photometer or the spectrometer.

A specific format for this file will be define. The users of the simulator have to write or generate input files in agreement with this format. An input file example is shown below, it is only indicative.

The Input file can be send from the test bench to the simulator through the network.

```
-- comment
# date
# file name

#Photometer
0 -- active, 1 inactive
#group1
#subgroup1
-- identifier resistor_value_in_megaohm --in decimal--
bolo1 4,5 4,2 4,3
bolo2 4,5 4,3 4,3


boloN 5.2 5.2 5.1
#subgroup1
-- identifier resistor_value_in_megaohm --in decimal--
therm1 4,5 4,5 4,5

thermN 4,5 4,5 4,5

#Spectrometer
1 -- inactive, 0 active
#group1
#subgroup1
-- identifier resistor_value_in_megaohm --in decimal--
bolo1 4,5 4,2 4,3
bolo2 4,5 4,3 4,3


boloN 5,2 5.2 5.1

#end
```

3.3.4   Output file

This is an ASCII file which contains results of measurements such as bias voltage and frequency, power supplies…

This file is generated by the simulator. A user can get this file through the network. An output file example is shown below, it is only indicative:

```
--comment
# date
# file name

--first acquisition
#1
identifier value-
bias_volt 4,5 4,2 4,3 0 0 0  -- in V
bias_freq 200 180 250 0 0 0 – in Hz
jfet_power_supply 3,2 … –in volt
```

```
DC_temperature_probe 1,1 1,1 1,3 1,4 0 0 0 – in µVDC_temperature_probe X Y – in A
Heaters_current 33 32 12 35 1.1 1.2 …. – in mA
DC_black_body_current 0,3 0,4 0,5 0,7 … – in  mA
JFET_heaters 1.2 …. in  mA

--acquisition number n
#N
identifier value-
bias_volt 4,5 4,2 4,3 0 0 0  -- in V
bias_freq 200 180 250 0 0 0 – in Hz
jfet_power_supply 3,2 …. –in volt
DC_temperature_probe 1,1 1,1 1,3 1,4 0 0 0 – in µVDC_temperature_probe X Y – in A
Heaters_current 33 32 12 35 1.1 1.2  … – in mA
DC_black_body_current 0,3 0,4 0,5 0,7 … – in  mA
JFET_heaters 1.2 …. in  mA


#end
```

3.4 Simulator mechanical specifications and EMC

The explanations given in this subsection are only indicative and result from a worst case analysis. It does not mean the simulator is going to be exactly package according to those explanations. The goal is to lay down a principle.

The simulator is packaged in an enclosure of :

- height = 1400 mm = 29U (1U = 44,45 mm)
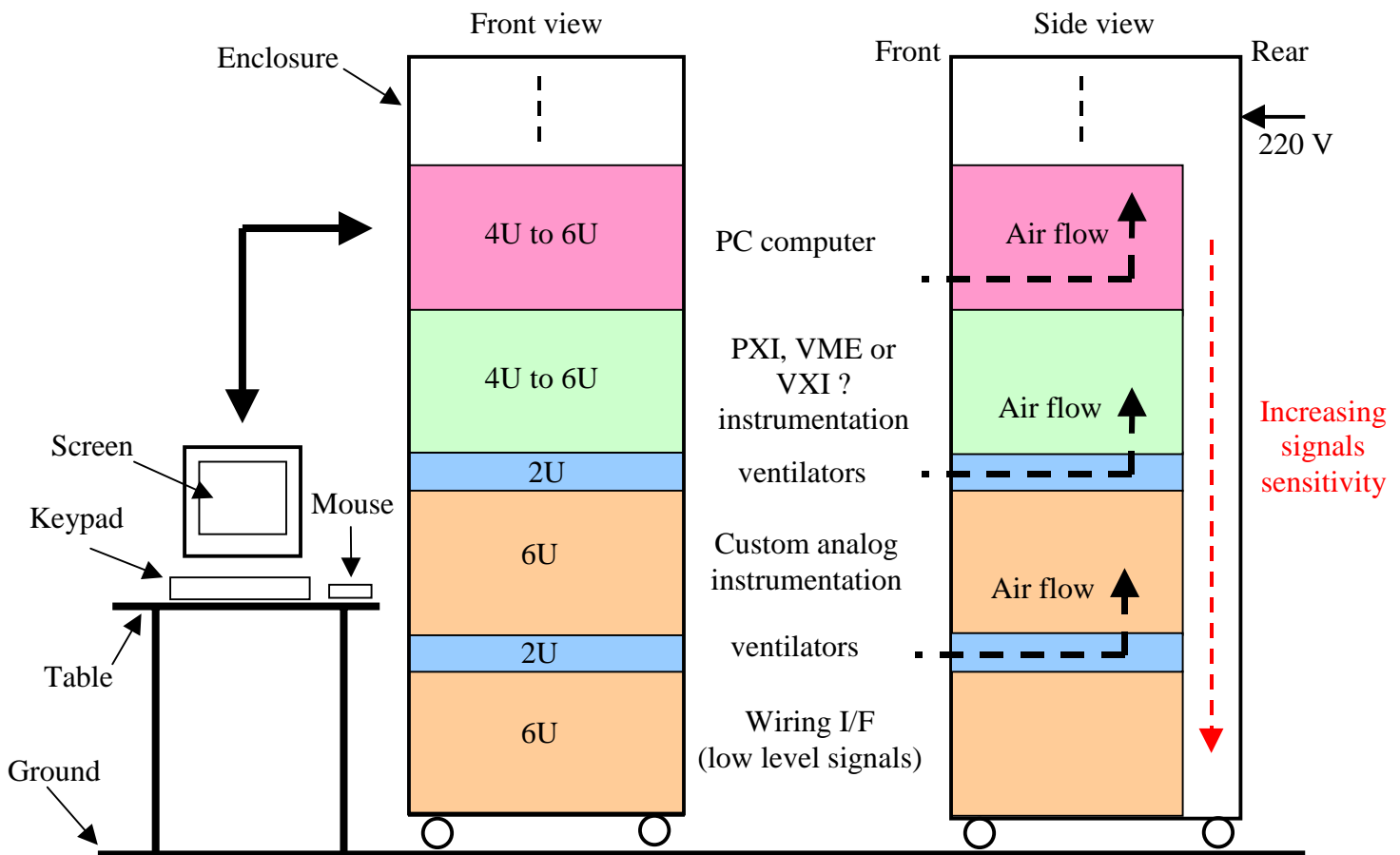- width = 600 mm (for 19"standard chassis)
- depth = 800 mm

Figure 14: *Simulator enclosure view*

The simulator enclosure includes:

- A PC computer chassis (TBC) - Size = 4U to 6U, 19".
- A PXI,VME,VXI … etc (TBD) chassis- Size = 4U to 6U, 19".
- A chassis dedicated to analog custom subsystems of the simulator - Size = 6U, 19".
- A chassis dedicated to wiring interface with DCU/DCU - Size = 6U, 19". The I/F includes two subinterfaces which are identical except for connectors :
  - ✓ The first uses actual cables between the FPU and DCU/DCU. The connectors type is (TBD).
  - ✓ The second uses other cables dedicated to DCU/DCU tests. The connectors type is (TBD).
- Two ventilators chassis to cool the simulator enclosure - Size = 2U, 19" for one ventilators chassis.

All the chassis are consistent with standard EMC rules (TBD).

The simulator enclosure is mounted on 4 rollers to be moved easily.

The computer screen, the keypad and the mouse stand on the side of the simulator enclosure, on a table provided by the user's simulator. There are not inside the enclosure.

The simulator is supplied with 220 V / 50 Hz.

A view of the simulator enclosure is depicted in **Figure 14**. The enclosure organisation is consistent with standard EMC rules.

4   Documentation

A user's manual will be delivered with each SBCC simulator.