SPIRE-RAL-PRJ-00624

10th April 2001 version updated in brown
24 August, 2001

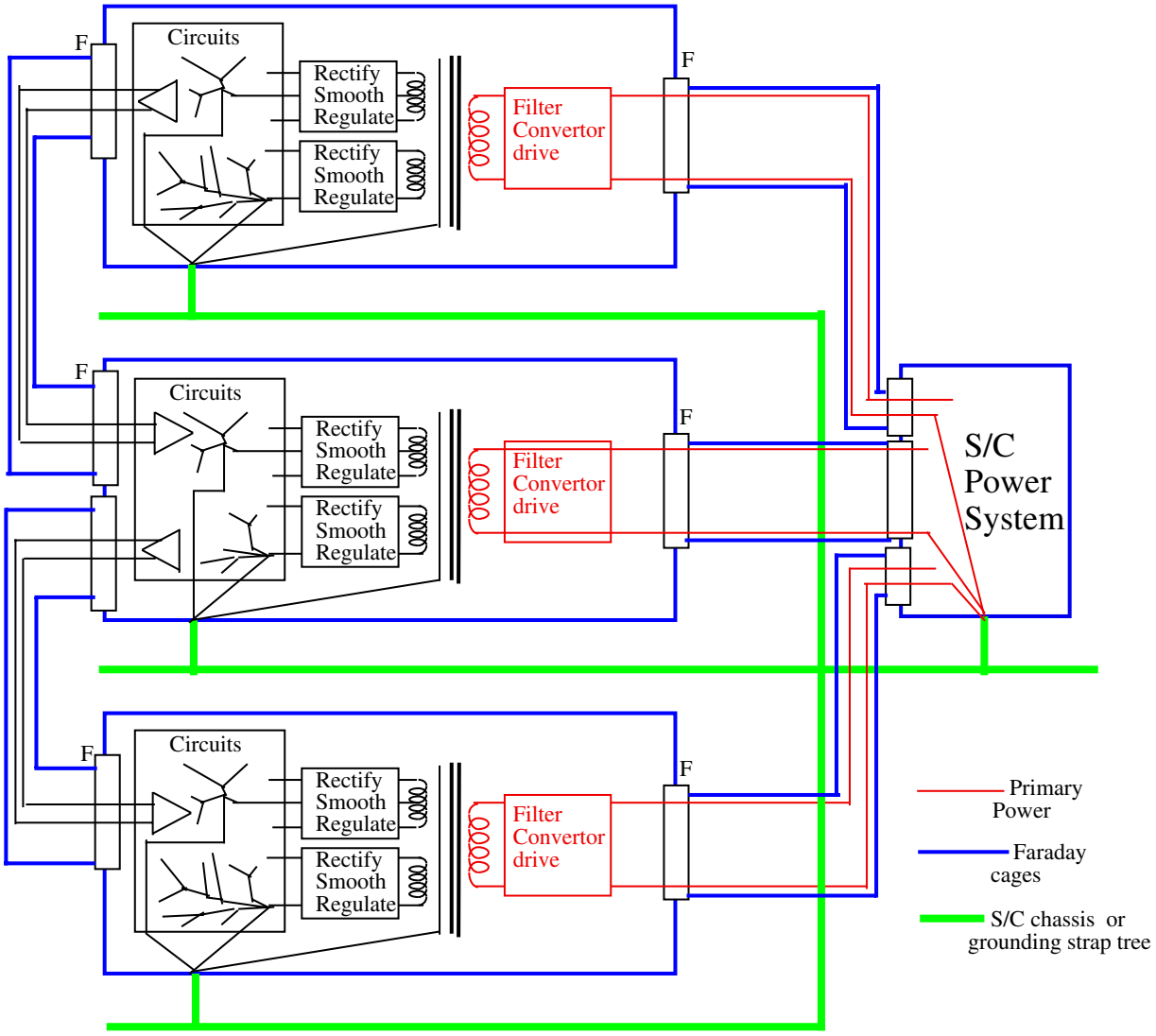
To: SPIRE Electronics +Sam(Thermal)+Berend(Structural Isolation), +Lionel (Cooler isolation/resistance)

From: John Delderfield

GROUNDING and SCREENING PHILOSOPHY

This note writes out the SPIRE grounding requirements explicitly, particularly as regards the bolometer systems. Requirements on the electronics are in red text. To present a perspective that is hopefully coherent, the rationale will be included. I appreciate that this will be a restatement of what is already clear to many recipients or regarded as good practise.

In general terms SPIRE shall conform to an ESA classical unit by unit secondary power configuration of this nature:



Each unit is electrically self-contained in its grounding.

- It has a chassis/box that is closed to form a conductive Faraday cage, i.e. enough thickness in skin depths/bulk conductivity (essentially inevitable) and with all apertures including vents and joints having controlled geometry with adequately small maximum dimensions.
- Except the S/C power system, primary power is isolated from chassis, although for each unit there is a small permissible input capacitance and possibly a large electrostatic protection resistor to chassis.
- Each unit is powered with secondary (or conditioned) power which is isolated from the primary power buses and unipoint grounded via a link to unit chassis, a joint which is best made near the same point on the chassis as is externally connected to S/C. Signal grounds are typically the same as or decoupled to such secondary grounds and the same rule applies. This internal link may need to be via an externally accessible strap to permit secondary ground isolation testing.
- All signal inputs and outputs are differential and ideally pass through filter connectors to protect the unit from external noise entering the unit via harnesses. Signal ground lines do not pass between units. Inputs are normally high impedance and are required to maintain a defined high impedance w.r.t. chassis. Outputs are required to have controlled slew rates, minimum skew to limit common mode spikes, and little ringing.
- The secondary grounds with each unit are carefully configured in a documented way and if multiple supplies are used the grounds for each supply are separately controlled with a minimum of joins between the supplies, classically just one at the unit unipoint.
- Theoretically there should be no current flow in any ground wire, which should only be used for signal voltage reference, but in unipolar supply situations, when 0V and signal ground are one and the same, current flow is unavoidable. This is just one example of the general requirement that any device taking a.c. current shall have adequate local decoupling/filtering, obviously to ensure its own correct operation, but also adequately to inhibit noise propagation to other elements in the unit; logic or digital functions can be the most troublesome with their a.c. components taking the form of switching noise.
- Depending on the susceptibility of circuits, logic signals that travel a distance across a unit may need to be slowed down with series resistors and squared up again on receipt by Schottky buffers such that excessive dV/dT noise is not broadcast.

There are several relaxations in the ideal that are commonly acceptable. Filter connectors introduce their own problems and the careful specification of input susceptibility and output emission levels often allows requirements to be met with un-filtered connectors. In such a cases, common mode filtering with defined differential mode bandpass is often introduced on signal inputs to compensate. Formal unipoint strapping to a S/C grounding tree is often discarded and a unit is simply conductively mounted by all of its mounting feet…..this is no problem as long as no other equipment is returning current along the S/C chassis and potentially thus inducing a.c. signals in the unit's Faraday cage.

On the other hand, there are many options for improving the operation of such standard configuration, to further limit the propagation of noise between elements inside it.

- internal division into a card rack and a compartment housing the noisy power supply with bulkhead filters between the two.
- improving the Faraday shield with thin metallic inter-board shields or even formal internal divisions with bulkhead filters. Such shields are often used if frequencies are being multiplied and shifted or if one board contains logic and other only analogue {All are electrostatic screening connected solidly to unit chassis; I'll omit the less common magnetic screening from this note}
- Accepting a certain level of ground current but defeating the induced ground voltage noise by using highly conducting low inductance ground planes. Unless a special analysis is performed these should only be used in conjunction with other good practice (local decoupling, separation of grounds, chassis isolation with unipoint contact, etc.). More complex scenarios exist: ground signal planes may be combined with power supply planes, the ensemble being multiply capacitively linked; physically thicker power planes may be sandwiched into PCBs, electrically isolated from the circuits on them but firmly joined to unit chassis so as to extract power but also to double as extended Faraday screens.
- Mismatching impedances/4-wiring. Mismatch is inherent in many architectures that use low impedance drive and high impedance inputs, but I'm referring here to using high impedance

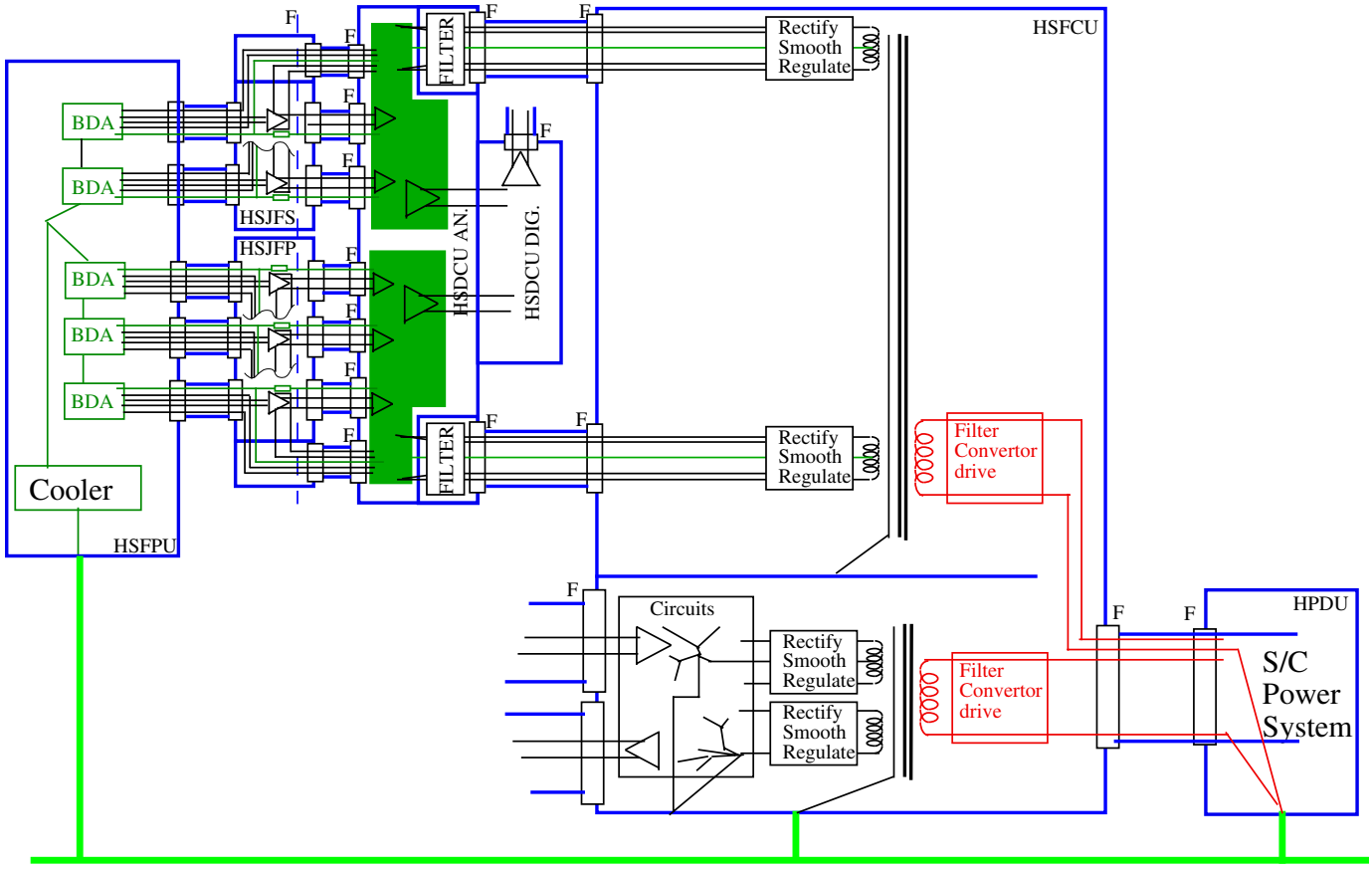
current drive into relatively low impedance input. Used with or without formal differential signals, this is another way of removing a dependance on a quiet voltage reference ground.

- Differential digital interfaces do not provide ideal isolation. In particular, the driver has to provide significant edge switching currents to drive harness capacitance, a situation that gets worse if the I/F is between units, the receiving unit inputs have capacitive filter elements, harness lengths are long and have screens, etc.. Depending on frequency, power, radiation environment and money, such interactions between supposedly separate grounds may be improved by using transformer coupled buses or opto-couplers.

The whole arrangement so far described is prefixed by "in general terms". The configuration is best suited to systems in which each unit operates over a restricted range of signal level. In Spire this would apply to the HSDPU. Otherwise transmission of noise from high level circuits such as power convertors to sensitive analogue elements get more and more impossible to achieve. Considering the front-end signal source in Spire, we have an noise spec. of 7nV/√Hz at about 2.5MΩ and 300mK. There comes a point when the need to control noise requires separate preamplifier unit(s), preferably with an electrostatically screen separating it (them) from any digital functions such as multiplexors or A-D convertors, with the signals then transferring to a conventional unit via balanced digital I/Fs. The power needs to be fed to this system's analogue sections extremely quietly, prefiltered and actively regulated with external sensing in an external unit. It must then be filtered in a separate compartment within the analogue unit that has bulkhead connectors feeding to the analogue system. Grounding has to be very carefully configured as secondary grounds are implicitly distributed outside of one unit. If one considers the whole volume of the various units in this supply system as if it were joined into one by the harness screens that join them, the grounding it should look like a unipoint tree as if it were still within one unit.

Multichannel operation requires adequate interchannel screening and a configuration that keeps any designed-in signal cross-talk to below specified levels.

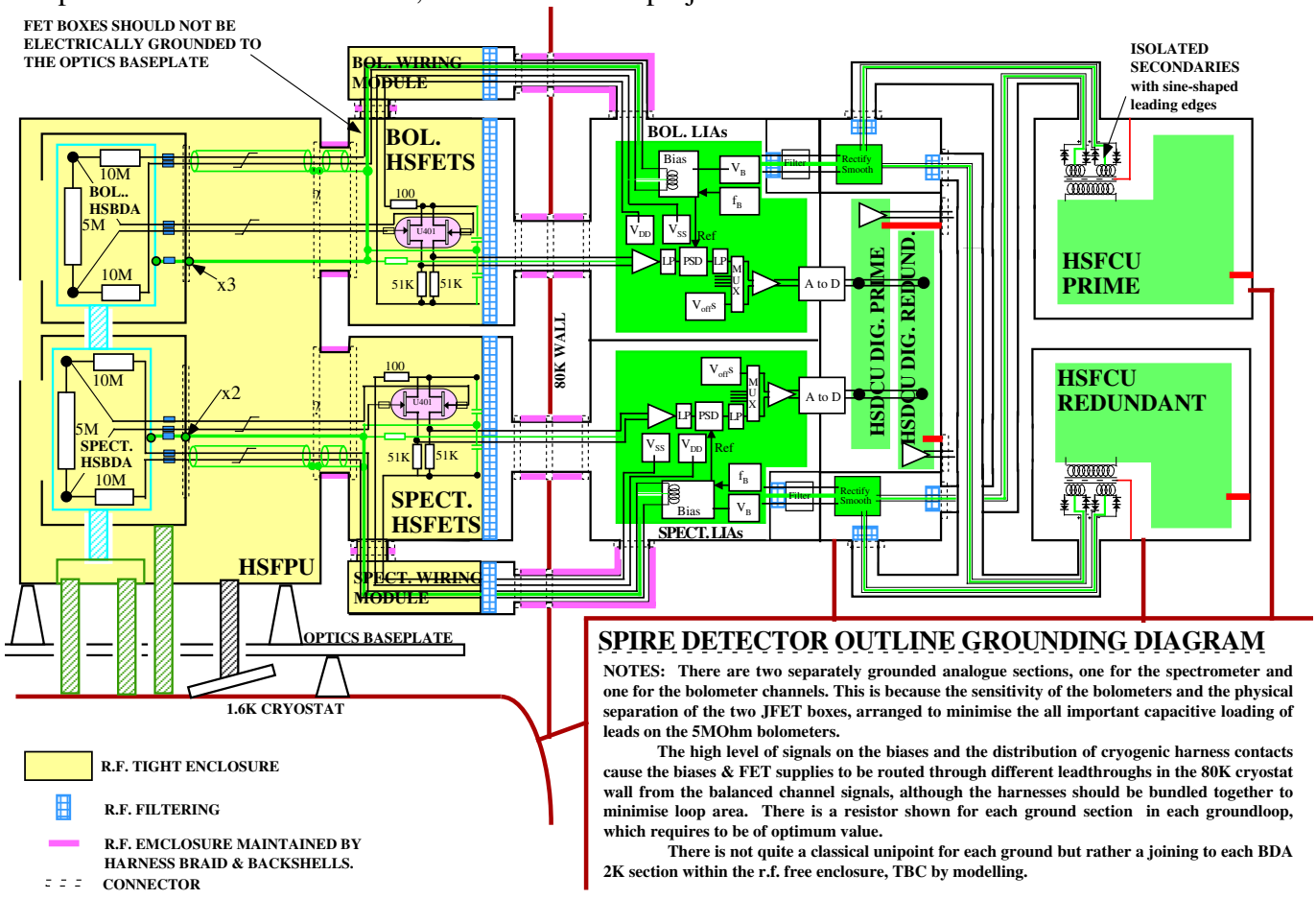
We conceived of the following concept early in the autumn of 2000, following the design decision to separate the spectrometer and photometer JFET units so they could be accommodated adequately near to their respective detectors, the specification then being <50pF along the cable as seen by each 5MΩ detector. It was also really stressed by those with experience that Spire's bolometric detectors are unbelievably sensitive and would make corrupted measurements if unwanted r.f. were to be dissipated in them, the biggest risk being that wires have to be attached to them!! So the following concept was adopted at a video conference from RAL to JPL with Christophe Cara present at the RAL end.



I've used up-to-date acronyms and ignored any redundancy in this drawing to minimise confusion. The essential specifications are:

- signal power gain from external JFET amplifiers
- separate analogue ground paths, without loops, between spectrometer and photometer systems
- maintenance of single point ground joins to S/C chassis
- analogue power, quiet and regulated, supplied from a unit external to the one that houses the sensitive analogue systems, without ground switching.
- ground-plane option invoked to keep a large area of analogue signal ground quiet in each of the spectrometer and photometer parts
- the detectors to be in a Faraday cage with full filtering on all wires entering it (non-bolometer ones not shown) extended with full shielding into the JFET boxes.
- MDM connectors on the JFET boxes not available cryogenic filtered, so a separate compartment division is introduced in the JFET boxes with ceramic feedthrough filtering to close the Faraday cage.
- unipoint analogue ground for the system at the 300mK BDA units that are unavoidable coupled with cold-plumbing busbar ink. This minimises Voltages between the bolometers and their local chassis.
- information transfer out of the digital part of the HSDCU via normal balanced ESA-type digital interfaces, both fast and slow, to the HSDPU (not shown but having its own separate conventional grounding scheme).
- The need to bundle together groups of long harnesses between HSJFETs and HSDCU (not shown here but see instrument block diagram) to minimise loop area between bias routed analogue ground lines and differential signal lines. Admittedly they are inside shielded harnesses but one cannot have much common mode signal at the DCU's inputs even with good CMRR before a 7nV/√Hz differential noise performance is degraded.
- An optimised multiplexing/transfer of data from the analogue sections of the DCU to the back-end digital ones to minimise current injection back into the analogue ground and hence potentially back to the detectors.

With all the above in mind, and having seen some circuits for the DCU, the following grounding scheme was published in November 2000, was circulated to project:



SPIRE DETECTOR OUTLINE GROUNDING DIAGRAM

NOTES: There are two separately grounded analogue sections, one for the spectrometer and one for the bolometer channels. This is because the sensitivity of the bolometers and the physical separation of the two JFET boxes, arranged to minimise the all important capacitive loading of leads on the 5MOhm bolometers.

The high level of signals on the biases and the distribution of cryogenic harness contacts cause the biases & FET supplies to be routed through different leadthroughs in the 80K cryostat wall from the balanced channel signals, although the harnesses should be bundled together to minimise loop area. There is a resistor shown for each ground section in each groundloop, which requires to be of optimum value.

There is not quite a classical unipoint for each ground but rather a joining to each BDA 2K section within the r.f. free enclosure, TBC by modelling.

Before we discuss the middle of this system, let's consider its ends, first towards HERSCHEL. Spire is defined at IIDB level as having a prime DPU and DRCU, plus a redundant pair, non-cross-strapped, of which the Herschel platform shall only empower one half at any one time. Now the DRCU is no longer a physical unit but has been split into two, the DCU and the FCU, both parts shall appear to the DPU and hence HERSCHEL to be simple prime/redundant units. The bolometers and the analogue section of the DCU are non-redundant, the former because it's not clear how they could be built into Spire, and the latter because it's difficult to achieve low noise from a bolometer into two preamplifiers plus the shear amount of electronics involved.

The Spire estimated MTBF must be met, which places a very high requirement for reliability on those elements which are not redundant. Formally there is no requirement that the bolometer bias and JFET supply generators be prime and redundant, merely that the functions be at least double wired across the cryoharness because of the noted less-than-ideal reliability of cryoharness. This is as shown in the above diagram. The DCU designer may choose to use prime and redundant bolometer bias and JFET supply generators if they are required to achieve the required MTBF, if they can be joined into the grounding system, if they do not degrade the bolometer S/N, and if EACH can still be at least double wired across the cryoharness. The cryoharness has now been defined to limit the loss to Spire if the "unthinkable" double **and** coincident wire breakage should occur in the a.c. bias and JFET supply wires that affect multiple pixels. The exact configuration of DCU units to supply these will be as suggested by a DCU FMECA.

The DCU digital sections, driving and receiving signals across via external I/F to other HERSCHEL SVM mounted units, have conventional ESA grounding configurations of the type with which this note starts, except that their power is supplied (not shown) just from the appropriate Prime or Redundant FCU. Data transfers of digitised bolometer signals leave the DCU in packet burst mode at quite high Baudrate which precludes the use of interfaces that might provide higher ground decoupling. Therefore these digital section of the DCU must be regarded as noisy in bolometer terms and be configured as shown in the diagram, i.e. within an isolated sub-compartment. The configuration of a DCU digital section power supply from the FCU and the section's input coupling from the preceding DCU section, shown conceptually in the grounding diagram as being an analogue section joined via an AtoD convertor, shall be such as to minimise charge injection/current into the latter's ground. This is because any such injection is potentially into the sensitive bolometers via the system analogue ground, and JPL expressed concern in this regard.

Second, consider some details the FPU end.

In setting up the grounding diagram with the JFET filters closing the wiring Faraday cage, their chassis have to be electrically isolated from the HERSCHEL optical bench, as noted in the grounding scheme. Please check that the mechanical outline of this is in the thermal model.

It also follows that the tightly bundled cables from the JFET filters to the outside of the FPU have to have a high coverage screen around each of them to keep the Faraday cage closed. Thermal analysis shows that these will be adequately heatsunk via the JFET module connectors, through their frame to the HOB. The thermal budget can stand an external shield around these cables [besides the 12-ax braids that I would like to keep insulated and associated with signal ground not chassis] terminated one end on JFET connector backshells and the other to the FPU wall.

All non-bolometer wiring entering the FPU does so via JPL provided filter boxes mounted such as to provide a closed Faraday cage. This clearly applies to the cooler's wiring and it is nominally isolated from chassis. Nevertheless, because JPL correctly identified the cooler as being very much coupled into the bolometer system, all signal sent to the cooler must be especially quiet. Please could the SCU design description document include these details and perhaps a breadboard cooler section of the SCU should be used on a sorption cooler at BDA unit level testing to check for problems. Any proportional heating needs to be heavily filtered in the SCU before being output so as to appear as "d.c." to the cooler heaters even discounting any filtering in the FPU boxes [which are intended for r.f. not power filtering!]. If temperature sensors are only conditioned in a duty cycle as they need to be read out, the start and finish of even this low level conditioning shall be ramped not stepped.

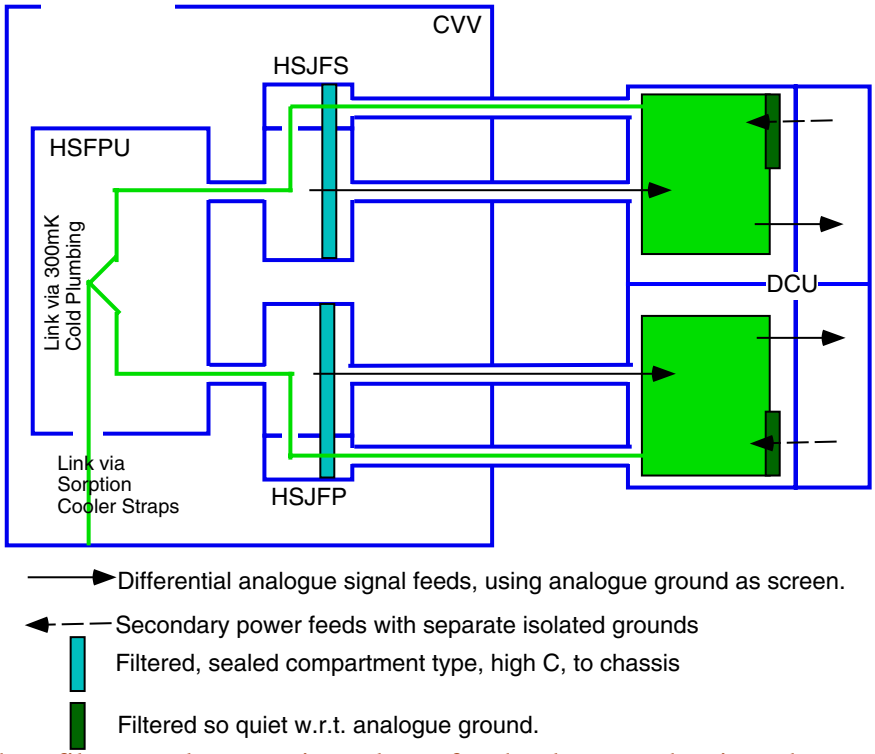
Now consider some more of the FPU grounding details. I have to admit that thinking things through to write this all out has made me aware of some details I'd overlooked. In keeping with the unit to S/C ideas spelt out above, all three main FPU mounting feet need mechanically to include electrical breaks. This is probably a new electrical requirement to be identified at system level, except that as has been pointed out it is actually part of a long-standing JPL bolometer requirement that the Faraday cage be isolatable. Thermally this should be no problem as the feet are seeking to achieve isolation anyway. Mechanically

the feet have to keep instrument alignment with the HERSCHEL telescope, so good tolerancing becomes essential at the isolated end to remove any slop as metal dowels etc. that end used as part of an alignment procedure would short out the insulation.

I originally thought the BDAs might form a Faraday cage themselves with an electrical break in the 300mK plumbing, but the BDA 300mK sections are suspended from 1.8K mounting rims linked by open Kapton ribbon harnesses which precludes this approach by definition…without thermally shorting out the Kevlar suspension. I had not at that stage caught up with the agreement that the FPU was the Faraday cage, and this approach was quickly reverted to. However, back in November, I outlined a marginally non-ideal configuration. The 1.8K BDA mounting rims interface to two almost closed boxes inside the FPU Faraday cage and are also places where internal signal grounds can be joined. The two boxes are themselves joined by a conducting thermal strap internal to the FPU box. I therefore show all of this joined in something akin to an internal distributed analogue ground plane that almost forms an internal secondary shield. In unit electrical grounding terms it is analogue ground isolated from chassis.

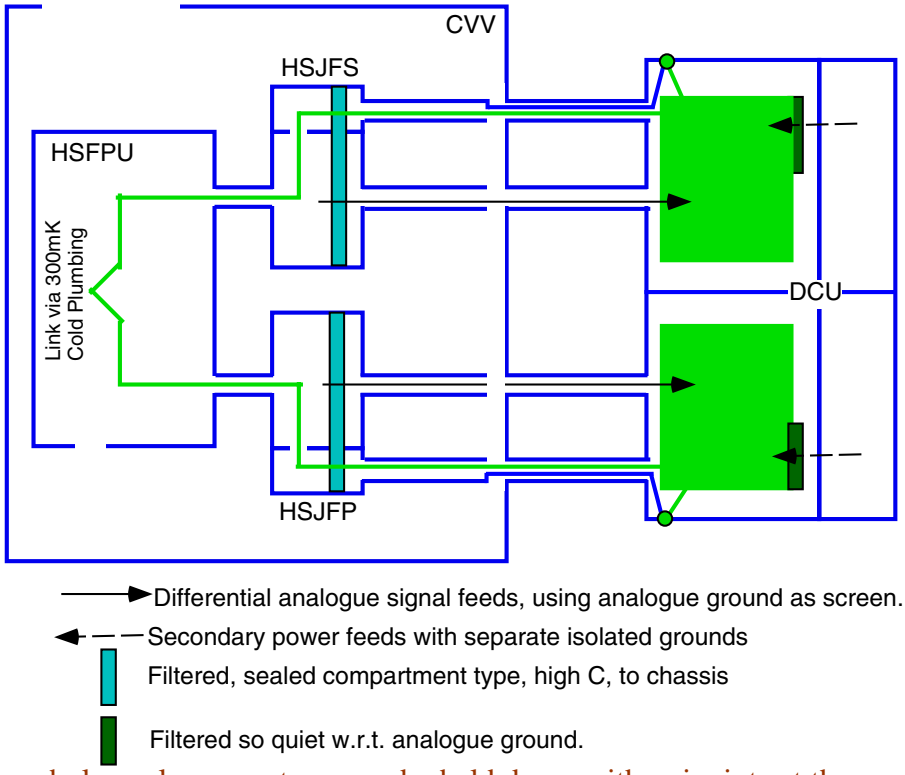
Now we come to a trade-off which RAL intends to resolve at system level first by estimation using a computer grounding model and second by test verification. This is, "Where do we join the bolometer analogue ground to chassis?". Viktor has expressed a preference for grounding it all at the DCU and having the cryogenic end including the FPU Faraday cage all isolated. The above grounding scheme actually baselines the opposite approach which is to isolate the DCU end and to electrically ground the very sensitive cryogenic end to cryostat by using the four electrical links that result from the thermal design. I have yet to see results from the computer grounding model and the safe baseline is to use electrical breaks in the four FPU thermal straps shown on the grounding diagram. Bruce is sure that there is an applicable qualified ISO way of doing this mechanically with sapphire sandwiches.

From a grounding viewpoint, it follows that all thermal/anti-microphony holdowns on the cryoharness shall not electrically short these harness shields to chassis except at the controlled CVV connector plane. This would follow automatically if the harness has an outer insulator covering. In implementing the "let's keep our options open approach", some compromises arise. The system drawn above, both schematically and in some greater detail, is for the original cold-end signal grounding point. This can be simplified as:

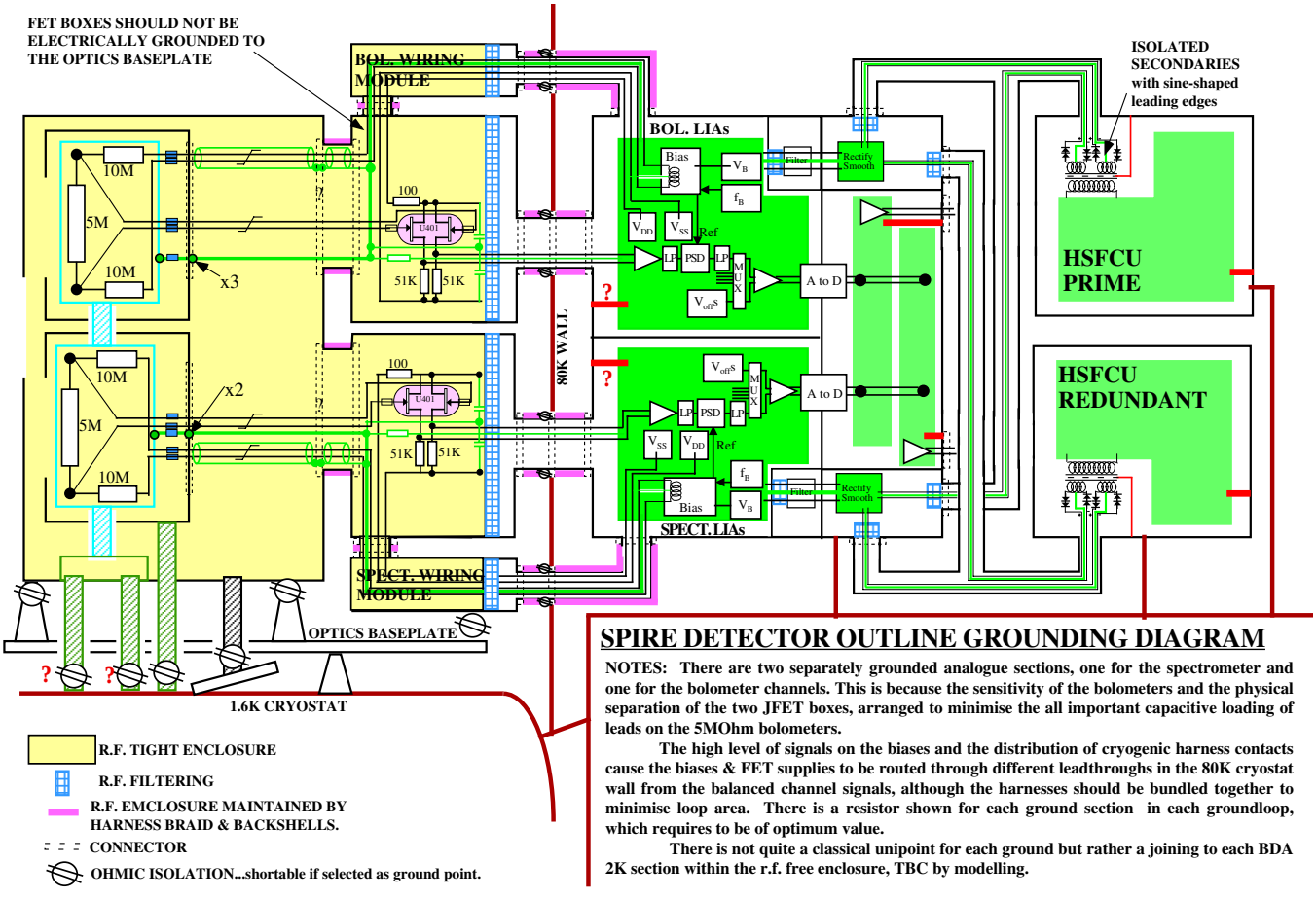


Note that the FET box filters enclose a quiet volume for the detectors but introduce ~100 x 9 x 2200pF = 2µF of capacitance between the analogue system and the FPU/JFET Faraday cage, effectively a short to R.F. With the closed harnesses forming a cage, even in this configuration the FPU/JFETs need electrical isolation of their mountings and the straps other than the one shown ideally still need galvanic breaks.

We have at present moved away from the above to the following:



The idea is that the whole analogue system may be held down with unipoints at the warm end. It's not as impossible as long thin-wired high inductance harness might imply because the lower inductance braids have always been configured in Spire to help "hold together" analogue grounds. Thus grounding presently looks like:



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There is not quite a classical unipoint for each ground but rather a joining to each BDA 2K section within the r.f. free enclosure, TBC by modelling.

It's main advantage arises because the DCU may not be a pure design and could include digital switching (hopefully using a logic ground that's not the analogue signal ground) in its "analogue" sections, thus introducing unwanted common-mode noise which may be better suppressed when returned to chassis

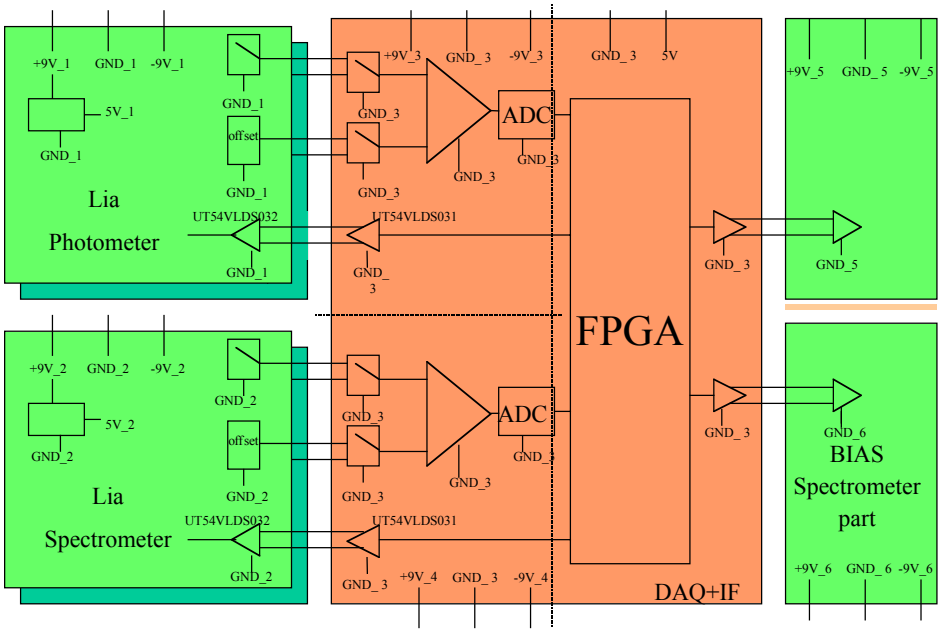
locally in the DCU. The inevitable side effect however is that Spire's nice closed Faraday cages need to be opened inside the CVV to avoid a loop caused by the FPU/JFET filter capacitance. This applies whether or not the wires to ground these harnesses to chassis are in fact carried through to the DCU as suggested by JPL or not…potentially they look like aerials!

Another option to be considered is fitting a length of braid to the backs of each Spire connector inside the CVV, to cover the harness shield break but to be insulated from the shield going on to the JFETs.

It will be gathered that my personal wish would be to ditch the DCU grounding option, but the DCU could drive us to it! It is just this optimisation that Doug's SPICE simulation will assess.

Now we reach the DCU analogue sections themselves. I suggested last year that the biases to each BDA be supplied via individual transformers to easily reference them quietly to the OV of the relevant JFET supply, clean off high frequencies, scale down a higher level synthesis to the required bias levels, provide some drive output short protection, etc. I still like this idea but it is not a requirement, merely a suggestion for implementation. I originally had the grounds for each of these biases joined into the grounding scheme at the BDAs, which is probably ideal, but combining the bias ground with the OV of the relevant JFET supply as is shown in the above version of the grounding scheme has real advantages w.r.t. the need for multiple wiring these functions along the cryogenic harness.

Now we need to appraise the DCU design, hopefully to find that it fits in with the Spire grounding scheme. I've taken Frederic's input and increased the text size + changed colours.



This is a very encouraging starting point. Comparing this with the grounding diagram, we can note the split between the spectrometer and photometer analogue grounds, G1+G5, versus G2+ G6. The isolation of the Lock-In-Amplifier grounds from the Bias/FET power supply grounds is an improvement on my solid ground plane for each side. I would encourage the ±9V powered high level analogue sections to be split into separate grounded sections as mentioned at the meeting and as shown by the dotted lines I've drawn in to the above. This should help keep the FPGA noise from propagating back to the analogue sections.

I do not think I should go further with the specifics until it is agreed how the power supplies, prime and redundant, are configured from the FCU into the DCU.

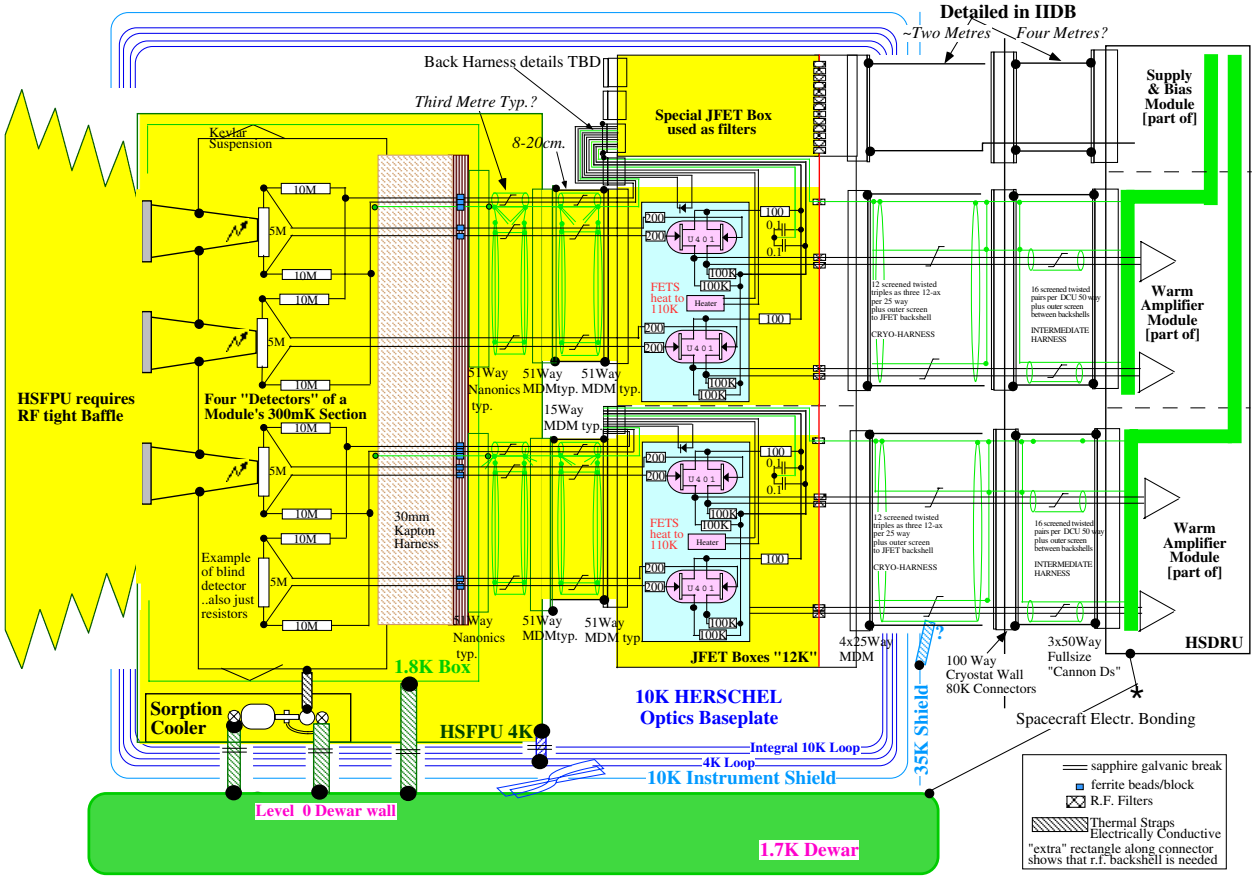
Spire will only change over from prime to redundant operation as whole and via a power down. For this scenario, relays are permissible with design analysis of their freedom from spike production. Relays may not be used to change ground lines between Spectrometer and Photometer data-taking as this changeover will be done with power on.

It's clear that the successful low noise operation of the DCU will depend on maximum attention being paid to its detailed implementation:

- keeping the low noise LIA inputs clean may need screens between the modules and even mesh cages connected to analogue ground over their ~x300 d.c. restoring pre-amplifier sections.

- Clearly keeping the PSD and offset selection switching noise out of the inputs is non-trivial, because in reality each LIA combines analogue with some slow speed digital function.
- The LIA grounding might best keep its analogue and digital functions on two separate ground-planes joined once on each module, to look like one ground from outside.
- Coupling these slow speed switching functions into the LIA from the prime and redundant FPGAs may best be accomplished using opto-couplers, one per side per LIA to add robustness and permit the easy O-Ring of signals.
- keeping digital noise out of the bias generators is equally demanding and could take a similar approach because, although signal levels are all much higher, ground currents are equally destructive of performance if they reach the bolometers. One would suggest a detailed discussion between the electronic designers to choose a configuration that keeps the digital exchange of information from the FPGA to the bias generators to a minimum.
- the DCU Faraday cage must be well closed and any signals taken outside it and back in again via harness "internal" to the unit must be identified, fully screened, and generally analysed.

Finally, let me insert a drawing specific to detector wiring that we had around some months ago but which was omitted from earlier versions of this document.



This is somewhat updated, but I've left a few unimplemented options: gate stopper R for FETS, power decoupling on JFETs, use of spare JFET junction as temperature sensor, possible use of ferrite behind the Nanonics (material and space problems). Anyway, it well illustrates some of the actual complexity.

Cheers

John

24/08/01