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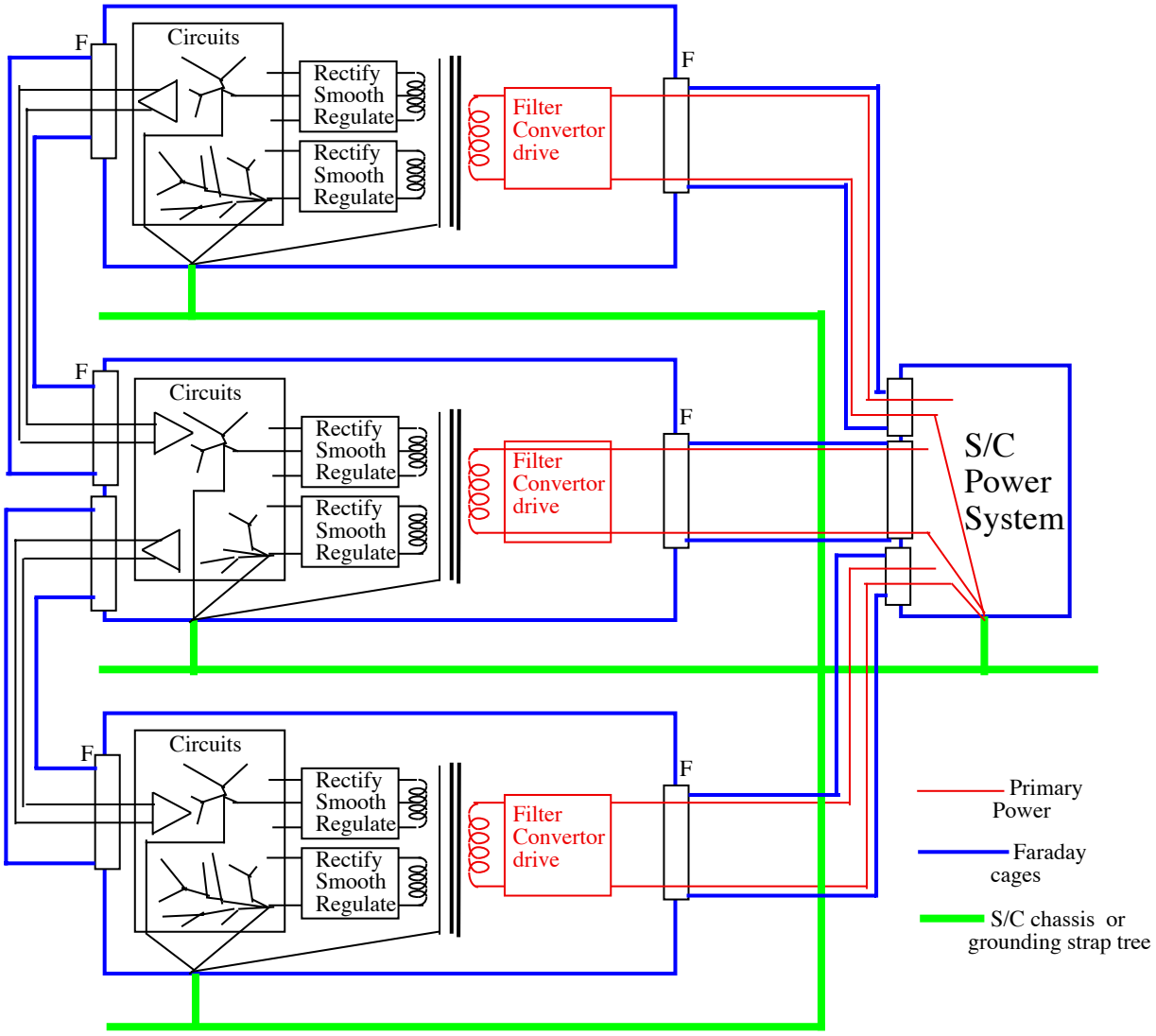
10th April 2001 version updated in brown
24th August, 2001
10th September added **Overall Grounding Diagram**
24th September Remove bias transformers & moved cold R
5th June 2002 addendum and tweaked overall diagram
13th August. Possible decision on choice of analogue grounding points
and put in latest CEA P/supply secondaries' drawing

To: SPIRE Electronics +Sam(Thermal)+Berend(Structural Isolation), +Lionel (Cooler isolation/resistance) Pete Hargrace(Isolation).
From: John Delderfield

# GROUNDING and SCREENING PHILOSOPHY

This note writes out the SPIRE grounding requirements explicitly, particularly as regards the bolometer systems. Requirements on the electronics are in red text. To present a perspective that is hopefully coherent, the rationale will be included. I appreciate that this will be a restatement of what is already clear to many recipients or regarded as good practise.

In general terms SPIRE shall conform to an ESA classical unit by unit secondary power configuration of this nature:



Each unit is electrically self-contained in its grounding.

- It has a chassis/box that is closed to form a conductive Faraday cage, i.e. enough thickness in skin depths/bulk conductivity (essentially inevitable) and with all apertures including vents and joints having controlled geometry with adequately small maximum dimensions.
- Except the S/C power system, primary power is isolated from chassis, although for each unit there is a small permissible input capacitance and possibly a large electrostatic protection resistor to chassis.
- Each unit is powered with secondary (or conditioned) power which is isolated from the primary power buses and unipoint grounded via a link to unit chassis, a joint which is best made near the same point on the chassis as is externally connected to S/C. Signal grounds are typically the same as or decoupled to such secondary grounds and the same rule applies. This internal link may need to be via an externally accessible strap to permit secondary ground isolation testing.
- All signal inputs and outputs are differential and ideally pass through filter connectors to protect the unit from external noise entering the unit via harnesses. Signal ground lines do not pass between units. Inputs are normally high impedance and are required to maintain a defined high impedance w.r.t. chassis. Outputs are required to have controlled slew rates, minimum skew to limit common mode spikes, and little ringing.
- The secondary grounds with each unit are carefully configured in a documented way and if multiple supplies are used the grounds for each supply are separately controlled with a minimum of joins between the supplies, classically just one at the unit unipoint.
- Theoretically there should be no current flow in any ground wire, which should only be used for signal voltage reference, but in unipolar supply situations, when 0V and signal ground are one and the same, current flow is unavoidable. This is just one example of the general requirement that any device taking a.c. current shall have adequate local decoupling/filtering, obviously to ensure its own correct operation, but also adequately to inhibit noise propagation to other elements in the unit; logic or digital functions can be the most troublesome with their a.c. components taking the form of switching noise.
- Depending on the susceptibility of circuits, logic signals that travel a distance across a unit may need to be slowed down with series resistors and squared up again on receipt by Schottky buffers such that excessive dV/dT noise is not broadcast.

There are several relaxations in the ideal that are commonly acceptable. Filter connectors introduce their own problems and the careful specification of input susceptibility and output emission levels often allows requirements to be met with un-filtered connectors. In such a cases, common mode filtering with defined differential mode bandpass is often introduced on signal inputs to compensate. Formal unipoint strapping to a S/C grounding tree is often discarded and a unit is simply conductively mounted by all of its mounting feet…..this is no problem as long as no other equipment is returning current along the S/C chassis and potentially thus inducing a.c. signals in the unit's Faraday cage.

On the other hand, there are many options for improving the operation of such standard configuration, to further limit the propagation of noise between elements inside it.

- internal division into a card rack and a compartment housing the noisy power supply with bulkhead filters between the two.
- improving the Faraday shield with thin metallic inter-board shields or even formal internal divisions with bulkhead filters. Such shields are often used if frequencies are being multiplied and shifted or if one board contains logic and other only analogue {All are electrostatic screening connected solidly to unit chassis; I'll omit the less common magnetic screening from this note}
- Accepting a certain level of ground current but defeating the induced ground voltage noise by using highly conducting low inductance ground planes. Unless a special analysis is performed these should only be used in conjunction with other good practice (local decoupling, separation of grounds, chassis isolation with unipoint contact, etc.). More complex scenarios exist: ground signal planes may be combined with power supply planes, the ensemble being multiply capacitively linked; physically thicker power planes may be sandwiched into PCBs, electrically isolated from the circuits on them but firmly joined to unit chassis so as to extract power but also to double as extended Faraday screens.
- Mismatching impedances/4-wiring. Mismatch is inherent in many architectures that use low impedance drive and high impedance inputs, but I'm referring here to using high impedance current drive into relatively low impedance input. Used with or without formal differential

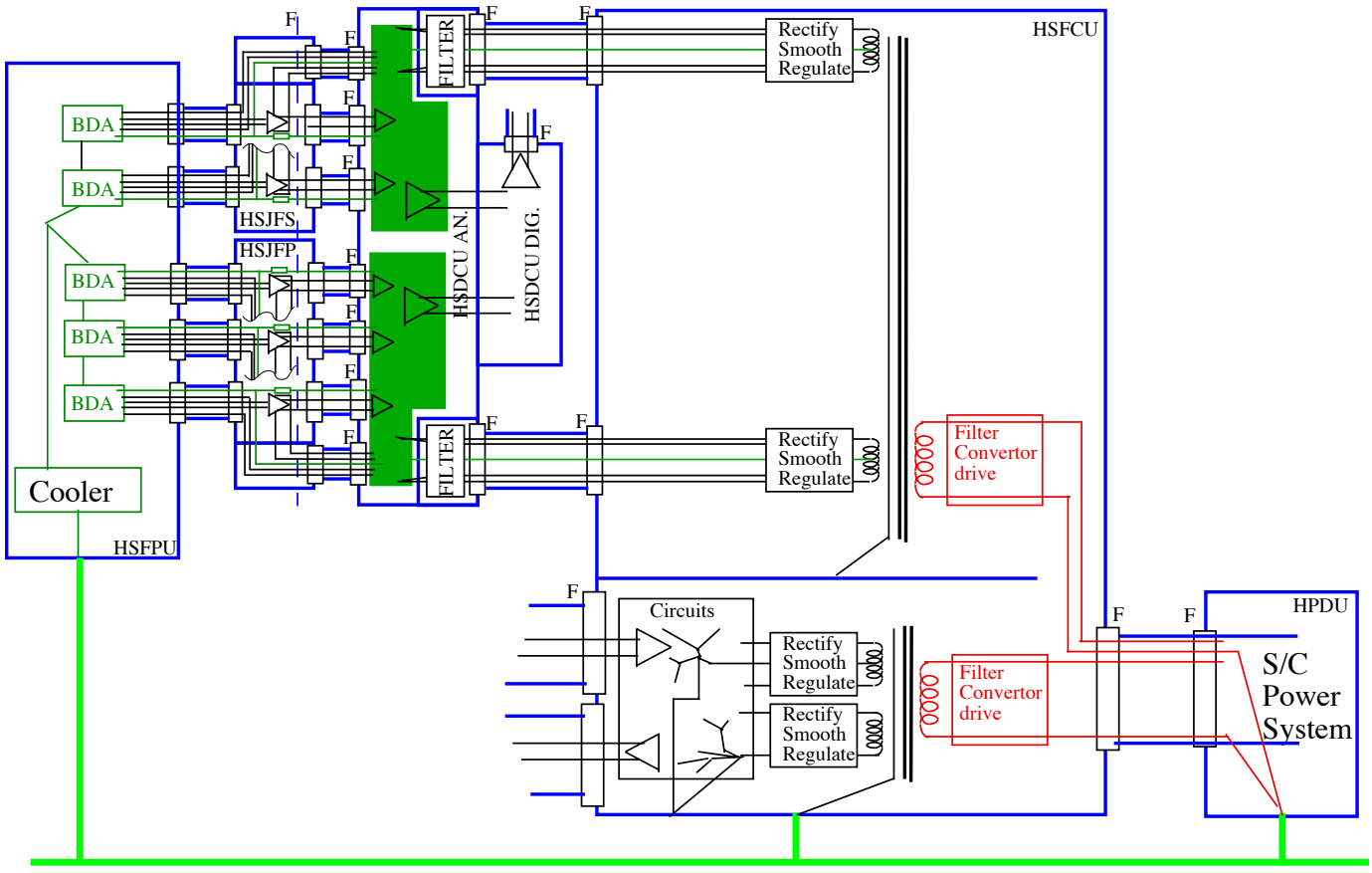
signals, this is another way of removing a dependance on a quiet voltage reference ground.

- Differential digital interfaces do not provide ideal isolation. In particular, the driver has to provide significant edge switching currents to drive harness capacitance, a situation that gets worse if the I/F is between units, the receiving unit inputs have capacitive filter elements, harness lengths are long and have screens, etc.. Depending on frequency, power, radiation environment and money, such interactions between supposedly separate grounds may be improved by using transformer coupled buses or opto-couplers.

The whole arrangement so far described is prefixed by "in general terms". The configuration is best suited to systems in which each unit operates over a restricted range of signal level. In Spire this would apply to the HSDPU. Otherwise transmission of noise from high level circuits such as power convertors to sensitive analogue elements get more and more impossible to achieve. Considering the front-end signal source in Spire, we have an noise spec. of 7nV/√Hz at about 2.5MΩ and 300mK. There comes a point when the need to control noise requires separate preamplifier unit(s), preferably with an electrostatically screen separating it (them) from any digital functions such as multiplexors or A-D convertors, with the signals then transferring to a conventional unit via balanced digital I/Fs. The power needs to be fed to this system's analogue sections extremely quietly, prefiltered and actively regulated with external sensing in an external unit. It must then be filtered in a separate compartment within the analogue unit that has bulkhead connectors feeding to the analogue system. Grounding has to be very carefully configured as secondary grounds are implicitly distributed outside of one unit. If one considers the whole volume of the various units in this supply system as if it were joined into one by the harness screens that join them, the grounding it should look like a unipoint tree as if it were still within one unit.

Multichannel operation requires adequate interchannel screening and a configuration that keeps any designed-in signal cross-talk to below specified levels.

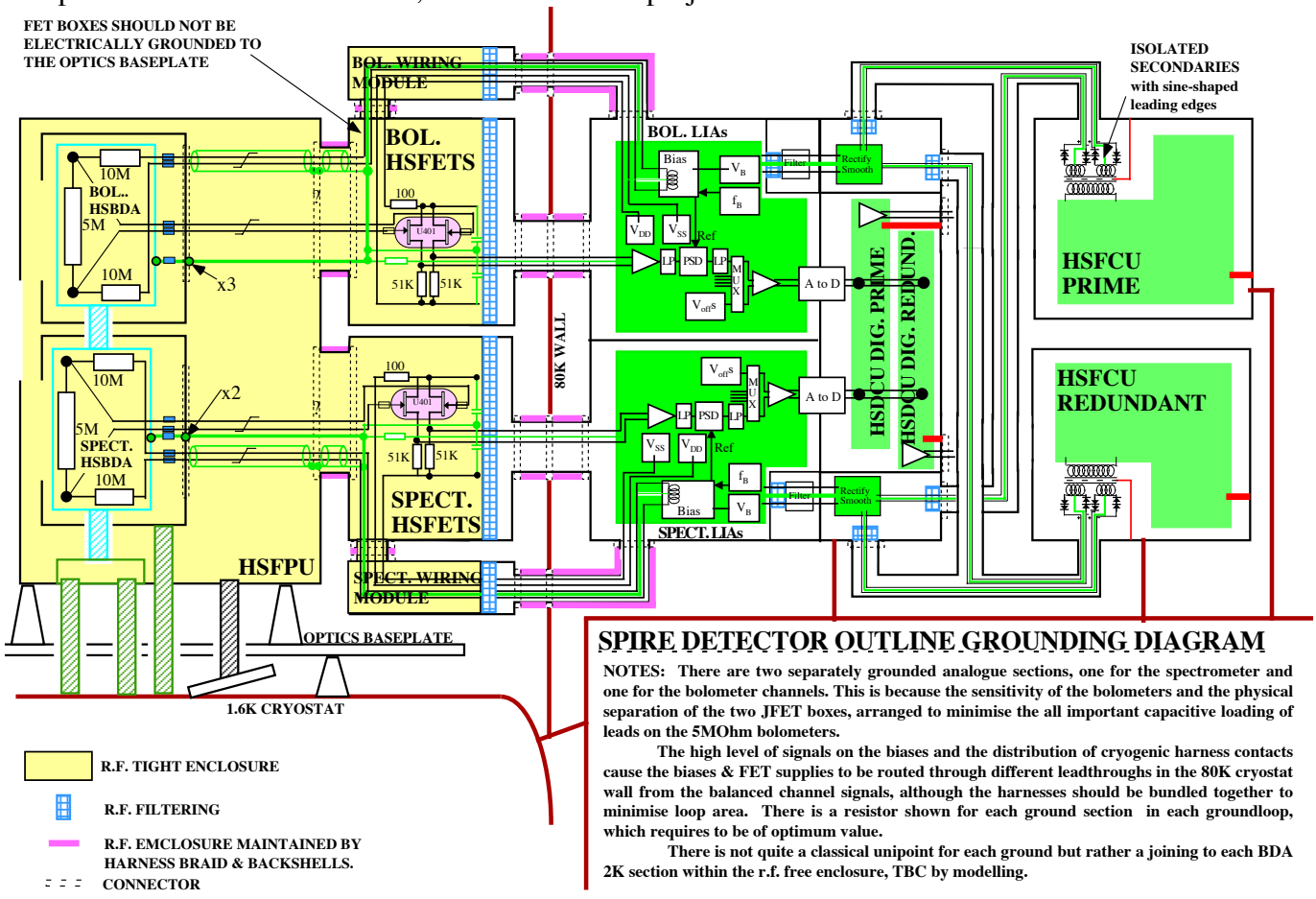
We conceived of the following concept early in the autumn of 2000, following the design decision to separate the spectrometer and photometer JFET units so they could be accommodated adequately near to their respective detectors, the specification then being <50pF along the cable as seen by each 5MΩ detector. It was also really stressed by those with experience that Spire's bolometric detectors are unbelievably sensitive and would make corrupted measurements if unwanted r.f. were to be dissipated in them, the biggest risk being that wires have to be attached to them!! So the following concept was adopted at a video conference from RAL to JPL with Christophe Cara present at the RAL end.



I've used up-to-date acronyms and ignored any redundancy in this drawing to minimise confusion. The essential specifications are:

- signal power gain from external JFET amplifiers
- separate analogue ground paths, without loops, between spectrometer and photometer systems
- maintenance of single point ground joins to S/C chassis
- analogue power, quiet and regulated, supplied from a unit external to the one that houses the sensitive analogue systems, without ground switching.
- ground-plane option invoked to keep a large area of analogue signal ground quiet in each of the spectrometer and photometer parts
- the detectors to be in a Faraday cage with full filtering on all wires entering it (non-bolometer ones not shown) extended with full shielding into the JFET boxes.
- MDM connectors on the JFET boxes not available cryogenic filtered, so a separate compartment division is introduced in the JFET boxes with ceramic feedthrough filtering to close the Faraday cage.
- unipoint analogue ground for the system at the 300mK BDA units that are unavoidable coupled with cold-plumbing busbar ink. This minimises Voltages between the bolometers and their local chassis.
- information transfer out of the digital part of the HSDCU via normal balanced ESA-type digital interfaces, both fast and slow, to the HSDPU (not shown but having its own separate conventional grounding scheme).
- The need to bundle together groups of long harnesses between HSJFETs and HSDCU (not shown here but see instrument block diagram) to minimise loop area between bias routed analogue ground lines and differential signal lines. Admittedly they are inside shielded harnesses but one cannot have much common mode signal at the DCU's inputs even with good CMRR before a 7nV/√Hz differential noise performance is degraded.
- An optimised multiplexing/transfer of data from the analogue sections of the DCU to the back-end digital ones to minimise current injection back into the analogue ground and hence potentially back to the detectors.

With all the above in mind, and having seen some circuits for the DCU, the following grounding scheme was published in November 2000, was circulated to project:




**SPIRE DETECTOR OUTLINE GROUNDING DIAGRAM**

**NOTES: There are two separately grounded analogue sections, one for the spectrometer and one for the bolometer channels. This is because the sensitivity of the bolometers and the physical separation of the two JFET boxes, arranged to minimise the all important capacitive loading of leads on the 5MOhm bolometers.**

**The high level of signals on the biases and the distribution of cryogenic harness contacts cause the biases & FET supplies to be routed through different leadthroughs in the 80K cryostat wall from the balanced channel signals, although the harnesses should be bundled together to minimise loop area. There is a resistor shown for each ground section in each groundloop, which requires to be of optimum value.**

**There is not quite a classical unipoint for each ground but rather a joining to each BDA 2K section within the r.f. free enclosure, TBC by modelling.**

Before we discuss the middle of this system, let's consider its ends, first towards HERSCHEL. Spire is defined at IIDB level as having a prime DPU and DRCU, plus a redundant pair, non-cross-strapped, of which the Herschel platform shall only empower one half at any one time. Now the DRCU is no longer a physical unit but has been split into two, the DCU and the FCU, both parts shall appear to the DPU and hence HERSCHEL to be simple prime/redundant units. The bolometers and the analogue section of the DCU are non-redundant, the former because it's not clear how they could be built into Spire, and the latter because it's difficult to achieve low noise from a bolometer into two preamplifiers plus the shear amount of electronics involved.

The Spire estimated MTBF must be met, which places a very high requirement for reliability on those elements which are not redundant. Formally there is no requirement that the bolometer bias and JFET supply generators be prime and redundant, merely that the functions be at least double wired across the cryoharness because of the noted less-than-ideal reliability of cryoharness. This is as shown in the above diagram. The DCU designer may choose to use prime and redundant bolometer bias and JFET supply generators if they are required to achieve the required MTBF, if they can be joined into the grounding system, if they do not degrade the bolometer S/N, and if EACH can still be at least double wired across the cryoharness. The cryoharness has now been defined to limit the loss to Spire if the "unthinkable" double **and** coincident wire breakage should occur in the a.c. bias and JFET supply wires that affect multiple pixels. The exact configuration of DCU units to supply these will be as suggested by a DCU FMECA.

The DCU digital sections, driving and receiving signals across via external I/F to other HERSCHEL SVM mounted units, have conventional ESA grounding configurations of the type with which this note starts, except that their power is supplied (not shown) just from the appropriate Prime or Redundant FCU. Data transfers of digitised bolometer signals leave the DCU in packet burst mode at quite high Baudrate which precludes the use of interfaces that might provide higher ground decoupling. Therefore these digital section of the DCU must be regarded as noisy in bolometer terms and be configured as shown in the diagram, i.e. within an isolated sub-compartment. The configuration of a DCU digital section power supply from the FCU and the section's input coupling from the preceding DCU section, shown conceptually in the grounding diagram as being an analogue section joined via an AtoD convertor, shall be such as to minimise charge injection/current into the latter's ground. This is because any such injection is potentially into the sensitive bolometers via the system analogue ground, and JPL expressed concern in this regard.

Second, consider some details the FPU end.

In setting up the grounding diagram with the JFET filters closing the wiring Faraday cage, their chassis have to be electrically isolated from the HERSCHEL optical bench, as noted in the grounding scheme. Please check that the mechanical outline of this is in the thermal model.

It also follows that the tightly bundled cables from the JFET filters to the outside of the FPU have to have a high coverage screen around each of them to keep the Faraday cage closed. Thermal analysis shows that these will be adequately heatsunk via the JFET module connectors, through their frame to the HOB. The thermal budget can stand an external shield around these cables [besides the 12-ax braids that I would like to keep insulated and associated with signal ground not chassis] terminated one end on JFET connector backshells and the other to the FPU wall.

All non-bolometer wiring entering the FPU does so via JPL provided filter boxes mounted such as to provide a closed Faraday cage. This clearly applies to the cooler's wiring and it is nominally isolated from chassis. Nevertheless, because JPL correctly identified the cooler as being very much coupled into the bolometer system, all signal sent to the cooler must be especially quiet. Please could the SCU design description document include these details and perhaps a breadboard cooler section of the SCU should be used on a sorption cooler at BDA unit level testing to check for problems. Any proportional heating needs to be heavily filtered in the SCU before being output so as to appear as "d.c." to the cooler heaters even discounting any filtering in the FPU boxes [which are intended for r.f. not power filtering!]. If temperature sensors are only conditioned in a duty cycle as they need to be read out, the start and finish of even this low level conditioning shall be ramped not stepped.

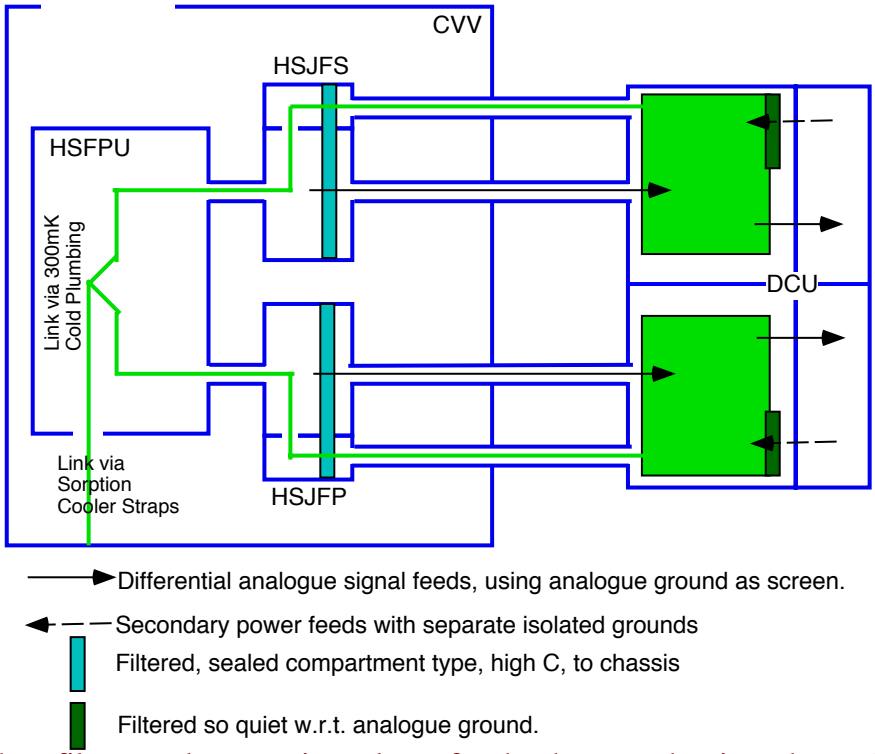
Now consider some more of the FPU grounding details. I have to admit that thinking things through to write this all out has made me aware of some details I'd overlooked. In keeping with the unit to S/C ideas spelt out above, all three main FPU mounting feet need mechanically to include electrical breaks. This is probably a new electrical requirement to be identified at system level, except that as has been pointed out it is actually part of a long-standing JPL bolometer requirement that the Faraday cage be isolatable. Thermally this should be no problem as the feet are seeking to achieve isolation anyway. Mechanically

the feet have to keep instrument alignment with the HERSCHEL telescope, so good tolerancing becomes essential at the isolated end to remove any slop as metal dowels etc. that end used as part of an alignment procedure would short out the insulation.

I originally thought the BDAs might form a Faraday cage themselves with an electrical break in the 300mK plumbing, but the BDA 300mK sections are suspended from 1.8K mounting rims linked by open Kapton ribbon harnesses which precludes this approach by definition…without thermally shorting out the Kevlar suspension. I had not at that stage caught up with the agreement that the FPU was the Faraday cage, and this approach was quickly reverted to. However, back in November, I outlined a marginally non-ideal configuration. The 1.8K BDA mounting rims interface to two almost closed boxes inside the FPU Faraday cage and are also places where internal signal grounds can be joined. The two boxes are themselves joined by a conducting thermal strap internal to the FPU box. I therefore show all of this joined in something akin to an internal distributed analogue ground plane that almost forms an internal secondary shield. In unit electrical grounding terms it is analogue ground isolated from chassis.

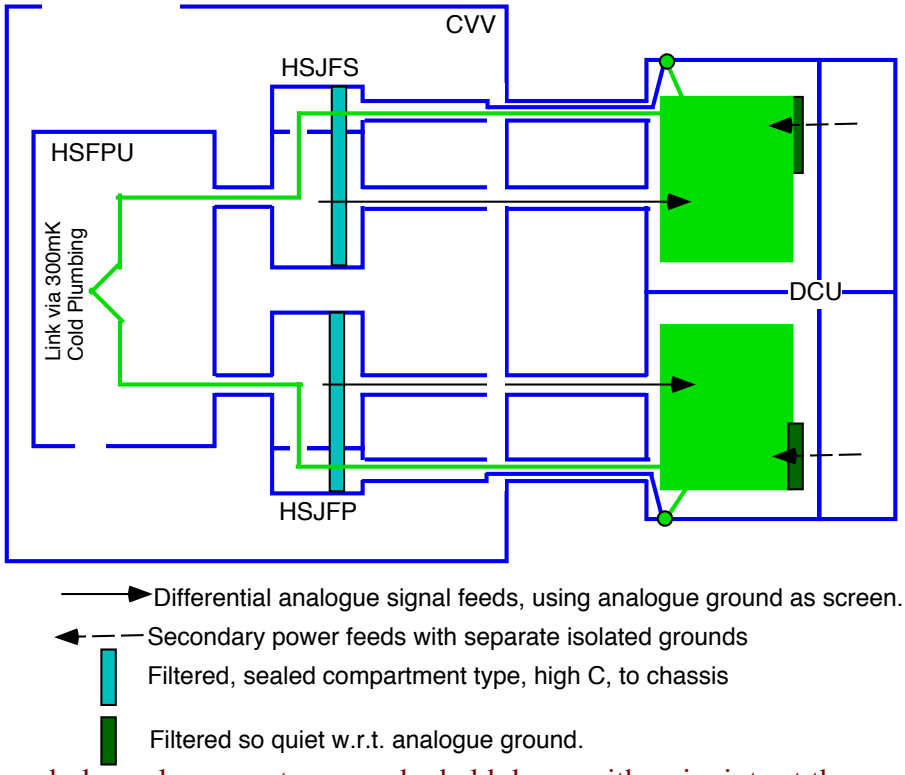
Now we come to a trade-off which RAL intends to resolve at system level first by estimation using a computer grounding model and second by test verification. This is, "Where do we join the bolometer analogue ground to chassis?". Viktor has expressed a preference for grounding it all at the DCU and having the cryogenic end including the FPU Faraday cage all isolated. The above grounding scheme actually baselines the opposite approach which is to isolate the DCU end and to electrically ground the very sensitive cryogenic end to cryostat by using the four electrical links that result from the thermal design. I have yet to see results from the computer grounding model and the safe baseline is to use electrical breaks in the four FPU thermal straps shown on the grounding diagram. Bruce is sure that there is an applicable qualified ISO way of doing this mechanically with sapphire sandwiches.

From a grounding viewpoint, it follows that all thermal/anti-microphony holdowns on the cryoharness shall not electrically short these harness shields to chassis except at the controlled CVV connector plane. This would follow automatically if the harness has an outer insulator covering. In implementing the "let's keep our options open approach", some compromises arise. The system drawn above, both schematically and in some greater detail, is for the original cold-end signal grounding point. This can be simplified as:

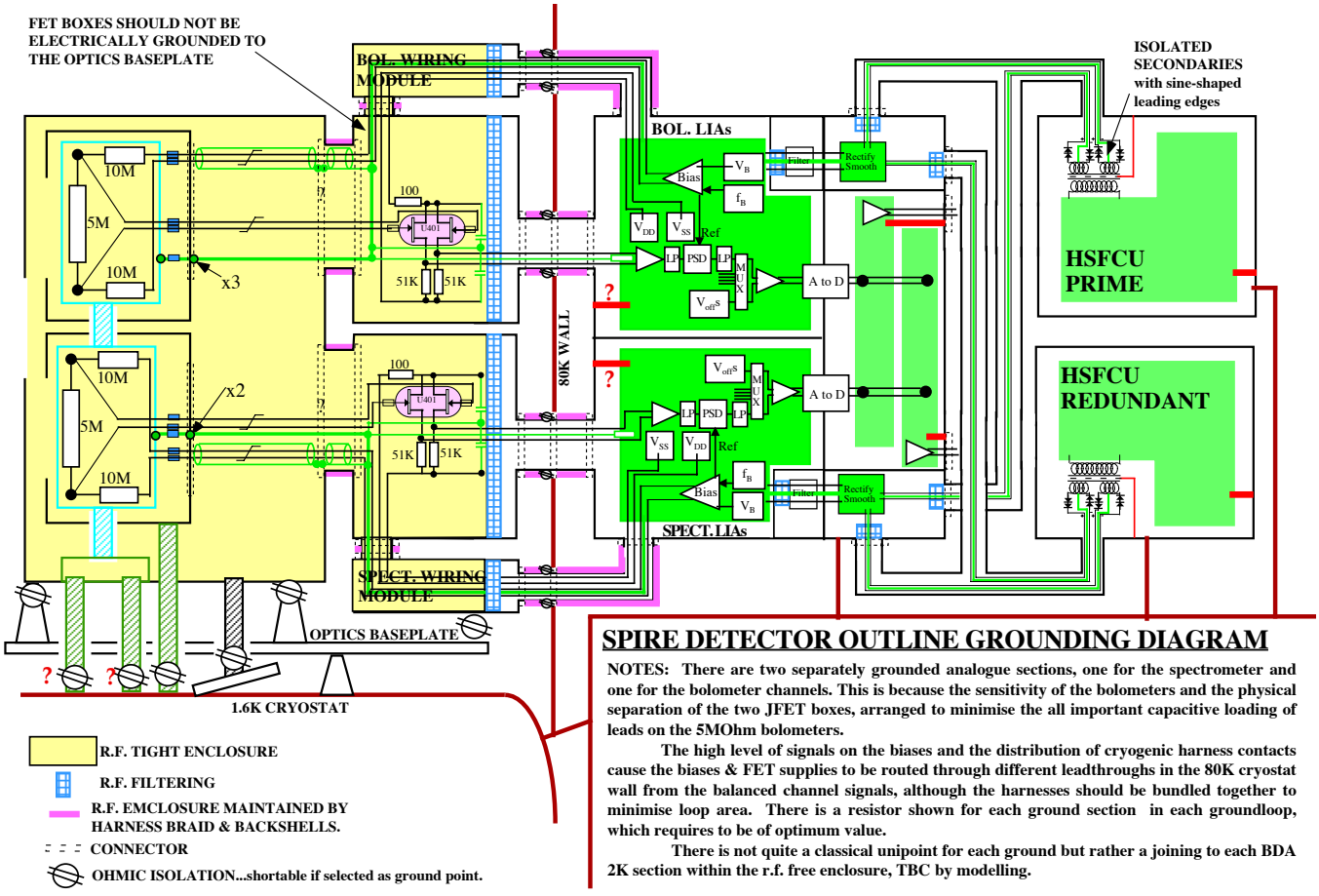



Note that the FET box filters enclose a quiet volume for the detectors but introduce ~100 x 9 x 2200pF = 2μF of capacitance between the analogue system and the FPU/JFET Faraday cage, effectively a short to R.F. With the closed harnesses forming a cage, even in this configuration the FPU/JFETs need electrical isolation of their mountings and the straps other than the one shown ideally still need galvanic breaks.

We have at present moved away from the above to the following:




The idea is that the whole analogue system may be held down with unipoints at the warm end. It's not as impossible as long thin-wired high inductance harness might imply because the lower inductance braids have always been configured in Spire to help "hold together" analogue grounds. Thus grounding presently looks like:

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There is not quite a classical unipoint for each ground but rather a joining to each BDA 2K section within the r.f. free enclosure, TBC by modelling.

It's main advantage arises because the DCU may not be a pure design and could include digital switching (hopefully using a logic ground that's not the analogue signal ground) in its "analogue" sections, thus introducing unwanted common-mode noise which may be better suppressed when returned to chassis

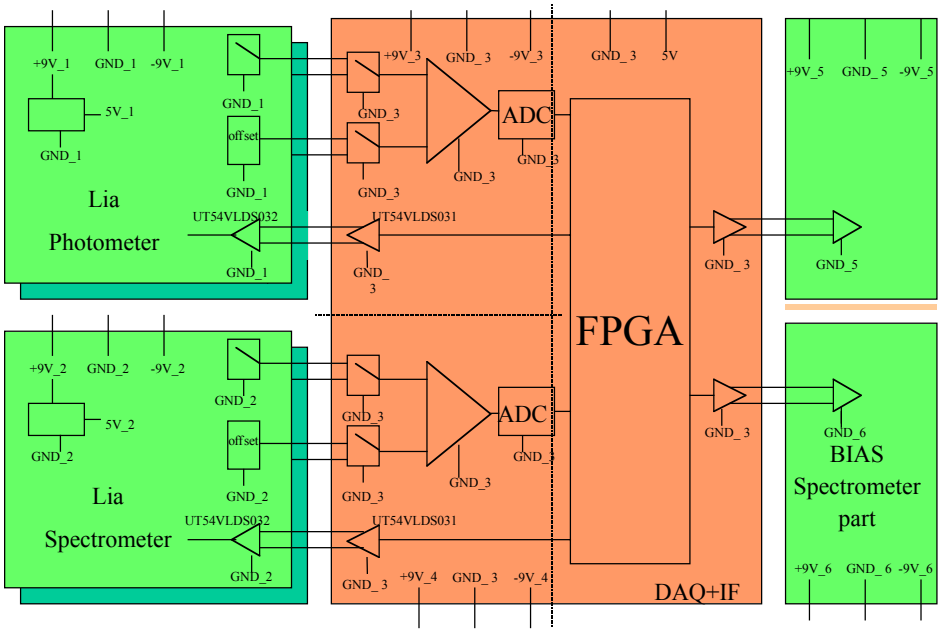
locally in the DCU. The inevitable side effect however is that Spire's nice closed Faraday cages need to be opened inside the CVV to avoid a loop caused by the FPU/JFET filter capacitance. This applies whether or not the wires to ground these harnesses to chassis are in fact carried through to the DCU as suggested by JPL or not…potentially they look like aerials!

Another option to be considered is fitting a length of braid to the backs of each Spire connector inside the CVV, to cover the harness shield break but to be insulated from the shield going on to the JFETs.

It will be gathered that my personal wish would be to ditch the DCU grounding option, but the DCU could drive us to it! It is just this optimisation that Doug's SPICE simulation will assess.

Now we reach the DCU analogue sections themselves. I suggested last year that the biases to each BDA be supplied via individual transformers to easily reference them quietly to the OV of the relevant JFET supply, clean off high frequencies, scale down a higher level synthesis to the required bias levels, provide some drive output short protection, etc. I still like this idea but it is not a requirement, merely a suggestion for implementation. I originally had the grounds for each of these biases joined into the grounding scheme at the BDAs, which is probably ideal, but combining the bias ground with the OV of the relevant JFET supply as is shown in the above version of the grounding scheme has real advantages w.r.t. the need for multiple wiring these functions along the cryogenic harness.

Now we need to appraise the DCU design, hopefully to find that it fits in with the Spire grounding scheme. I've taken Frederic's input and increased the text size + changed colours.




This is a very encouraging starting point. Comparing this with the grounding diagram, we can note the split between the spectrometer and photometer analogue grounds, G1+G5, versus G2+ G6. The isolation of the Lock-In-Amplifier grounds from the Bias/FET power supply grounds is an improvement on my solid ground plane for each side. I would encourage the ±9V powered high level analogue sections to be split into separate grounded sections as mentioned at the meeting and as shown by the dotted lines I've drawn in to the above. This should help keep the FPGA noise from propagating back to the analogue sections.

I do not think I should go further with the specifics until it is agreed how the power supplies, prime and redundant, are configured from the FCU into the DCU.

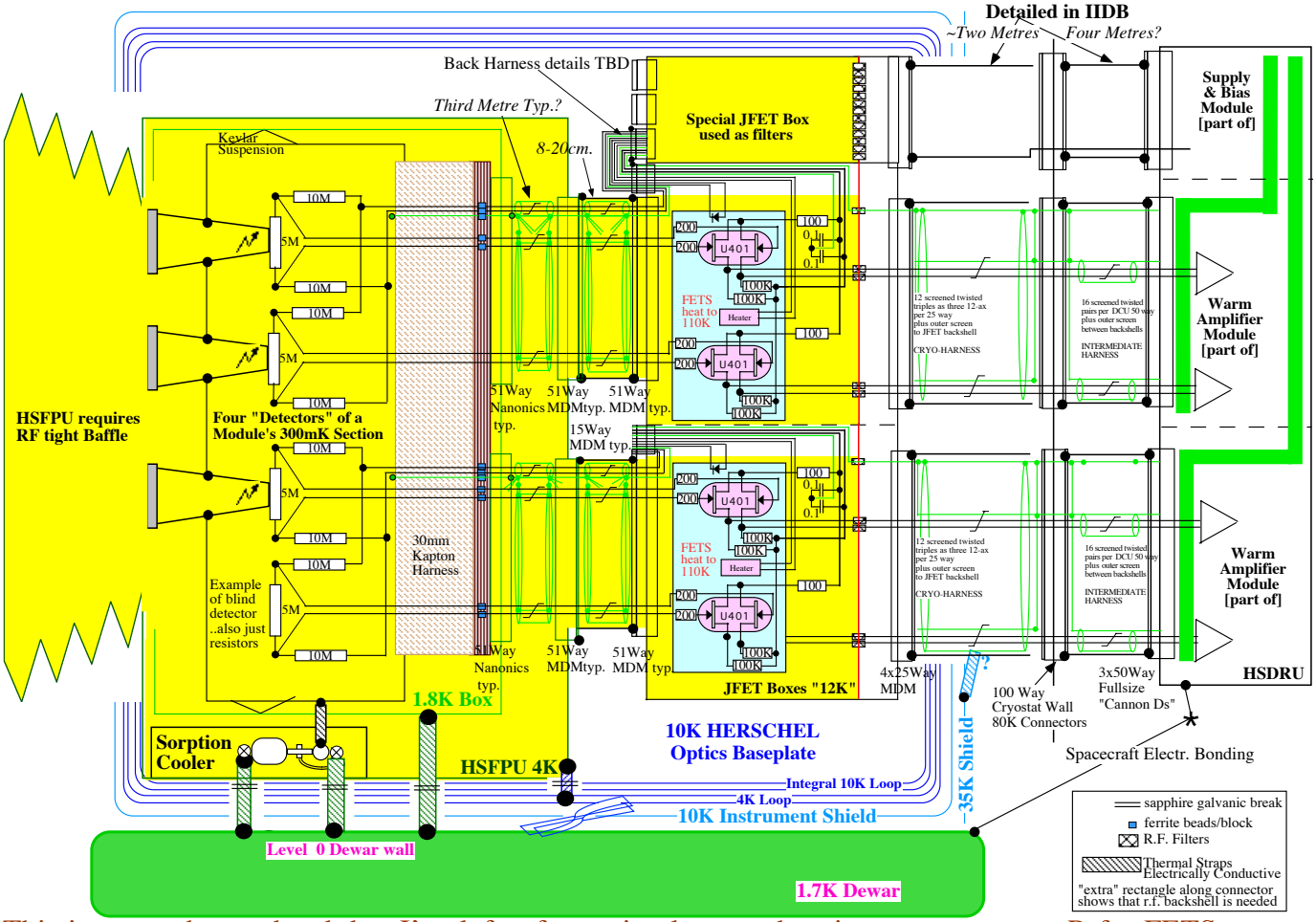
Spire will only change over from prime to redundant operation as whole and via a power down. For this scenario, relays are permissible with design analysis of their freedom from spike production. Relays may not be used to change ground lines between Spectrometer and Photometer data-taking as this changeover will be done with power on.

It's clear that the successful low noise operation of the DCU will depend on maximum attention being paid to its detailed implementation:

- keeping the low noise LIA inputs clean may need screens between the modules and even mesh cages connected to analogue ground over their ~x300 d.c. restoring pre-amplifier sections.

- Clearly keeping the PSD and offset selection switching noise out of the inputs is non-trivial, because in reality each LIA combines analogue with some slow speed digital function.
- The LIA grounding might best keep its analogue and digital functions on two separate ground-planes joined once on each module, to look like one ground from outside.
- Coupling these slow speed switching functions into the LIA from the prime and redundant FPGAs may best be accomplished using opto-couplers, one per side per LIA to add robustness and permit the easy O-Ring of signals.
- keeping digital noise out of the bias generators is equally demanding and could take a similar approach because, although signal levels are all much higher, ground currents are equally destructive of performance if they reach the bolometers. One would suggest a detailed discussion between the electronic designers to choose a configuration that keeps the digital exchange of information from the FPGA to the bias generators to a minimum.
- the DCU Faraday cage must be well closed and any signals taken outside it and back in again via harness "internal" to the unit must be identified, fully screened, and generally analysed.

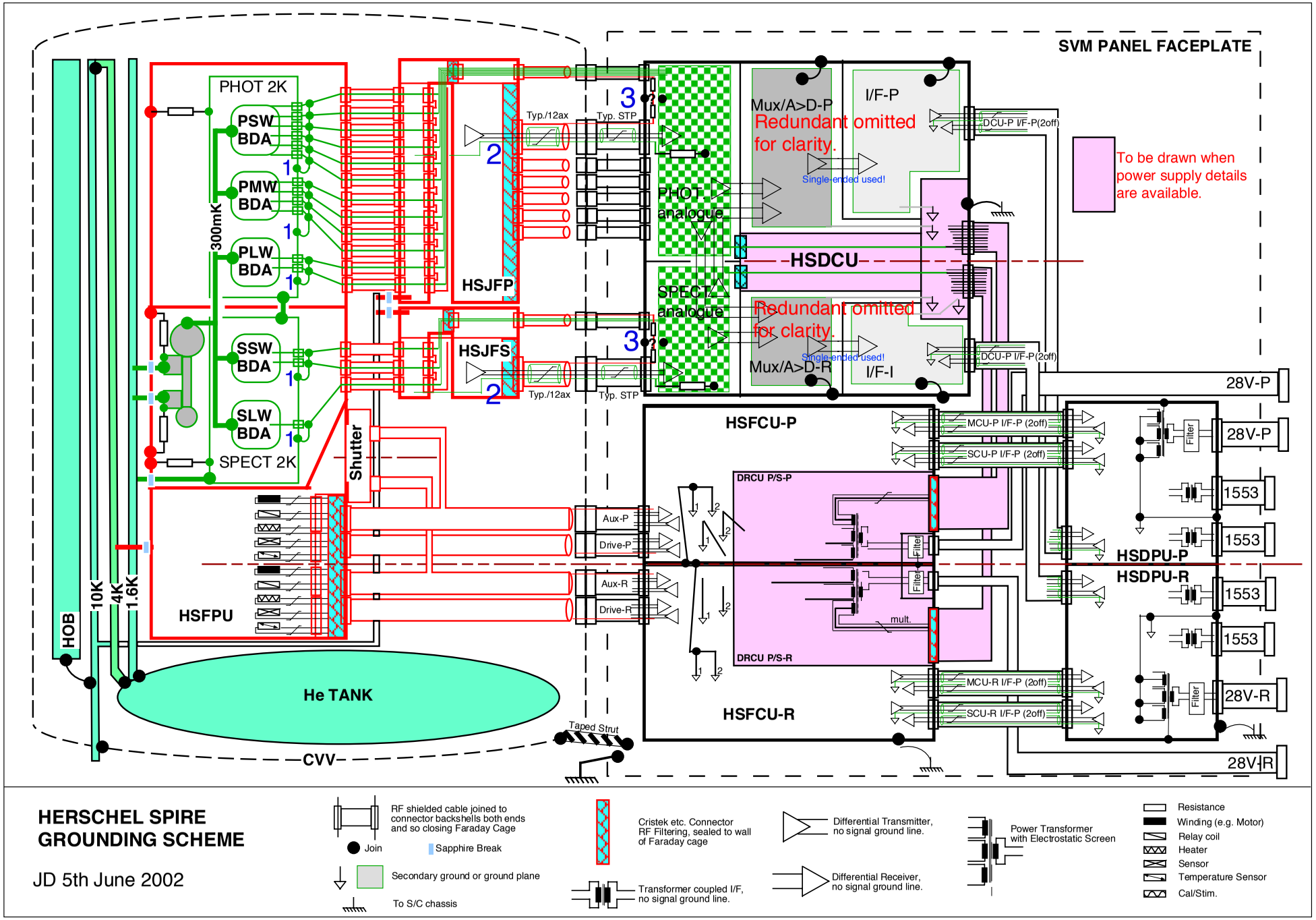
Finally, let me insert a drawing specific to detector wiring that we had around some months ago but which was omitted from earlier versions of this document.




This is somewhat updated, but I've left a few unimplemented options: gate stopper R for FETS, power decoupling on JFETs, use of spare JFET junction as temperature sensor, more separate grounds in the JFETS than are actually implemented, possible use of ferrite behind the Nanonics (material and space problems). Anyway, it well illustrates some of the actual complexity.

John
24/08/01

The most critical area is undoubtedly the bolometric signals already discussed, but we ought to consider the whole Spire instrument on the HERSCHEL spacecraft. A simplified drawing of this follows. The HSFPU is shown with some Faraday cage dividing partitions within it. These are indicative of metal optical baffles containing mesh filters that seal both around the filter and into the HSFPU outer box to divide up the box into several RF sealed vented cavities.


SVM PANEL FACEPLATE
PHOT 2K
PSW BDA
PMW BDA
PLW BDA
SSW BDA
SLW BDA
SPECT 2K
300mK
Shutter
HSFPU
HSJFP
HSJFS
Typ./12ax
Typ. STP
PHOT analogue
SPECT analogue
Mux/A>D-P
I/F-P
Redundant omitted for clarity.
Single-ended used!
DCU-P I/F-P(2off)
To be drawn when power supply details are available.
HSDCU
Mux/A>D-R
I/F-I
DCU-I I/F-P(2off)
28V-P
HSFCU-P
MCU-P I/F-P (2off)
SCU-P I/F-P (2off)
DRCU P/S-P
Aux-P
Drive-P
Aux-R
Drive-R
Filter
1553
HSDPU-P
HSDPU-R
mult.
DRCU P/S-R
HSFCU-R
MCU-R I/F-P (2off)
SCU-R I/F-P (2off)
28V-R
HOB
10K
4K
1.6K
He TANK
Taped Strut
CVV
HERSCHEL SPIRE
GROUNDING SCHEME
JD 5th June 2002
RF shielded cable joined to connector backshells both ends and so closing Faraday Cage
Join
Sapphire Break
Secondary ground or ground plane
To S/C chassis
Cristek etc. Connector RF Filtering, sealed to wall of Faraday cage
Transformer coupled I/F, no signal ground line.
Differential Transmitter, no signal ground line.
Differential Receiver, no signal ground line.
Power Transformer with Electrostatic Screen
Resistance
Winding (e.g. Motor)
Relay coil
Heater
Sensor
Temperature Sensor
Cal/Stim.

Let's follow this diagram through. The DPU houses electrically separate prime and redundant sides. It has two independent power supplies, again prime and redundant. Each half follows the classical electrical grounding model mentioned earlier, with no secondary grounds leaving the unit. Each side actually has a master clock interface to the S/C systems that uses a differential receiver, not shown for clarity, but this also conforms to the model…...the unit is essentially all digital.

The FCU similarly has prime and redundant halves but includes further features. Its design implementation has multiple secondaries, such as to power its DPU interfaces with minimal noise injection from the dQ/dt taken to drive the cables. The FCU powers and conditions loads in the FPU which are anything but standard electrical interfaces. These are hopefully all differential functions because the circuit have both harness and RF filter capacitance to the FPU grounding system, drawn in red, and associated with the DCU. Also single-ended signals are only really suited to internal logic on a dedicated secondary both as regards noise susceptibility and noise emission. Any single-ended drivers feeding the FPU would probably need a dedicated secondary to avoid noise in the unit's secondary grounds. Lastly, since there are requirements for extremely low noise in the DCU front-end, it is powered by secondary power distributed from the FCU to avoid it needing to include an active switching power supply.

The complexity of the DCU is disguised in the drawing because it only shows grounds not power rails, and only a minimum number of grounds are separately delineated. As discussed earlier in this note, the bolometers require two analogue ground systems, one for the spectrometer and one the photometer, carried back to the bolometer bias and JFET power supplies. Although thus split, and although wired and partitioned to be robust, the analogue system is non-redundant from prime/redundant viewpoint and thus has to be powered by either prime or redundant FCU power conditioning. There is a further complication not shown on the diagram: the bolometer bias and JFET power supplies apparently do need to be prime and redundant (as per CEA FMECA not yet received). They work attached to the non-redundant detector system analogue grounds. So these elements are analogue but not cross-coupled as regards prime or redundant FCU power conditioning .

It's absolutely vital that digital switching logic should not couple externally into the analogue front ends leaving charge to be returned, via the FPU if that is where we decide to most strongly ground the system. One would expect very careful (slowed edge?) coupling of the PSD clock that has to be in the LIAs. Hence the drawing shows an intermediate mixed analogue/digital groundplane similar to Frederick's block diagram a couple of pages back.

To finish, the DCU also includes conventionally configured prime/redundant digital interface circuits, albethey powered by secondaries that are wired from the FCU.

**Summary:**
There are details to be answered such as heater strap capacitance across the sapphire, sorption pump heat switch ohmic value to 4K, and whether double RF outer screens are needed. But, to repeat, choosing the optimum place to ground the bolometer signal grounds to chassis remains the biggest unanswered question.

**Addendum June 2002**

After setting the SPIRE grounding philosophy in place at the end of 2000 and evolving it somewhat during 2001, the minutes of a meeting at CEA on 12th December 2001 said:
"Plan is:
"CEA to combine the power implementation plan with the current system design, target mid-Jan 2002.
"Pass it RAL for assessment. If it seems OK, CEA should then negotiate it with JPL."

However, after our recent CEA Paris meeting in late May I concluded to myself:

- CEA has proposed a power supply primary scheme which to a very large extent follows what is functionally required, but the secondary side implementation is still missing, which they accepted l needed addressing urgently and Dominique would produce forthwith.
- We are now getting into a discussion about whether to change our three options for the DCU analogue OV to chassis link, rather than waiting until after testing/simulation. This arises because CEA restated that they thought the DCU could not be made to work with the required noise performance other than by making this link at the DCU, and they in fact propose to implement the link in the very distributed low inductance fashion mentioned as a general possibility for units earlier in this document, namely tying many ground-plane rims to chassis.

However JPL could not attend the Paris meeting, and the interaction with JPL mentioned in December has only recently been achieved, and is very much on-going. [Just as communications were attached to early issues of this document, I now temporarily append two summaries kindly provided by Matt, one of the CEA meeting and one of the telecon. with JPL. (August 13th, moved to end as additional information)]

Dominique tabled SAp-SPIRE-DE-0000-02 concerning grounding. It explores some factors associated with efficiency of shielding / long harnesses at different frequencies, something I had put off exploring until after RAL's SPICE model results, but in many other respects of good practise it picks up factors already worked through in this document.

A point to make about why CEA and JPL presently have differing opinions is that CEA's basic models consider how to get differential voltages from the FCU into the LIA, whereas JPL take this as read and are fundamentally worried about the corruption of that voltage itself either by induced bolometer heating or by microphonics modulating the voltage via charge injection. Both the two groups' concerns need to be addressed!

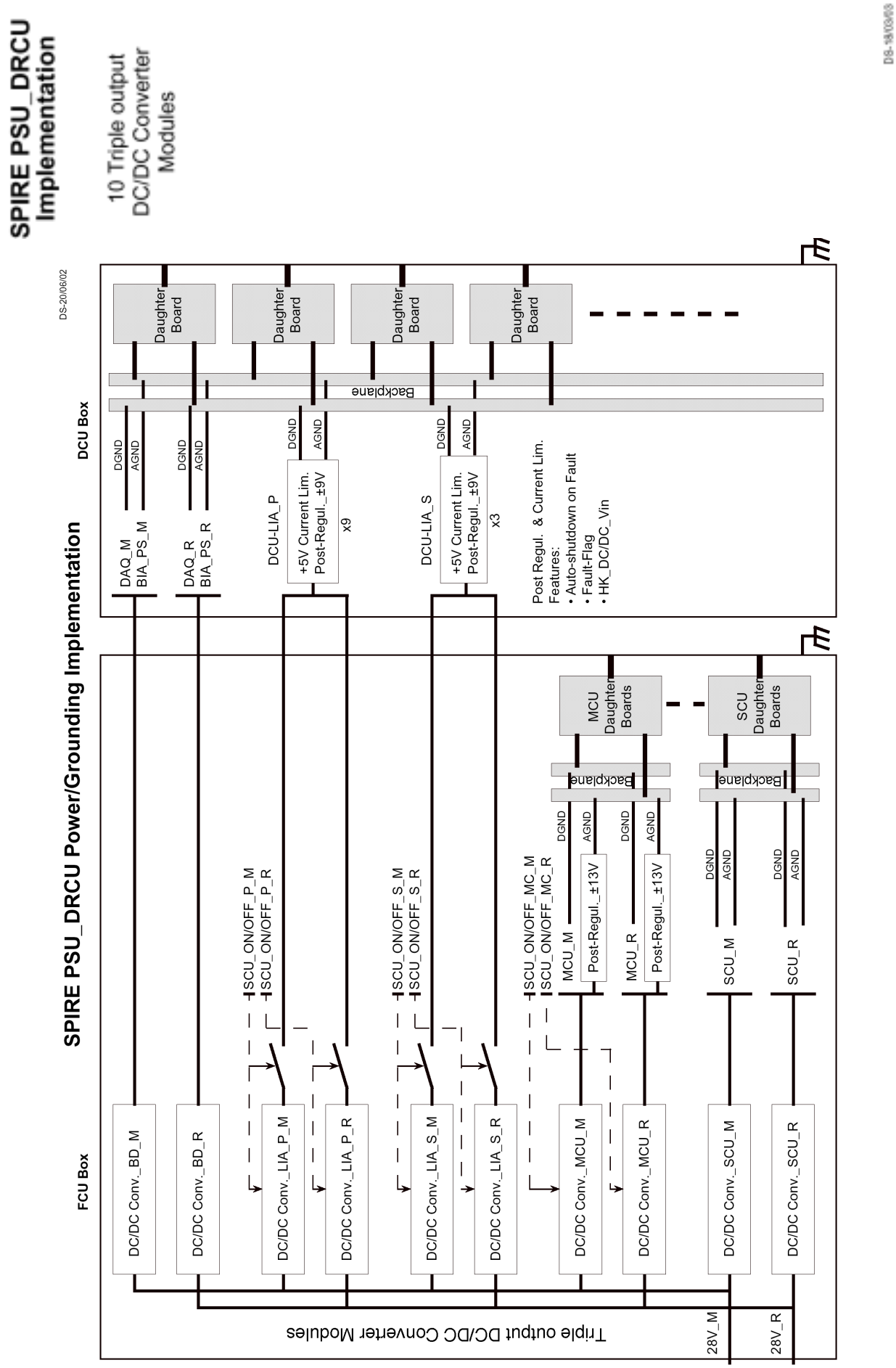
**Power Supply Primaries.**

Let's first consider the CEA proposal for power functional configuration shown on the next page. We may need to revisit this when the whole power-supply scheme is available but it seems possible to proceed for now on such a basis.

There are five Primary(Main) convertors on the Primary(Main) 28V supply and similarly on the Redundant. For those DRCU units which have Primary and Redundant sides these run the corresponding sub-systems. For the LIAs, which are non-redundant, the secondary grounds all remain connected but the power rails are relay connected/disconnected as needed, depending on which power module(s) is /are active. ON-OFF is coordinated through the SCU which enables or disables power module oscillators [which implies some transient state current values on the 28V bus that the monitoring S/W will need to know about!]

To note in passing, the number of power modules would not seem to be an overriding driver for CEA since they decided not to take up the offer of 5V power from the DPU for the logic and interfaces. Note also that rather than dioding together S/C supplies to power non-redundant supplies feeding non-redundant LIA systems [maybe split into smaller groups than spectrometer/photometer], both Prime and Redundant supplies are used for such systems [in a way presumably akin to CEA's earlier decision based on single point failure analysis not to make the bolometer biases all non-redundant and more grouped.]

It's not yet clear whether a "triple output" on the drawing means three separate windings with three grounds and as many taps as may suite, or whether it means three voltage rails. Either way, I only say above "possible to proceed" because I note that at any one time only one module is active and powering the DCU despite its power requirements. Also whilst the FCU merits its own supply for biases and digital I/Fs, the apparently more sensitive DCU does not. How good will the isolation be between the sections of the DCU identified earlier in this document when in either of the spectrometer and photometer




mode they are all run from one power supply module which does not have any inter-winding screens. If it is an error that the top two power supplies shown above stop in the FCU but in fact they power the DCU, then again I wonder whether noise can be kept off the critical bolometer bias secondaries and their grounds (there's secondary regulation shown here) if the same convertor is also running lots of logic.

## Points for thought.

We ought to be quite clear just what is being joined together and what is not.

The DCU digital formatting and I/F section grounds have always been joined to chassis in the DCU, see SPIRE Overall Grounding Diagram.

The same applies to the A to D convertor ground(s) as per the diagrams on pages 8 and 10. However this ground is clearly a potential route for transferring noise back to the analogue front ends, and as Dominique always points out no isolation is perfect. Therefore I was dismayed to learn at the recent Paris meeting that the concept of a minimum line balanced logic interface from this to the digital formatting and I/F section as per the diagram on page 10 not been implemented by CEA who have replaced it with a single-ended ground referenced (and ground current driving) configuration. I'm very afraid of increased ground noise due to this coupling of power currents/logic switching currents.

Let me add some more factors into the discussion, some quite detailed:

a. I'm still concerned about the real LIA input common-mode rejection. The whole CEA analysis of EMC relies on the LIA being able to be an "inert" high impedance measuring box, not disturbing what is connected to its inputs but just quietly measuring differential voltages. This requires an excellent CMRR. Spire has only had a simulated CMR response without Monte Carlo component spread simulation for a long while, but the QM test plan included all sorts of LIA tests but not the measurement of either direct CMMR or intermodulation type distortion. I pointed this out to Christophe at the meeting and hope the matter is being addressed. The situation has been made more demanding by CEA who forced disconnection of the direct connection of the JFET signal ground arriving at the LIA inputs by not implementing transformer coupled a.c. biases / separate bias analogue grounds.

b. We have various impedances in this system which are neither very low nor very high. The 2K boxes are on thermal standoffs from the 4.5K FPU case, and so these links are shown on the grounding diagram as resistors. There are TBoptimised resistors where the Faraday cage link wires and the signal ground wires join to analogue 0V at the DCU input.

c. RAL has not facilitated this process by not a having produced any results from our SPICE model.

d. ESA is presently saying it will proceed against SPIRE's wishes and leave the external shielding off the harnesses inside the CVV, presumably inserting just a wire. I disagree strongly with this.

e. In terms of keeping voltage reference wires clean by not passing supply/signal currents along them, although identified at previous reviews, CEA have not followed this approach by separating the PSD logic etc. from the LIA analogue amplifier supply. So power currents from many channels and with bias frequency components will pass along this ground wire giving it a differing potential at the LIAs to that which it has at the FCU. I would have thought this an inappropriate complication to obtaining the requisite noise performance.

f. We have long discussed the return of noise as close as possible to the source, and in particular h.f. common mode power supply switching noise. There has **never** been any intention of sending it all the way via a ground return at the cold end, and this thread in the discussion is I hope decoupleable from other considerations. In discussions with Christophe many months ago, he referenced CEA's experience as proved by the Sextant power supply in their foyer, a unit which supplies secondary power to another unit remote from itself, said that this was the approach which CEA would take for Spire, and highlighted an r.f. filter connector between the partitions in this frame to achieve just such a local return and hence containment of CM noise. [One related query is that p10 of DES/00/A/037/T shows a unit that looks different to me from the open hybrid in your foyer. Am I incorrect?].

g. I note the use of local supply regulators on the DCU modules. This seems crucial. However, RAL's experience is that standard integrated bandgap or zener based regulators need very careful design so they do not source noise into low noise front ends, often with both reference-to-regulator filtering and post-regulator filtering. Additionally it is often necessary to pre-filter the "raw" voltage to remove h.f. which integrated regulators cannot reject well with their limited closed loop bandwidth.

h. The LIA inputs are high impedance and come inside the DCU before reaching the MAT transistors. To minimise cross-talk and noise pick-up, are these connectors harnessed in screened twisted pairs?

i. Everyone notes the nasty mismatch that can occur between Cristek filter pins, but I have yet to see a simulation of the reduction of CMRR versus frequency that this induces….one good reason for

avoiding the 70K low noise but only half working JFET option!

j. Akin to Dominque's Sap-SPIRE-DS-000-02 but more specific, I note the following noise sources:

- Digital devices and their supplies inside the DCU
- The SPIRE power conditioning system
- Signal/Chassis couplings from the SPIRE DPU
- The HERSCHEL power system: conducted, radiated, magnetically coupled
- External r.f. sources (do we work OK during downlink even though we don't need to?)
- Effects of cryoharness and HERSCHEL CVV/SVM not being solidly joined
- Noise from other SVM equipments and currents induced in SVM panels, although they meet standard ESA specifications. Spire equipments are mixed with others on "our" SVM panel.
- Fields inside CVV due to other instruments inside and due to much reduced external fields still admitted by the CVV input aperture.

There may be others, but these worry me most at the moment!

k. We already have a **distributed** coupling at HF all the way along the harness between the inner analogue grounds and the outer RF shield. This is made more relevant by the comparatively high resistance and inductance of a cryo-harness. SPICE models need to show a sort transmission line network and not single impedances.

l. I really do not like the broken outer screen just inside the CVV 128ways with the Faraday shield link wires running all through the I and S harnesses to anchor down the SPIRE sensor. These wires are potentially injection aerials. The design was changed to this because of JPL's isolation from CVV specification. I would like to see all these shields rejoined RF tight.

m. If we want to retain the CEA option of multiple point analogue links to the DCU chassis, I think we have to keep this chassis EMC clean. Besides all the internal detail necessary to achieve this, to be furnished by CEA, should we change to optical unshielded signal links to the DCU and place the whole unit on a Chomerics thermally conducting, electrically insulating gasket?

**The Way Forward.**

Consider a detector level drawing such as is included earlier in this document, but now updated to follow the present hardware implementations. This is shown on the next page but really needs to be printed at A3 or A2 for best visibility.

The detailed drawing already shows up some answers.

We really only have a choice of two points to link analogue ground and chassis grounds. This is because after the outer screens on the inner parts of harnesses F1-15 (i.e. inside the FPU Faraday cage) were removed for thermal reasons the analogue ground links to the metalwork at point 1. are needed anyway just to hold down the 2K boxes properly. [One small point Jamie, JPL's 10209725 still shows a connector at the FPU wall (with a link wire) both of which I would understand have gone.] More importantly, the metalwork around the high-impedance detectors **is** then joined to analogue ground whichever point we link that analogue ground to the outer system chassis. Berend: could you please estimate the electrical impedance of the 2K box mounts because we may require to increase this with some Vespel bushes, but if they achieve good thermal isolation they should have significant electrical impedance anyway. So in some regard Viktor's concern is unfounded, but in my view it probably remains a concern because of the very low noise levels which Spire must achieve.

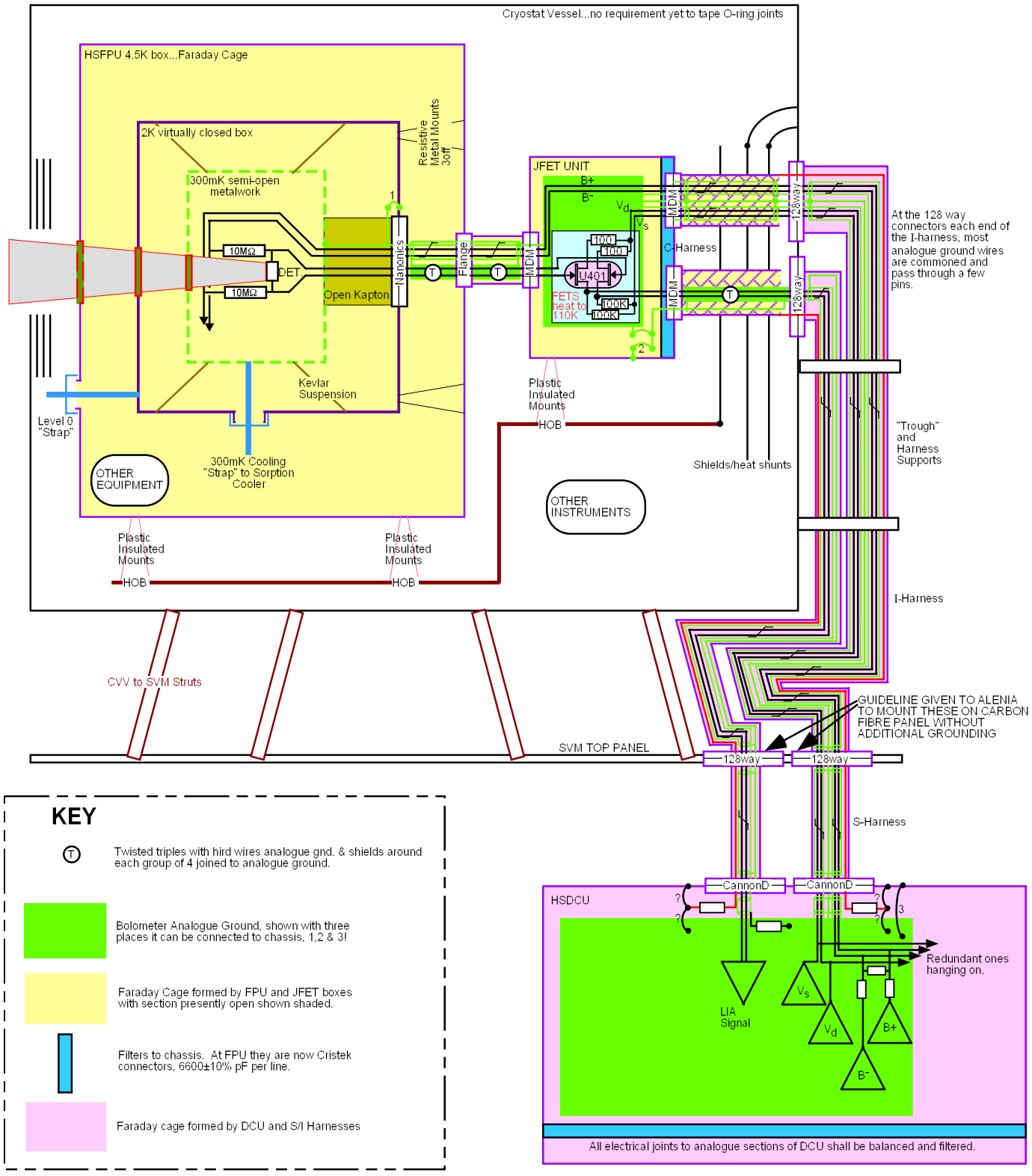
Even after linking at 1, we are still left with an analogue ground that is essentially floating except for stray impedances and gratuitous noise injections. If it were ideally floating we could ground it anywhere! Do we choose location 2 or 3?

But there is already a large (maybe 0.2μF) link from analogue ground to JFET box chassis due to the paralleling of connector pin capacitances, so at all high frequencies joining at point 3 amounts to joining in two places (a loop) which on the face of it is non-optimum. This and a realistic LIA CMRR should not be omitted from any analysis.

[There is one further possible factor. I would presently expect the analogue ground that travels with the

JFET output signals to be linked to the JFET local analogue ground so any induced current return to source. The resistor the other end of these lines in the DCU I would expect to be maybe 27K and just a "quietner". However the option has been provided by JPL to unlink these analogue grounds at the JFET end and presumably hold them down somewhat harder at the DCU. As they would add to the LIAs' input capacitance and return current to the wrong place I propose these links always stay fitted].

## SINGLE DETECTOR DETAIL GROUNDING




Please would people make all models used to predict what is good and bad for this system have elements that closely follow the real hardware configuration? Keep the information exchanging and I will arrange another telecon.

John

Sent 14 July 2002

To: SPIRE Grounding Tiger Team
From: John Delderfield

## SPIRE GROUNDING SCHEME PROPOSAL

Please find together with this note a revised SPIRE grounding scheme. By this I mean a revision of those elements joined to bolometer bias grounds, the area all the discussion has been about. This is the way forward I have had in mind for a couple of weeks.

During that time I have sought consensus on aspects of it by floating ideas into the "Tiger Team". Responses have varied from lack of comment, to partial ones, and through to ones that have introduced other factors, sometimes unintended by the idea floated. So in a sense I apologise that this is imposed from System level but in a sense I don't apologise because I hear a recurrent sentiment, "This is a SPIRE system job".

I would also accept the observation that the configuration is more complicated than subsystems other than the HSDCU would wish and I feel that as such it has bent over backwards to accede to CEA's wishes. However, if this permits us all to get ahead again with SPIRE it is probably worth the pain it will cause with MSSL, ESA, and possibly JPL.

In essense SPIRE is changed from a system that is intended for grounding "everything" low noise together at the cold end but with a warm end link that may be tried, to one in which elements are carefully held apart at the cold end, albeit within a closed Faraday cage, so they can all be linked to that cage at the warm end. For the detectors/JFETS this only really applies w.r.t. low frequencies because high frequencies (well above signal frequency) continue to join to the Faraday cage at the capacitive feedthrough "wall". This I regard as an inviolate feature of the design, and actually means that warm end grounding is inevitably a split frequency approach as seen from the detectors/JFETS.

I had thought about presenting a menu of choices, but in a way CEA are right, choices are very restricted. Unless one goes completely to a "we'll try it and see" approach {which was never my inclination}, the hardware has to be isolated properly into signal strings so that it can be pulled together at one point without introducing loops. Such breaks are now have to be included at the cold end.

The only real alternative to what I've drawn here is to return to cold end grounding, to remove the link to chassis in the warm electronics as being incompatible rather than pretending it is an option, and to proceed with the design SPIRE had in place 18 months ago. CEA might correct me if I'm wrong, but I presuppose given recent history that they would not be willing to proceed on this basis. So I won't propose it as an alternative.

To spell out the extra hardware ground breaks that are needed:

- The 2K boxes are isolated from HSFPU chassis
- They are isolated from each other
- The 300mK cooling straps are isolated.

All these place extra and unwelcome mechanical and thermal design constraints on optimised cold-end sub-systems, some of which are already built, which is the point of my earlier bending over backwards sentiment.

So, to conclude, I hope this closes out the matter. I will chair tomorrow's Tiger Team meeting with just one question on the agenda, "Can anyone see why this cannot work?". The fact that it cannot be realistically analysed, which is almost true of all options, will not be accepted as applicable to the question.

I will then put my tin hat on and use my greatest diplomacy to bring other elements into line with it!

There is one detail of implementation which it is appropriate to spell out as it enables this decision to be reversible, if painfully, thus answering the very real concern of some that we should not do anything such that at the end of the day JPL say, "See the ground should have been at the cold end" and we cannot do it. There is an argument that says we should seek to make all ground links as low impedance as possible because that's the best that we can do. The logic is flawed in its motive because this might make fixed currents induce the lowest voltage but it is of no value if the voltage that being induced is already low enough to not have any significant effect on the system, and very low impedances can permit very low

magnetic fields to induce higher currents in any inadvertent loops. I also like to carry heritage through from model to model. So the implementation of all links from groundplane to pcb areas clamped to module frames shall remain wire links. At least on the first model these should all be populated with wires of about a third the number of strands that can be fitted and the system assessed. Then one LIA board shall be reworked to use the full gauge wire for which the plated through holes are rated and these channels re-assessed. Since these electronics should be designed to have minimal CM emission I anticipate no difference will be found, thus proving even the thinner links are low enough impedance and fully continuous groundplane into the module clamp points is not needed.

Best regards,

John.

PS In a way I have been unhappy with the functioning of this Tiger Team. Nothing innovative has come out in the meetings themselves that has justified the writing of minutes. I don't think this is anyone's fault. With hindsight a team that **only** meets on the telephone is not a good basis to work things through at any sustained intensity, and it might be incorrect to term it a Tiger Team at all. Quite clearly the majority of us involved were never able to put this as our number one priority, and nor were we required to make such a commitment, so matters have proceeded much more as "normal work" than as a Tiger Team. Apart from the odd outburst about sabotage which served admirably to keep us all awake, I must thank everyone for their underlying cooperative approach.

---

Changes since Overall grounding scheme version of 5th June.

Shutter removed.

Joined up instrument Faraday cage, see increase in red lines, by re-connecting shields at CVV wall.

Made resistors in Faraday shield link wires very narrow line because they would not be fitted in this scheme. I am assuming that the wire's fractional contribution to heatleak is small and that just running totally inside a Faraday cage they cannot be a source of pickup. Besides the test harness layup is made.

Removed all grounding option numbers as we are being forced at this stage to define one baseline.

Remove 2K detector box resistances to HSFPU chassis. This scheme requires the mountings be "isolated". Put isolation in 2K box link...would separate S/C strap be easier?

Reposition 300mK pump in drawing to show it more correctly on the Photometer side.

Put in 300mK ground breaks, distinguishing between sapphire and other ground breaks.

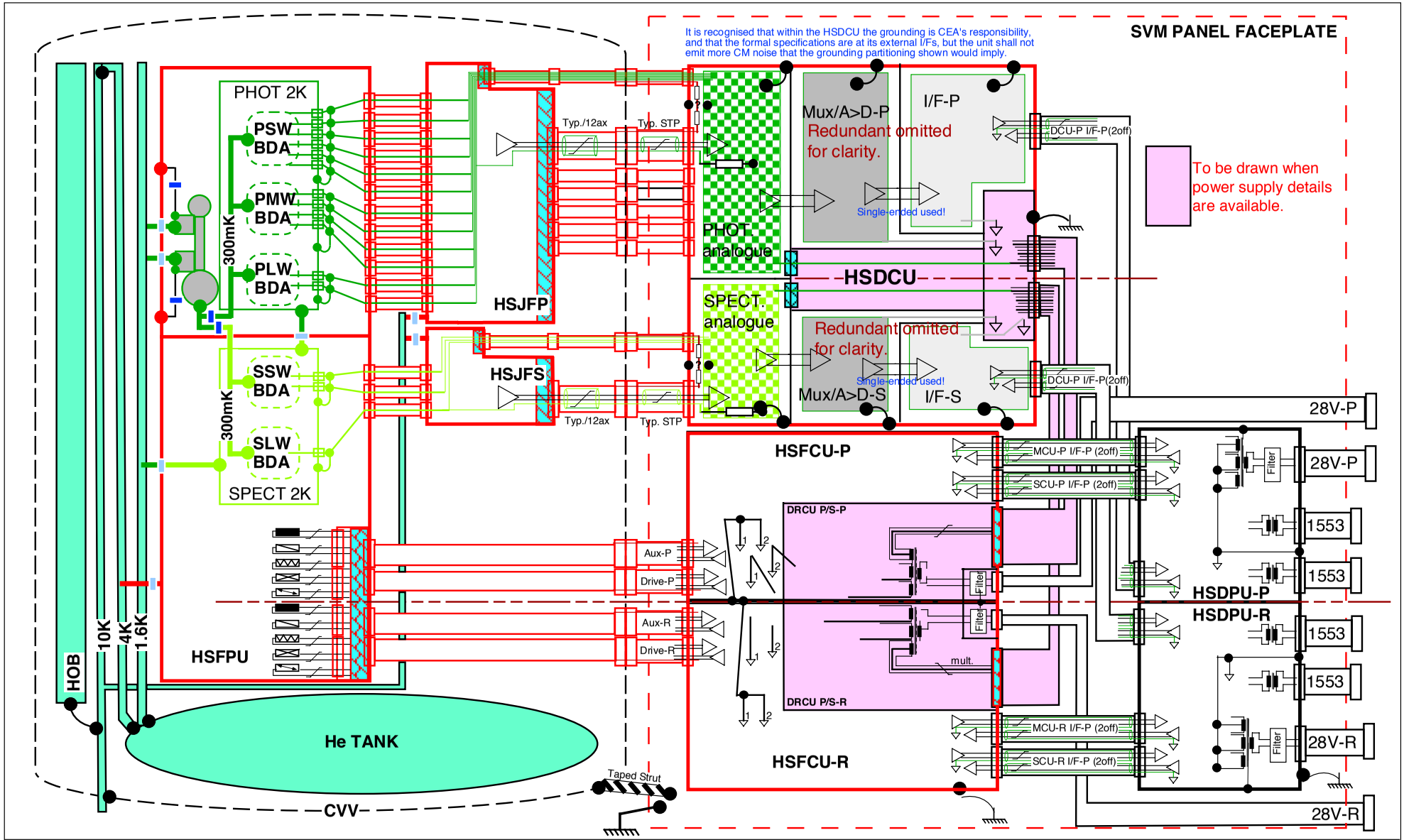
Simplify way backharness with bias grounds is drawn.

Add ground LINKS from LIA analogue ground to HSDCU chassis, previously only a "can we include as an option to try" link.

Change Spectrometer ground colour so no-one can assume it's the same as the Photometer!

Remove cross-feeds from Spectrometer LIA to Photometer, and visa versa, which where a left-over from old ideas.

Add note giving CEA flexibility within HSDCU.




**HERSCHEL SPIRE GROUNDING SCHEME**

JD 15th July 2002

RF shielded cable joined to connector backshells both ends and so closing Faraday Cage

Join | Sapphire Break | Other Break

Secondary ground or ground plane

To S/C chassis

Cristek etc. Connector RF Filtering, sealed to wall of Faraday cage

Transformer coupled I/F, no signal ground line.

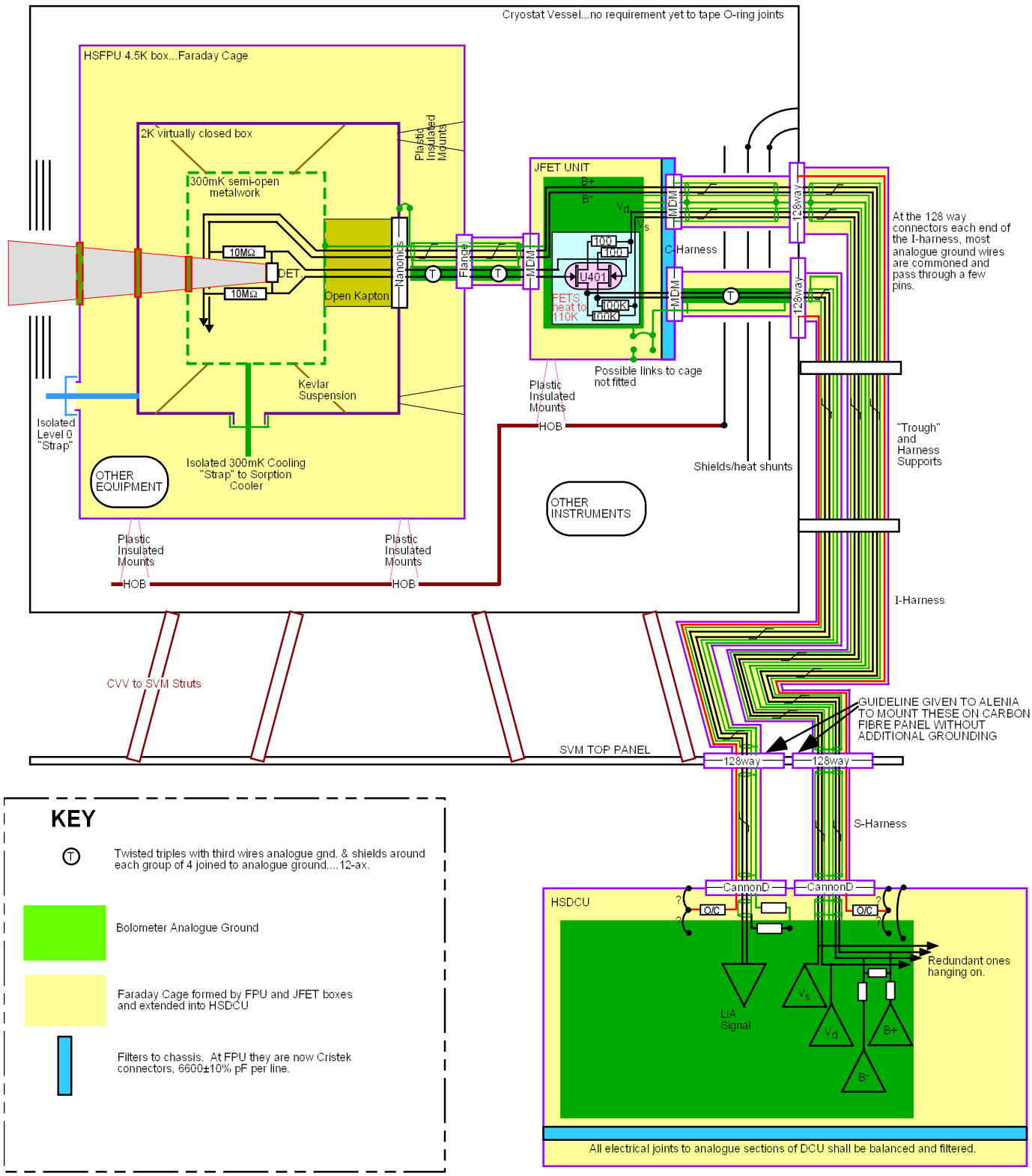
Differential Transmitter, no signal ground line.

Differential Receiver, no signal ground line.

Power Transformer with Electrostatic Screen

Resistance
Winding (e.g. Motor)
Relay coil
Heater
Sensor
Temperature Sensor
Cal/Stim.

# SINGLE DETECTOR DETAIL GROUNDING



## Aditional Information

### Minutes of DRCU Meeting at SAP 28/5/02

**Present** Jean Louis Augueres
Jean Bruston
Christophe Cara
John Delderfield
Matt Griffin.
Eric Sawyer
Dominique Schmitt
Laurent Vigroux

**Objectives**

· Clarify SPIRE grounding concept and DRCU design
· Review DRCU document status
· Establish plan for the DRCU DDR

**1. Grounding**

· Grounding scheme was sent to RAL about 2 weeks ago.
· Note on EMC/grounding by Dominique Schmidt distributed yesterday.
· Summary of overall system by Christophe. Power supply system diagram and switching concept explained.
· The number of converters running simultaneously has been minimised.
· John stated that all SPIRE DRCU converters running simultaneously should be synchronised.
· Dominique stated that the current injection spec as seen by the DRCU is not fully specified by the spacecraft. Filtering can be difficult to achieve. It is an aimed to have the shortest path for induced currents to ground. The dominant noise sources are in the warm side of the instrument and thus all noise sources should be minimised by design. This should apply to all platform equipments. Dominique believes that CEA's proposed scheme is the best one.
· There will be common mode voltages between the warm electronics and the HOB, this is a concern to JPL. JPL believe that signals will be injected into the detector system.
· Due to many unbalanced components, any current injected into the system by the power supply will get into the detector signal. Currents can be reduced by minimising loops.
· John explained that the only contentious issue regarding grounding is the configuration of the detector analogue ground, not the overall grounding scheme within the FCU.
· The JPL requirements document specifies that the analogue ground is at the BDA end and that the spectrometer and photometer grounds are separate.
· Implementation of the ground at the cold end is seen as very problematic by SAp:
    - o Serious compromise to the construction of the DCU grounding scheme.
    - o Implementing filtering needed for this option may require active components for filtering the low frequencies. Such filters are only effective at high frequency anyway. Filters need a reference ground and can inject current in many places. Selection of suitable filters is very difficult. Implementing filtering needed to have the option may require active components for filtering the low frequencies.
    - o If filters referenced to chassis are incorporated in the DCU undesirable currents will be injected into the system.
· It was noted that the DCU design includes local conditioning of the analogue supplies as they enter each LIA module. Were bypassing of HF common mode noise to be introduced at the FCU power supply output, this conditioning could allow the analogue ground to be disconnected from the DCU chassis and connected instead at the cold end. This would result in spike currents at the PSU end being returned locally, but at the same time having the signal analogue ground at the cold end. (***Note: Discussions of the SPIRE Project Team after the meeting concluded that this might allow the cold-end grounding to be implemented without major modification to the PSU as currently envisaged, and without major design changes to the DRCU - this should be discussed with SAp and CEA at the next telecon.***)
· A typical data sheet of one form of the Sextant power supply module was handed to RAL.
· Electrostatic shields within the toroidal converters are not practicable.
· Tests with the JPL/SAp cryostat system will not be very representative - the first representative test will be on the CQM instrument.

**Summary of position on grounding.**

Three options are:
1. Implement CEA grounding scheme.
2. Implement grounding at the cold end.
3. Ground at both ends.

**Option 1 (Current CEA proposal)**

· The system grounding scheme needs some iteration between CEA and RAL to define it in detail.

· This option requires electrical breaks in the 300 mK straps on the photometer and spectrometer sides to maintain separate grounds for the two sides of the instrument. There are concerns about the feasibility of doing this without suffering a large DT across the break or excess stray capacitance.
Action: Matt to arrange for feasibility study on implementing electrical isolation at 300 mK rather than 2 K. Maximum allowed capacitance is not clear - a few 10s of pF will be assumed for now.
· The first representative test will be the CQM. If problems are identified at that stage, major modifications to the electronic system architecture would be necessary. This would create problems as the power supply is contracted to a commercial organisation with a very stringent specification. Such recovery action and cost impact would need to be catered for by CEA as a contingency.
· This option is easier to model and understand, according to Dominique.

**Option 1 summary:**
Pro:
1. Compatible with existing CEA design and schedule for PSU procurement
2. More understandable
Con:
1. Requires change to the BDA SSSD, (which specifies that the ground be at the cold end)
2. Requires thermal isolation at 300-mK level - feasibility is not assured. If it proves impossible or unacceptable to implement this, then a solution with the analogue ground at the cold end is essential.
3. There is a risk that CQM testing could reveal fundamental problems - CEA would then have to implement a recovery plan.

**Option 2 (Modify DRCU to make it possible to ground at the cold end)**
· This would require redesign by CEA (extra filters etc). This could raise some technical issues such as accommodating large filter components, active filtering, mass etc.
· This option is possible but may introduce extra unforeseen problems and certainly more complication. It is also more difficult to analyse.
· There could be significant cost and schedule impact (although less that if recovery action is needed after CQM testing)
· DCU testing at unit level could be more difficult with a temporary ground being required.
· Dominique believes that grounding at the cold end makes the system more sensitive to mismatches in stray capacitance and harness properties.

**Option 2 summary:**
Pro:
1. More flexible - can try out both options with the CQM
2. Reduces technical risk at CQM level
Con:
1. Requires changes to existing CEA design and to PSU specification
2. More complex, difficult to analyse and model
3. More sensitive to mismatches in capacitance, harness properties
4. More difficult to test DCU before delivery.
3. Adds schedule and financial complexity to CEA programme which may affect project schedule

**Option 3 (Ground at both ends)**
· This is unlikely to be a viable option. It's against normal best practice - it might work but nobody would feel confident about it.

**Action summary**
· CEA to supply more details of grounding scheme and overall implementation of all individual power supplies.
· Cardiff to investigate feasibility of electrical isolation on the 300-mK straps.
· Telecon to be arranged with JPL ASAP to discuss optimum grounding option. **(*Note: RAL will try to set this up for 4.15 pm UK time Thursday*).**
· Objective = Make decision within one week to allow design and PSU procurement to go ahead.

**2. DRCU Documentation Status**
· DRCU specification document 0.91: Updates planned, should wait until power supply grounding concept is agreed.
· DRCU design description 0.1: Reasonably complete updating required
· DRCU ICD 0.6: Significant work required.
· Interface drawings
    - o Required by ESA/Alcatel.
    - o More information required as per IID-A.
    - o New ICD will incorporate design updates.
    - o New drawings to be available 7 June

**3. New IID-A Issue 3 redlined copy distributed by Alcatel**
· This version is regarded by ESA as an ECR. It has no formal status at present.
· Instrument teams are providing comments on it.

· None of the proposed changes should be taken as meaning that we have to modify existing designs.
· SPIRE and the other instruments are being designed according to the IID-Bs
· In reviewing the proposed changes, ESA will have to take into account and objections from the instrument teams based on schedule/cost implications of design changes that may be needed

**4. Plan for DRCU DDR**

· A formal DDR on the DRCU is still outstanding
· Like all DDRs, it shall be based on a review of the documentation, with a meeting/presentations to be arranged if it's deemed useful

4

· To expedite the process and ensure earliest possible consolidation of the key design documents and all information that impacts the system or other subsystems, a two phase approach shall be adopted.
· Phase 1 shall review:
    - o DRCU Specification Document
    - o DRCU Design Description Document
    - o DRCU ICDs
    - o Commanding Document
· Documents for Phase 1 shall be distributed by end of June: they can be distributed earlier as and when they become available.
· A Review Board will be identified by SAp in consultation with the Project Team. ESA will be invited to participate and be on the Review Board (with Jean Bruston as point of contact)
· Phase 1 of the review will be closed out by the end of July
· Phase 2 shall review of all other documents in the standard list for SPIRE DDRs, and shall be completed by date TBD ***(Suggest end September)***.
· CEA stated that two new people would shortly be starting work on Herschel, one PA specialist and one electronic engineer.

Date: Fri, 31 May 2002 15:46:01 +0100
To: Jean-Louis Augueres <augueres@cea.fr>, Jamie Bock <jjb@astro.caltech.edu>,
Christophe Cara <ccara@cea.fr>, John Delderfield <J.Delderfield@rl.ac.uk>,
Victor Hristov <vvh@astro.caltech.edu>,
Gerald Lilienthal <gerald.lilienthal@jpl.nasa.gov>,
Gary Parks <gparks@mail1.jpl.nasa.gov>, Eric Sawyer <e.c.sawyer@rl.ac.uk>,
Dominique Schmitt <dschmitt@cea.fr>,
Laurent Vigroux <vigroux@discovery.saclay.cea.fr>
From: Matt Griffin <Matt.Griffin@astro.cf.ac.uk>
Subject: Grounding/filtering Tiger Team
Cc: Peter Hargrave <peter.hargrave@astro.cf.ac.uk>,
Bruce Swinyard <b.m.swinyard@rl.ac.uk>

Hello all,

Here are some conclusions from yeterday's telecon and my proposal for how to reach a conclusion on this complex issue.

1. The SPIRE grounding concept has been that the detector/JFET hardware and the warm electronics be designed such that it be possible to implement the single point ground either at the warm or the cold end.

2. The BDA/JFET design has been implemented with a view to cold end grounding but may be compatible with warm-end grounding. The proposed DRCU design is stated not to be, and would require that the analogue ground for the detector signals be at the warm end.

3. Viktor and Dominique (both highly experienced and competent in this business) are not in agreement as to the optimum grounding scheme.

4. Jamie emphasises that the most important issue is not whether the ground is at the cold or warm ends but the level of filtering on the power lines, and wishes the flexibility of option 1 to be retained.

5. There is also a requirement that the photometer and FTS grounds be separate. This requires that the 300-mK thermal straps have an electrical break in the event of the ground being at the warm end. To meet (1) above, we therefore need to have this as an option. It should therefore be implemented in the 300-mK strap development programme and qualified in the STM.

6. It is not yet clear (to me anyway) what the technical/schedule/cost impact is going to be if it is concluded that the cold-end ground option has to be retained or that additional filtering is needed in the DRCU.

7. A Tiger Team is now established to:
- study the options and relevant trade-offs
- recommend a solution to be implemented

* I shall chair the relevant telecons.
* John shall organise the Tiger Team, requesting, collating, and analysing all necessary inputs from the team, reporting on the technical evaluation, and leading the relevant e-mail/telecon discussions.
* Tiger Team membership
  - Matt and Laurent as PI and Co-PI
  - JPL: Jamie, Viktor
  - SAp: Dominique, Christophe, Jean-Louis
  - RAL: John, Eric (Bruce is now on holiday until June 24)
* The first telecon is provisionally scheduled for Thursday 6th at 16.00 UK time. Telecons will be set up by RAL (please don't phone in - let Eric and John know your number and they will phone out).

8. Following the evaluation and recommendation, a decision will need to be made on what to implement, which should be by consensus between Matt, Laurent, and Jamie.

Cheers,

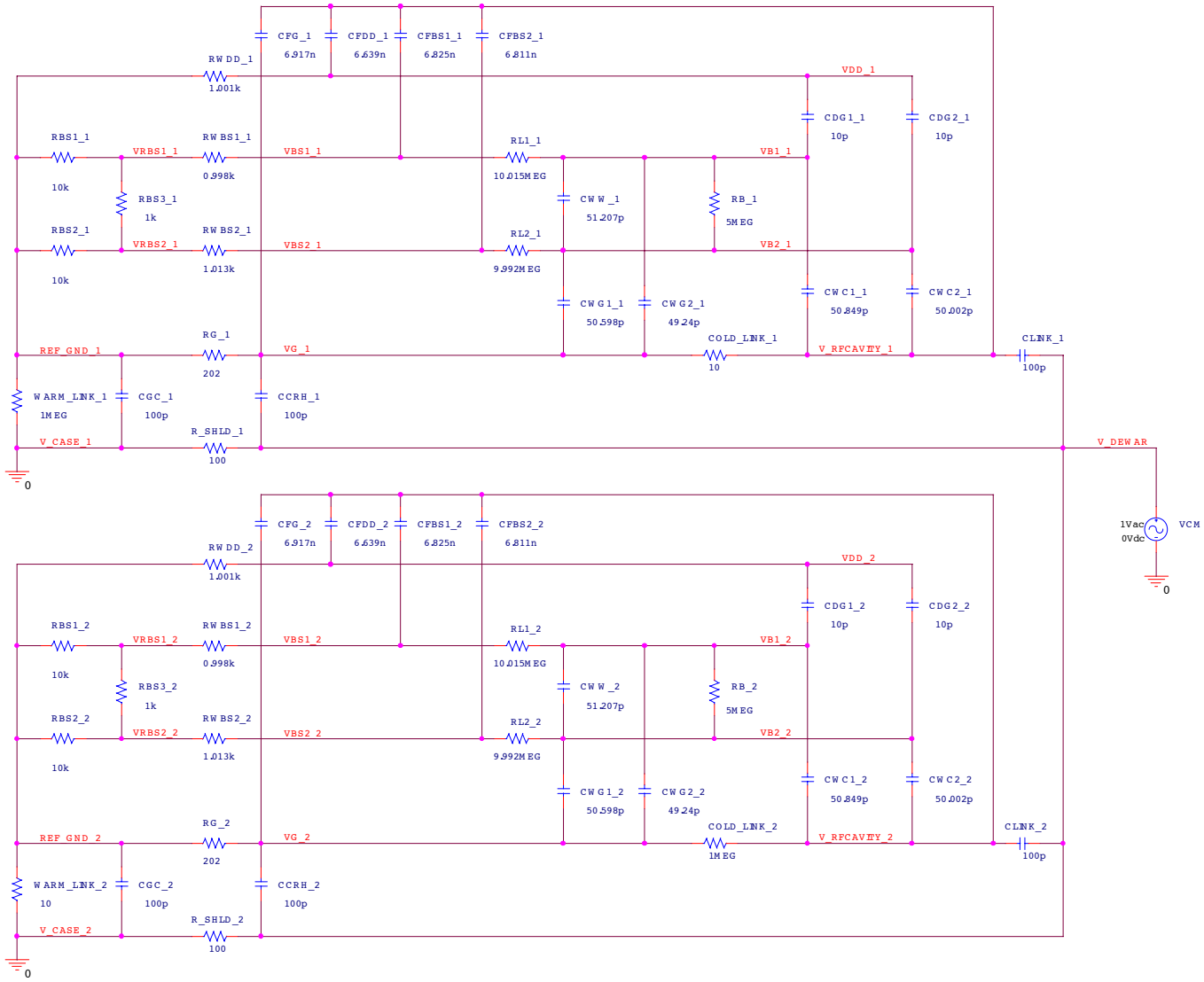
Matt

## NAIVE MODELS FOR THE SAP AND THE JPL GROUNDING SCHEMES

In this work I did a naive comparison of the power propagated into a bolometer due to EMI source acting between the bolometer reference ground and the dewar for the both proposed grounding cases:

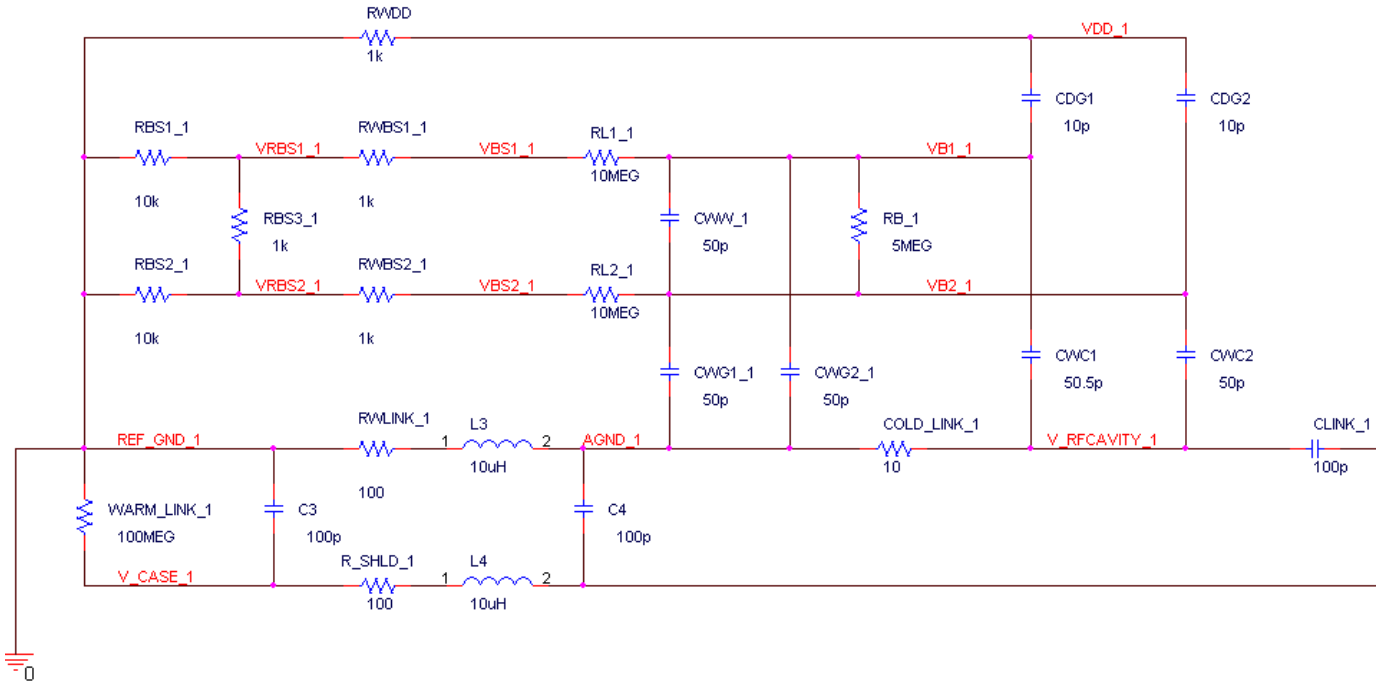
- JPL/Caltech with a direct link between the bolometer reference ground and the Faraday cage,
- SAp case with a bolometr reference ground tied to the frame ground, then connected to the Farday cage.

The schematic diagram of the PSPICE simulation is shown here:



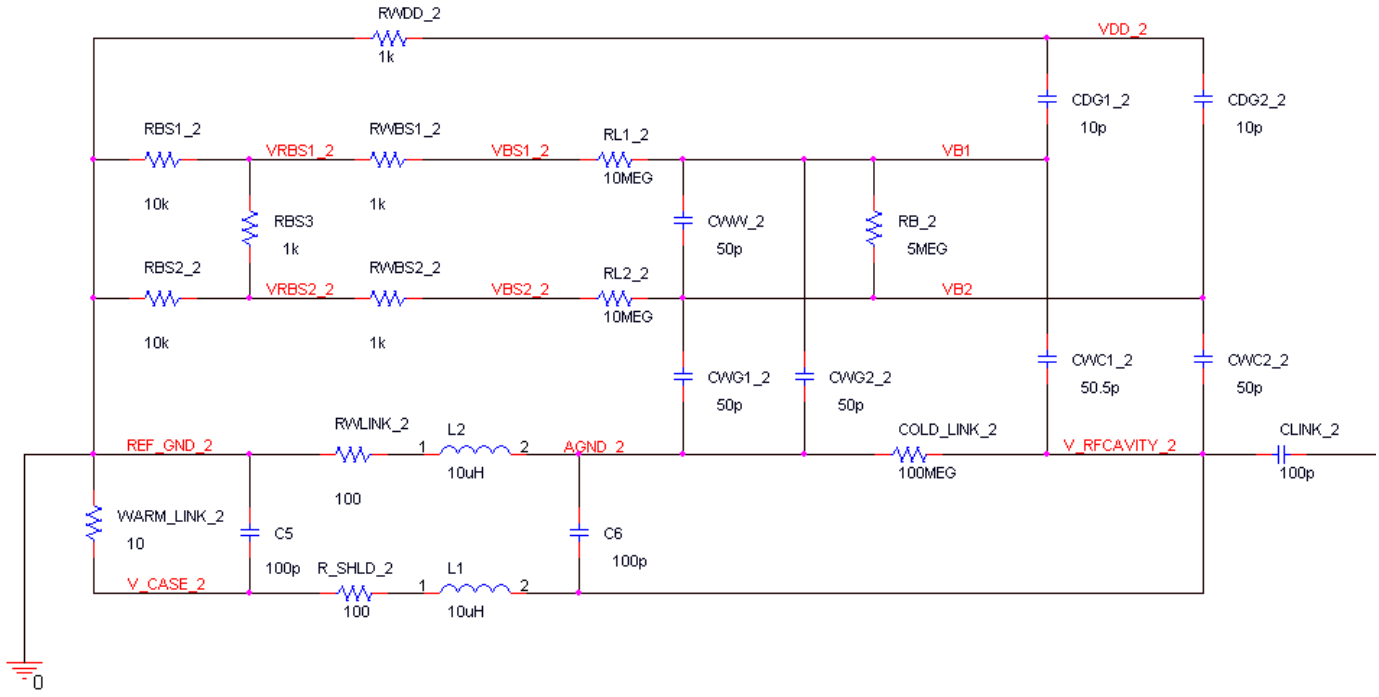

The schematic have two identical blocks that represent the links between the warm electronics bias driver and a bolometer located into the Faraday cage. Each Faraday cage is capacitive coupled to the dewar with a common EMI voltage source acting on the dewar wall.

The upper block represents the JPL/Caltech grounding strategy with a high impedance link between the bolometer reference ground and the chassis, and a low impedance link between the bolometer reference wiring and the Faraday cage.



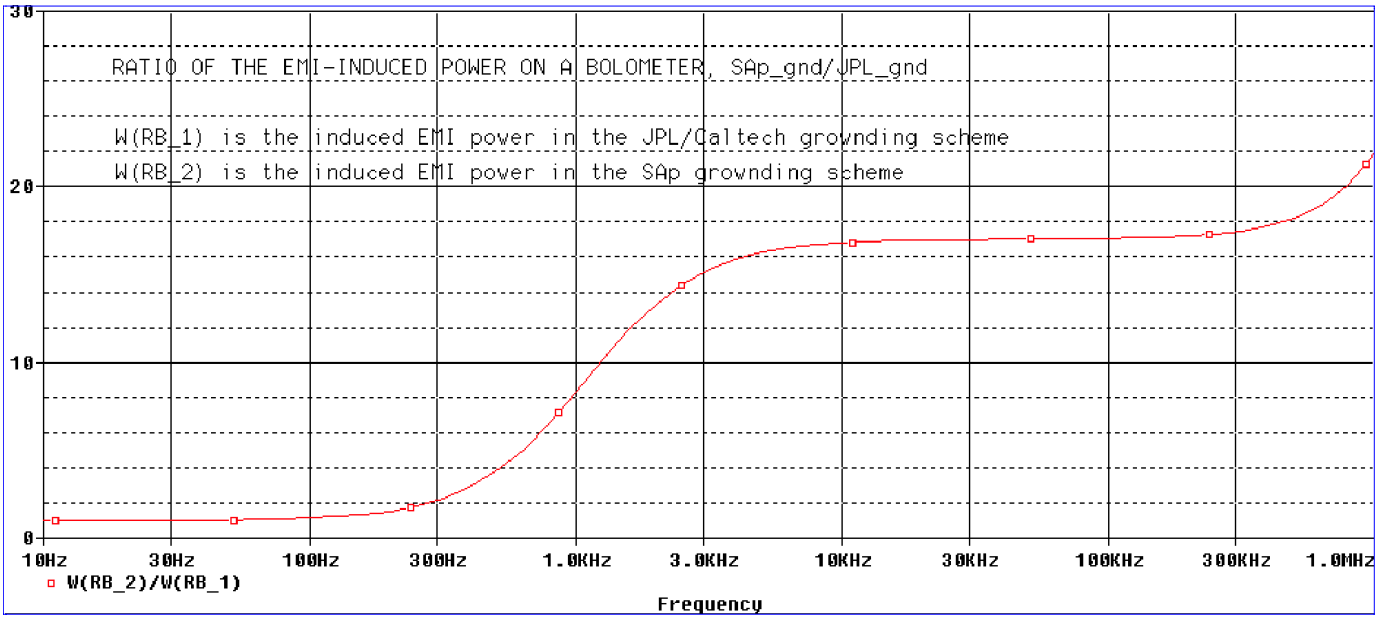

Here WARM_LINK_1 is the high impedance link between the reference ground and the chassis, the COLD_LINK_1 is the low impedance link between the wired reference ground and the Faraday cage. The chassis is connected to the dewar via the common over shield. All but one of the capacitive coupling to the both bolometer terminals are balanced. The CWC1 and CWC2 that represent the capacitive coupling between the bolometer wires and the Faraday cage are mismatched by 1%.

The lower block represents the SAp grounding strategy with a low impedance link between the bolometer reference ground and the chassis, then a low impedance link between the chassis and the Faraday cage.




Here WARM_LINK_2 is the low impedance link between the reference ground and the chassis, the COLD_LINK_2 is the high impedance link between the wired reference ground and the Faraday cage. The chassis is connected to the Faraday cage via the common over shield. Again all but one of the capacitive coupling to the both bolometer terminals are balanced. The CWC1_2 and CWC2_2 that represent the capacitive coupling between the bolometer wires and the Faraday cage are mismatched by 1%.

To estimate the relative merits for each of the grounding schemes, a ratio of the power dissipated on the respective bolometer due to the common EMI source is taken.




According this naive simulation, the SAp grounding scheme will perform SIGNIFICANTLY worse than the JPL/Caltech one. At very low EMI source frequencies both grounding schemes perform in similar fashion, at medium frequency range characteristic for the SMPS ripples at operational frequency of 20-100 KHz, the SAp grounding is worse, and at the high frequency end, associated with the SMPS switching noises, the SAp scheme performs even worse.

Viktor Hristov
4/5/02