SPIRE-RAL-PRJ-00624

as distributed on 5th April but with Q&A attached at end

10th April 2001

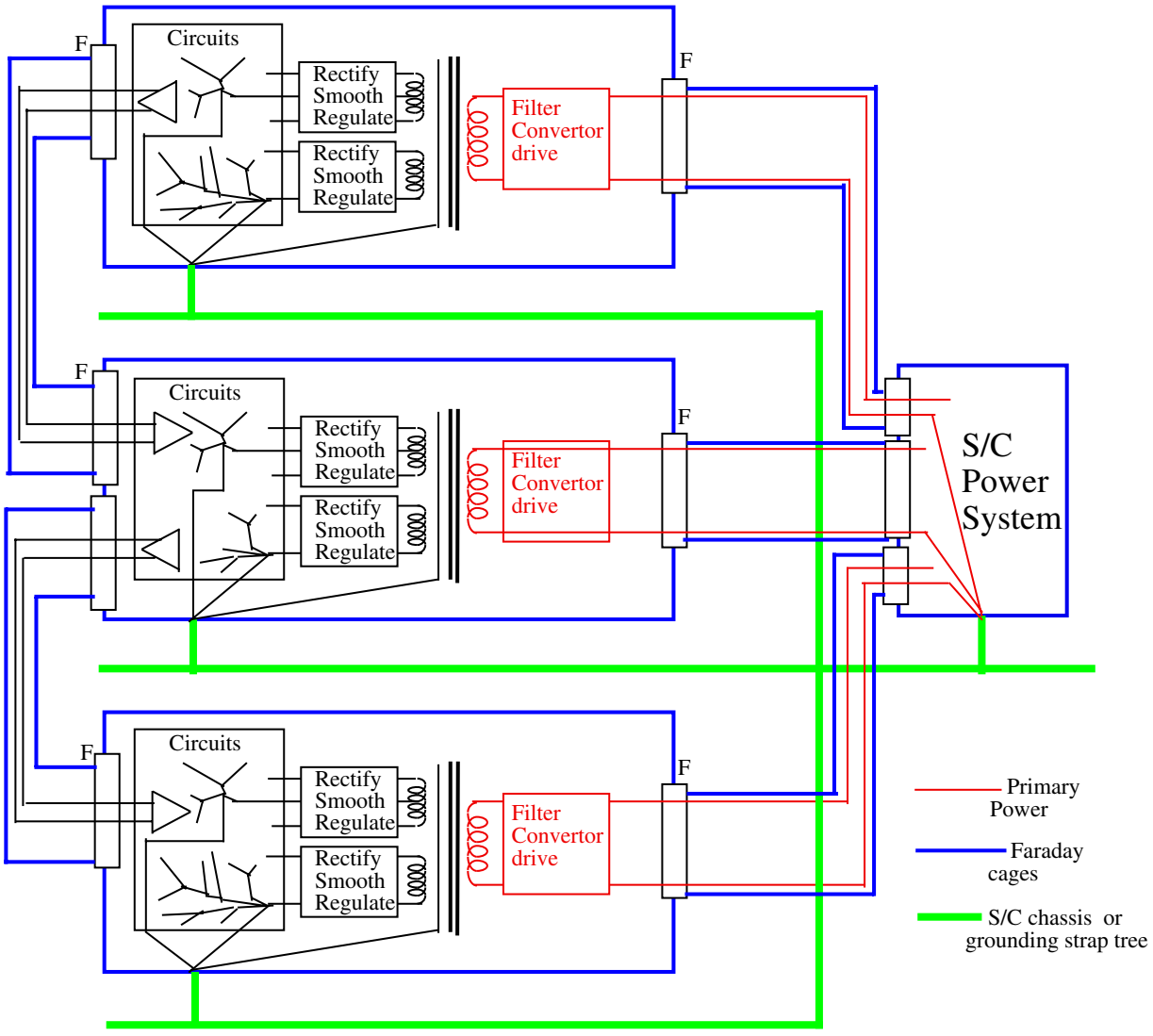
To: SPIRE Electronics +Sam(Thermal)+Berend(Structural Isolation), +Lionel (Cooler isolation/resistance)

From: John Delderfield

GROUNDING and SCREENING PHILOSOPHY

This note arises from my action from Monday's meeting to write out the SPIRE grounding requirements explicitly, particularly as regards the bolometer systems. Requirements on the electronics are in red text. To present a perspective that is hopefully coherent, the rationale will be included. I appreciate that this will be a restatement of what is already clear to many recipients or regarded as good practise.

In general terms SPIRE shall conform to an ESA classical unit by unit secondary power configuration of this nature:



Each unit is electrically self-contained in its grounding.

- It has a chassis/box that is closed to form a conductive Faraday cage, i.e. enough thickness in skin depths/bulk conductivity (essentially inevitable) and with all apertures including vents and joints having controlled geometry with adequately small maximum dimensions.
- Except the S/C power system, primary power is isolated from chassis, although for each unit there is a small permissible input capacitance and possibly a large electrostatic protection resistor to chassis.
- Each unit is powered with secondary (or conditioned) power which is isolated from the primary power buses and unipoint grounded to unit chassis, a joint which is best made near the same point on the chassis as is externally connected to S/C. This internal link may need to be via an externally accessible strap to permit secondary ground isolation testing.
- All signal inputs and outputs are differential and ideally pass through filter connectors to protect the unit from external noise entering the unit via harnesses. Signal ground lines do not pass between units. Inputs are normally high impedance and are required to maintain a defined high impedance w.r.t. chassis. Outputs are required to have controlled slew rates, minimum skew to limit common mode spikes, and little ringing.
- The secondary grounds with each unit are carefully configured in a documented way and if multiple supplies are used the grounds for each supply are separately controlled with a minimum of joins between the supplies, classically just one at the unit unipoint.
- Theoretically there should be no current flow in any ground wire, which should only be used for signal voltage reference, but in unipolar supply situations, when 0V and signal ground are one and the same, current flow is unavoidable. This is just one example of the general requirement that any device taking a.c. current shall have adequate local decoupling/filtering, obviously to ensure its own correct operation, but also adequately to inhibit noise propagation to other elements in the unit; logic or digital functions can be the most troublesome with their a.c. components taking the form of switching noise.
- Depending on the susceptibility of circuits, logic signals that travel a distance across a unit may need to be slowed down with series resistors and squared up again on receipt by Schottky buffers such that excessive dV/dT noise is not broadcast.

There are several relaxations in the ideal that are commonly acceptable. Filter connectors introduce their own problems and the careful specification of input susceptibility and output emission levels often allows requirements to be met with un-filtered connectors. In such a cases, common mode filtering with defined differential mode bandpass is often introduced on signal inputs to compensate. Formal unipoint strapping to a S/C grounding tree is often discarded and a unit is simply conductively mounted by all of its mounting feet…..this is no problem as long as no other equipment is returning current along the S/C chassis and potentially thus inducing a.c. signals in the unit's Faraday cage.

On the other hand, there are many options for improving the operation of such standard configuration, to further limit the propagation of noise between elements inside it.

- internal division into a card rack and a compartment housing the noisy power supply with bulkhead filters between the two.
- improving the Faraday shield with thin metallic inter-board shields or even formal internal divisions with bulkhead filters. Such shields are often used if frequencies are being multiplied and shifted or if one board contains logic and other only analogue {All are electrostatic screening connected solidly to unit chassis; I'll omit the less common magnetic screening from this note}
- Accepting a certain level of ground current but defeating the induced ground voltage noise by using highly conducting low inductance ground planes, but unless a special analysis is performed these should only be used in conjunction with other good practice (local decoupling, separation of grounds, chassis isolation with unipoint contact, etc.). More complex scenarios exist: ground signal planes may be combined with power supply planes, the ensemble being multiply capacitively linked; physically thicker power planes may be sandwiched into PCBs, electrically isolated from the circuits on them but firmly joined to unit chassis so as to extract power but also to double as extended Faraday screens.
- Mismatching impedances/4-wiring. Mismatch is inherent in many architectures that use low impedance drive and high impedance inputs, but I'm referring here to using high impedance current drive into relatively low impedance input. Used with or without formal differential signals, this is another way of removing a dependance on a quiet voltage reference ground.

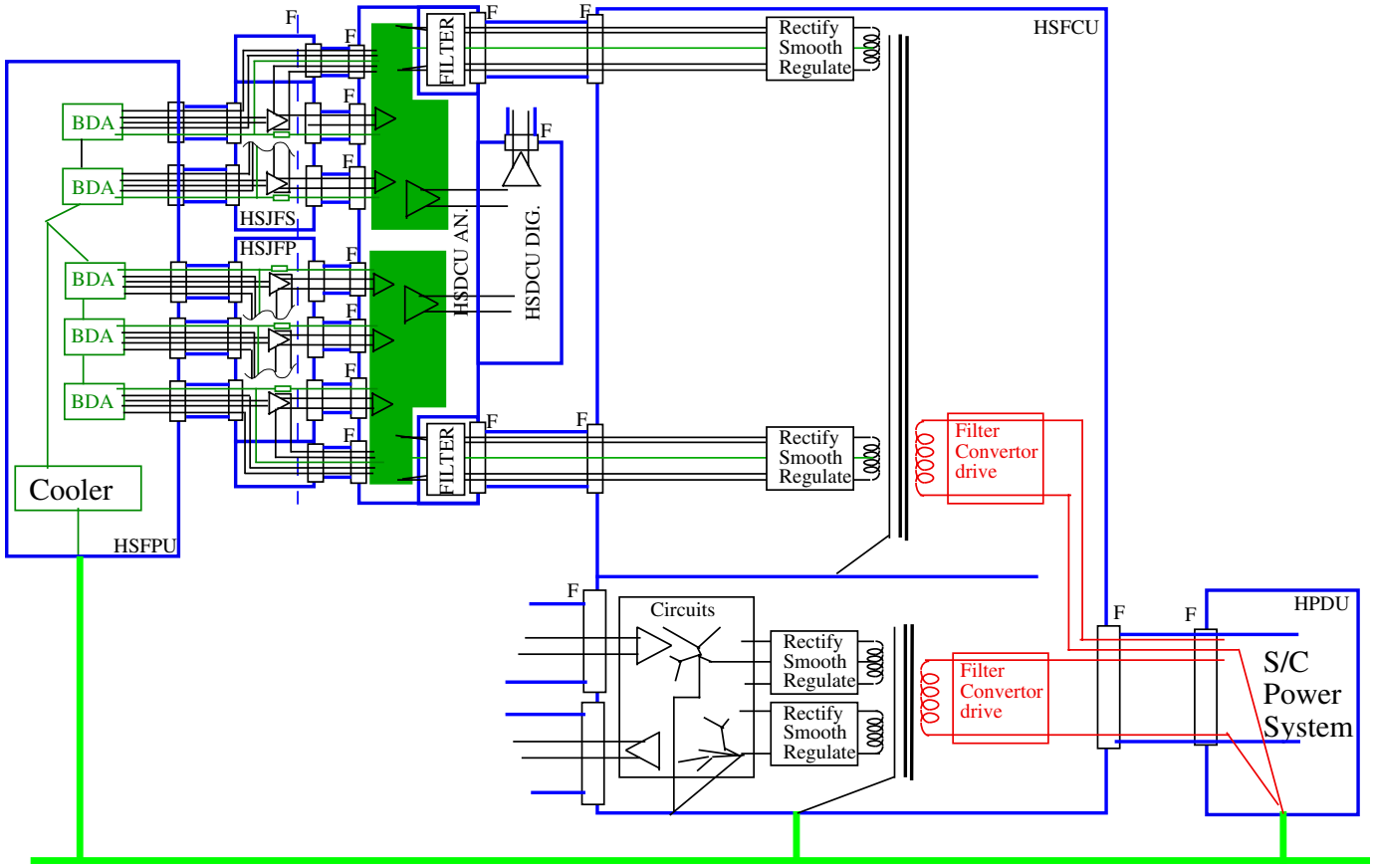
Differential digital interfaces do not provide ideal isolation. In particular, the driver has to provide significant edge switching currents to drive harness capacitance, a situation that gets worse if the I/F is between units, the receiving unit inputs have capacitive filter elements, harness lengths are long and have screens, etc.. Depending on frequency, power, radiation environment and money, such interactions between supposedly separate grounds may be improved by using transformer coupled buses or opto-couplers.

The whole arrangement so far described is prefixed by "in general terms". The configuration is best suited to systems in which each unit operates over a restricted range of signal level. In Spire this would apply to the HSDPU. Otherwise transmission of noise from high level circuits such as power convertors to sensitive analogue elements get more and more impossible to achieve. Considering the front-end signal source in Spire, we have an noise spec. of 7nV/√Hz at about 2.5MΩ and 300mK. There comes a point when the need to control noise requires separate preamplifier unit(s), preferably with an electrostatically screen separating it (them) from any digital functions such as multiplexors or A-D convertors, with the signals then transferring to a conventional unit via balanced digital I/Fs. The power needs to be fed to this system's analogue sections extremely quietly, prefiltered and actively regulated with external sensing in an external unit. It must then be filtered in a separate compartment within the analogue unit that has bulkhead connectors feeding to the analogue system. Grounding has to be very carefully configured as secondary grounds are implicitly distributed outside of one unit. If one considers the whole volume of the various units in this supply system as if it were joined into one by the harness screens that join them, the grounding it should look like a unipoint tree as if it were still within one unit.

Multichannel operation requires adequate interchannel screening and a configuration that keeps any designed-in signal cross-talk to below specified levels.

We conceived of the following concept early in the autumn of 2000, following the design decision to separate the spectrometer and photometer JFET units so they could be accommodated adequately near to their respective detectors, the specification then being <8pF along the cable as seen by each 5MΩ detector. It was also really stressed by those with experience that Spire's bolometric detectors are unbelievably sensitive and would make corrupted measurements if unwanted r.f. were to be dissipated in them, the biggest risk being that wires have to be attached to them!!

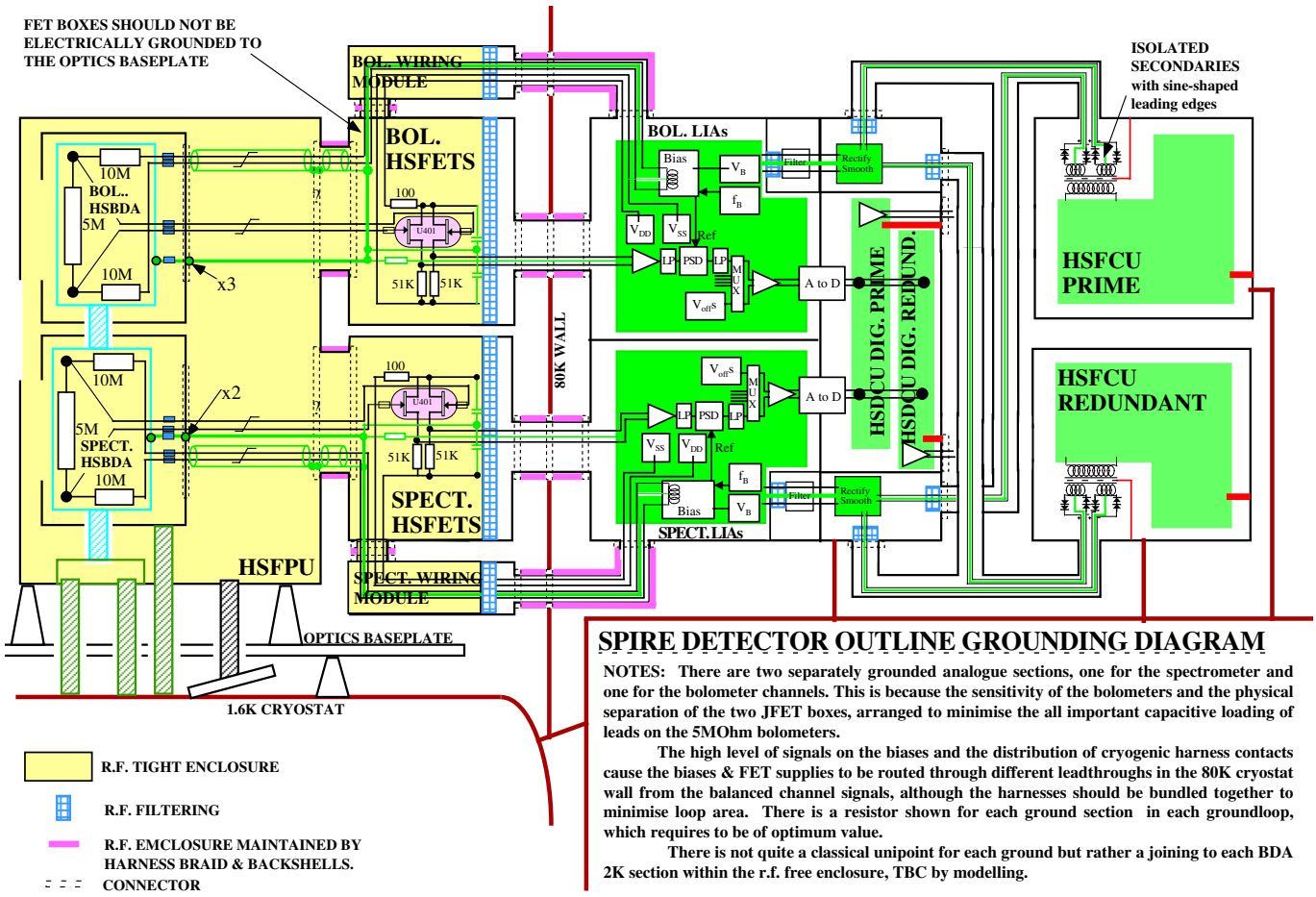
So the following concept was adopted at a video conference from RAL to JPL with Christophe Cara present at the RAL end.



I've used up-to-date acronyms and ignored any redundancy in this drawing to minimise confusion. The essential specifications are:

- signal power gain from external JFET amplifiers
- separate analogue ground paths, without loops, between spectrometer and photometer systems
- maintenance of single point ground joins to S/C chassis
- analogue power, quiet and regulated, supplied from a unit external to the one that houses the sensitive analogue systems.
- ground-plane option invoked to keep a large area of analogue signal ground quiet in each of the spectrometer and photometer parts
- the detectors to be in a Faraday cage with full filtering on all wires entering it (non-bolometer ones not shown) extended with full shielding into the JFET boxes.
- MDM connectors on the JFET boxes not available cryogenic filtered, so a separate compartment division is introduced in the JFET boxes with ceramic feedthrough filtering to close the Faraday cage.
- unipoint analogue ground for the system at the 300mK BDA units that are unavoidable coupled with cold-plumbing busbar ink. This minimises Voltages between the bolometers and their local chassis.
- information transfer out of the digital part of the HSDCU via normal balanced ESA-type digital interfaces, both fast and slow, to the HSDPU (not shown but having its own separate conventional grounding scheme).
- The need to bundle together groups of long harnesses between HSJFETs and HSDCU (not shown here but see instrument block diagram) to minimise loop area between bias routed analogue ground lines and differential signal lines. Admittedly they are inside shielded harnesses but one cannot have much common mode signal at the DCU's inputs even with good CMRR before a 7nV/√Hz differential noise performance is degraded.
- An optimised multiplexing/transfer of data from the analogue sections of the DCU to the back-end digital ones to minimise current injection back into the analogue ground and hence potentially back to the detectors.

With all the above in mind, and having seen some circuits for the DCU, the following grounding scheme was published in November 2000, was circulated to project, and on which few comments have been received:



SPIRE DETECTOR OUTLINE GROUNDING DIAGRAM

NOTES: There are two separately grounded analogue sections, one for the spectrometer and one for the bolometer channels. This is because the sensitivity of the bolometers and the physical separation of the two JFET boxes, arranged to minimise the all important capacitive loading of leads on the 5MOhm bolometers.

The high level of signals on the biases and the distribution of cryogenic harness contacts cause the biases & FET supplies to be routed through different leadthroughs in the 80K cryostat wall from the balanced channel signals, although the harnesses should be bundled together to minimise loop area. There is a resistor shown for each ground section in each groundloop, which requires to be of optimum value.

There is not quite a classical unipoint for each ground but rather a joining to each BDA 2K section within the r.f. free enclosure, TBC by modelling.

I have to be honest and say that this is the version that I now have on my computer and not the exact one from last November, but they differ only in detail.

Before we discuss the middle of this system, let's consider its ends, first towards HERSCHEL. Spire is defined at IIDB level as having a prime DPU and DRCU, plus a redundant pair, non-cross-strapped, of which the Herschel platform shall only empower one half at any one time. Now the DRCU is no longer a physical unit but has been split into two, the DCU and the FCU, both parts shall appear to the DPU and hence HERSCHEL to be simple prime/redundant units. The bolometers and the analogue section of the DCU are non-redundant, the former because it's not clear how they could be built into Spire, and the latter because it's difficult to achieve low noise from a bolometer into two preamplifiers plus the shear amount of electronics involved.

The Spire estimated MTBF must be met, which places a very high requirement for reliability on those elements which are not redundant. Formally there is no requirement that the bolometer bias and JFET supply generators be prime and redundant, merely that the functions be at least double wired across the cryoharness because of the noted less-than-ideal reliability of cryoharness. This is as shown in the above diagram. The DCU designer may choose to use prime and redundant bolometer bias and JFET supply generators if they are required to achieve the required MTBF, if they can be joined into the grounding system, if they do not degrade the bolometer S/N, and if EACH can still be at least double wired across the cryoharness. Such redundancy causes the bolometer JFET unit frames to need to house duplicated filter units but it is believed that this can be accommodated together with double the amount of back-harness.

The DCU digital sections, driving and receiving signals across via external I/F to other HERSCHEL SVM mounted units, have conventional ESA grounding configurations of the type with which this note starts, except that their power is supplied (not shown) just from the appropriate Prime or Redundant FCU. Data transfers of digitised bolometer signals leave the DCU in packet burst mode at quite high Baudrate which precludes the use of interfaces that might provide higher ground decoupling. Therefore these digital section of the DCU must be regarded as noisy in bolometer terms and be configured as shown in the diagram, i.e. within an isolated sub-compartment. The configuration of a DCU digital section power supply from the FCU and the section's input coupling from the preceding DCU section, shown conceptually in the grounding diagram as being an analogue section joined via an AtoD convertor, shall be such as to minimise charge injection/current into the latter's ground. This is because any such injection is potentially into the sensitive bolometers via the system analogue ground, and JPL expressed concern in this regard.

Second, consider some details the FPU end.

In setting up the grounding diagram with the JFET filters closing the wiring Faraday cage, their chassis have to be electrically isolated from the HERSCHEL optical bench, as noted in the grounding scheme. Please check that the mechanical outline of this is in the thermal model.

It also follows that the tightly bundled cables from the JFET filters to the outside of the FPU have to have a high coverage screen around each of them to keep the Faraday cage closed. However it's vital that these cables be heatsunk to the optical bench to minimise JFET heating of the FPU, so they need an external insulator at least where they are clamped. I believe that the thermal budget can stand an external shield around these cables [besides the 12-ax braids that I would like to keep insulated and associated with signal ground not chassis] terminated one end on JFET connector backshells and the other to the FPU wall. Please check that the mechanical outline of this is in the thermal model.

All non-bolometer wiring entering the FPU does so via JPL provided filter boxes mounted such as to provide a closed Faraday cage. This clearly applies to the cooler's wiring and it is nominally isolated from chassis. Nevertheless, because JPL correctly identified the cooler as being very much coupled into the bolometer system, all signal sent to the cooler must be especially quiet. Please could the SCU design description document include these details and perhaps a breadboard cooler section of the SCU should be used on a sorption cooler at BDA unit level testing to check for problems. Any proportional heating needs to be heavily filtered in the SCU before being output so as to appear as "d.c." to the cooler heaters even discounting any filtering in the FPU boxes [which are intended for r.f. not power filtering!]. If temperature sensors are only conditioned in a duty cycle as they need to be read out, the start and finish of even this low level conditioning shall be ramped not stepped.

Now consider some more of the FPU grounding details. I have to admit that thinking things through to write this all out has made me aware of some details I'd overlooked. In keeping with the unit to S/C ideas spelt out above, all three main FPU mounting feet need to include electrical breaks, probably as necked

plus simple bushes/washers at one end or the other. This is probably a new electrical requirement to be identified at system level, except that as has been pointed out it is actually part of a long-standing JPL bolometer requirement that the Faraday cage be isolatable. Thermally this should be no problem as the feet are seeking to achieve isolation anyway. Mechanically the feet have to keep instrument alignment with the HERSCHEL telescope, so good tolerancing becomes essential at the isolated end to remove any slop as metal dowels etc. that end used as part of an alignment procedure would short out the insulation.

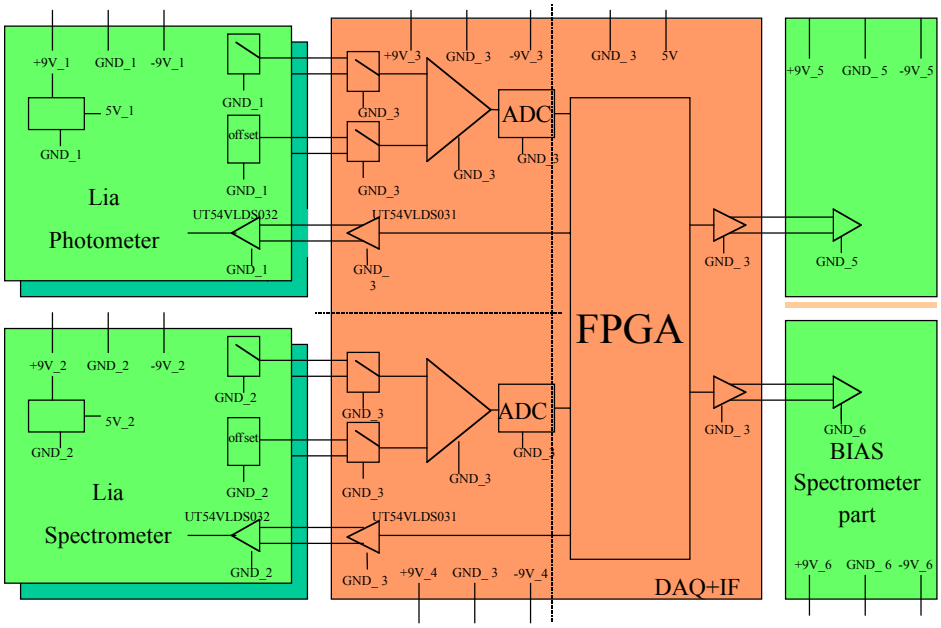
I originally thought the BDAs might form a Faraday cage themselves with an electrical break in the 300mK plumbing, but the BDA 300mK sections are suspended from 1.8K mounting rims linked by open Kapton ribbon harnesses which precludes this approach by definition…without thermally shorting out the Kevlar suspension. I had not at that stage caught up with the agreement that the FPU was the Faraday cage, and this approach was quickly reverted to. However, back in November, I outlined a marginally non-ideal configuration. The 1.8K BDA mounting rims interface to two almost closed boxes inside the FPU Faraday cage and are also places where internal signal grounds can be joined. The two boxes are themselves joined by a conducting thermal strap internal to the FPU box. I therefore show all of this joined in something akin to an internal distributed analogue ground plane that almost forms an internal secondary shield. In unit electrical grounding terms it is analogue ground isolated from chassis.

Now we come to a trade-off which RAL intends to resolve at system level first by estimation using a computer grounding model and second by test verification. This is, "Where do we join the bolometer analogue ground to chassis?". Viktor has expressed a preference for grounding it all at the DCU and having the cryogenic end including the FPU Faraday cage all isolated. The above grounding scheme actually baselines the opposite approach which is to isolate the DCU end and to electrically ground the very sensitive cryogenic end to cryostat by using the four electrical links that result from the thermal design. I have yet to see results from the computer grounding model and the safe baseline is to use electrical breaks in the four FPU thermal straps shown on the grounding diagram. Bruce is sure that there is an applicable qualified ISO way of doing this mechanically with sapphire sandwiches.

From a grounding viewpoint, it follows that all thermal/anti-microphony holdowns on the cryoharness shall not electrically short these harness shields to chassis except at the controlled CVV connector plane. This would follow automatically if the harness has an outer insulator covering.

Now we reach the centre of the system, the DCU analogue sections themselves. I suggested last year that the biases to each BDA be supplied via individual transformers to easily reference them quietly to the OV of the relevant JFET supply, clean off high frequencies, scale down a higher level synthesis to the required bias levels, provide some drive output short protection, etc. I still like this idea but it is not a requirement, merely a suggestion for implementation. I originally had the grounds for each of these biases joined into the grounding scheme at the BDAs, which is probably ideal, but combining the bias ground with the OV of the relevant JFET supply as is shown in the above version of the grounding scheme has real advantages w.r.t. the need for multiply wiring these functions along the cryogenic harness.

Now we need to appraise the DCU design, hopefully to find that it fits in with the specified Spire grounding scheme. I've taken Frederic's input and increased the text size + changed colours.



This is a very encouraging starting point. Comparing this with the grounding diagram, we can note the split between the spectrometer and photometer analogue grounds, G1+G5, versus G2+ G6. The isolation of the Lock-In-Amplifier grounds from the Bias/FET power supply grounds is an improvement on my solid ground plane for each side. I would encourage the ±9V powered high level analogue sections to be split into separate grounded sections as mentioned at the meeting and as shown by the dotted lines I've drawn in to the above. This should help keep the FPGA noise from propagating back to the analogue sections.

I do not think I should go further with the specifics until we have seen the way the power supplies, prime and redundant, are configured from the FCU into the DCU.

Spire will only change over from prime to redundant operation as whole and via a power down. For this scenario, relays are permissible with design analysis of their freedom from spike production. Relays may not be used to change ground lines between Spectrometer and Photometer data-taking as this changeover will be done with power on.

It's clear that the successful low noise operation of the DCU will depend on maximum attention being paid to its detailed implementation:

- keeping the low noise LIA inputs clean may need screens between the modules and even mesh cages connected to analogue ground over their ~x300 d.c. restoring pre-amplifier sections.
- Clearly keeping the PSD and offset selection switching noise out of the inputs is non-trivial, because in reality each LIA combines analogue with some slow speed digital function.
- The LIA grounding might best keep its analogue and digital functions on two separate ground-planes joined once on each module, to look like one ground from outside.
- Coupling these slow speed switching functions into the LIA from the prime and redundant FPGAs may best be accomplished using optocouplers, one per side per LIA to add robustness and permit the easy ORing of signals.
- keeping digital noise out of the bias generators is equally demanding and could take a similar approach because, although signal levels are all much higher, ground currents are equally destructive of performance if they reach the bolometers. One would suggest a detailed discussion between the electronic designers to choose a configuration that keeps the digital exchange of information from the FPGA to the bias generators to a minimum.
- the DCU Faraday cage must be well closed and any signals taken outside it and back in again via harness "internal" to the unit must be identified, fully screened, and generally analysed.

I hope that this document has worked grounding matters through. I'm certainly not averse to re-issung it with corrections or clarifications so PLEASE comment. It will come out again anyway when the DCU power supply configuration is clearer to me.

The meeting heard reference to preliminary testing of one of these systems. Please could I be pointed to those results on DMS/Livelink, or please could Viktor/Frederic circulate a copy.

Finally, Lionel, what is the electrical resistance coldtip to heatswitrch I/Fs at running temperature?

Cheers

John

5/4/01

Date: Fri, 6 Apr 2001 16:32:58 -0700 (PDT)
From: James Bock jjb@astro.caltech.edu
To: John Delderfield <j.delderfield@rl.ac.uk>
cc: "'Colin Cunningham'" <crc@roe.ac.uk>, "'Christophe CARA'" <ccara@cea.fr>, "'Viktor Hristov'" <vvh@phobos.caltech.edu>, Frederic Pinsard <pinsard@cea.fr>, D.K.Griffin@rl.ac.uk, bruce swinyard <B.M.Swinyard@rl.ac.uk>, ken king <K.J.King@rl.ac.uk>, lionel duband <Lionel.Duband@cea.fr>
Subject: Re: SPIRE GROUNDING DEFINITION
MIME-Version: 1.0

Dear John,

In reading through your document, I see many suggestions on the grounding. Needless to say, we are going to have to make choices on Frederic's design quite soon so CEA can start fabrication. So I assume Frederic will send us his new diagram soon and the system will comment on its compliance to the grounding philosophy. (philosophers usually don't stay grounded long)

I'VE PUT REQUIREMENTS IN RED. THESE ARE NOT JUST "SUGGESTIONS" BUT THEY ARE OPEN TO DISCUSSION.

I re-emphasize that the requirement to be able to isolate the FPU faraday cage was noted a long time ago. I do not know if it has fully propagated to Berend and Lionel, so I am stating it here for their benefit. In particular, electrical isolation of the thermal straps is required. For the IRTS cooler, we isolated the 2 K strap with a sheet of kapton. We will need this flexibility if Viktor is correct about the ground connection to chassis.

THIS IS WELL NOTED, AGREES WITH THE TEXT, AND IS WHY I SENT THE DOCUMENT TO BEREND AND LIONEL.

On the requirement of having an insulator on the shields of the BDA harnesses, I don't think an insulator is needed from JFETs to BDA as the shield will only short to the FPU. Correct?

YES BUT MAINLY NO. INSIDE FPU IS DEBATABLE BUT I DO NOT WANT TO START WITH MULTIPLE UNAVOIDABLE JOINTS BETWEEN FARADAY CAGE AND SIGNAL GROUND. OUTSIDE THE FPU DEFINITELY NO BECAUSE THE HARNESS IS HEATSUNK TO OPTICAL BENCH AS IT LEAVES THE JFETS AND UNINSULATED IT WOULD COMPLETELY SHORT OUT WHAT YOU ARE CORRECTLY SO KEEN TO PRESERVE IN THE "RE-EMPHASIS".

Finally, making a ground connection at 300 mK may present some problems. It may have to be a wire bond connection, and that makes me nervous. There is very, very little room in the BDA. I don't know if we can clamp the kapton cable and make a reliable contact. So we will make it possible to connect at 2 K.

THE GROUNDING DIAGRAM DETAIL PRESENTLY SHOWS JOINS AT BOTH PLACES, BUT SUBJECT TO MODELLING AS STATED. I ALSO WOULD BE NERVOUS ABOUT WIRE BONDS FROM KAPTON CABLE TO CHASSIS, BUT I CANNOT SEE WHY SOME EXPOSED METALISATION AROUND THE HOLES THROUGH WHICH DOWELS/SCREWS PASS TO HOLD DOWN THE END OF THE KAPTON HARNESS, WITH FLARED CROSS-SECTION ON TO TRACKS AND MAYBE WITH SLIGTHLY RAISED CLAMP SURFACE AROUND DOWELS/SCREWS SHOULD NOT PROVIDE A VERY SECURE GROUND. AFTER ALL IT HAS TO HOLD THE KAPTON WELL ENOUGH THAT A LARGE NUMBER OF VERY FINE WIRE BONDS TO THE DETECTORS/ RESISTORS REMAINS INTACT DURING VIBRATION AND TEMPERATURE CYCLING.

Jamie

Date: Sat, 7 Apr 2001 08:49:42 -0700 (PDT)
From: Viktor Hristov <vvh@astro.caltech.edu> X-Sender: vvh@boom.caltech.edu
To: James Bock <jjb@phobos.caltech.edu>
cc: John Delderfield <j.delderfield@rl.ac.uk>, "'Colin Cunningham'" <crc@roe.ac.uk>, "'Christophe CARA'" <ccara@cea.fr>, "'Viktor Hristov'" <vvh@phobos.caltech.edu>, Frederic Pinsard <pinsard@cea.fr>, D.K.Griffin@rl.ac.uk, bruce swinyard <B.M.Swinyard@rl.ac.uk>, ken king <K.J.King@rl.ac.uk>, lionel duband <Lionel.Duband@cea.fr>
Subject: Re: SPIRE GROUNDING DEFINITION
MIME-Version: 1.0

Jamie,

Instead of braking a probable loop through our GND mecca by insulating the RF-cage from the frame ground (what may have serious implication on the overal fridge performance if this requirement has not been taken in account during the design stage), some have to isulate ALL digital grounds that have to be connected at some point to our analog ground from the chassys, or to use optical or whatever decoupling to transfer the digital signals between the sensitive analogue moduleas and the FPGA/DAS one.

Viktor.

SAM IS CHECKING OUT ANY THERMAL IMPLICATIONS NOW. I SUSPECT THE NEED FOR CONTROL HEADROOM AT 300mK COULD BE MORE SIGNICANT THAN 1.6K AND 4K IMPEDANCES. ANYWAY, THANKS FOR THE VERY FINE SENTIMENT THAT THE ELECTRONICS MAY HAVE TO BE MORE AWKWARD TO PERMIT THE CRYOGENICS TO WORK WELL.
I DON'T THINK I WOULD EVER MAKE A PILGRIMAGE OR BOW DOWN TO A GND SYSTEM!!!!!!

Date: Tue, 10 Apr 2001 11:54:11 +0200
From: Christophe CARA <ccara@cea.fr>
X-Accept-Language: fr-FR,en
MIME-Version: 1.0
To: "Delderfield, J (John)" <J.Delderfield@rl.ac.uk>,
James Bock <jjb@astro.caltech.edu>, augueres@cea.fr, pinsard@cea.fr CC: "'Swinyard Bruce'" <b.m.swinyard@rl.ac.uk>
Subject: Comments on John grounding scheme note

Hi John,

You will find attached a note with comments and response to your note on grounding scheme.

I would like to add a general comment to this note:

Nominally designer are working on the basis of a list of specifications derived from upper level requirements.
The specifications are expressed in term of noise level, linearity, coupling on so on. Then the designers have the responsibility of building an equipment in compliance with those specification. They demonstrate this compliance by performing tests before integrating with the rest of the instrument.
In that case an unit may look like a black box (except for the designers with interfaces and performances well defined). Even if is difficult to work on this basis we have to take care of avoiding specifying an electronics in a down to top approach.

I FIND THE MENTIONING OF BLACK BOXES AND ISOLATION CONTRARY TO THE VERY FIRST POINT IN THE ATTACHED NOTE WHICH SAYS "Let's go now to the reality". I AGREE WITH AVOIDING A "down to top approach". I AM ADVOCATING THE OPPOSITE, WITH A CHECK BACK UP TO VERIFY COMPLIANCE.

I would also to stress out the necessity to quickly conclude on the grounding scheme! Since its definition have impact on PSU specification and according to ALCATEL the development of a qualification model will take 1.5 year (we must add to this delay 6 to 9 months for administrative activity) it is clear we don't have so much time to spend !

COULDN'T AGREE MORE, WHICH WAS WHY IT WAS PUBLISHED IN NOVEMBER.

See you

Christophe

ATTACHMENT
Page 1 :
OK, this is a basic configuration in the case each box has its own converter and signal are differential. Let's go now to the reality…
YES

Page 2 :
- Point 1 : here are some details on the mechanical design of the DCU box. All the individual board of the DCU are screwed for mechanical robustness on stiffeners. This is true for the LIA boards but also for the other DCU boards: DAQ_I/F and BIAS. Additionally those stiffeners will enable power dissipated by the electronics to be conductively efficiently coupled with the box and then to the S/C through the feet of the box.
The stiffeners will be also electrically connected to the DCU box due to the foreseen mounting concept: all the mechanical elements of box are grounded.
THERMAL AND MECHANICAL POINTS WELL TAKEN. OBVIOUSLY THE HEAT HAS TO GET TO THE OUTSIDE OF THE UNIT FROM THE INSIDE AND THEN AWAY FROM UNIT. YOU WILL KNOW BETTER THAN I WHETHER ESA HAS AGREED TO DO THE LATTER VIA CONDUCTION INTO THE SVM.
I SEE ONE POTENTIAL GROUNDING PROBLEM: I WOULD NOT WANT TOO MUCH CAPACITANCE FROM LIA ANALOGUE GROUNDS TO DISTRIBUTED UNIT CHASSIS. CAN YOU PROVIDE INFORMATION IN THIS REGARD FOR VIKTOR TO COMMENT ON, AND TO GO INTO DOUG'S MODEL.
WHILE WE CONSIDERING PHYSICAL DETAILS, HOW DO THE DCU MODULES KEEP R.F. OUT OF THE VARIOUS JOINTS?
- Point 2 : this requirement is taken into account for the PSU specification since it is already stated in the IID-A.
SEE LAST SENTENCE, FIRST PARA., PAGE 1!
- Point 3 : based on our previous designs we foresee to implement a grounding strap between the secondary power return and the box internally. This strap is obviously only connected after secondary isolation testing.
THIS APPROACH IS FINE AND LESS PRONE TO EMC THAN A SIMPLE EXTERNAL STRAP…ONLY FIT STRAP OF COURSE IF SECONDARY NEEDS GROUNDING IN THE UNIT.
- Point 4 : the present design does not include filter connectors. It is difficult to demonstrate the need for such connectors and procurement of space grade parts is not obvious.
AS MENTIONED IN NOTE'S NEXT PARAGRAPH
An alternative option consists of using I/O decoupling capacitors or serial inductors as close as possible from the connectors. To be efficient decoupling capacitors must be connected shortly to a low impedance “ground”: the best candidate being normally the box itself, which constitutes a Faraday cage. However in our case since the LIA ground shall be isolated from the DCU ground to avoid loop, the chassis surrounding the board can’t be used as a common mode current return path.
AGREED
- Point 8 (second half of the page): the DCU power supply is located inside the FCU. The DCU is fed with rectified, filtered and regulated secondary power lines through an external harness.
UNDERSTOOD, BUT THE REGULATION AND FILTERING HAS TO BE REFERENCED AS STATED TO THE ANALOGUE GROUND IN THE DCU, NOT EVEN JUST THE DCU CHASSIS.
- Point 9 : it is difficult to implement thin inter-board shields because of the possible vibration problems. In order to achieve electrostatic shielding between the DAQ_I/F board ground planes will be intensively used and noisy tracks will be located in internal layers of the PCB.
I SEE EVERY ADVANTAGE IN BURYING NOISY DAQ_I/F BOARD TRACKS BETWEEN GROUND PLANES. THIS IS AKIN TO THE IDEAS IN PAGE TWO'S PENULTIMATE PARAGRAPH. IT WOULD TEND TO INCREASE CAPACITANCE TO GROUND, BUT FOR THE DAQ_I/F BOARD I THINK WE AGREE THIS IS LINKED TO DCU CHASSIS AND SO PROBLEMS ARE SMALL.

THE SAME APPROACH COULD BE USED ON THE LIA BOARDS WITH THE PLANES BEING CHASSIS ISOLATED ANALOGUE GROUND, BUT I WOULD MUCH PREFER INTERBOARD SHIELDS IN THIS CASE……THIN 0.5MM METAL CAN BE VERY RIGID IF IT'S PRESSED INTO A 3D FORM AND THEN MULTIPLY AFFIXED TO YOUR BOARD STIFFENERS.

We also have the possibility to interleave the different boards as shown below:
position 1 : DAQ_I/F Main
position 2 : BIAS Redundant
position 3 : LIA
…
position 15 : BIAS Main
position 16 : DAQ_I/F Redundant
Assuming that main and redundant electronics are never working together this configuration increases isolation between digital and analog functions.
THIS IS INTERESTING. I'VE RAISED QUESTION OF MODULE ORDER BEFORE AND NOT RECEIVED ANY FEEDBACK. PLEASE EXPAND AND SEE MY PREVIOUS QUESTIONS.
Page 3 :
Top of page: the interface between DCU and DPU are definitively based on RS422 electrical standard. The bandwidth of this standard is limited to 10 MHz while the

DCU maximum bit rate is around 2 or 3 Mbps. According to de-rating rules the ratio between the maximum RS422 frequency and the SPIRE bit rate is relatively well optimised: in that case we can assume the bandwidth of the link is not over specified.
AGREED, THANKS FOR THE DETAILS, BUT I DON'T THINK THAT I'VE SUGGESTED THAT THE I/F IS OVER-SPECIFIED AND 3Mps IS VERY FAST COMPARED TO 5Hz. BOLOMETERS.

SO WHILST I FOUND THE GENERAL COMMENTS IN THE BODY OF YOUR E-MAIL A LITTLE DIFFICULT TO APPRECIATE, THE ATTACHMENT MAKES REALLY GOOD SENSE. THE CRUX AS TO WHETHER WE CAN KEEP THE NOISE OUT OF THE SENSITIVE ANALOGUE PARTS OF THE SYSTEM APPEARS TO ME TO CENTRE ON POWER SUPPLY DETAILS AND OPTIMISING ALL I/Fs TO THESE ANALOGUE SYSTEMS. PLEASE COULD YOU EXPAND ON DESIGN DETAILS IN THESE AREAS.

P.S. QUESTION OF REDUNDANT BIAS/JFET SUPPLY IS STILL OPEN AND DEPENDANT ON MY UNDERSTANDING WHERE ALL THE JFET BOX WIRES ARE IN TYPE II HARNESS PLUS JPL (VIKTOR) BEING HAPPY THAT HANGING ALL THE UNPOWERED STUFF PERMANENTLY ON THE POWERED SYSTEM WILL NOT DEGRADE SPIRE'S SIGNAL TO NOISE….I'M WORRIED ABOUT THIS LAST FACTOR AND NONE OF THE ABOVE INPUTS I'VE RECEIVED ADDRESS IT.