Subject:	**SPIRE GROUNDING and SCREENING PHILOSOPHY**

PREPARED BY: J. DELDERFIELD ……..

2003.08.15 13:17:49 +01'00'

APPROVED BY: K. KING…….. **Date:** …….

APPROVED BY: M. GRIFFIN…….. **Date:** …….

CHANGE RECORD

ISSUE	DATE	CHANGE(S) MADE
0.1	1/4/2001	First Controlled Issue, cold-end grounded
0.2	10/4/2001	Q&A attached at end and tidied for IIDR.
0.3	24/8/2001	Updated following meetings, including initial cold-end strap/cooler isolation
0.4	10/9/2001	Added overall Spire grounding diagram
0.5	24/8/2001	Removed transformer drive for bias, not implemented, and move ground loop control resistors to warm end from cold. 1+2+3 options on bolometer ground.
0.7	7/6/02	Updated to include situation during Tiger Team activities.
0.8	13/8/02	Addition of proposal of way forward from JD [originally issued separately under the title "Spire_Grounding.pdf" on 16/7/02]
1.0	1/10/02	Conclusions of Spire Grounding Review included and reformatted.
1.1	15/8/03	Include updated detailed grounding drawings. Inside CVV the ESA-provided cryoharness implements the FPU Faraday cage links as wires for the FCU harnesses + wire level screens for the bolometer harnesses. Also cooler tip to photometer detector isolation removed…ECRs 39 and 62.

ACRONYM LIST

Term	Meaning
ADC	Analogue to Digital Converter
AIV	Assembly, Integration and Verification
AME	Absolute Measurement Error
AOCS	Attitude and Orbit Control System
APART	Arizona's Program for the Analysis of Radiation Transfer
APE	Absolute Pointing Error
ASAP	Advanced Systems Analysis Program
AVM	Avionics Model
BDA	Bolometer Detector Array
BFL	Back Focal Length
BRO	Breault Research Organization
BSM	Beam Steering Mirror
CDMS	Command and Data Management System
CDMU	Command and Data Management Unit
CDR	Critical Design Review
CMOS	Complimentary Metal Oxide Silicon
CPU	Central Processing Unit
CVV	Cryostat Vacuum Vessel
DAC	Digital to Analogue Converter
DAQ	Data Acquisition
DCU	Detector Control Unit = HSDCU
DPU	Digital Processing Unit = HSDPU
DSP	Digital Signal Processor
DQE	Detective Quantum Efficiency
EDAC	Error Detection and Correction
EGSE	Electrical Ground Support Equipment
EMC	Electro-magnetic Compatibility
EMI	Electro-magnetic Interference
ESA	European Space Agency
FCU	FCU Control Unit = HSFCU
FIR	Far Infrared
FIRST	Far Infra-Red and Submillimetre Telescope
FOV	Field of View
F-P	Fabry-Perot
FPGA	Field Programmable Gate Array
FPU	Focal Plane Unit
FTS	Fourier Transform Spectrometer
FWHM	Full Width Half maximum
GSFC	Goddard Space Flight Center
HK	House Keeping
HOB	Herschel Optical Bench
HPDU	Herschel Power Distribution Unit
HSDCU	Herschel-SPIRE Detector Control Unit
HSDPU	Herschel-SPIRE Digital Processing Unit
HSFCU	Herschel-SPIRE FPU Control Unit
HSO	Herschel Space Observatory
IF	Interface
IID-A	Instrument Interface Document - Part A

Term	Meaning
IID-B	Instrument Interface Document - Part B
IMF	Initial Mass Function
IR	Infrared
IRD	Instrument Requirements Document
IRTS	Infrared Telescope in Space
ISM	Interstellar Medium
JFET	Junction Field Effect Transistor
ISO	Infrared Space Observatory
LCL	Latching Current Limiter
LIA	Lock-In Amplifier
LVDT	Linear Variable Differential Transformer
MAC	Multi Axis Controller
LWS	Long Wave Spectrometer (an instrument used on ISO)
MCU	Mechanism Control Unit = HSMCU
M-P	Martin-Puplett
NEP	Noise Equivalent Power
NTD	Neutron Transmutation Doped
OBS	On-Board Software
OMD	Observing Modes Document
OPD	Optical Path Difference
PACS	Photodetector Array Camera and Spectrometer
PCAL	Photometer Calibration source
PID	Proportional, Integral and Differential (used in the context of feedback control loop architecture)
PLW	Photometer, Long Wavelength
PMW	Photometer, Medium Wavelength
POF	Photometer Observatory Function
PROM	Programmable Read Only Memory
PSW	Photometer, Short Wavelength
PUS	Packet Utilisation Standard
RMS	Root Mean Squared
SCAL	Spectrometer Calibration Source
SCUBA	Submillimetre Common User Bolometer Array
SED	Spectral Energy Distribution
SMEC	Spectrometer Mechanics
SMPS	Switch Mode Power Supply
SOF	Spectrometer Observatory Function
SPIRE	Spectral and Photometric Imaging Receiver
SRAM	Static Random Access Memory
SSSD	SubSystem Specification Document
STP	Standard Temperature and Pressure
SVM	Service Module
TBC	To Be Confirmed
TBD	To Be Determined
TC	Telecommand
URD	User Requirements Document
UV	Ultra Violet
WE	Warm Electronics
ZPD	Zero Path Difference

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	Lund	x	-						
	Hibberd								
	Trougnou	x	x						
Alenia	Cesa	x	x						
Astrium	Faas	x	x						
PA	Clark								

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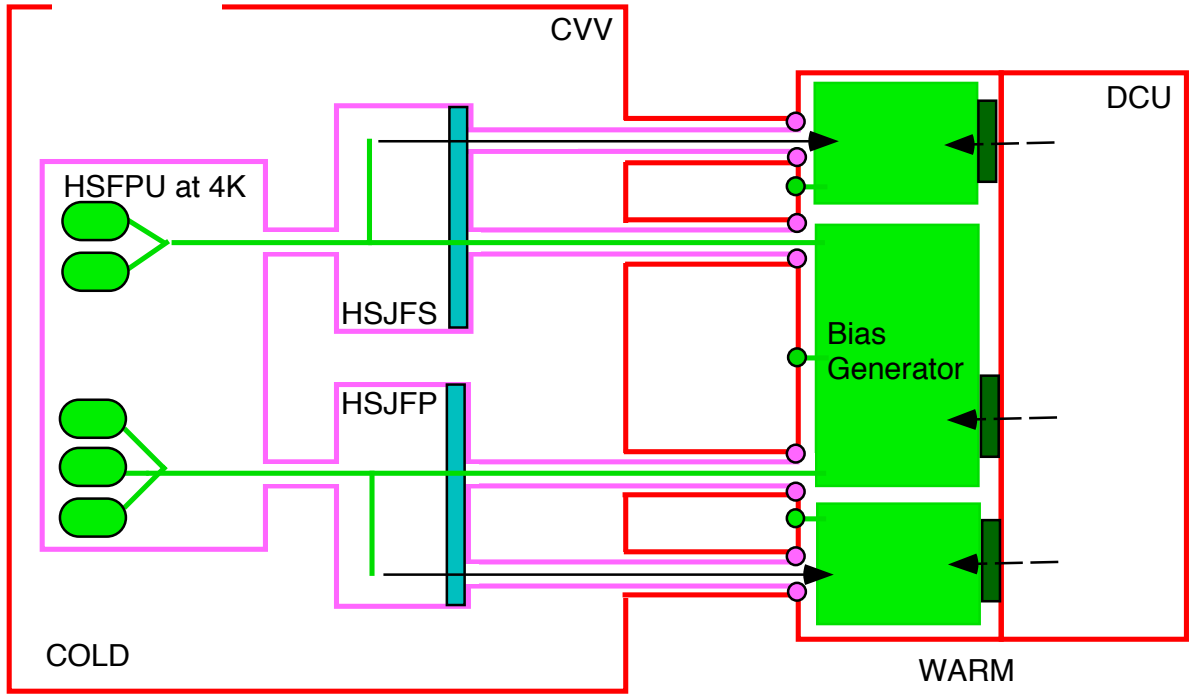
Reference Documents

Minutes EMC WG meeting #14.	H-P-ASPI-MN-1360
GROUNDING SCHEME-JPL	SPIRE-RAL-MHO-001375
GROUNDING OVERVIEW_JD	SPIRE-RAL-MHO-001367
SPIRE Grounding Review Minutes	SPIRE-UCF-MOM-001405

1 Document Scope

Sections 3 and 4 of this document define the grounding scheme that is required to be implemented in the Herschel Spire instrument, and section 5 provide some rationale for this together with some more detailed implementation requirements.

2 Simplified Grounding



300mK BDAs in two 2K boxes tied into analogue ground but otherwise isolated

Analogue Ground-plane, DCU Bias Gnd., extended to cold-end by harness inner shields, etc..

Differential analogue signal feeds, using analogue ground as screen but with this screen not low impedance connected at the warm end..

External S/C level Faraday cage provided by main chssis, CVV, etc.

Spire specific low noise Faraday cage, HSFPU/HSJFS/HSJFP chassis all linked with harness overshield to backshell, joined back to DCU, Ohmically isolated at the cold end, and with a inner volume filtered at the JFET units' I/F

Filter MDM connectors, T-section with C to case.

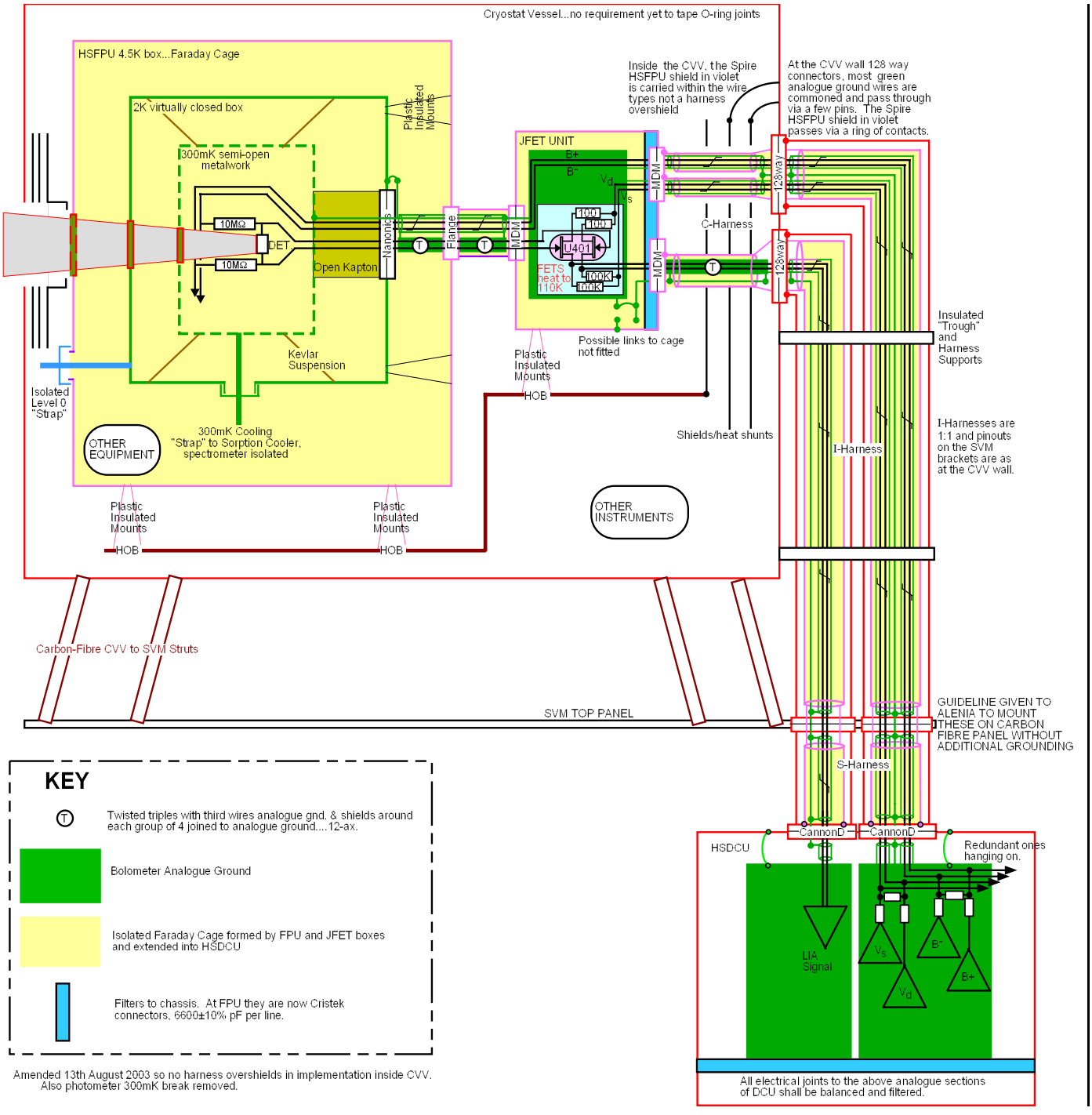
Secondary power feed with extra filters so very quiet w.r.t. bias analogue ground.

The above derives from the minutes of the Spire Grounding Review which record agreement as follows:

1. The 4-K box will be a Faraday shield closed by RF filters.
2. The 4-K box will be connected to the DCU chassis via the harness over-shield (inside the cryostat) as defined in the Harness Definition Document.
3. This overshield will have to go via multiple contacts not backshell at the CVV connectors, which is acceptable.
4. The 2-K detector boxes shall be isolated from 4-K box
5. The 2-K boxes shall be connected to 0 V in the DCU via analogue connections in the bias line
6. The 300-mK stages shall be connected to the 2-K stages inside their BDAs
7. The 300-mK thermal straps shall have an electrical break to keep the photometer and spectrometer grounds isolated..this shall be on spectrometer side..
8. The spectrometer and photometer 2-K boxes shall be isolated from each other.
9. The inner shields around signal lines shall be connected to 0 V at the JFETs but not at the DCU side (TBC).
10. The inner shields (only on the bias lines) are connected to 0 V at the DCU and to 2-K box (TBC)

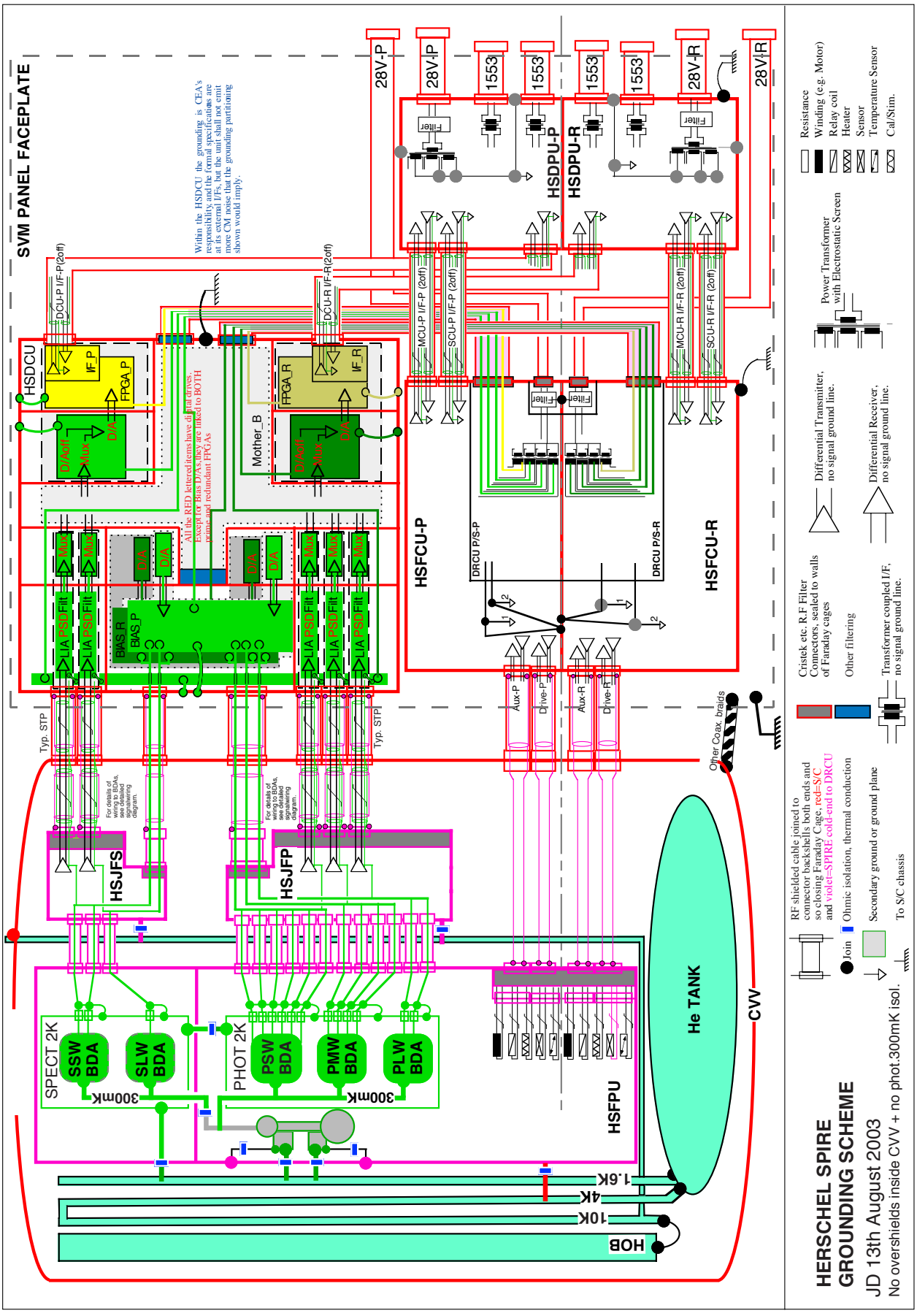
3 Single Detector Configuration

If the above simplified scheme is extended for one detector to include all the signal wires and cable types the following results:



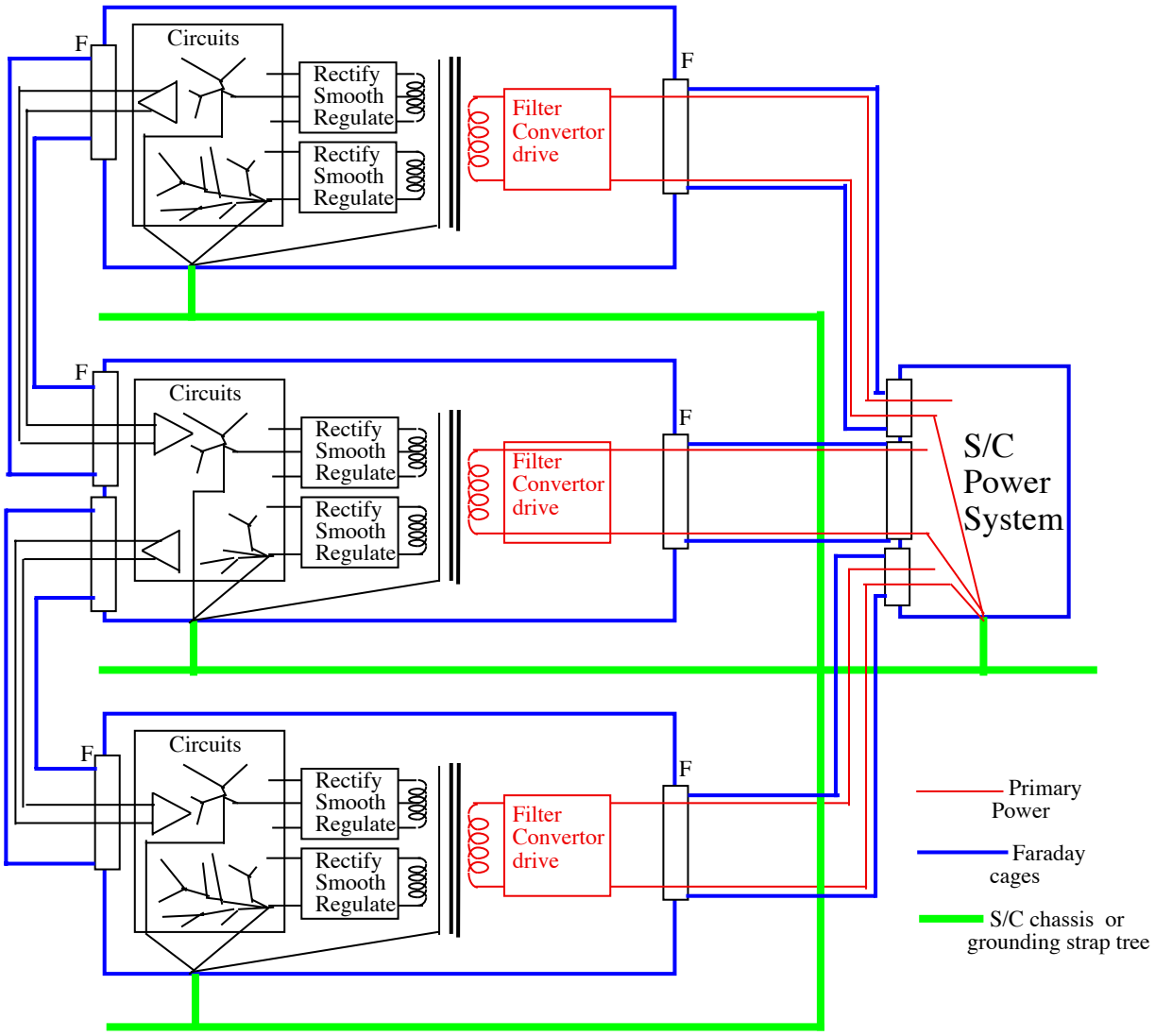
Amended 13th August 2003 so no harness overshields in implementation inside CVV. Also photometer 300mK break removed.

4 Overall Spire Grounding Diagram.



5 General Guidelines and Philosophy.

In general terms SPIRE shall conform to an ESA classical unit by unit secondary power configuration as shown in the following figure:



Each unit is electrically self-contained in its grounding.

1. It has a chassis/box that is closed to form a conductive Faraday cage, i.e. enough thickness in skin depths/bulk conductivity (essentially inevitable) and with all apertures including vents and joints having controlled geometry with adequately small maximum dimensions.
2. Except the S/C power system, primary power is isolated from chassis, although for each unit a small input capacitance is permissible and possibly a high valued resistor to chassis for electrostatic protection.
3. Each unit is powered with secondary (or conditioned) power which is isolated from the primary power buses and unipoint grounded via a link to unit chassis, a joint which is best made near the same point on the chassis as is externally connected to S/C. Signal grounds are typically the same as or decoupled to such secondary grounds and the same rule applies. This internal link may need to be via an externally accessible strap to permit secondary ground isolation testing.
4. All signal inputs and outputs are differential and ideally pass through filter connectors to protect the unit from external noise entering the unit via harnesses. Signal ground lines do not pass between units. Inputs are normally high impedance and are required to maintain a defined high impedance w.r.t. chassis. Outputs are required to have controlled slew rates, minimum skew to limit common mode spikes, and little ringing.

5. The secondary grounds with each unit are carefully configured in a documented way and if multiple supplies are used the grounds for each supply are separately controlled with a minimum of joins between the supplies, classically just one at the unit unipoint.
6. Theoretically there should be no current flow in any ground wire, which should only be used for signal voltage reference, but in unipolar supply situations, when 0V and signal ground are one and the same, current flow is unavoidable. This is just one example of the general requirement that any device taking a.c. current shall have adequate local decoupling/filtering, obviously to ensure its own correct operation, but also adequately to inhibit noise propagation to other elements in the unit; logic or digital functions can be the most troublesome with their a.c. components taking the form of switching noise.
7. Depending on the susceptibility of circuits, logic signals that travel a distance across a unit may need to be slowed down with series resistors and squared up again on receipt by Schottky buffers such that excessive dV/dT noise is not broadcast.

There are several relaxations in the ideal that are commonly acceptable. Filter connectors introduce their own problems and the careful specification of input susceptibility and output emission levels often allows requirements to be met with un-filtered connectors. In such a cases, common mode filtering with defined differential mode bandpass is often introduced on signal inputs to compensate. Formal unipoint strapping to a S/C grounding tree is often discarded and a unit is simply conductively mounted by all of its mounting feet…..this is no problem as long as no other equipment is returning current along the S/C chassis and potentially thus inducing a.c. signals in the unit's Faraday cage.

On the other hand, there are many options for improving the operation of such standard configuration, to further limit the propagation of noise between the functional elements inside it.

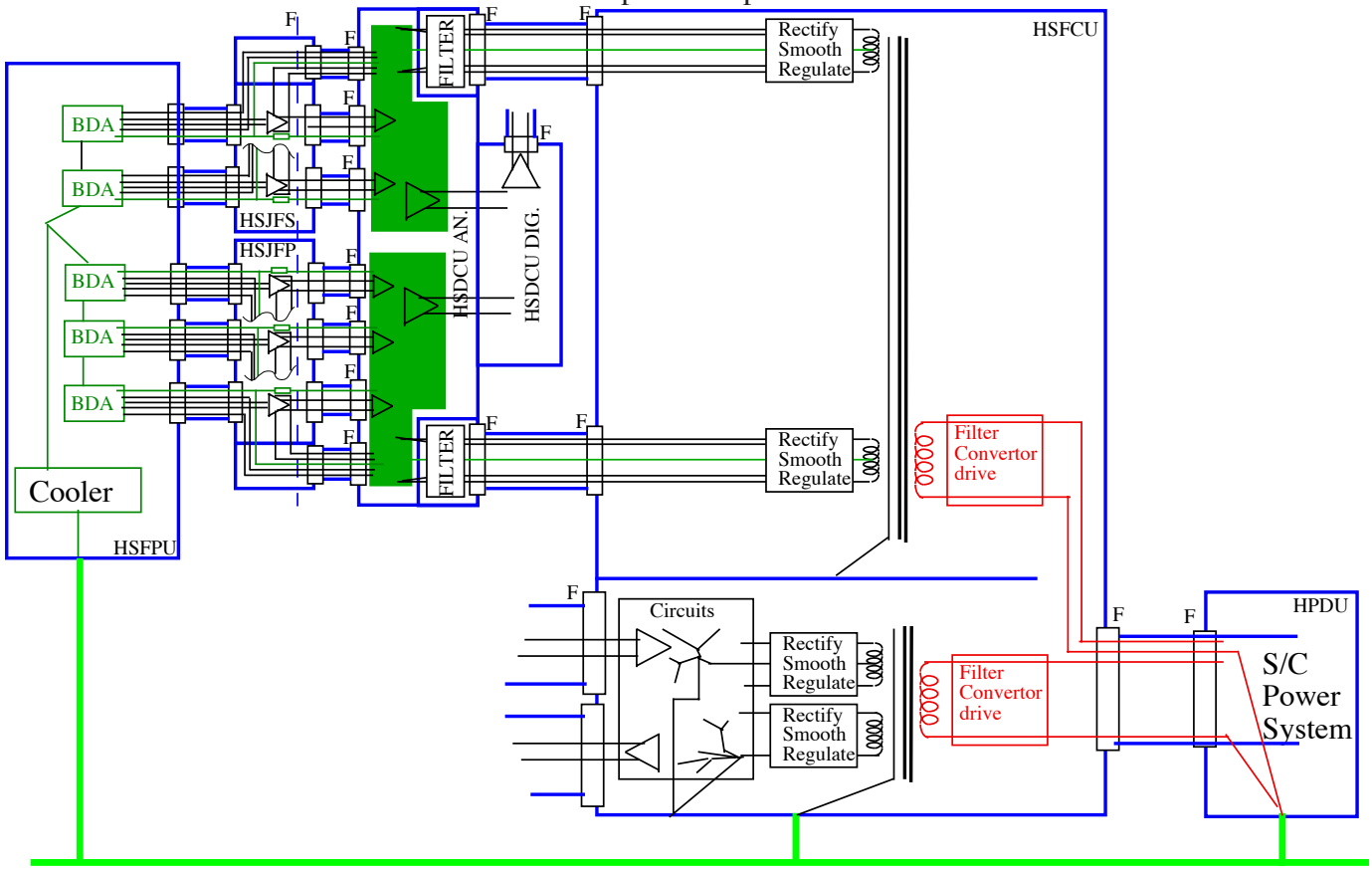
8. internal division into a card rack and a power supply compartment with bulkhead filters between the two.
9. improving the Faraday shield with thin metallic inter-board shields or even formal internal divisions with bulkhead filters. Such shields are often used if frequencies are being multiplied and shifted or if one board contains logic and other only analogue {All are electrostatic screening connected solidly to unit chassis; I'll omit the less common magnetic screening from this note}
10. Accepting a certain level of ground current but defeating the induced ground voltage noise by using highly conducting low inductance ground planes. Unless a special analysis is performed these should only be used in conjunction with other good practice (local decoupling, separation of grounds, chassis isolation with unipoint contact, etc.). More complex scenarios exist: ground signal planes may be combined with power supply planes, the ensemble being multiply capacitively linked; physically thicker power planes may be sandwiched into PCBs, electrically isolated from the circuits on them but firmly joined to unit chassis so as to extract power but also to double as extended Faraday screens.
11. Mismatching impedances/4-wiring. Mismatch is inherent in many architectures that use low impedance drive and high impedance inputs, but I'm referring here to using high impedance current drive into relatively low impedance input. Used with or without formal differential signals, this is another way of removing a dependance on a quiet voltage reference ground.
12. Differential digital interfaces do not provide ideal isolation. In particular, the driver has to provide significant edge switching currents to drive harness capacitance, a situation that gets worse if the I/F is between units, the receiving unit inputs have capacitive filter elements, harness lengths are long and have screens, etc.. Depending on frequency, power, radiation environment and money, such interactions between supposedly separate grounds may be improved by using transformer coupled buses or opto-couplers.

The whole approach so far described is prefixed by "in general terms". The configuration is best suited to systems in which each unit operates over a restricted range of signal level. In Spire this would apply to the HSDPU. Otherwise transmission of noise from high level circuits such as power convertors to sensitive analogue elements get more and more impossible to achieve. Considering the front-end signal source in Spire, we have an noise spec. of 7nV/√Hz at about 2.5MΩ and 300mK. There comes a point when the need to control noise requires separate preamplifier unit(s), preferably with an electrostatically screen separating it (them) from any digital functions such as multiplexors or A-D convertors, with the signals then transferring to a conventional unit via balanced digital I/Fs. The power needs to be fed to this system's analogue sections extremely quietly, prefiltered and actively regulated with external sensing in an

external unit. It must then be filtered in a separate compartment within the analogue unit that has bulkhead connectors feeding to the analogue system. Grounding has to be very carefully configured as secondary grounds are implicitly distributed outside of one unit. If one considers the whole volume of the various units in this supply system as if it were joined into one by the harness screens that join them, the grounding it should look like a unipoint tree as if it were still within one unit.

Multichannel operation requires adequate interchannel screening and a configuration that keeps any designed-in signal cross-talk to below specified levels.

We conceived of the following concept early in the autumn of 2000, following the design decision to separate the spectrometer and photometer JFET units so they could be accommodated adequately near to their respective detectors, the specification then being <50pF along the cable as seen by each 5MΩ detector. It was also really stressed by those with experience that Spire's bolometric detectors are unbelievably sensitive and would make corrupted measurements if unwanted r.f. were to be dissipated in them, the biggest risk being that wires have to be attached to them!! So the following was adopted at a video conference from RAL to JPL with Christophe Cara present at the RAL end.



Note that the above has since been revised but it serves well show principles. Redundancy is omitted to minimise confusion. The principles are:

1. signal power gain from external JFET amplifiers
2. separate analogue ground paths, without loops, between spectrometer and photometer systems
3. maintenance of single point ground joins to S/C chassis
4. analogue power, quiet and regulated, supplied from a unit external to the one that houses the sensitive analogue systems, without ground switching.
5. ground-plane option invoked to keep a large area of analogue signal ground quiet in each of the spectrometer and photometer parts
6. the detectors to be in a Faraday cage with full filtering on all wires entering it (non-bolometer ones not shown) extended with full shielding into the JFET boxes.
7. the JFET boxes are cryogenic filtered to close the Faraday cage.
8. unipoint analogue ground for the system at the 300mK BDA units that are unavoidable coupled with cold-plumbing busbar ink. This minimises Voltages between the bolometers and their local chassis. THIS POINT HAS BEEN CHANGED SINCE AUTUMN 2000 AGREEMENT..

9. information transfer out of the digital part of the HSDCU via normal balanced ESA-type digital interfaces, both fast and slow, to the HSDPU (not shown but having its own separate conventional grounding scheme).
10. The need to bundle together groups of long harnesses between HSJFETs and HSDCU (not shown here but see instrument block diagram) to minimise loop area between bias routed analogue ground lines and differential signal lines. Admittedly they are inside shielded harnesses but one cannot have much common mode signal at the DCU's inputs even with good CMRR before a 7nV/√Hz differential noise performance is degraded.
11. An optimised multiplexing/transfer of data from the analogue sections of the DCU to the back-end digital ones to minimise current injection back into the analogue ground and hence potentially back to the detectors.

Let's consider more points about Spire, first as seen from HERSCHEL. Spire is defined at IIDB level as having a prime DPU and DRCU, plus a redundant pair, non-cross-strapped. Now the DRCU is no longer a physical unit but has been split into two, the DCU and the FCU, both parts must still appear to the DPU and hence HERSCHEL to be a simple prime/redundant unit. The bolometers analogue sections of the DCU are non-redundant and need to be runable from both prime and redundant "back-ends". Spire will only change over from prime to redundant operation as whole and via a power down. So relays are permissible, with design analysis of their freedom from spike production, but they may not however be used to change ground lines when switching between Spectrometer and Photometer modes..

The Spire estimated MTBF must be met, which places a very high requirement for reliability on those elements which are not redundant. Formally there is no requirement that the bolometer bias and JFET supply generators be prime and redundant, merely that the functions be at least double wired across the cryoharness because of the noted less-than-ideal reliability of cryoharness. Based on FMECA, the DCU has prime and redundant bolometer bias and JFET supply generators to achieve the required MTBF. They must be joined into the grounding system so as not degrade the bolometer S/N, and EACH must still see double wiring across the cryoharness. The cryoharness has now been defined to limit the loss to Spire if the "unthinkable" double **and** coincident wire breakage should occur in the a.c. bias and JFET supply wires that affect multiple pixels

The DCU digital sections, driving and receiving signals across via external I/F to other HERSCHEL SVM mounted units, have conventional ESA grounding configurations of the type with which this note starts, except that their power is supplied (not shown) just from the appropriate Prime or Redundant FCU. Data transfers of digitised bolometer signals leave the DCU in packet burst mode at quite high Baud which precludes the use of interfaces that might provide higher ground decoupling. Therefore these digital section of the DCU must be regarded as noisy in bolometer terms and be configured as shown in the diagram, i.e. within an isolated sub-compartment. The configuration of a DCU digital section power supply from the FCU and the section's input coupling from the preceding DCU section, shown conceptually in the grounding diagram as being an analogue section joined via an AtoD convertor, shall be such as to minimise charge injection/current into the latter's ground. This is because any such injection is potentially into the sensitive bolometers via the system analogue ground, and JPL expressed concern in this regard.

For RF screening and noise rejection, the tightly bundled cables from the JFET filters to the outside of the FPU have to have a high coverage screen around each of them to keep the Faraday cage closed. Thermal analysis shows that these will be adequately heatsunk via the JFET module connectors, through their frame to the HOB, but the heatsinking situation may alter if level 3 is implemented

All non-bolometer wiring entering the FPU does so via JPL provided filter modules mounted such as to keep the Faraday cage closed. This clearly applies to the cooler's wiring and it is isolated from chassis. Nevertheless, because JPL correctly identified the cooler as being very much coupled into the bolometer system, all signals sent to the cooler must be especially quiet. Any proportional heating used on the 300mk needs to be heavily filtered in the SCU before being output so as to appear as "d.c." even discounting any filtering in the FPU boxes [which are intended for r.f. not power filtering!]. If temperature sensors are only conditioned in a duty cycle as they need to be read out, the start and finish of even this low level conditioning shall be ramped not stepped.

Now consider some more of the FPU "mechanical" grounding details. In keeping with the isolated the

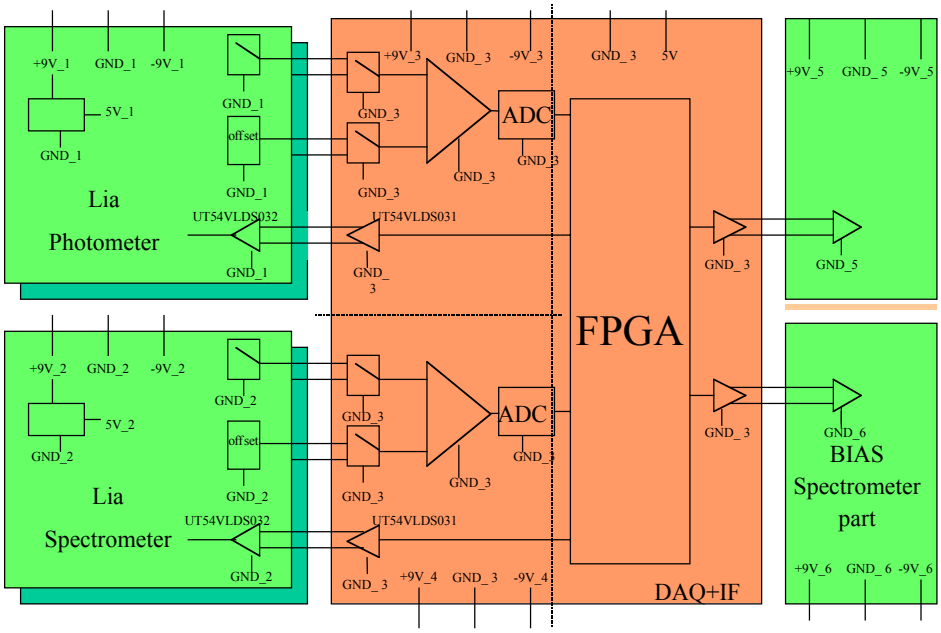
Faraday cage ideas spelt out above, all three main FPU mounting feet need mechanically to include electrical breaks. Thermally this should be no problem as the feet are seeking to achieve isolation anyway. Mechanically the feet still have to keep instrument alignment with the HERSCHEL telescope.

In 2000, I originally thought the BDAs might form a Faraday cage themselves with an electrical break in the 300mK plumbing, but the BDA 300mK sections are suspended from 1.8K mounting rims linked by open Kapton ribbon harnesses which precludes this approach by definition…without thermally shorting out the Kevlar suspension. I had not at that stage caught up with the agreement that the FPU was the Faraday cage, and this approach was quickly reverted to. Note that the FET box filters enclose a quiet volume for the detectors but introduce ~100 x 9 x 2200pF = 2μF of capacitance between the analogue system and the FPU/JFET Faraday cage, effectively a short to R.F.

After the September 2002 grounding review, we have introduced the electrical isolations shown in section 4, lifting off and separating the 1.8K detector boxes to keep them linked to analogue ground as the overall analogue to chassis link is moved to the warm elkectronics.

Thermal/anti-microphony/RF loop reducing holdowns on the cryoharness shall not electrically short these harness shields to chassis.. This would follow automatically if the harness has an outer insulator covering, but otherwise local taping is necessary.

Consider the DCU analogue sections. I originally suggested the a.c. biases to each BDA be supplied via individual transformers to easily reference them quietly to the OV of the relevant JFET supply, clean off high frequencies, scale down a higher level synthesis to the required bias levels, provide some drive output short protection, etc. I still like this idea but it is not a requirement, merely a suggestion. Taking a Frederic drawing and increasing the text size + changed colours, we have



We can note the split between the spectrometer and photometer analogue grounds, G1+G5, versus G2+ G6, and isolation of the Lock-In-Amplifier grounds from the Bias/FET power supply grounds. I would encourage the ±9V powered high level analogue sections to be split into separate grounded sections as mentioned at the meeting and as shown by the dotted lines I've drawn in to the above. This should help keep the FPGA noise from propagating back to the analogue sections. The grounding diagram in section 3 is derived from a later DRCU Design Description, laid out a little differently.

It's clear that the successful low noise operation of the DCU will depend on maximum attention being paid to its detailed implementation:

1. keeping the low noise LIA inputs clean may need screens between the modules and even mesh cages connected to analogue ground over their ~x300 d.c. restoring pre-amplifier sections.
2. Clearly keeping the PSD and offset selection switching noise out of the inputs is non-trivial, because in reality each LIA combines analogue with some slow speed digital function.

3. The LIA grounding might best keep its analogue and digital functions on two separate ground-planes joined once on each module, to look like one ground from outside.
4. Coupling these slow speed switching functions into the LIA from the prime and redundant FPGAs may best be accomplished using opto-couplers, one per side per LIA to add robustness and permit the easy O-Ring of signals.
5. keeping digital noise out of the bias generators is equally demanding and could take a similar approach because, although signal levels are all much higher, ground currents are equally destructive of performance if they reach the bolometers. One would suggest a detailed discussion between the electronic designers to choose a configuration that keeps the digital exchange of information from the FPGA to the bias generators to a minimum.
6. the DCU Faraday cage must be well closed and any signals taken outside it and back in again via harness "internal" to the unit must be identified, fully screened, and generally analysed.

If you have managed to read this far, further information can be found in the listed reference documents!