SPIRE

DPU Interface Control Document

Prepared by: Riccardo Cerulli-Irelli (Custodian)
Renato Orfei
Anna Di Giorgio

Distribution List :

K. King		
B. Swinyard		
J. Delderfield		
J.L. Auguères		
C. Cara		
D. Pouliquen		
D. Ferrand		
G. Olofsson		
R. Orfei		
A. Di Giorgio		
A. Longoni		

Document Status Sheet:

Document Title: FIRST- SPIRE DPU Interface Control Document			
Issue	**Revision**	**Date**	**Reason for Change**
Draft 1		22/11/2000	First draft
Draft 2		5/12/2000	Low speed I/F timing

Document Change Record:

Document Title: FIRST- SPIRE DPU Interface Control Document	
DOCUMENT REFERENCE NUMBER:	
Document Issue/Revision Number: Draft 2	
Section	**Reason For Change**
3.3	S/C connectors and pin functions
4.2	Low speed I/F protocol and timing

Applicable documents

Document Reference	Name	Reference
AD1	FIRST/Planck Instrument Interface Document Part A	PT-IID-A-04624
AD2	FIRST/Planck Instrument Interface Document Part B Instrument “SPIRE”	PT-HIFI-02125
AD3	SPIRE Instrument Requirements Document	SPIRE-RAL-PRJ-000034 Issue .30
AD4	SPIRE Operating Modes	

Reference documents

Document Reference	Title	Reference
RD1	SPIRE DPU Subsystem Specification Document	SPIRE-IFS-PRJ-000462 Issue 1.0

Acronyms

CDMS	Central Data Management System
CNR	Consiglio Nazionale delle Ricerche
CPU	Control Processing Unit
DPU	Digital Processing Unit
DRU	Detector Readout Unit
DSP	Digital Signal Processor
EGSE	Electronic Ground Support Equipment
ESA	European Space Agency
FIRST	Far InfraRed and Submillimeter Telescope
HK	HouseKeeping
HW	HardWare
ICD	Interface Control Document
ICU	Instrument Control Unit
I/F	Interface
IFSI	Istituto di Fisica dello Spazio Interplanetario
NA	Not Applicable
OBS	On-Board Software
PDU	Power Distribution Unit
S/C	Spacecraft
S/S	Subsystem
SPIRE	Spectral and Photometric Imaging REceiver
SPU	Signal Processing Unit
SR	Software Requirement
SSD	Software Specification Document
SVVP	Software Verification and Validation Plan
SW	SoftWare
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TC	Telecommand
TM	Telemetry

Table of contents

1 Scope of the document

This document describes the interfaces of the SPIRE Digital Processing Unit with the FIRST spacecraft (S/C), the Instrument Control Unit (ICU) and the Detector Readout Unit (DRU)
The following block diagram shows the simplified overall layout of SPIRE and the interfaces described in this document.

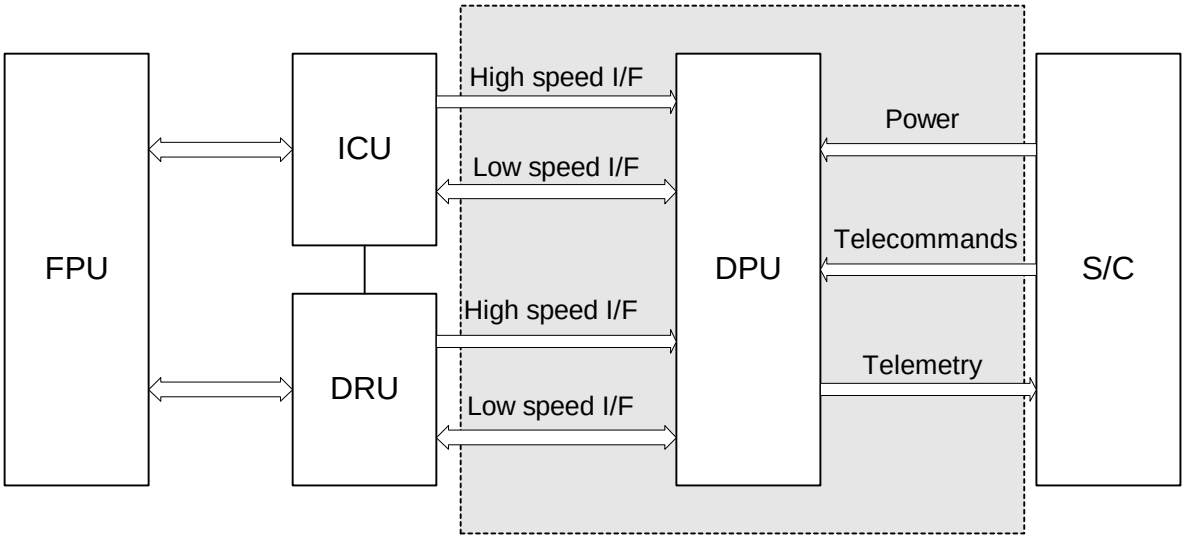

Figure 1-1 SPIRE DPU interfaces schematic view

2 Description of DPU subsystem

The DPU is based on a 20 MHz clock TEMIC TSC21020 Digital Signal Processing (DSP) developed by Analogue Devices and implemented for flight use by TEMIC.
The DSP implements Harvard architecture, i.e. the data bus (32 bit) and the programme bus (48 bit) are completely separated, so increasing the execution speed.
The program area is implemented with PROMs, EEPROMs and RAM. The PROMs store the initial boot loader and emergency recovery modules. The instrument program is stored in EEPROMs and copied in RAM at run time for execution. Program area may be used as data memory.
The DPU/ICU includes a synchronized DC/DC converter to supply internal circuitry.

2.1 Overall DPU block diagram

The following diagram shows the main DPU blocks, the electrical interfaces and the memory dimensions.

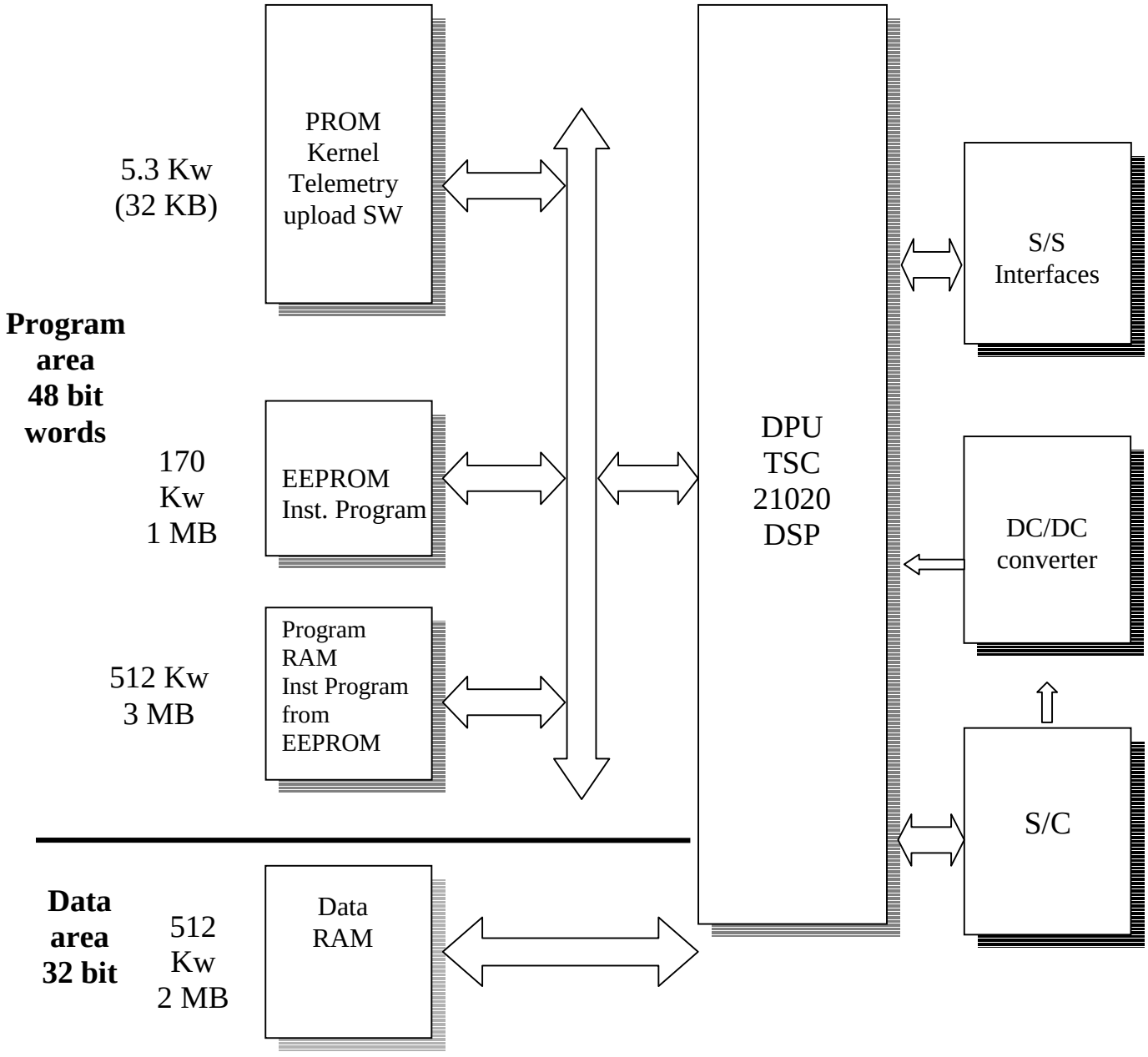

Figure 2-1 DPU CPU memory organisation

2.2 Redundancy concept

The top level DPU redundancy concept is shown in the following diagram:

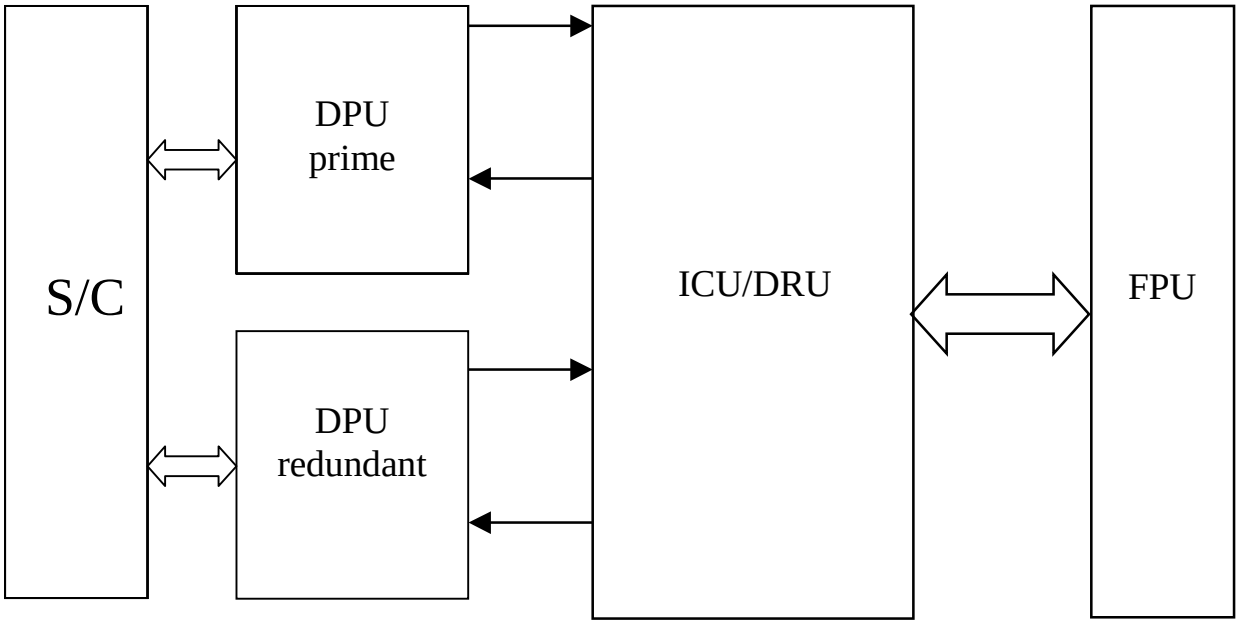

Figure 2-2 DPU redundancy concept

The DPU box contains two complete units in cold redundancy states. The S/C prime/redundant 28V power bus controls the switching between the two units.
As a consequence, the DPU interfaces with both S/C and S/S are doubled.

3 DPU - Spacecraft interfaces

3.1 Mechanical I/F

The prime and redundant DPUs are included in the same mechanical box whose dimensions, without feet, are:

240x218x194 mm (TBC)

The box interfaces with the S/C with 6 feet.
In figure 3.1 (TBW) the mechanical interface control drawing is shown

Figure 3-1 TBW

The total weight allocated to the DPU is 7 Kg.

3.2 Electrical I/F

3.2.1 Telemetry and Telecommand

The DPU interfaces with the S/C TM and TC subsystems (CDMS) with a redundant couple of wires implementing the MIL-STD 1553 B in the long stub configuration (transformers coupling). Each DPU section (prime and redundant) is connected to both prime and redundant bus lines, as shown in Fig 3.2

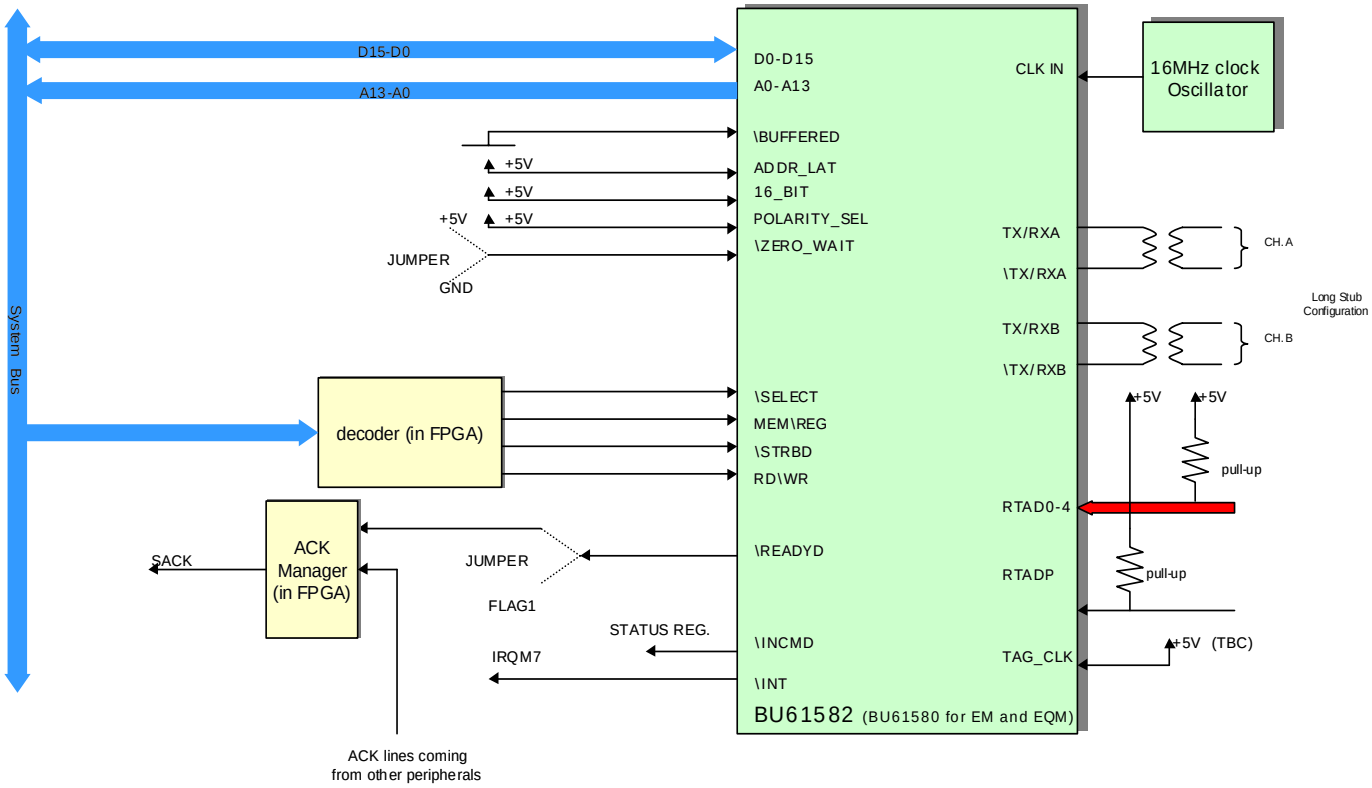

Figure 3-2 Detailed DPU Spacecraft interface

The nominal bit rate is 100 Kbps with a burst mode of 300 Kbps (TBC)

3.2.2 Power

The DPU gets the power trough the 28 V wire redundant power lines and separated for DPU DC/DC converter prime and DC/DC converter redundant. A S/C command decides which DPU is operated with the other in cold stand-by mode.

3.2.3 DC/DC Synch

Each DPU DC/DC converter gets the redundant 131072 Hz synchronising signal from the S/C. The synch is transformer coupled with the transformer located in the S/C and the receiver DPU interface should have an impedance >= 5Kohm in parallel to <= 200pF.

3.3 Connectors and pin functions

From the prime DPU there will be 3 Cannon DBMA9 (TBC) connectors respectively to prime CDMS, redundant CDMS and prime PDU. The same will apply to the redundant DPU so that a total of 6 connectors ad 6 cables will be used to electrically connect the DPU to the spacecraft.

3.3.1 DPU to PDU Prime

Unit DPU
Connector ID J01
Connector type DBMA9P
Connector name TO PDU_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	CH_GND					
2	28_V_P		AWG26	PDU P		
3	PWR_RET_P		AWG26	PDU P		
4	CH_GND					
5	CH_GND					
6	CH_GND					
7	28_V_P		AWG26	PDU P		
8	PWR_RET_P		AWG26	PDU P		
9	CH_GND					

3.3.2 DPU-Prime to CDMS-Prime

Unit DPU
Connector ID J03
Connector type DBMA9S
Connector name FM P_CMDS_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	1553B LINE 1 P		AWG26	CDMS P		
2	1553B LINE 2 P		AWG26	CDMS P		
3	CH_GND					
4	SYNCH LINE 2- P		AWG26	CDMS P		
5	SYNCH LINE SHIELD					
6	1553B LINE SHIELD			CDMS P		
7	CH_GND					
8	SYNCH LINE 1+ P		AWG26	CDMS P		
9	OVERALL SHIELD					

3.3.3 DPU-Prime to CDMS-Redundant

Unit DPU
Connector ID J04
Connector type DBMA9S
Connector name FM R_CMDS_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	1553B LINE 1 R		AWG26	CDMS R		
2	1553B LINE 2 R		AWG26	CDMS R		
3	CH_GND					
4	SYNCH LINE 2- R		AWG26	CDMS R		
5	SYNCH LINE SHIELD					
6	1553B LINE SHIELD			CDMS R		
7	CH_GND					
8	SYNCH LINE 1+ R		AWG26	CDMS R		
9	OVERALL SHIELD					

3.3.4 DPU to PDU Redundant

Unit DPU
Connector ID J02
Connector type DBMA9P
Connector name TO PDU_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	CH_GND					
2	28_V_R		AWG26	PDU R		
3	PWR_RET_R		AWG26	PDU R		
4	CH_GND					
5	CH_GND					
6	CH_GND					
7	28_V_R		AWG26	PDU R		
8	PWR_RET_R		AWG26	PDU R		
9	CH_GND					

3.3.5 DPU-Redundant to CDMS-Prime

Unit DPU
Connector ID J05
Connector type DBMA9S
Connector name FM P_CMDS_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	1553B LINE 1 P		AWG26	CDMS P		
2	1553B LINE 2 P		AWG26	CDMS P		
3	CH_GND					
4	SYNCH LINE 2- P		AWG26	CDMS P		
5	SYNCH LINE SHIELD					
6	1553B LINE SHIELD					
7	CH_GND					
8	SYNCH LINE 1+P		AWG26	CDMS P		
9	OVERALL SHIELD					

3.3.6 DPU-Redundant to CDMS-Redundant

Unit DPU
Connector ID J06
Connector type DBMA9S
Connector name FM R_CMDS_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	1553B LINE 1 R		AWG26	CDMS R		
2	1553B LINE 2 R		AWG26	CDMS R		
3	CH_GND					
4	SYNCH LINE 2- R		AWG26	CDMS R		
5	SYNCH LINE SHIELD					
6	1553B LINE SHIELD					
7	CH_GND					
8	SYNCH LINE 1+ R		AWG26	CDMS R		
9	OVERALL SHIELD					

4 DPU - Subsystems interfaces

4.1 General Information

The DPU interacts with the subsystems via dedicated low speed bidirectional and high speed monodirectional serial interfaces.
The two physical subsystem units are logically divided into three independent units each connected to the DPU with one high speed and one low speed interface.
Both the DPU and the S/S (interfaces) are fully redundant, so that the total number of serial interfaces is 12.

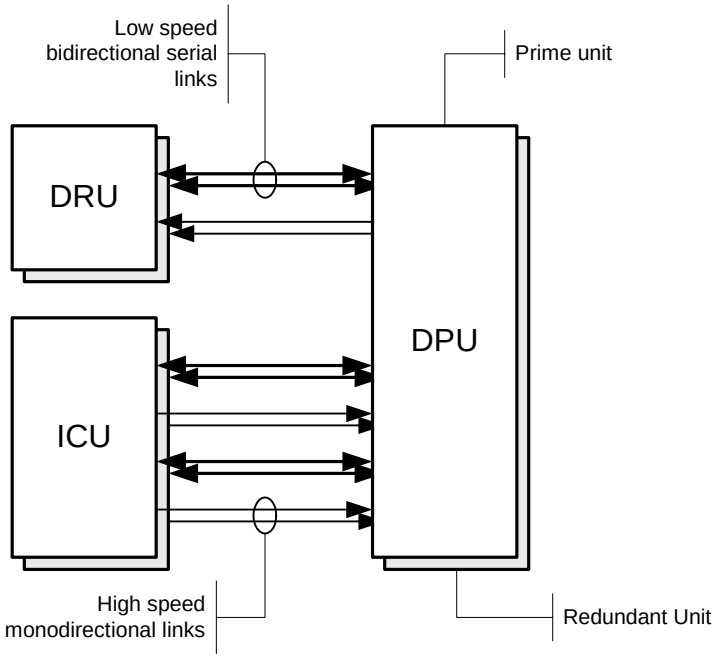

Figure 4-1 DPU - Subsystems Interfaces schematic view

All interfaces adopt the RS 422 differential electrical interface as shown in figure 4-2.

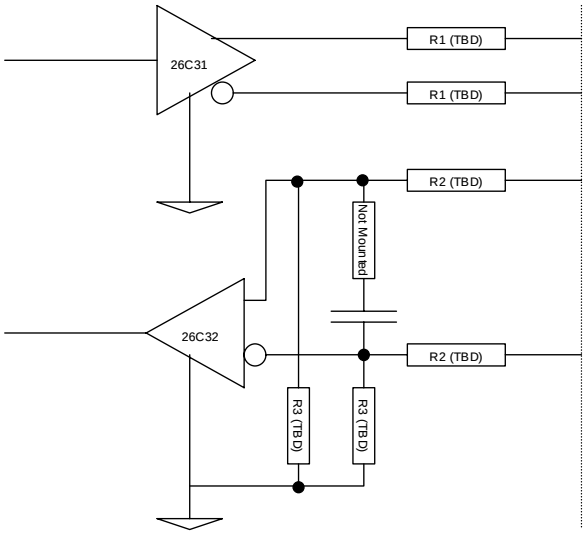

Figure 4-2 Balanced line drivers and receivers

4.2 Low Speed Interface

The low speed bidirectional I/F is organized as a bus with the DPU acting as controller so that all data transactions with the subsystem are initiated by DPU.
The low speed interface protocol is shown in figure 4-3.

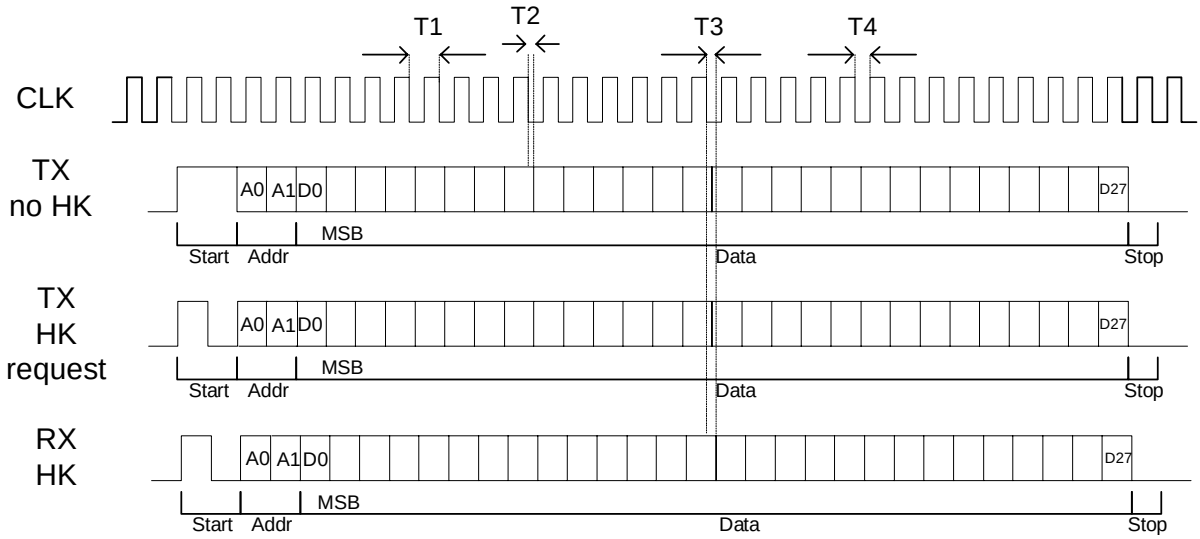

Figure 4-3 Low speed interface protocol

With reference to the figure, the tolerances on the indicated time parameters are:

Parameter	Min. Value (TBC)	Max. Value (TBC)	Unit
T1	3.17	3.23	μs
T2	0	0.7	μs
T3	0.05	1.2	μs
T4	1.53	1.66	μs

Commands sent by the DPU via the TX lines are always received by all the subsystems, the address field of the command word selecting the relevant unit. One address is reserved as a broadcast command. The subsystem addressing is made according to the following table:

A0	A1	Subsystem
0	0	DRE
1	0	MCE
0	1	SCE
1	1	Broadcast

The DPU can send both commands and/or HK requests as signalled by the second start bit of the command word. When requested, the subsystems will send responses via the RX line.

A command is made of 2 start bits, 2 address bits, 28 data bits and 1 stop bit.
A HK request is issued by setting the second start bit according to the following table:

Start0	Start1	HK
1	1	No
1	0	Yes

The HK response will have the same form of the requesting command, the address field indicating the originating subsystem.

The command word data field can be subdivided in every way, the baseline is shown in the following table:

From	To	Description
D0	D7	Command identifier
D8	D27	Command parameters

As the selection of the input RX channel is done by the sub-unit address field of the last TX command sent, no command can be sent to a different sub-unit until the last HK RX corresponding to the last command sent is received. Figure 4-4 shows the transmission reception sequence.

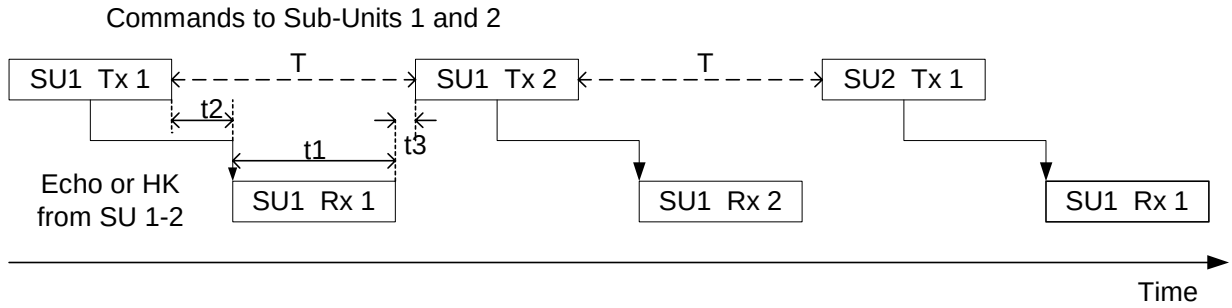

Figure 4-4 Low speed interface – transmission reception protocol

In order to avoid system lock a TBD us timeout **TO** is defined. In any case, a new HK request cancels the previous request whether already sent or not.

The following table shows the timing requirements with and without HK request.

Parameter	**Min value [us] TBC**	**Max value [us] TBC**	**Description**
TO	TBD	TBD	Time-Out
t1	101	104	Command word length
t2	0	TBD	HK response time
t3	10	NA	Time to next command
T	10	NA	No HK request
T	Minimum value between (t1+t2+t3) and TO		With HK request

The DPU side of the low speed I/F is shown in figure 4-5. The DPU originated clock line has a fixed frequency of 312.5 KHz. The clock signal generated by DPU is distributed to all subsystems and can be used for synchronisation purposes, after a dedicated broadcast command is issued (see section 4.4).

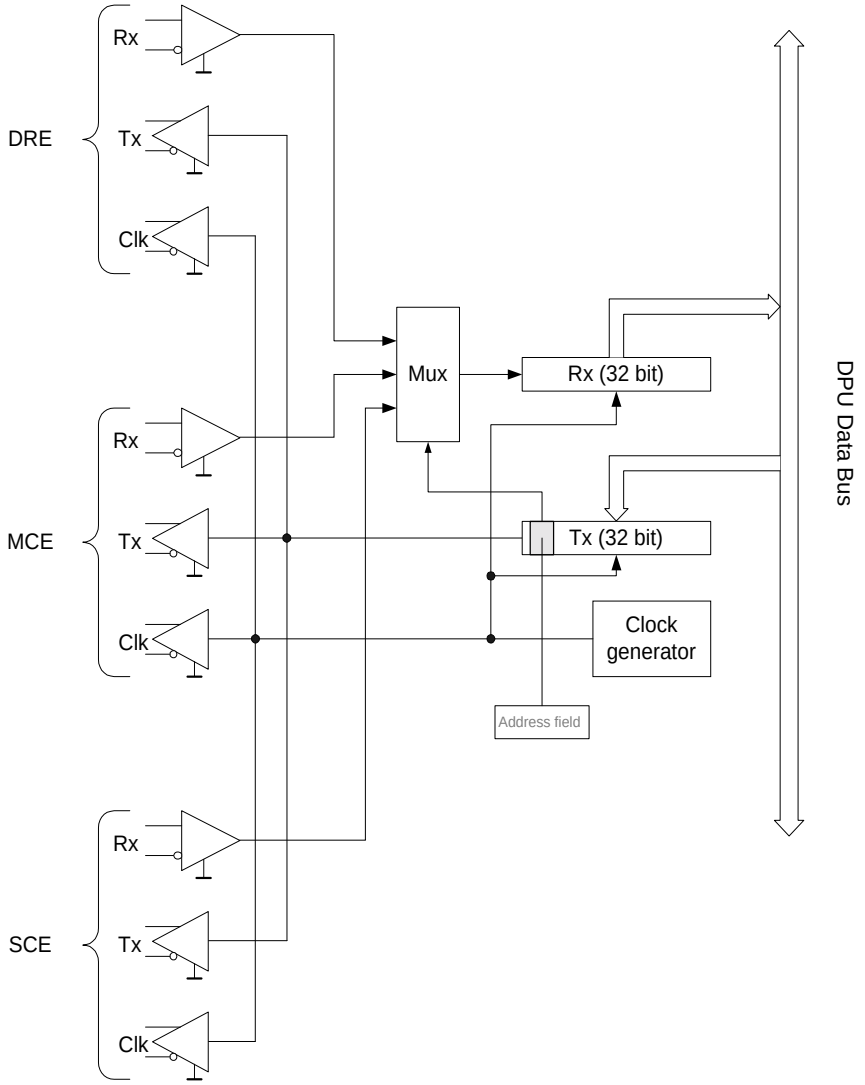

Figure 4-5 Detailed bidirectional low speed interface

The detailed subsystems commands lists are reported in sections 5 and 6 (TBW).

4.3 High Speed Interface

The high speed data link (science data link) is made by three monodirectional fast synchronous serial input interfaces, each of which with 8 KW 16 bits FIFO. The FIFOs half full signal generates an interrupt on the DSP. Three independent interfaces are required since simultaneous data transfer can occur.
The high speed I/F will transfer data from ICU/DRU sub-units to DPU as 16 bit words using a clock up to 2.5 MHz (baseline 1 MHz TBC). Being the interface unidirectional, all signals are generated by ICU/DRU.

The DPU side of the 3 high speed I/F is shown in the following figure:

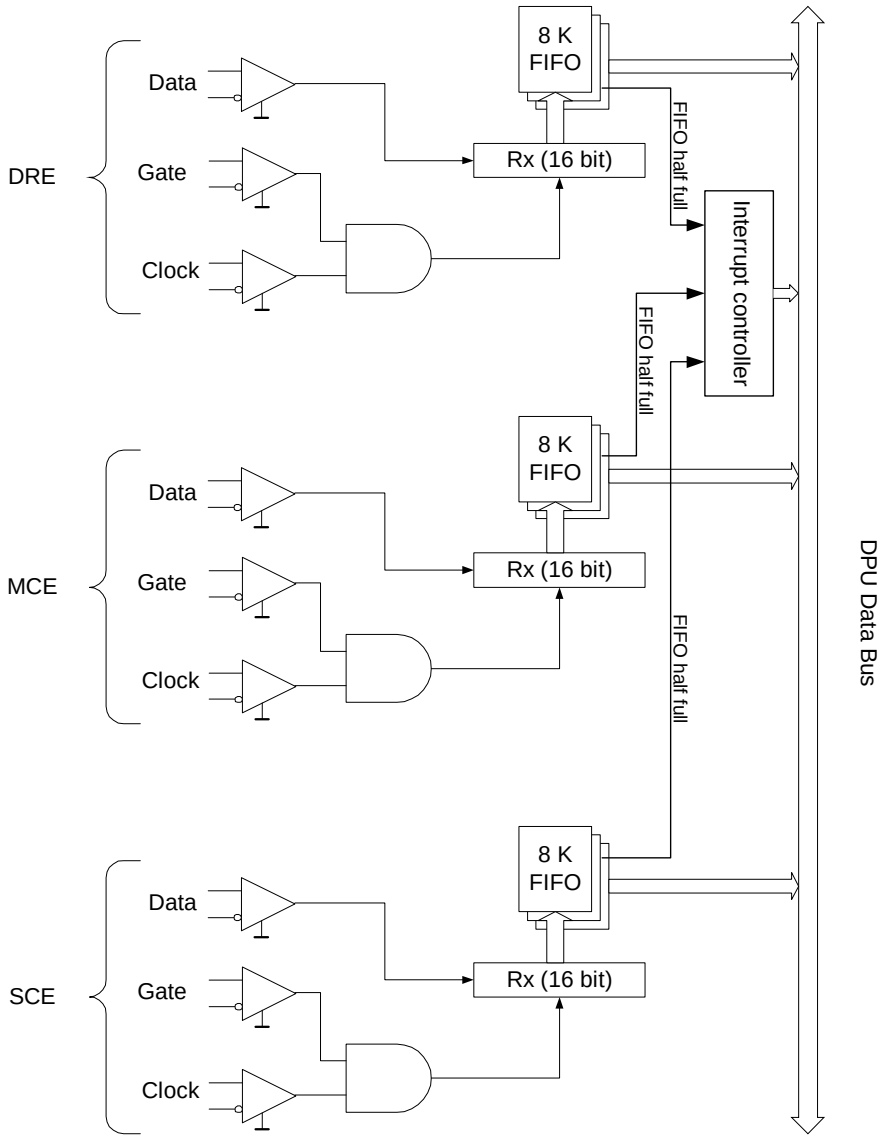

Figure 4-6 Detailed monodirectional high speed interface

The clock, gate and data signals coming from the subsystems are as in figure 4-7.

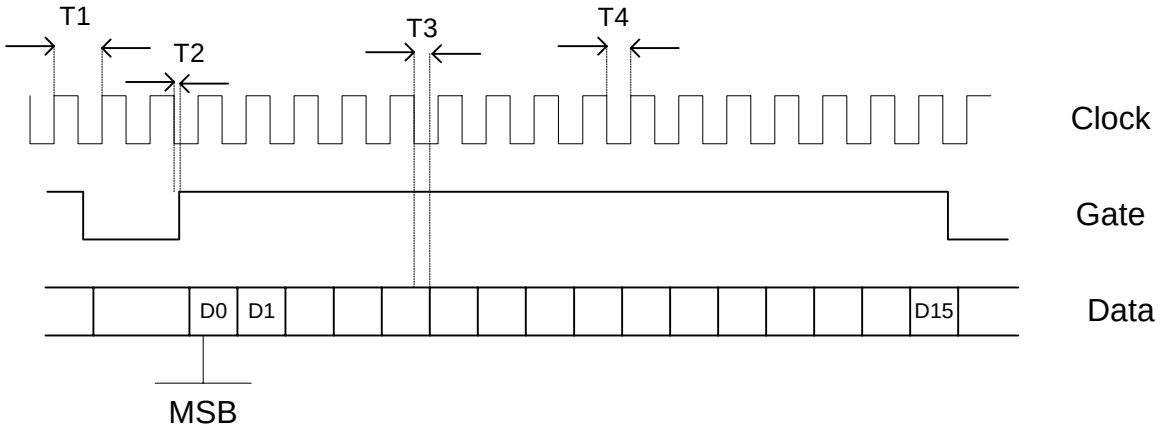

Figure 4-7 High speed interface protocol

Signal lines are defined as in figure and the clock frequency is 1 MHz (TBC). The tolerances on the indicated time parameters are:

Parameter	Min. Value (TBC)	Max. Value (TBC)	Unit
T1	990	1010	ns
T2	0	100	ns
T3	0	300	ns
T4	450	550	ns

4.4 DRU/ICU data

The SPIRE telemetry parameters can be split into two types:

1. **Science Parameters**: detector data plus those data required to process the detector data.
2. **Housekeeping parameters**: data required to monitor the configuration and health and safety status of the instrument.

Housekeeping parameters are provided on the *Low Speed RX* data line from DRU and ICU to the DPU in response to a HK request . Each request will return one or more data values within a 32 bit word. 28 bits are available for data.
The DPU will request the housekeeping data from the DRU/ICU subsystems at regular intervals (1sec TBC) and place them, along with the DPU parameters into a single housekeeping TM packet. There will be a single instance of each housekeeping parameter in a housekeeping TM packet. In the case of a value being invalid, the OBS will set a flag in the Housekeeping indicating this.

Science parameters are provided on the *High Speed data lines* from DRU and ICU to the DPU following a request for data issued on the Low Speed data line. The science information is provided in the form of frames containing a fixed set of science parameters.

The number of frame types per subsystems is:
- DCU: 10 (test pattern, all photometric arrays, both spectrometer arrays, 5* one detector array, 2 others TBD)
- SCU: 2 (test pattern, all data)
- MCU: 2 (test pattern, delta time + 2 other channels (selectable))

The number of acquisition rates available will be limited to 3 for the MCU and 4 for the DCU and SCU

Each frame is composed of :
- a header word (16bits);
- a frame time (TBD bits – see later)
- a number of data words;
- a check word (16bits)

Both word and frame definitions are subsystem dependent and will be described in sections 5 and 6 (TBW).

The DPU will copy the science data frames into a telemetry packet (including the check word). It will also check the header and the check word with the data in the frame and, if check fails, it will take action to resynchronise with the data stream (TBC).

4.5 Data acquisition Timing

Each DRU/ICU subsystem maintains its own counter driven by the 312.5 KHz clock provided by the DPU on the low speed interface. Thus the counters remain in synchronisation at all times and can provide the time to an accuracy of ~3 microseconds.

The counters are reset to 0 by a command from the DPU, which is broadcast to all three subsystems at the same time. Thus the counters should be identical (provided the reset pulse is generated from the received command in the three subsystems in a time that is identical, within <~3 microseconds).
The time taken to reset the counters after the DPU issues the command is not critical, as this is used only to provide a link to the absolute time maintained by the DPU (received from the S/C). The accuracy of this time value is 1000 microsec.
The counters are used to mark each frame with the elapsed time since the last reset command.

Because the frames from the FTS are generated asynchronously with the detector data frames, it is not possible to include data from different subsystems into a single TM packet. The DPU will therefore generate separately:

1. DCU science packets;
2. MCU science packets;
3. SCU science packets;
4. DPU science packets (TBC)

Each TM packet will contain, in addition to the standard header information and the data frames

the absolute DPU time of the last counter reset command.

4.6 Connectors and pin functions

From the prime DPU there will be 3 Cannon DBMA25P (TBC) connectors respectively to DCE, MCE and SCE, carrying both low speed and high speed interfaces signals.
The same will apply for the redunded DPU so that a total of 6 connectors and a total of 6 cables will be used to interconnect the subsystems. The connectors and cables pin function are defined in the following tables.

4.6.1 DPU to DCE - Prime

Unit DPU
Connector ID J07
Connector type DBMA25P
Connector name TO DCE_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_DCE_P+		AWG26	DRU		
3	TX_DCE_P+		AWG26	DRU		
4	RX_DCE_P+		AWG26	DRU		
5	RX_SHD					
6						
7						
8	CLK_DCE_P+		AWG26	DRU		
9	CLK_SHD					
10	DAT_DCE_P+		AWG26	DRU		
11	GAT_DCE_P+		AWG26	DRU		
12	GAT_SHD					
13						
14						
15	CLK_DCE_P-		AWG26	DRU		
16	TX_DCE_P-		AWG26	DRU		
17	RX_DCE_P-		AWG26	DRU		
18						
19						
20						
21	CLK_DCE_P-		AWG26	DRU		
22	DAT_DCE_P-		AWG26	DRU		
23	DAT_SHD					
24	GAT_DCE_P-		AWG26	DRU		
25						

4.6.2 DPU to MCE - Prime

Unit DPU
Connector ID J08
Connector type DBMA25P
Connector name TO MCE_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_MCE_P+		AWG26	ICU	J08	
3	TX_MCE_P+		AWG26	ICU	J08	
4	RX_MCE_P+		AWG26	ICU	J08	
5	RX_SHD					
6						
7						
8	CLK_MCE_P+		AWG26	ICU	J08	
9	CLK_SHD					
10	DAT_MCE_P+		AWG26	ICU	J08	
11	GAT_MCE_P+		AWG26	ICU	J08	
12	GAT_SHD					
13						
14						
15	CLK_MCE_P-		AWG26	ICU	J08	
16	TX_MCE_P-		AWG26	ICU	J08	
17	RX_MCE_P-		AWG26	ICU	J08	
18						
19						
20						
21	CLK_MCE_P-		AWG26	ICU	J08	
22	DAT_MCE_P-		AWG26	ICU	J08	
23	DAT_SHD					
24	GAT_MCE_P-		AWG26	ICU	J08	
25						

4.6.3 DPU to SCE - Prime

Unit DPU
Connector ID J09
Connector type DBMA25P
Connector name TO SCE_P

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_SCE_P+		AWG26	ICU		
3	TX_SCE_P+		AWG26	ICU		
4	RX_SCE_P+		AWG26	ICU		
5	RX_SHD					
6						
7						
8	CLK_SCE_P+		AWG26	ICU		
9	CLK_SHD					
10	DAT_SCE_P+		AWG26	ICU		
11	GAT_SCE_P+		AWG26	ICU		
12	GAT_SHD					
13						
14						
15	CLK_SCE_P-		AWG26	ICU		
16	TX_SCE_P-		AWG26	ICU		
17	RX_SCE_P-		AWG26	ICU		
18						
19						
20						
21	CLK_SCE_P-		AWG26	ICU		
22	DAT_SCE_P-		AWG26	ICU		
23	DAT_SHD					
24	GAT_SCE_P-		AWG26	ICU		
25						

4.6.4 DPU to DCE - Redundant

Unit DPU
Connector ID J10
Connector type DBMA25P
Connector name TO DCE_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_DCE_P+		AWG26	DRU		
3	TX_DCE_P+		AWG26	DRU		
4	RX_DCE_P+		AWG26	DRU		
5	RX_SHD					
6						
7						
8	CLK_DCE_P+		AWG26	DRU		
9	CLK_SHD					
10	DAT_DCE_P+		AWG26	DRU		
11	GAT_DCE_P+		AWG26	DRU		
12	GAT_SHD					
13						
14						
15	CLK_DCE_P-		AWG26	DRU		
16	TX_DCE_P-		AWG26	DRU		
17	RX_DCE_P-		AWG26	DRU		
18						
19						
20						
21	CLK_DCE_P-		AWG26	DRU		
22	DAT_DCE_P-		AWG26	DRU		
23	DAT_SHD					
24	GAT_DCE_P-		AWG26	DRU		
25						

4.6.5 DPU to MCE - Redundant

Unit DPU
Connector ID J11
Connector type DBMA25P
Connector name TO MCE_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_MCE_P+		AWG26	ICU		
3	TX_MCE_P+		AWG26	ICU		
4	RX_MCE_P+		AWG26	ICU		
5	RX_SHD					
6						
7						
8	CLK_MCE_P+		AWG26	ICU		
9	CLK_SHD					
10	DAT_MCE_P+		AWG26	ICU		
11	GAT_MCE_P+		AWG26	ICU		
12	GAT_SHD					
13						
14						
15	CLK_MCE_P-		AWG26	ICU		
16	TX_MCE_P-		AWG26	ICU		
17	RX_MCE_P-		AWG26	ICU		
18						
19						
20						
21	CLK_MCE_P-		AWG26	ICU		
22	DAT_MCE_P-		AWG26	ICU		
23	DAT_SHD					
24	GAT_MCE_P-		AWG26	ICU		
25						

4.6.6 DPU to SCE - Redundant

Unit DPU
Connector ID J12
Connector type DBMA25P
Connector name TO SCE_R

Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_SCE_P+		AWG26	ICU		
3	TX_SCE_P+		AWG26	ICU		
4	RX_SCE_P+		AWG26	ICU		
5	RX_SHD					
6						
7						
8	CLK_SCE_P+		AWG26	ICU		
9	CLK_SHD					
10	DAT_SCE_P+		AWG26	ICU		
11	GAT_SCE_P+		AWG26	ICU		
12	GAT_SHD					
13						
14						
15	CLK_SCE_P-		AWG26	ICU		
16	TX_SCE_P-		AWG26	ICU		
17	RX_SCE_P-		AWG26	ICU		
18						
19						
20						
21	CLK_SCE_P-		AWG26	ICU		
22	DAT_SCE_P-		AWG26	ICU		
23	DAT_SHD					
24	GAT_SCE_P-		AWG26	ICU		
25						

5 DPU - Instrument Control Unit specific interfaces

5.1 MCE Commands words

TBW on the base of input from S/S

5.2 MCE Housekeeping data words

TBW on the base of input from S/S

5.3 MCE Frames definition

TBW on the base of input from S/S

5.4 SCE Commands

TBW on the base of input from S/S

5.5 SCE Housekeeping data words

TBW on the base of input from S/S

5.6 SCE Frames definition

TBW on the base of input from S/S

6 DPU-Detector Readout Unit specific interfaces

6.1 DCE Commands

TBW on the base of input from S/S

6.2 DCE Housekeeping data words

TBW on the base of input from S/S

6.3 DCE Frames definition

TBW on the base of input from S/S