Section 10: Appendix 11

Appendix 2: Compliance & Outstanding issues

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2.2 General

At the release date of this document (20.Jul.01) the following issues are known. Any remaining issues not resolved by the DDR date (30.Jul.01) will be folded together with DDR raised issues and appropriate design changes made.

The design will be placed under configuration control on 31.Jul.01 and all changes thereafter will be raised as discussed in the Product Assurance plan (Engineering Change Requests and CTD'S)

2.3 *Compliance matrix*

The current design status is compared to the requirements (RD 5) where data from single-axis tests is relevant it has been noted. Two axis prototype and Development model tests will complete the bulk of the table over the following 1-4 months.

Requirement	Met by baseline design	Design description reference	Supporting test data	Notes
Angular Travel - Chop Axis	Yes	Drawing SPIRE-BSM-020-001		
Angular Travel - Jiggle Axis	Yes	Drawing SPIRE-BSM-020-001		
Minimum Step Size	Yes	???		
Chop Frequency	Yes	???	Yes	
Jiggle Frequency	Yes	???		
Holding position	Yes	???	Yes	
Stability	Yes	???	Yes	
Position Measurement	Yes	???	Yes	
Settling Time	Yes	???	Yes	
Chop repeatability	Yes	???		
Mechanical Dimensions	Yes	Mech ICD	partial	2 axis prototype does not have baffle
Operating Temperature	Yes	???	Single axis : Yes	Cooldown data supports modelling
Thermal Isolation	Yes	???		
Cold Power Dissipation	Yes	???	Yes ???	
Warm Electronics Power Dissipation	TBD	N/A	N/A	LAM
Mirror Surface Dimensions	Yes	???	Yes	2 axis prototype mirror is correct size
Mirror Surface Finish	Yes	???		
Mirror Surface Reflectivity	Yes	???		
Mirror Surface Emissivity	N/A	N/A		

Requirement	Met by baseline design	Design description reference	Supporting test data	Notes
Baffle	TBC	???		Beam profile currently has minor foul from motor & sensor
Position of Rotation Axes	Yes	???		
Orthogonality of Rotation Axes	Yes	???		
Fail Safe (No Drive Signal) Position	Yes	???		
Fail Safe (Mechanical Failure) Position	Yes	???		
Mass	Yes	???		
Cool-down time	Yes	???		
Reliability	Yes	???		Non-quantitative spec
Failure Modes	Yes	???		
Operational Safety	Yes	N/A		ATC safety risk assessment performed
Lifetime	Yes	???		
Operating modes	Yes	???		
Jiggle Mode	Yes	???		
Chopping Mode	Yes	???		
Scan mapping	Yes	???		
Stare or 'holding' mode	Yes	???		
Combinations of Modes	Yes	???		
Data Outputs	TBC	???		
Data Inputs	Yes	???		
Exported vibration	Yes	???		

Requirement	Met by baseline design	Design description reference	Supporting test data	Notes
Stray Magnetic fields	TBC	???		No externally imposed spec
Electro-Magnetic Compatibility	TBC	???		No externally imposed spec
ICD's	Yes	???		
Design requirements	Yes	???		
Electronics Card Format	Yes	???		
Mirror Flatness (optical alignment)	Yes	???		
Mirror Reflectivity (optical alignment)	Yes	???		
Cleanliness	Yes	???		
Material selection	Yes	???		
Storage	Yes	???		
Shock	N/A	???		
Quasi Static Loads	Yes	???		
Sine Vibration	Yes	???		
Random Vibration	TBC	???		Margins lower than ideal
Vacuum Level	Yes	???		
Vacuum Outgassing	Yes	???		
Temperature	Yes	???		
Magnetic Fields	Yes	???		
Survival Temperature	Yes	???		Magnets limited to 80 deg C
Radiation environment	TBC	???		Infineon sensor requires rating. LAM to rate BSMe

2.4 *Known Issues*

ID	Issue	Plan to resolve
1.	Motor corners clip the 20% oversize optical beam	Chamfer corners and shields - work in hand as at 20.Jul.01
2.	Chop sensor assembly edge clip the 20% oversize optical beam	Chamfer corners, move sensor back slightly
3.	Chop sensor is G10 and emisivity/cooling needs to be modelled	Consider material change
4.	Jiggle flex pivots inconel survivability data needs updating in discussions with TRW	Resolve with TRW
5.	Harness cut-outs and securing to the BSM structure interface need to be determined	Mock up harness on 2 axis prototype and make design changes
6.	Harness layout to be optimized to allow overlay of prime on redundant.	
7.	MPIA motor space envelope is TBC after Zeiss optimization	Liaise with MPIA/Zeiss
8.	Parts list needs update after LAM finalize MCU parts list	Liaise with LAM. Update at SMEC/MCU DDR
9.		