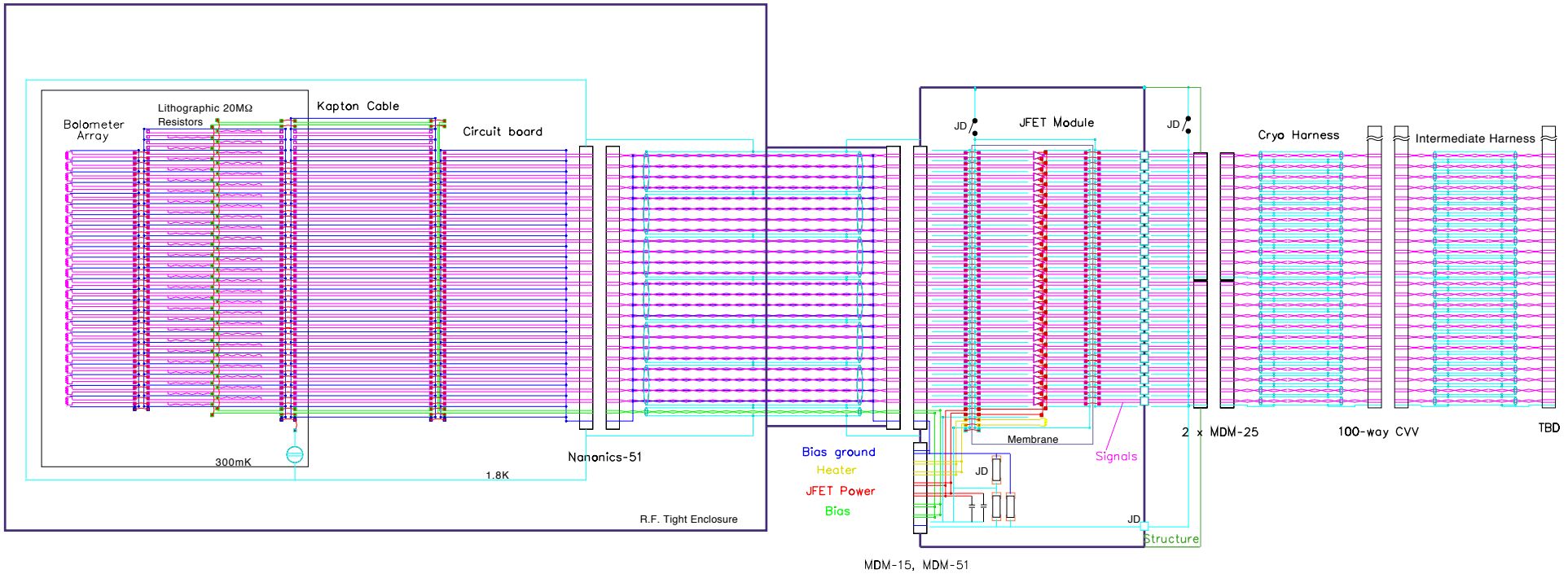
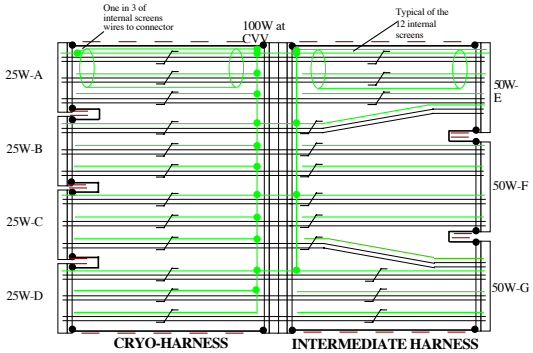


Jamie
On Friday we got the wiring diagram you sent opened at long last and hence understood. It shows masses of useful detail and unpacks to >32,000 elements! I've reproduced it above but taken the liberty of shortening some of the twisted wires to make the file a little shorter, and also added some section boxes, etc. as described below.

1. The 51 Nanonics have 48 contacts for 24 twisted signals, 2 contacts for the biases and one ground pin. This is an encouraging start because it's the same as I drew! I believe there's a link via a mounting screw on the Lithographic Resistor module from said ground to the 300mK chassis…please confirm. However, if the 300mK is hung on Kevlar string and not electrically joined to the 1.8K BDA body, I think that near the "1.8K" label on the diagram there should be a link on the BDA's "circuit board" joining this same ground to BDA 1.8K chassis, i.e. just inside the Nanonics connector.

2. Going right to the other end of the system, we both have JFET signal outputs on 2x25W MDMs going towards the warm electronics each with 24 contacts for 12 twisted signals and one ground pin. We differ as to how these are then harnessed. I don't think ESA would want to use a screened twisted pair for every channel as you have drawn, so I have suggested a cable lay-up that differs from this, shown for on 100 way and hence two JFET module outputs as follows:



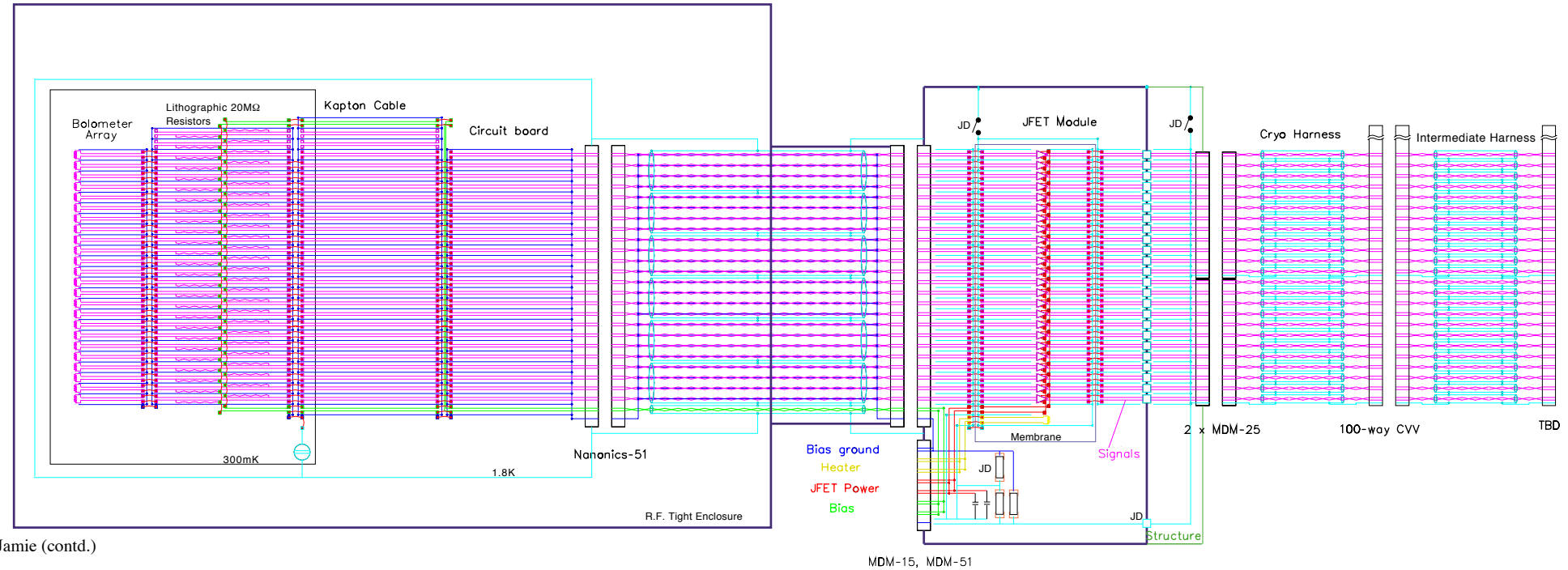
48 channels (each +,- and signal ground) as twisted triples, grouped as four triples in a "12-ax" with an insulated screen. So there are three 12-ax to each 25 way changing to four for each 50way connector on the warm electronics.

All of the signal grounds in the triples pass through the 50 way connectors, but only 4 can pass through the 100 ways, the rest being NC in the intermediate harness at that point. The four that pass shall correspond to the 4 single grounds that also pass through the 25 way connectors. A wire ring shall be supported on each side of the 100 way on the 4 ground contacts that pass through it. The signal grounds in triples in the cryo harness that do not have contacts on the 25 way connectors shall be made-off on one of these rings but NC at the JFET end.

The "12-ax" screens all pass the 50 ways on pins, are made off on the rings at the 100 ways, and are spliced (by tails) on to the ground pins in the 25 ways.

All of this harness is enclosed in outer r.f. screen, EMC sealed to connector boots, overwrapped with double-wound insulation, shown as brown dashed line.

This links to a defined set of pins on Christophe's DCU which I will not repeat here. I think the capacitance of my suggestion should be lower, there's considerably less metal used as screens, and I have kept the signal grounds separate from r.f. screens. If you have any misgivings about my suggestion, please raise them, otherwise it would be simplest to keep it as-is since ESA already have this information.



Jamie (contd.)

3. The circuit board in the BDA behind the Nanonics should be a good way of heatsinking the harness at this point. I have asked MSSL to let JPL know which of the 6 Nanonics positions would best suit mechanical accommodation in the BDAs for which all 6 connectors are not fitted.

4. For the signals between the BDA and the JFET module I suggested screened twisted pairs, the shields to carry the ground, inside an r.f screen at least for the part between the JFET box and the FPU wall. JPL has used twisted triples with the third wire carrying the ground. Since a shield is about 30 times higher cross-section than a conductor, your 24 conductors as against my 4 shields is some 5 times higher ground impedance, but this might not matter. Clearly this harness lay-up is J.P.L.'s decision, subject to thermal requirements, although whatever is used has to fit in with the overall grounding philosophy, i.e. the several signal grounds separate from chassis except for a link at the 1.8K boxes. Have you any feeling about the inter-channel cross-talk trade-off?

5. The FPU's R.F. Tight Enclosure on the above is drawn on by myself. There are back-to-back connectors baselined at the pointwhere this harness transits said wall at 12K. These should be included in your diagram until it is clear that they may be removed. The harness certainly needs heatsinking at this interface. Also, the JFET module's r.f. filtered volume has to be rigorously extended back to the FPU for the outer part of this cable run, so I have taken the liberty if drawing a couple of lines on your drawing. Just by way of comment, these terminate on a connector body...I note some light blue lines seemingly bridging connector I/Fs on the above!

6. I take the point from your diagram, and other communications, that all wires leaving a JFET module on the "back-harness" do so without passing through the r.f. filters, so the back-harness itself has to be fully R.F. Faraday caged screened and the wiring modules which interface this harness to other parts of the Cryo-Harness have to include their own R.F. filtering. I will amend my drawings to suit.

7. The JFET module as drawn seems to omit the12Kelvin 100Ohm drain resistors drawn on other JPL circuits and any power supply decoupling / cold FET gate resistors as drawn in some documents. Please comment.

8. Trying to improve international relations, I've left the real problems until the end. I'm quite happy to assume, as you seem to,that theJFET mosdules themselves are sufficiently small that one can join electrically to anywhere on their insides and not pick up EMC, i.e. the grounds thus joined do not have to be a true unipoint. However I've drawn some ground bit on the diagram and labelled them "JD". These are primarily to bring the configuration in line with the SPIRE grounding diagram. There are three grounds in the module, a ground travelling to the bolometers, a ground going with the signals to the warm electronics, and a ground associated with the ±ve supplies to the "amplifier" or JFET source-follower pairs. The last two of these are just shown as shorted to chassis, so I've changed these shorts to switches (probably wire-bonds) and the default would be not to fit them, i.e. to follow the present grounding diagram. I've included pads on the JFET PCB for surface mounts to interconnect grounds, possibly with shorts, and to decouple power rails as mentioned in 7 above.

9. Lastly, but by no means least, we come to what is carried on the back-harness connector. This harness is isothermal at 12K and can employ standard gauge MDM copper wiring, so I query the need to double up on pins not least because only 24 channels can be affected by the unlikely failure .... that's not to say that functions for a whole BDA do not need to be at least double along the Cryo-harness from the Wiring Modules to the warm electronics. We could do with the grounds passing into the backharness, and two wires for JFET temperature (important thermal information for flight) which actually comes to 11 functions in all: Bias(2)&gnd., V+V-&gnd., heater(2), temp. diode (2) and gnd. towards signal outputs. At one pin per function these would fit your proposed connector with 4 spare for doubling up if needed. Maybe you could respond as to whether you could implement these suggestions.

Cheers, John