Notes and Actions from SPIRE Warm Electronics and Operations System Summit 18/20 October 2000 RAL
Bruce Swinyard

Here are some rather scrambled notes on the proceedings of the SPIRE Warm Electronics Summit. They will hopefully act as an aide memoire – the actions are appended as a table and will be followed up. The agreement note on the DPU/DRCU is also appended – please take note this will form the basis of the DPU/DRCU interface document.

Present:
Bruce Swinyard – RAL (All)
Ken King – RAL (All)
Sunil Sidher – RAL (All)
John Delderfield – RAL (All)
Brian Stobie – ATC (All)
Colin Cunningham – ATC (Afternoon day two and day three only)
Laurent Vigroux – SAp (Day one only)
Christophe Cara – SAp (All)
Jean-Louis Augueres – SAp (Day 1 and 2 Only)
Riccardo Cerulli – IFSI (All)
Anna Digiorgio – IFSI (All)
Didier Ferrand – LAM (All)
Michel Jevaud – LAM (All)
Goran Olofsson – SO (All)
Hans-Gustav Floren – SO (All)
Jamie Bock – JPL (Day two and three only)
Peter Hargrave – QMW (Day three only)
Alex Ellery – QMW (Day three only)

Video Conference held on afternoon of 19/10/2000 to JPL with: Jerry Lilienthal – JPL; Viktor Hristov – Caltech and Frederick Pinsard SAp.

Day One
Operating Modes and Control

i) The agenda were agreed

ii) **Operating Modes:**

How does the DRCU turn on – CC says that the power is put onto all sub-units at once – need to define modes of the sub-units – DF has done this for the MCU – need to centrally draw all this together to produce start up procedure

Discussion of how the instrument gets to SAFE mode and what SAFE should be – decision to draw up a unit level criticality to see under what circumstances the anomaly action will be taken and whether there is any possibility of carrying on

with some bits still working.

DF has done a failure mode analysis for the MCU – need this for all units

Observation modes – LV recommends we reduce the number but add sub-modes into them – POINT SOURCE – SCAN etc.

Action: JD/BMS write a draft instrument start up procedure.
Action: BMS/LV independently draw up criticality analysis to see when anomaly action will be carried out.
Action BMS review observing modes with an aim of reducing total number with additional sub-modes if necessary.

iii) **Commanding**

Ken presented discussed commanding scheme to the instrument – table driven from DPU.
These need to be down converted into low level commands by OBS. Need list of commands needed by DPU. DF has list for MCU – maybe ~100 or so elementary parameters to MCU with a few commands

Action: CC to put list of elementary DRCU commands and associated parameters into the DCRU/DPU interface document.
Action: Ken to construct command procedures from the elementary command list to carry out the instrument commanding scheme once he has the elementary DRCU command and parameter list

iv) Electrical System Design

See attached viewgraphs.

There will now be two units for DRCU namely DCU and MSCU also there will be three SPIRE warm interconnect harnesses.
Ground test configuration is different as it includes the shutter – at present this is routed through the DRCU to its control electronics. It is preferred that this is avoided and a standoff connector is provided on the spacecraft.
We will add extra connectors onto the DPU and not have Y-harness for the two DRCU units.
ICDs – CEA will write the DPU/DRCU ICD – Christophe also wants ICDs with all DRCU sub-units which he will write and between DRCU and cold FPU – it is expected that the sub-system providers will contribute a great deal to these probably they will have to write them? COMMENTS?

DAY Two

v) Instrument Control (actually started day one but continued and summarised here)

Scheme for controlling BSM mode and FTS mode presented and discussed at length. Basic scheme is accepted for commanding BUT JBB wants to know what the required sampling rate is on the position if we just run asynchronously.

Christophe needs the requirements on the different rates of sampling of the detectors and what accuracy is required on the sampling.

Telemetry requirements

- ➔ What is the length of an operation for the length of the counter that is required
- ➔ What is the longest operation we can do without resetting the MCU counters.
- ➔ The MCU needs some headroom on the data sent across – 24 Bits – IFSI can put in place a 24 bit FIFO if required.
- ➔ Data rate to DPU is will be greater than 100 kbps – DPU will need to do some data reduction before sending to CDMS.
- ➔ Need to sort out the number of detectors per array into modulo 24. To include dead channels
- ➔ DCU telemetry proposal is that all HK and science data packets will go through the hi-speed link – Christophe has defined T1 throu' T4
- ➔ Problem with this is that Anna needs to have to poke about in the FIFO to get the HK data out.

What we can decide is that HK data can come on request from the DPU on the lo-speed line. We can divide the data streams into HK and science. "Science" HK data will go across the hi-speed line. Test packet will be sent across the hi-speed line when the DRCU starts up.

For MCU need to define what the packet contents have to be for the SPECTROMETER and PHOTOMETER modes. The other suggestion is that the MCU sends over 4 word "packets" with identifier – how does this get into the TM from the DPU?

All this was discussed at some length in parallel with a video conference to JPL to discuss the grounding scheme for the detectors. The results of the DPU-DRCU interface discussion are summarised in Ken's agreement note – appended.

Action: BMS/JD define requirements on the detector sampling rate for each defined operating mode.

Action: BMS define requirements on the BSM position sampling for asynchronous operation of the BSM in chopped modes.

Action: CCara re write the DPU/DRCU interface document in accordance with the agreement document appended to these minutes.

vi) **Grounding scheme for the detectors**

Viktor proposed and grounding diagram for the two JFET box option. This involves routing the bias supplies for the Spectrometer JFETs through the instrument FPU. No-one likes this very much.

Alternative scheme proposed by John Delderfield is to separate the two sides of the instrument completely with two separate power supplies one for the spectrometer and one for the photometer. The star point can then be either through the 300 mK thermal straps and the cooler to the cryostat or, as the detectors are naturally electrically isolated at the cold end – it can be placed in the warm electronics. This decision can be made at a later stage.

The basic scheme was agreed and will be implemented in the DRCU. The digital interface will have to be galvanically or opto-isolated to prevent ground loops between the two sides of the instrument.

The SIRTF scheme was presented – this has the star point in the warm electronics.

There was discussion of how the EMC susceptibility should be modelled and some discussion of how the RF filtering would work.

Action: JD to draw up an official version of grounding diagram and circulate for approval.

Action: JJB to send sample of Cooner wire to RAL for EMC evaluation

Action:JD to co-ordinate drawing up of basic equivalent circuit for detector system.

Day Three:

vii) DRCU Simulator Requirements

Discussion of the note on the DRCU requirements – see commented note attached to minutes.

Action: BMS/KJK revise and formally issue DRCU simulator requirements

Action: H-G Floren write DRCU Simulator Software Specification document.

viii) **Sub-system requirements on warm electronics**

Calibrators:

See viewgraphs

Beeman devices – commercial devices – o.k. for power but slow. Impedance about 150-200 Ohm

Specification: 5 mA 1.5 V 300 Ohm

Or Carbon fibre based one?

SCAL Minco heater 275 Ohm.

Detectors
The following questions need to be addressed in the detector warm electronics specification:

Bandwidth on the noise specification is wrong in the specification document – should be different for photometer and spectrometer.
Noise budget is 7 nV/rt(Hz) total from electronics and 7 nV/rt(Hz) from detectors – the total noise budget for the detector signal chain needs to be defined and written down.
Change requirements to isolate spectrometer and photometer into separate channels.
Noise specification for JFET and bias power supply needs to be defined
Frequency specification required on common mode rejection requirement.
Change maximum sampling rate for photometer to 16 Hz.
What is the expected duration of JFET heater power?
Need to define exactly how many pixels we are going to have per array – including "engineering" channels.

BSM
Brian is working on the electrical interface document – not yet complete.

SMEC/MCU
See viewgraphs - MCU design description document will be provided in the near future.
What will be the redundancy philosophy for the optical heads?

Cooler
Christophe presented the current scheme for the cooler control modes based on the "Cryogenic Sorption Cooler Drive Electronic Preliminary Definition" SBT/CT/2000-43 (to be given a SPIRE number). One issue that arose here was the control of the pump temperature during recycle rather than just applying some fixed current to the heater.

Thermometry
Bruce presented an updated scheme for the thermometry based on the exclusive use of Lakeshore Cernox thermistors. These come in three sub-types to cover the different ranges. The temperature resolution presented was based on using 12 bits digitisation – it was agreed that this was the wrong approach and the real resolution requirements over a given range should be quoted – Christophe will then convert these into electronics requirements.

Action: PH provide detailed electrical requirements for calibrators either in specification document or in electrical interface document such as being written for BSM

Action: Brian Stobie complete and issue BSM electrical interface document

Action: JJB to answer the points raised in the minutes either in the detector specification document or to write a dedicated detector electrical interface document

Action: DF complete and issue MCU design description document

Action: BMS/JD review and comment on cooler drive electronics document

Action: BMS define required resolution on thermometry and redundancy philosophy and re-issue technical note.

Action: BMS define redundancy requirements on optical encoder.

ix) **DPU/DRCU interface discussion of KJK note**

See Ken's note:
Need to define about ten packet contents list for DCU to DPU data transfer
SCU will have a single packet type for data plus test pattern
DPU needs to have a packet to send down information from the DPU to tell us what it's up to.
Timing – sub-unit counters will be driven by DPU clock at 312.5 kHz – timing to ~3 us accuracy. Counters will be reset by broadcast command from DPU – counters will be synchronised to within 3 useconds with dedicated hardware in interface.
Specification on absolute timing requirement needs to be written down somewhere.
For absolute timing need to report "start of scan" absolute time in low speed HK.
DPU will collect frames and bundle into four science packets: DCU; SCU; SMEC; BSM

Summary of discussion on SPIRE telemetry

1. DRCU Subsystems data:

Each DRCU subsystem (DCU, MCU, SCU) plus the DPU provides telemetry parameters. These parameters can be split into two types:

- **Science parameter** (detector data plus those data required in order to process the detector data)
- **Housekeeping parameter** (data required to monitor the configuration and health and safety status of the instrument)

Is it possible that the same parameter may be required for both purposes? In this case we should be able to request it in both forms – this is not currently possible with DCU and SCU parameters.
Action: System Team to determine whether it is necessary for any parameters to be included, both as housekeeping and science parameters. Due date: 1st November 2000.

Housekeeping parameters are provided on the Low Speed data line from the DRCU subsystem to the DPU in response to a request (GET PARAMETER command). Each request will return one or more data value(s) within a 32 bit word. 30 bits are available for data. The DPU may rearrange the data when it puts it into the TM packets.

Science parameters are provided on the High Speed data line from the DRCU subsystem to the DPU following a request for data. The information is provided in the form of 'frames' containing a fixed set of science parameters.

The number of frame types per subsystem is:

- DCU: 10 (test pattern, all photometric arrays, both spectrometer arrays, 5 * one detector array, 2 others TBD)
- SCU: 2 (test pattern, all data)
- MCU: 2 (test pattern, delta time+2 other channels (selectable))

Action: The System Team to identify the required contents of each frame type. Due date: 1st December 2000.

The request from the DPU may take the form of:

- send one frame;
- start sending frames at a given rate;
- send N frames at a given rate

The number of rates available will be limited to 3 for the MCU and 4 for the DCU and SCU. (When using the FTS, the rate is determined by the scan rate, not a fixed time interval)

Each frame is composed of:

- a header word (16 bits);
- a frame time (TBD bits – see later)
- a number of data words;
- a check word (16bits)

The DPU will copy the frame into a telemetry packet (including the check word). It will also check the header and check word with the data in the frame and, if the check fails, it will take action to resynchronise with the data stream.

How does the DPU synchronise with the data stream? – it is envisioned that the DPU will stop the current data sending, clear the DPU FIFO and restart the data at an appropriate time. This would lead to the loss of data from, for example, a scan, or jiggle position).
Action: Di Giorgio to define the action taken by the OBS if the science data in a frame fails the check. Due date: 1st December 2000.

2. Timing

Each DRCU subsystem maintains its own counter driven by the 312.5kHz clock provided by the DPU on the low speed interface. Thus the counters remain in synchronisation at all times and can provide the time to an accuracy of ~3 microseconds.

The counters are reset to 0 by a command from the DPU, which is broadcast to all three subsystems at the same time. Thus the counters should be identical (provided the reset pulse is generated from the received command in the three subsystems in a time that is identical, within < ~3 microsecs).

The time taken to reset the counters after the DPU issues the command is not critical, as this is used only to provide a link to the absolute time maintained by the DPU (received from the S/C). The accuracy of this time value is ~ 100 microsecs.

Action: System Team to define the required accuracy of the absolute time assignable to a data value. Due date: 1st November 2000.

The counters are used to mark each frame with the elapsed time since the last reset command. A 32 bit counter will not overflow for ~10,000 seconds (3hrs), so the reset command must be sent more frequently than this. It is suggested to reset the counters at the start of each FTS scan or measurement.

In the case of scanning the FTS, can we get away with only reporting the least significant 16 bits in order to reduce data rate? In this case the full time of the start of scan needs to be reported.
Action: Ferrand to propose a method for reporting the time of fringe crossing in the MCU science frames that minimises the data rate. Due date: 1st December 2000.

We also need to know at what time relative to the frame time are the parameters sampled.

Action: Cara to provide in the DRCU-DPU ICD a place to hold the information relating to the time of data sampling relative to the science frame time. Due date 15th November 2000.

3. TM Packets

The DPU will request the housekeeping data from the DRCU subsystems at regular intervals (1 sec TBC) and place them, along with the DPU parameters into a single housekeeping TM packet. There will be a single instance of each housekeeping parameter in a housekeeping packet. In the case of a value being invalid the OBS will set a flag in the housekeeping to indicate this.

Because the frames from the FTS are generated asynchronously with the detector data frames, it is not possible to include data from different DRCU subsystems into a single TM packet. The DPU will therefore generate separately:

- DCU Science Packets
- MCU Science Packets
- MSCU Science Packets
- DPU Science Packets

Because the length of some of these packets will be small, and we need to reduce the packet overhead, the DPU will group frames of the same type into a single Science TM packet. Note that the size of a TM packet of a given type is not fixed, as at the end of an operation the number of frames available may be less than the number required to fill a Science TM packet.

Each TM packet generated by the DPU must contain, in addition to the normal PUS header information and the data frames:

- The absolute DPU time of the last counter reset command.
- The identification information for the Observation and Building Block being executed (this information is sent to the DPU by the spacecraft at the start of each Observation or building block)

SUMMARY OF ACTIONS

ID	Actionee	Description	Priority	Need and Date
AI-SYS-0523-1.	JD/BMS	write a draft instrument start up procedure.	High	Final definition of instrument operations Present at Systems Review 24/11/2000
AI-SYS-0523-2.	BMS/LV	independently draw up criticality analysis to see when anomaly action will be carried out.	High	Final definition of instrument operations Present at Systems Review 24/11/2000
AI-SYS-0523-3.	BMS	review observing modes with an aim of reducing total number with additional sub-modes if necessary.	Medium	ditto 24/11/2000
AI-SYS-0523-4.	CCara	put list of elementary DRCU commands and associated parameters into the DCRU/DPU interface document.	Urgent	For ICD 15/11/2000
AI-SYS-0523-5.	KJK	construct command procedures from the elementary command list to carry out the instrument commanding scheme once he has the elementary DRCU command and parameter list	Urgent	For OBS URD 15/11/2000
AI-SYS-0523-6.	BMS/JD	define requirements on the detector sampling rate for each defined operating mode.	Urgent	For ICD 10/11/2000
AI-SYS-0523-7.	BMS	define requirements on the BSM position sampling for asynchronous operation of the BSM in chopped modes.	High	For final definition of instrument operations 24/11/2000
AI-SYS-0523-8.	CCara	re write the DPU/DRCU interface document in accordance with the agreement document appended to WE summit minutes	Urgent	For signing off at interface meeting 15/11/2000
AI-SYS-0523-9.	JD	draw up an official version of grounding diagram and circulate for approval	Urgent	For DRCU/FPU interface document 10/11/2000
AI-SYS-0523-10.	JJB	send sample of Cooner wire to RAL for EMC evaluation	High	For final definition of wiring harness 24/11/2000
AI-SYS-0523-11.	JD	co-ordinate drawing up of basic equivalent circuit for detector system	High	For EMC modelling Present at systems review 24/11/2000
AI-SYS-0523-12.	BMS/KJK	revise and formally issue DRCU simulator requirements	High	To allow specification to be written 10/11/2000
AI-SYS-0523-13.	H-G F	write DRCU Simulator Software Specification document	High	To allow start of software development cycle 24/11/2000
AI-SYS-0523-14.	PH	provide detailed electrical requirements for calibrators either in specification document or in electrical interface document	Urgent	To allow DRCU/FPU ICD to be finalised 15/11/2000
AI-SYS-0523-15.	BStobie	complete and issue BSM electrical interface document	Urgent	To allow MCU design to be finalised 10/11/2000
AI-SYS-0523-16.	JJB	answer the points raised in the WE summit minutes either in the detector specification document or an electrical interface document	Urgent	To allow DRCU/FPU ICD to be finalised 15/11/2000

AI-SYS-0523-17.	DF	complete and issue MCU design description document	Urgent	To finalise DPU/DRCU ICD 15/11/2000
AI-SYS-0523-18.	BMS/JD	review and comment on cooler drive electronics document	High	To allow DRCU/FPU ICD to be finalised 10/11/2000
AI-SYS-0523-19.	BMS	define required resolution on thermometry and redundancy philosophy and re-issue technical note	Urgent	Ditto 10/11/2000
AI-SYS-0523-20.	BMS	define redundancy requirements on optical encoder	High	To allow finalisation of MCU detailed design 10/11/2000
AI-SYS-0523-21.	System Team	determine whether it is necessary for any parameters to be included in both housekeeping and science telemetry streams	Urgent	May impact of hardware design 1st November 2000
AI-SYS-0523-22.	System Team	identify the required contents of each frame type	High	Needed for final definition of DRCU/DPU ICD 20 November 2000
AI-SYS-0523-23.	Di Giorgio	define the action taken by the OBS if the science data in a frame fails the check	Medium	To be presented at system review 20 November 2000
AI-SYS-0523-24.	System Team	define the required accuracy of the absolute time assignable to a data value	Urgent	Needed for hardware design 1 November 2000
AI-SYS-0523-25.	DF	propose a method for reporting the time of fringe crossing in the MCU science frames that minimises the data rate	High	To be presented at system review 20 November 2000
AI-SYS-0523-26.	CCara	provide in the DRCU-DPU ICD a place to hold the information relating to the time of data sampling relative to the science frame time	High	15th November 2000

DRCU Simulator Requirements
Notes for WE Summit 18/20 October 2000
Bruce Swinyard
Ken King

Scope:
A unit is required that will allow the DPU and OBS to be run and tested in the absence of the DRCU and the cold FPU units.

This unit is required by:

IFSI for initial acceptance testing of the DPU interfaces to s/c higher level protocol for each model
IFSI for initial acceptance testing of the On Board Software functionality for each model
RAL for integration and test of the instrument AIV facility using the DPU AVM
RAL for verification of the AVM
ESA for the AVM (deliverable item)
RAL for integration of the QM DPU into test facility
RAL for integration of the PFM into test facility

What will the users do with it:
At IFSI the DPU acceptance tests will be designed to test the specifications written out in the DPU Specification Document and the OBS URD which reflect the requirements written in the IRD (is this sufficient?). In outline the tests that require a DRCU simulator to be present are:

Test high-level interface protocol to S/C (PUS protocols etc)
Test high and low speed interfaces between DPU and DRCU – again both hardware and protocols as given in ICD
Static OBS Functionality – acceptance of commands; TM generation; OBS performance requirements
OBS Management functions – presumably as given in the DPU specification document.

We wish to discover from these tests whether the DPU/OBS can "run" the instrument in all its operating modes with the correct data collection; extraction of real time parameters (if necessary); algorithm execution and real time commanding and execution of a command queue from the S/C to simulate instrument operation – again with correct data collection; TM formatting and transmission to CDMS.

We need to test the response of the OBS/DPU to various failure conditions both in the DRCU (failure to initialize; PSU failure; interface failure etc) and within one of the sub-systems (loss of SMEC position sensor; loss of drive coils etc). We will also test the autonomy functions of the OBS – that is switching to SAFE mode in the event of DRCU/sub-system failure of OFF in the event of DPU failure. In testing the failure modes it is mandatory that the DRCU simulator will cause no failure propagation into the DPU or the 28 V supply.

On the QM and flight model we also need to test that the power consumption of the DPU is within tolerance for all operating conditions and that it meets the environment specification – EMC/EMI; Thermal Vac Test; Vibration test etc. What will be the test criteria? Do these tests need the DRCU simulator?

At RAL the DRCU Simulator plus the AVM DPU will be used to integrate the EGSE and calibration facility computers and to do end to end tests on the AIV Facility command and data handling systems. We will also test the EGSE autonomy procedures and the quick look analysis system. This implies the need for representative simulated data from the simulator for a number of instrument operating modes.

At RAL the AVM verification will be a repeat of a subset of the acceptance tests carried out at IFSI plus a test of running simulated instrument operations – again these tests need simulated science data sets.

At ESA the AVM will be used for testing the interface between the S/C and the instrument using the ESA provided CDMS simulator rather than the S/C simulator in the SPIRE EGSE. They will also use it to carry

out end to end testing of the CCE and they will use it to test all instrument autonomy functions. At ESA the DRCU simulator will derive its power from the ESA S/C simulator – this implies that the DRCU simulator must work over the specified voltage range of the primary 28V.

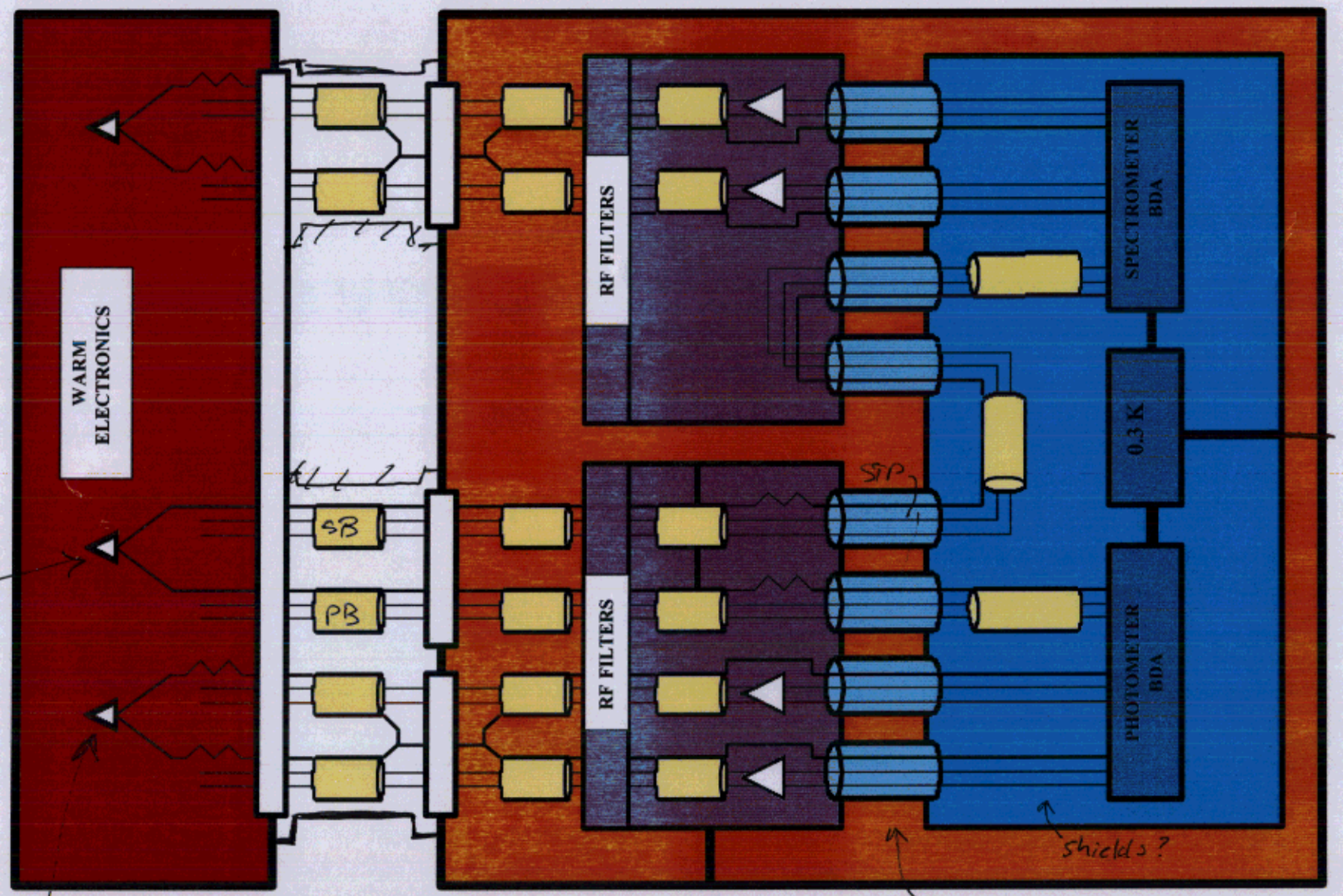
So what does it have to do:
From above the following capabilities are clearly needed:

1. Hardware to simulate the bi-directional command/HK serial link from DRCU to DPU
2. Hardware to simulate the three uni-directional high speed data links from the DRCU to DPU
3. Hardware/software to simulate the command handling within the DRCU
4. Hardware/software to simulate the data collection; formatting and transmission within the DRCU
5. Software to generate DRCU housekeeping (voltages; currents; temperatures etc)
6. Software to simulate the response of each sub-system in all(?) operating modes
7. Software to generate the DRCU "test" data sets
8. Simulation of fault conditions in the DRCU
9. Simulation of fault conditions within all or a sub-set of the sub-systems.
10. Simulation of DRCU start up procedure and acknowledgement to DPU
11. Software to generate simulated data representing selected operating modes of the instrument (Photometer chop; spectrometer; cooler recycle etc…)
12. Must be able to operate from 28 V supply within range specified for S/C primary bus voltage.

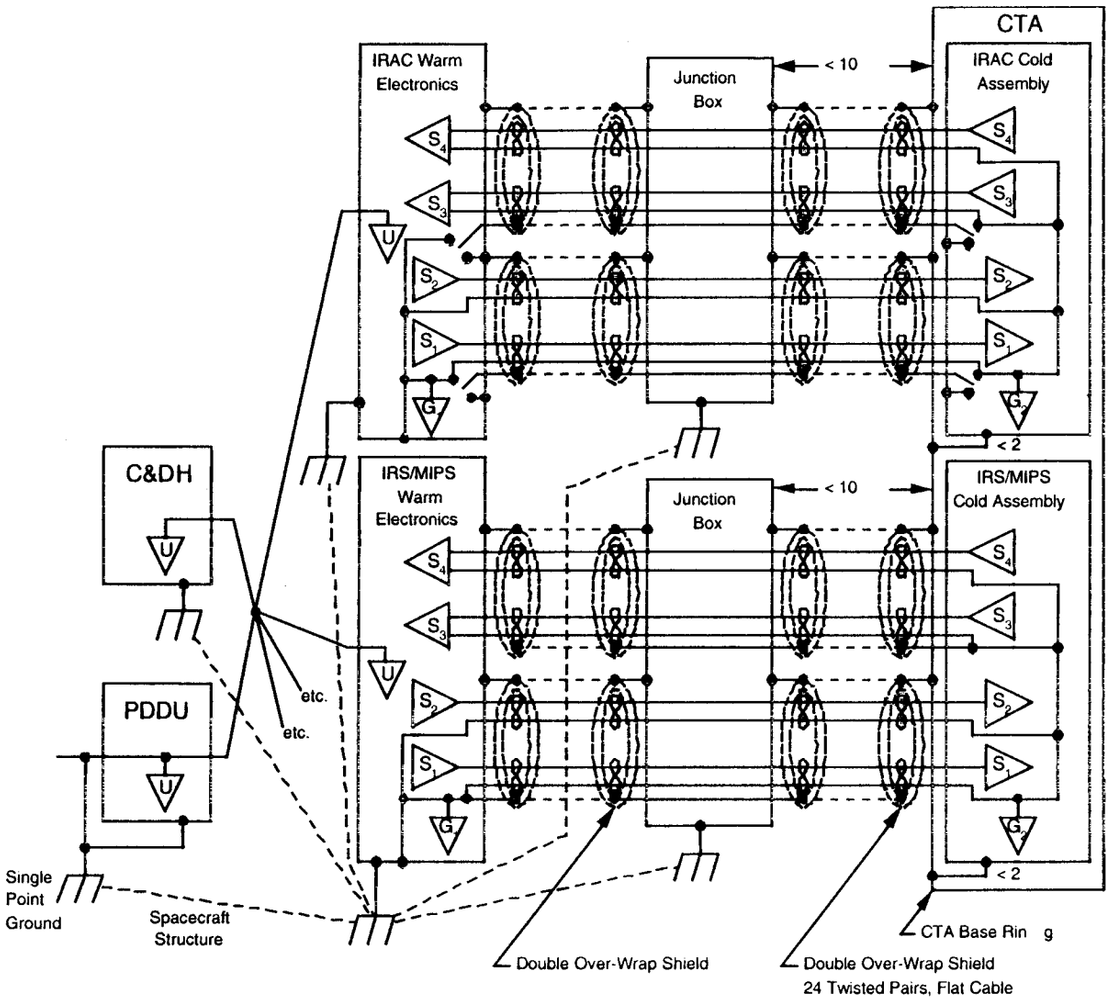
How many do we need:
Three: IFSI – RAL -ESA

When:
For IFSI – 1 June 2001 (!!!)
For RAL/AVM – 1 April 2002
For RAL/PFM – 1 January 2003

WESCOTT VIKTOR'S SCHEME



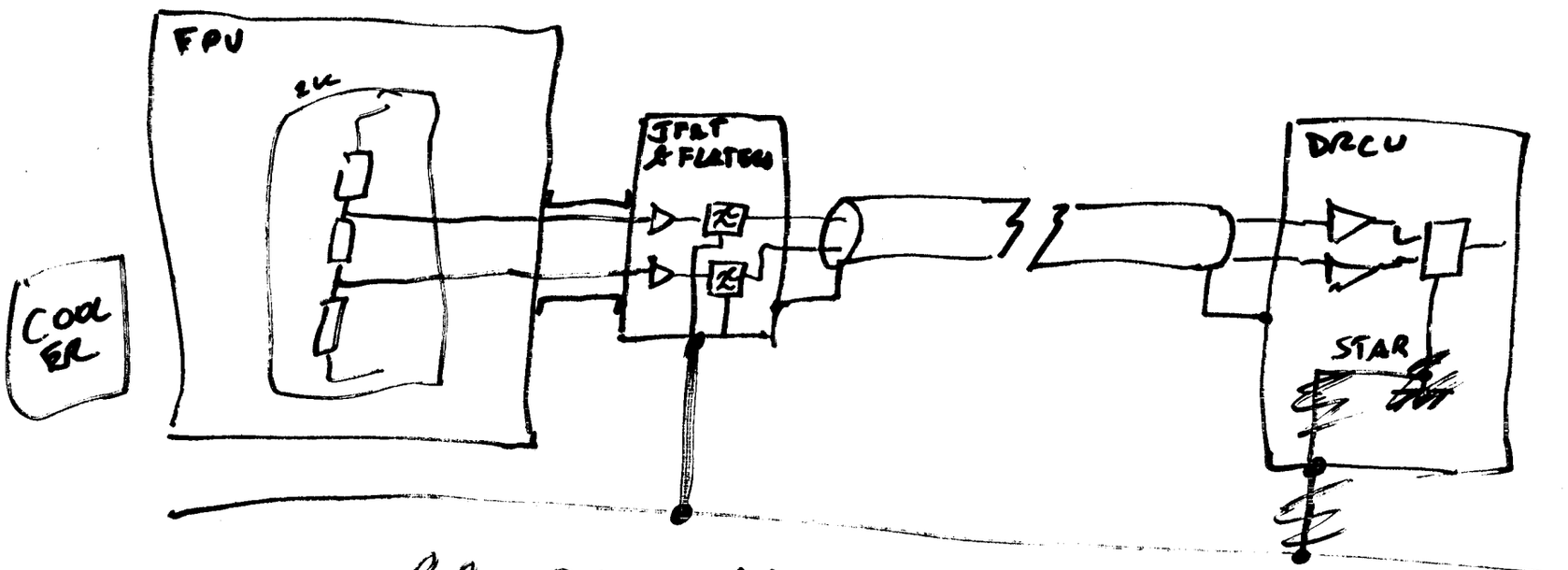
WE SUMMIT



SIRTF Grounding Scheme

WE SUMMIT COLIN'S VIEW

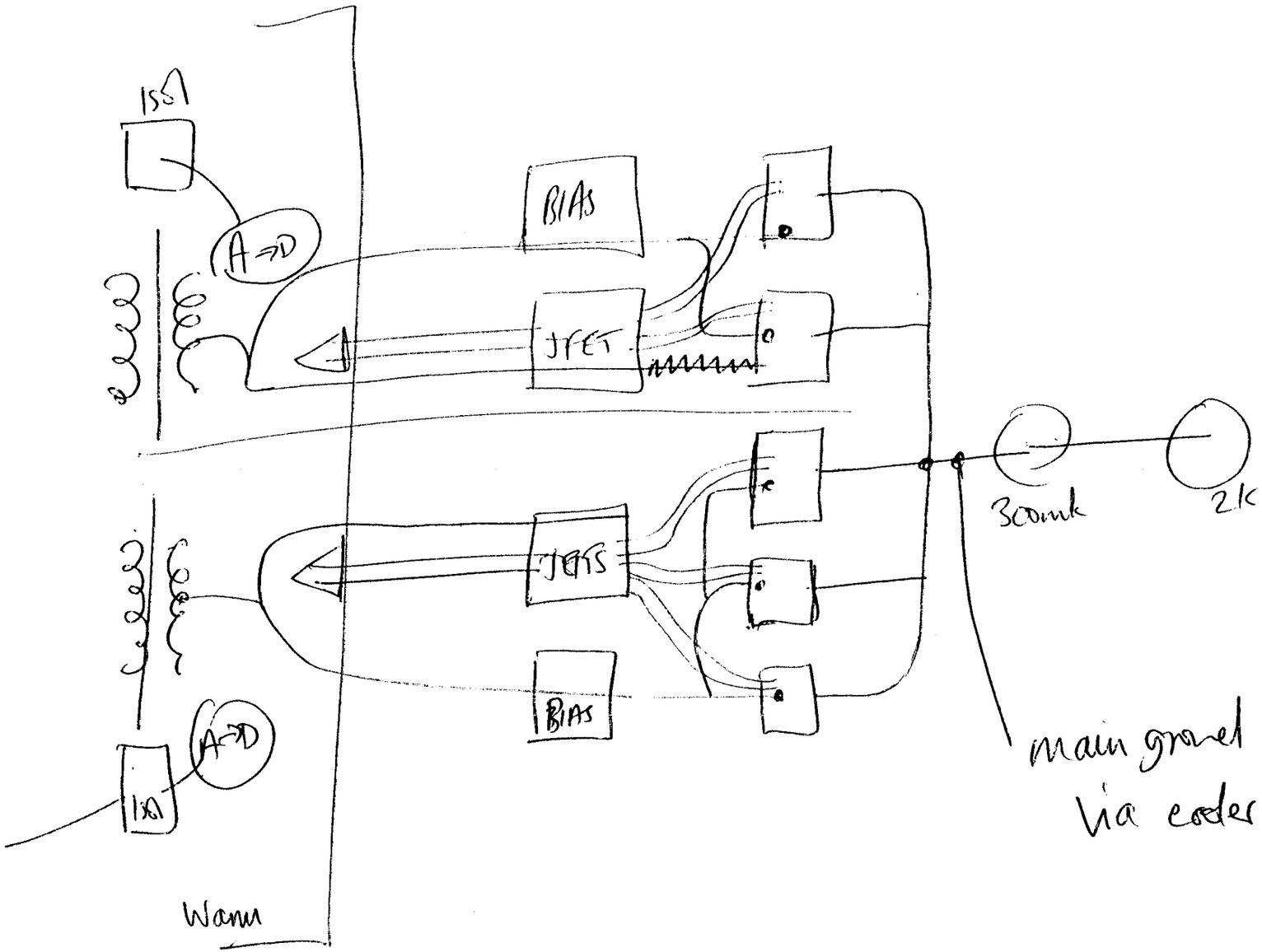
- FLOATING FPU BOX
- GROUNED THROUGH SHIELDS TO DRCU 'STAR'



PROBLEMS:

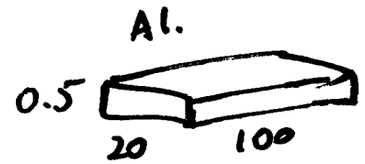
- RF FILTER RETURN CURRENTS
- ISOLATION OF FPU BOX & SHIELDS
- FPU 'GROUND MECCA' ?
- INDUCTANCE OF GROUND PATH FROM FPU

WE SUMMIT JOHN'S SCHEME



ISSUES: COLIN

- GROUND STRAP FOR FPU – NOT POSSIBLE!



~ 500mW 1.5→4K!

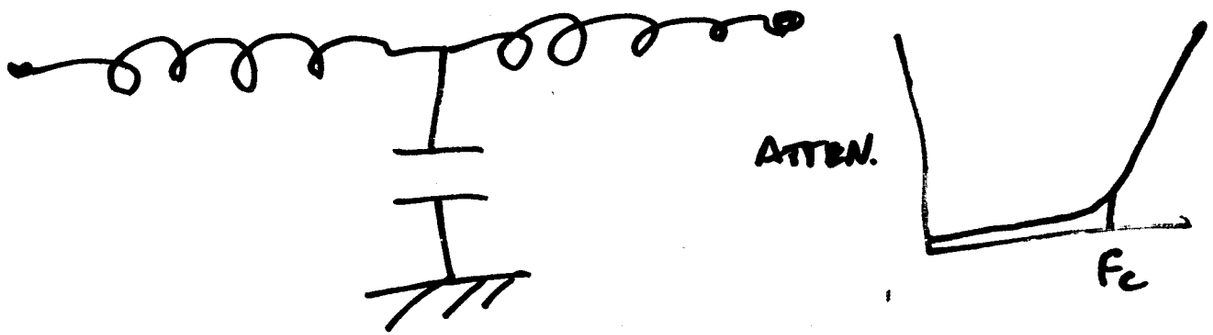
- MODELLING:
  - CONDUCTED RF – PSPICE
  - RADIATIVE RF – SLOTS, APERTURE VENTS
    – MODELLING HARD, MAY NOT BE REALISTIC

- SENSITIVITY OF BOLOMETERS?
  – TEST CONDUCTIVE RF SUSCEPTIBILITY
  ↳ SPEC FILTERS & BOX & SHIELDS

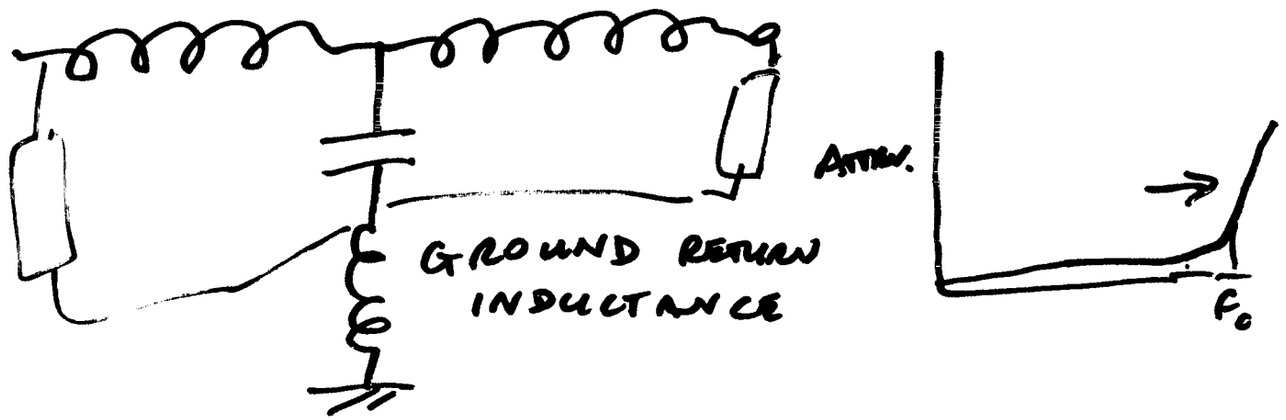
COLIN

RF FILTERS

IDEAL:



REAL:



SPIRE WE Meeting
October. 18-20, 2000 - RAL

MCU Preliminary Design

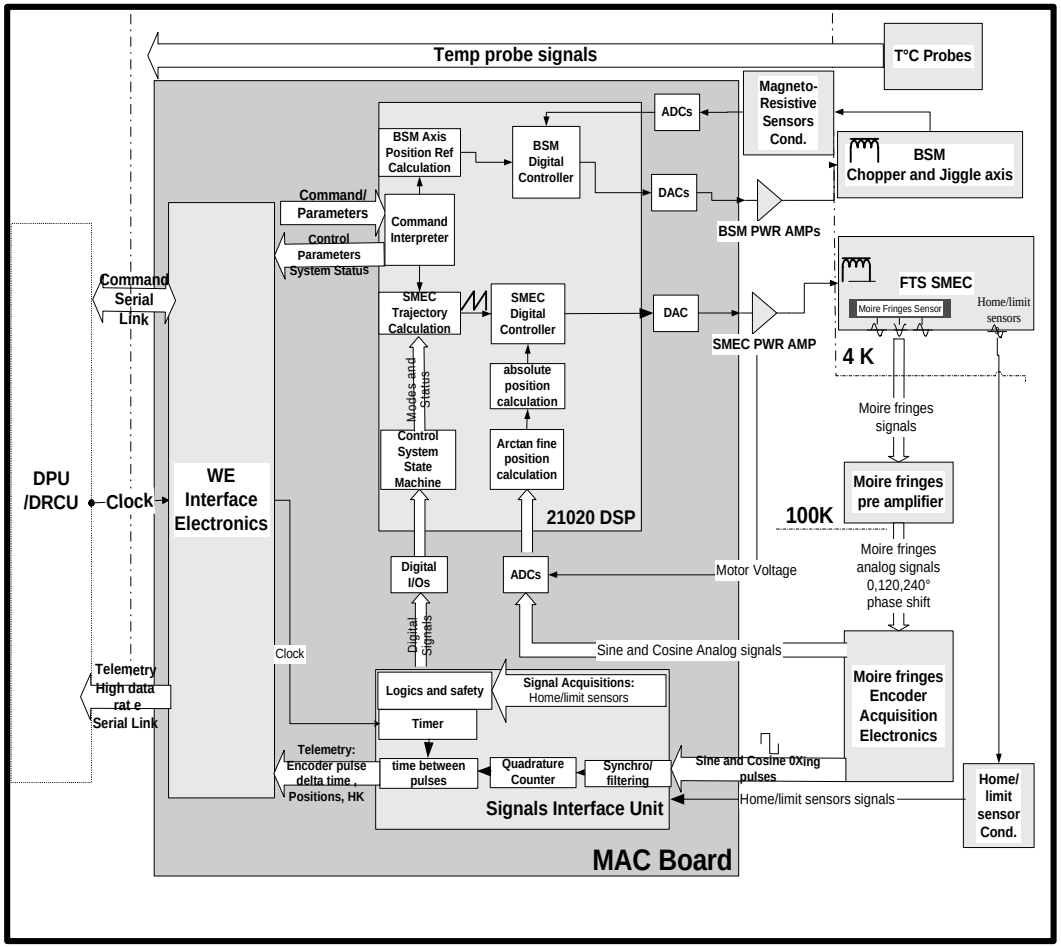
MCU FUNCTIONS

The MCU is dedicated to:

- the control of 3 axis of the SPIRE instrument:
  - the velocity scan (i.e. a position ramp) of the SMEC,
  - the position control of the 2 axis BSM subsystem (chopper and jiggle axis),
- provide H/K data of the 3 axis for telemetry and scientific interferogram calibration and detector synchronisation purpose.

MCU GENERAL ARCHITECTURE

- The MCU control electronics comprises a digital control board (MAC) based on a 21020 DSP associated with :
  - analog electronics for power amplification of the actuators
  - acquisition electronics for sensors preamplification and conditioning.
- The MAC Board is common for all axis, but the power and signal conditioning electronics are splitted according to the 2 BSM and SMEC subsystems.



MCU PRINCIPLE OF OPERATION

- **The trajectory control of the 3 axis is performed by the 21020 DSP on the basis of PID controllers + mechanical modes notch filters sampled @ 100 ms. Advanced control algorithms may be implemented on request instead of PIDs in case of optimal control needs.**
- **The MCU communication with DPU shall be done through 2 serial lines :**

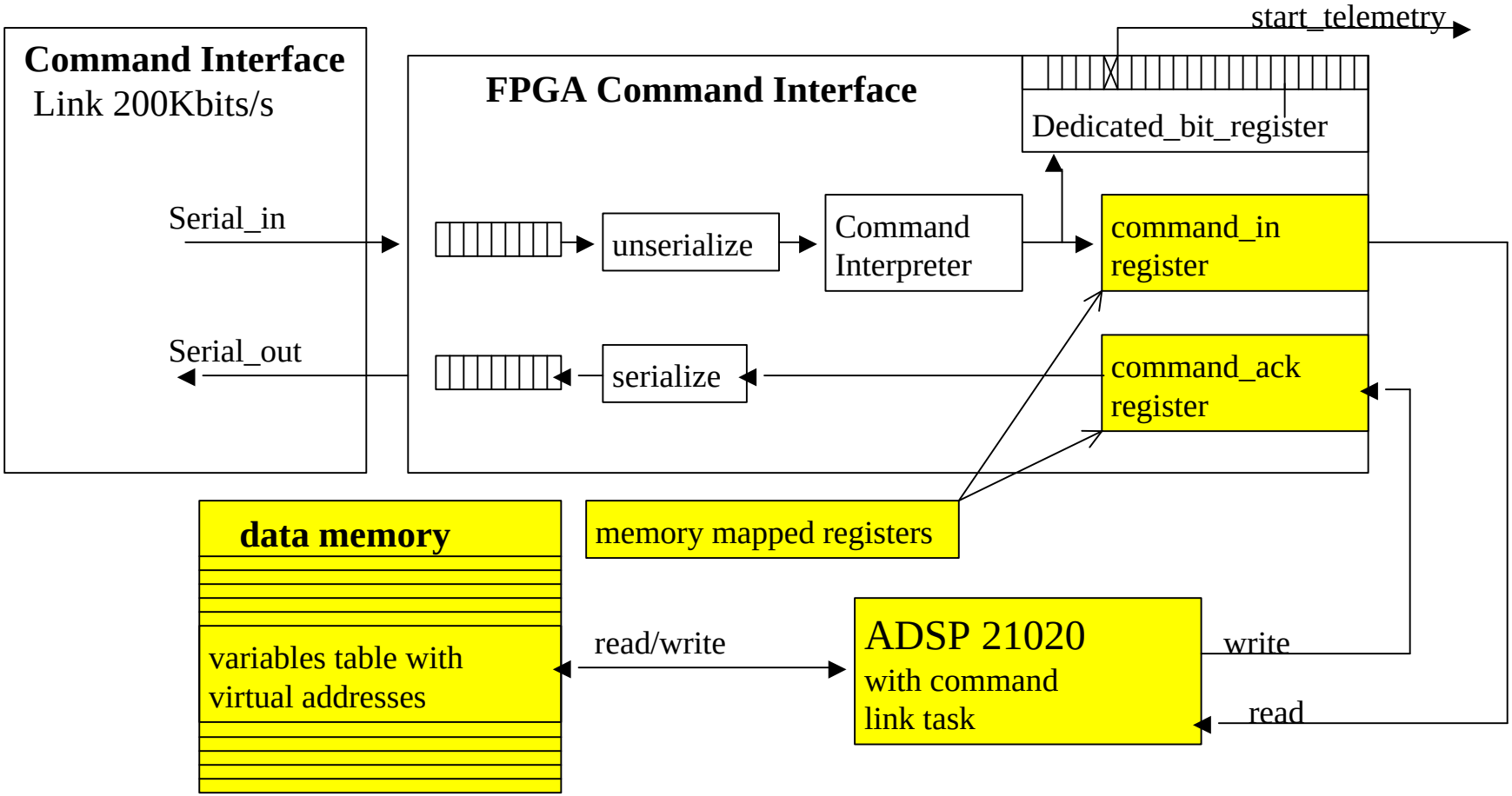
  - **Low rate command interface link 200 kbits, based on 32 Bits word. By mean of a FPGA dedicated to serial interface, the commands and parameters are de-serialised and put in an input register to be read by the 21020 DSP. A 32 bits word is then sent towards the DPU as acknowledge through an output register. This acknowledge may contain a requested parameter on a 'get' type command. The status is obtained by a ' get_status ' command.**

  - **High rate telemetry interface link 1Mbits, based on 16 bits words. Data may be provided in 32 bits format in two words. A FPGA is dedicated for this function, linked with the acquisition electronics:**

Low rate command interface

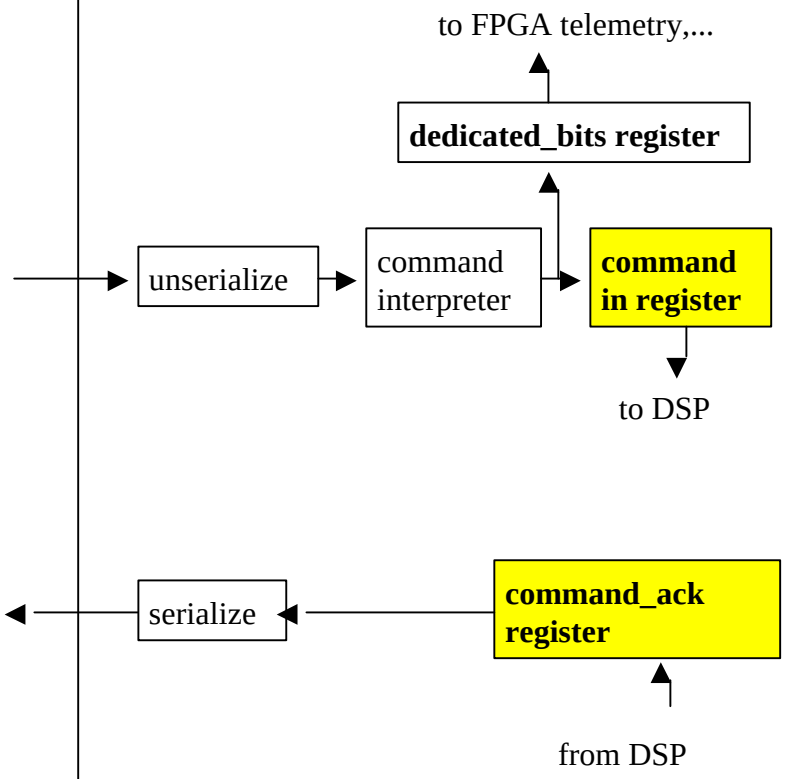
- **The MCU shall receive a 32 bits word for each command. The 32 bit word shall include (i) 2 or 3 bits for subsystem id (ii) 7/8 bits for command type (e.g. set scan_length), (iii) the rest for the parameter itself. There are 2 registers (for command receipt and command reply) in interface with MCU DSP.**
- **There is a specific broadcast @ a dedicated address.**
- **The MCU communication FPGA shall decode if the command concerns its subsystem, since all systems shall be adressed. In case of the specific command ' start telemetry ', a synchro signal is directly sent to the high rate communication FPGA without read out and interpretation from the DSP.**
- **The MCU Low rate serial line FPGA puts the parameter value after header decoding in a register. The DSP reads every cycle of the common time sharing monitoring of the 3 axis (ie 100 ms) the interface register and put in its own data memory the parameters according to a table pointer.**
- **For each command, a handshake is done with DPU, so that only one command can be sent at one time until the parameter of the control shall be taken into account (the communication philosophy is based on the fact that other SPIRE subsystem has no micro controller on board, and that the principles shall be as simple as possible and hardware oriented. Consequently, each command shal be interpreted with an acknowledge message before another possible command receipt, and then a FIFO interfacing the MCU communication system is not necessary).**
- **With this handshake, two commands can be sent in about 320 ms.**
- **The handshake shall consist of only one 32 bits word return.**
- **Since the DSP readout of the command is done periodically every 100 ms, the delay for a command to be taken into acount is between about 350 and 500 ms randomly.**

MCU/DPU communication hardware

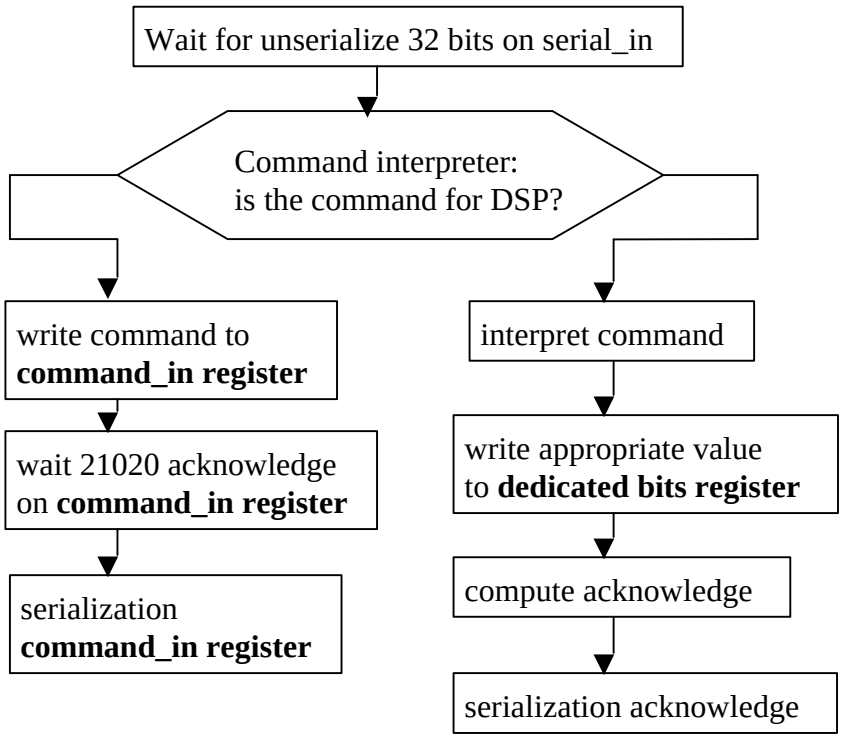


MCU/DPU communication FPGA Command Interface

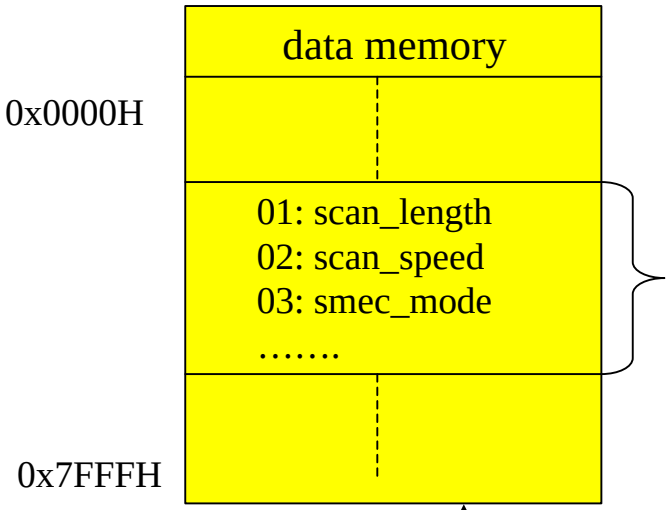
FPGA commmand interface:



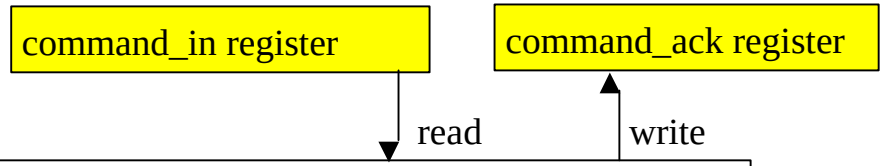
FPGA commmand interface state machine:



MCU/DPU communication:DSP 21020 command link task



Variables table: 01,02,…. are virtual addresses, independant of the data memory physical address. variables table are notified in program by:
.SEGMENT /DM dm_sram;
.VAR scan_length,scan_speed,smec_mode,…;
then we read or write in program by
f0=dm(scan_length); or *dm(smec_mode)=f1;*



command link task:

1) read command_in register if not empty (if empty, jump step 7)
2) decode virtual address (bits 28-22)
3) if bit 29=1 (« set »), then write parameter (bits 21-0) at virtual address
4) if bit 29=0 (« get »), then read parameter at virtual address
5) write acknowledge to command_ack register
6) end of command link task

High rate telemetry serial link

- **Some specific values such as position and motor current samples are delivered on a fast mono directional serial link to provide data for telemetry purpose (see following table).**
- **The telemetry shall use a 1Mbit/s 16 bits serial link but data on 32 bits (ie 2 succesive words).**
- **For the sharing of telemetry channel, we consider that :**
  - **there is only one common FPGA connected to one high rate serial link,**
  - **this FPGA shall have 3 communication mode :**
    - **Photometric mode : the telemetry data are the BSM axis without info on SMEC.**
    - **FTS scan mode : the telemetry data are the delta time SMEC position with some optional BSM information. In this mode, the BSM is static and the Scan is operating.**
    - **FTS Step and integrate mode where the 3 axis data are mixed.**
- **Nota:Technical data should not disturb scientific data => no specific technical mode BUT we use the complete available communication bandwidth (to be allocated in both nominal and burst rates)**

BSM and SMEC telemetry

Subsystem	Data	Photometer Mode	FTS Scan mode	Scan + Jiggle mode	FTS Step and integrate
SMEC	delta t between positions	not relevant	@500um/s deliver every 2 um: 250Hz= **4ms**	**Same as FTS Scan mode**	not relevant
	absolute position	not relevant	not relevant		Position step of 25 µm sampled @ 4ms during 1 sec
	motor current	not relevant	100 ms		each FTS step cycle
	Motor voltage	not relevant	not relevant		/
	DSP:Mean position error	not relevant	@ the end of each scan (max 0.5Hz in very low resolution mode)		each FTS step cycle
	DSP: Mean Speed	not relevant	id.		not relevant
Chopper	Chopper positions	every programmable N cycle*(N can be 0*): 100 positions sampled @ 1ms **and then** 10 points/cycle of 2Hz = 50ms **continuously**	/		
	Chopper Mean position	/ may be provided	@ the end of each FTS scan		
	Chopper Mean position error	/ may be provided	@ the end of each FTS scan		
	Chopper HK (current)	same rate as position	@ the end of each FTS scan		same as photo mode
Jiggle	Jiggle position	every programmable N cycle *(N can be 0*): 100 positions sampled @ 1ms **and then** 10 points/cycle of TBD Hz = TBD ms **continuously**	/		or Mean position only after each cycle ?
	DSP:Mean Jiggle position	@ each chopper cycle = 500 ms	@ the end of each scan (max 0.5Hz)		
	DSP:Mean Jiggle position error	@ each chopper cycle = 500 ms	@ the end of each scan (max 0.5Hz)		
	Jiggle HK	same rate as position	@ the end of each FTS scan		

SMEC Control System Functional requirements (1)

Description	Value	Justification vs. System Level requirements and assumptions	Design Status
Maximum mirror travel wrt ZPD position	– 0.3 to +3.2 cm	Total OPD Required: 14 cm Folding factor: 4 Single sided interferograms Short travel beyond zero path difference for phase correction: -0.3 cm	**OK** The total travel shall include an additional range for trajectory transcient (about 1 mm)
Minimum step size	5 μm 7.5 μm	Band A (equiv. to 20 μm OPD) Band B (equiv. to 30 μm OPD)	**OK** The encoder signals provide 2 μm position resolution
Maximum Step control	50 μm	The step size must be variable between 5 and 50 μm	**OK**
Fly back	1/10 of the scan total cycle max	'fly back' facility must be included to allow the mirrors to be placed rapidly at any arbitrary point in the scan range	Flyback speed: **OK** Flexibility of the starting point: **OK**

Subsystem Requirements: Functional requirements (2)

Description	Value	Justification vs. System Level requirements and assumptions	Design Status
Max/Min Mirror velocity:	0.1/0.01 cm s^{-1}	For assumed detector response Rate of change of OPD: 0.2 cm s^{-1}	**OK**
Velocity stability	10 μm/s rms after detector filtering		**OK** depending on the external disturbances level (<10mg)
Position measurement accuracy	0.1 μm for a range < 3mm 1 μm then (TBC)	Required OPD position accuracy is 1/50 of the smallest step size. Simulation confirms that this adds minimal system noise to the resultant interferogram	**OK**
Sampling frequency	80 Hz	The position is sampled at the frequency required for Band A – i.e.(mirror velocity)/(step size Band A)	**OK** The time tagged positions can be sampled at 250 hz provide 2μm resolution

SMEC Operation modes

Mode	Switching Event	Related functions
Off		The power is off. No function available
On	Power on	The set of boards (main or redundant) board is powered, The software is downloaded from Prom memory to SRam memory The software is initialized after reset.
Ready/Stand by	End of automatic boot	The communication is available. The status of the system is available. The control loops are opened with a DAC command forced to 0 on actuators.
Initialize	Init command	The loop is closed. The mechanism searchs for limit switches and then is initialized at home position, waiting for a scan start-up
Scan	Scan configuration and start command	Automatic scan including flyback according to the set-up. **Scan mode**:the motion can asymetrical with flyback or symetrical **Step mode**: position step on request **Open loop** mode: ramp without encoder nor back emf **Degraded closed loop** using back emf without encoder

Constraints requirements

Description	Justification	Inst. Req. Ref.	Design Status
It shall be possible to break all control loops implemented in hardware. This will allow the control of the loop through the on board computer (this may be a degraded mode of operation)	/	IRD-REL-R02	**OK**
Backup modes of operation should be available for all nominal observing modes	/	IRD-REL-R03	**OK** the backup modes are: - speed control using the velocity feedback on the motor - current control using the PWR amplifer with the acquisition of motor current

As far as possible all control loops shall be implemented through the on board software. *I.e. the on board computer (SPU or DPU) shall be in control of the loop*	Flexibility	IRD-REL-R01	**OK**
The electronics shall be the same for 300 K and 4K	Same conditions during calibration and tests	TBD	**Not completely** in the case of the motor emf speed feedback due to the variation of the motor resistance between 300K and 4K
The reliability shall be consistent with the 4.5 year mission length	/	TBD	**TBD** 2 redundant boards, 2 coils, 2 optical encoder heads + reliability analysis to be done.

WE Subsystem I/Fs Requirements

System	Subsystem	Item	Req.Value	Design Status
WE Cabinet interface	Electronic Board	Dimensions	TBD	4 Double Europe size Board
DPU interface	**fully compatible with normalized WE interfaces**			**OK** Shall be complient with DRCU Requirements
	Bidirect. Low rate Serial link	Max data flow	TBD	
	Mono dir High rate serial link	Max data flow	1 word/ms (TBC)	
		Data format	2 words of 16 bits TBC	
	Synch. Link	Max data flow	TBD	
		Sync. Accuracy	TBD	
	Grounding	Network Conf.	TBD	
FTS Cryo interface	Motor	Max current (4K)	< 8 mA max (EID)	OK
		Max current (300K)	TBD	the motor is driven on current reference; no impact due to motor resistance variation but the motor power voltage depends on the harness equivalent resistance and the related voltage drop in cabling.
	Incremental encoder	preampifier signals levels	100 µA TBC	Could have to be placed as near as possible to the encoder optical head (i.e 100K)
	Harness	Length	5 to 10 meters **Need to know the equivalent resistance through the whole length @various temp**	Due to geometry
		Material	TBD..	SS or Cst TBC
		Thermal dissipation	<< 10mW total allocation for FTS	OK
Space environment at L2 Orbit	FTS WE	Total Dose	12 krad (2MM AL) IID-A	TBD
		SEU	free	**OK** (the FPGA 1440A used for the logics is RT)
		SEU Immunity	30 MeV/mg/cm^2	as a goal less than 1 logical error/24H (TBC)

SMEC Command list

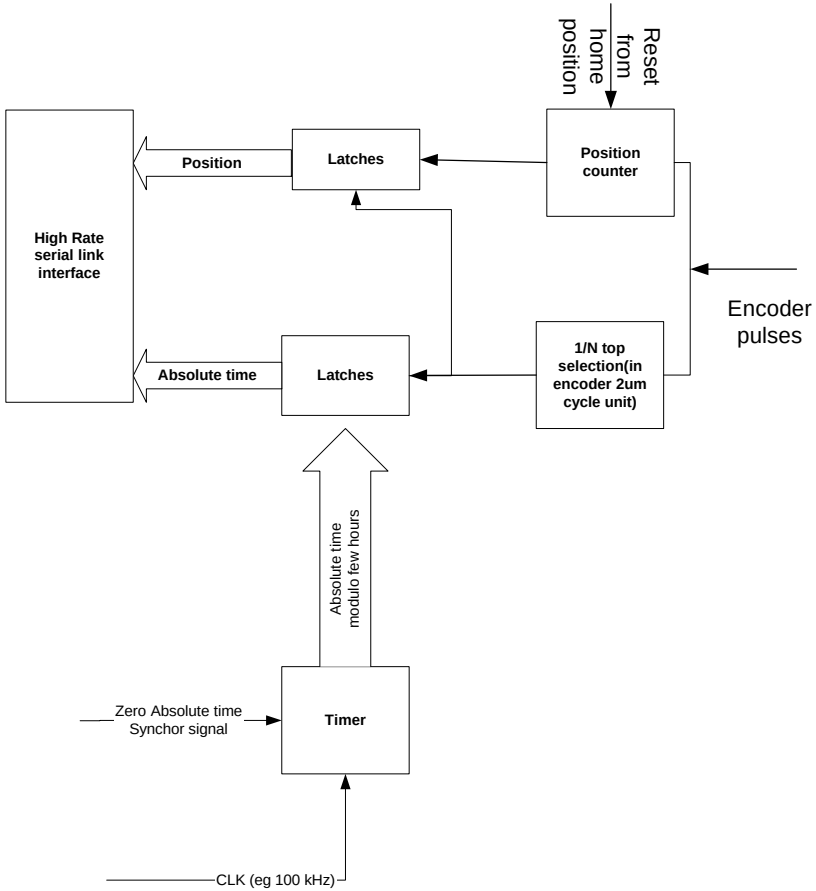
A command is a 32 bits word with the following allocation:

Bits 31-30	Bits 29-22	Bits 21-0
MCU header	Command type	Parameter

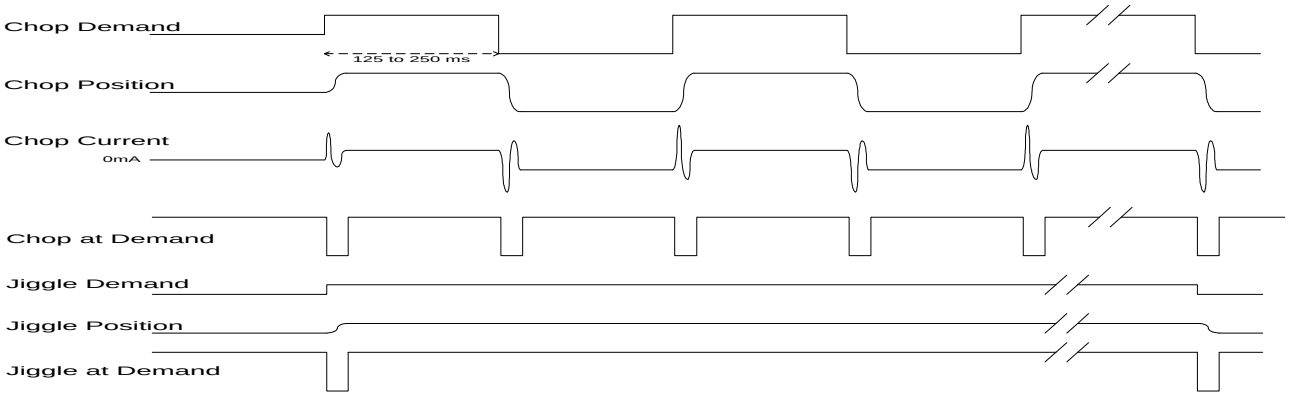
Command type	Parameter spec	Action
set_scan_length **get_scan_length**	B0-B21: scan length	Load / update a table defining a spectrometer scan. The scan is defined as a start position, ie a number of position sensor fringes move
set_scan_speed_ref	B0-21: scan speed if value=0 the servo is in position mode.	Load the desired speed of the control
get_scan_speed_ref	B0-21: actual scan speed reference	Readout of the last speed reference load
get_scan_mean_speed	B0-B21: actual scan mean measured speed	Allows to verify the velocity scan error
set_SMEC_mode	SMEC Mode definition: B0: start/stop B1-B3: control mode: - open loop, - closed loop with encoder, - closed loop with back EMF	Start/stop a spectrometer scan measurement in a specific mode.
get_SMEC_mode	B0-B3: idem set_SMEC_mode B4-B21: error/internal mode status	The error / internal mode status word allows the DPU to identify problems
set_SMEC_pos	B0-B21: position reference from the home position	Moves the SMEC by a step by step way. Unit= 1 um Range: 5.5 cm: 55000 values
get_SMEC_pos	B0-B21: actual position from the home position	Allows the measurement of a position step by step. Usefull for engineering mode to get position for step response.
start_telemetry	1 dedicated bit	Starts the telemetry on synchronized signal
set_telemetry_mode	B0: jiggle or smec scan telemetry B1-B8: telemetry data mux selection B9-B12: number of encoder zero crossing to be sampled B13-B21: length of telemetry sample	Configure the telemetry FPGA mode and select dedicated I/O to be transfered

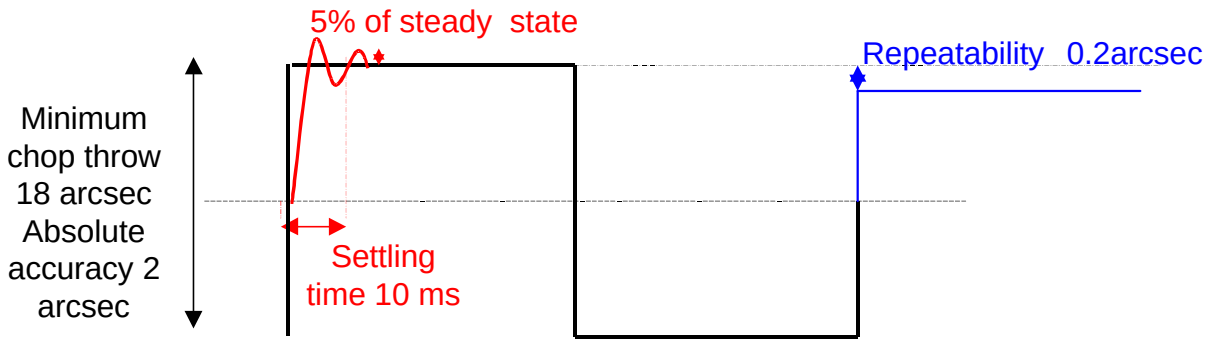
SMEC Synchro with DPU

- **The measurement of the delta time elapsed between 2 or more encoder zero crossing may start on the receipt of a specific synchronization signal**.
- This synchro signal reset the internal timer of the delta time count in the Encoder Interface Unit FPGA.
- Since that the first delta time value provided to telemetry is representative of the time delay between the synchro signal provided by the DPU/DRCU and the first optical encoder pulse of the scientific scan.



BSM CONTROL SYSTEM





BSM Operation modes

- **Off**
- **On**
  - **On axis in Chop (z) at angle q_c=0**
  - **On axis in Jiggle (y) at angle q_j=0**
  - **Moving to position (q_c ,q_j)**
  - **Holding in position (q_c ,q_j)**

- **TBC modes - which could be all software driven by master controller, by sending stream of positions to BSM controller**
  - **Chopping on z axis**
  - **Jiggling on z axis**
  - **Jiggling on y axis**

BSM Command list

- **Chop axis** :
  - Set point
  - Proportional Term
  - Integral Term
  - Derivative Term
  - TBC : Waveform : 1024 points - default is to drive by a series of set point commands from the DPU processor

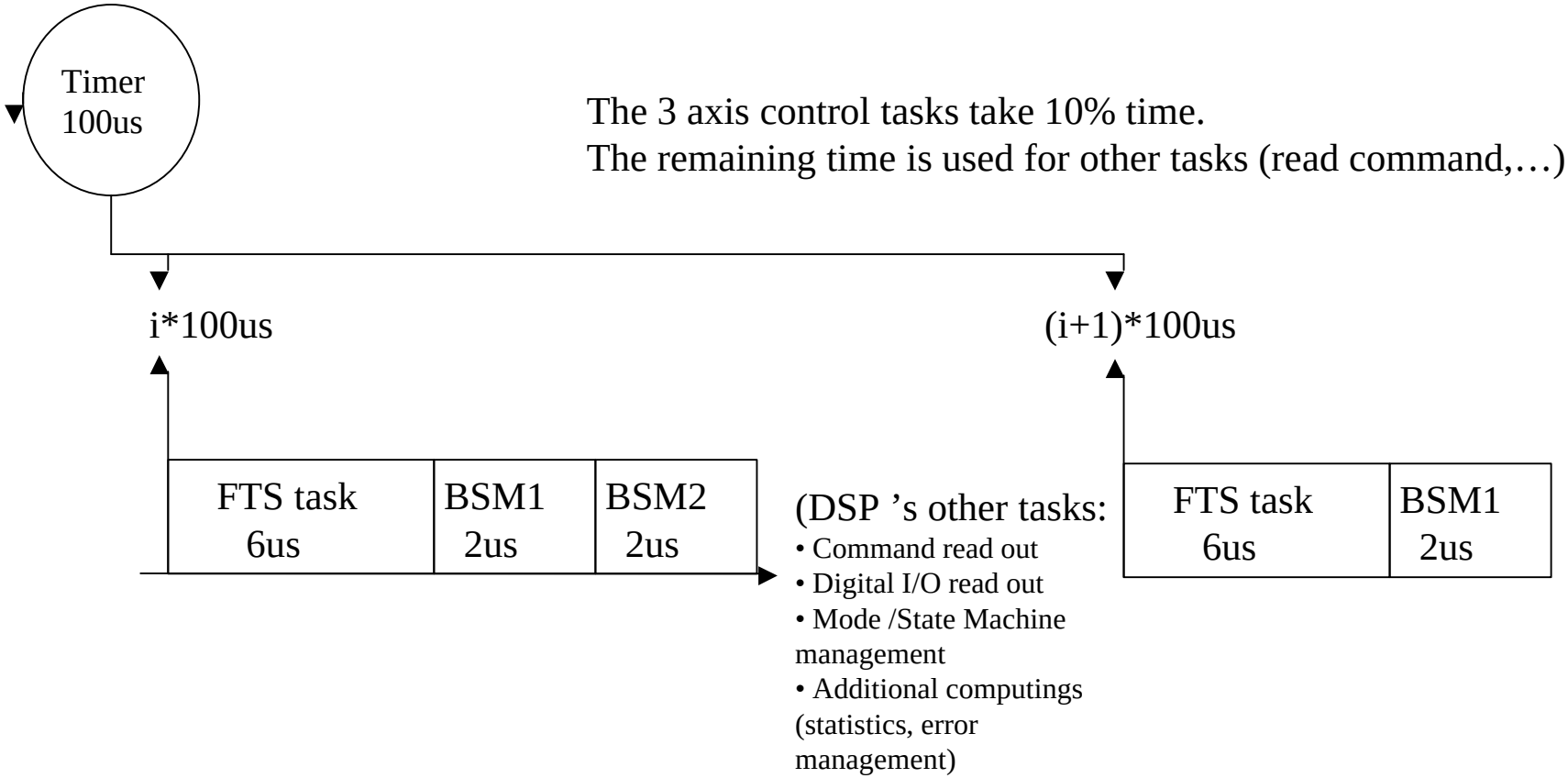
- **Jiggle axis** :
  - Set point
  - Proportional Term
  - Integral Term
  - Derivative Term
  - TBC : Waveform : 1024 points - default as above

- **Status Parameters**
  - Chop axis position
  - Chop axis motor current
  - Chop axis position error
  - Chop axis moving flag
  - Jiggle axis position
  - Jiggle axis motor current
  - Jiggle axis position error
  - Jiggle axis moving flag

MCU 21020 DSP Software principles

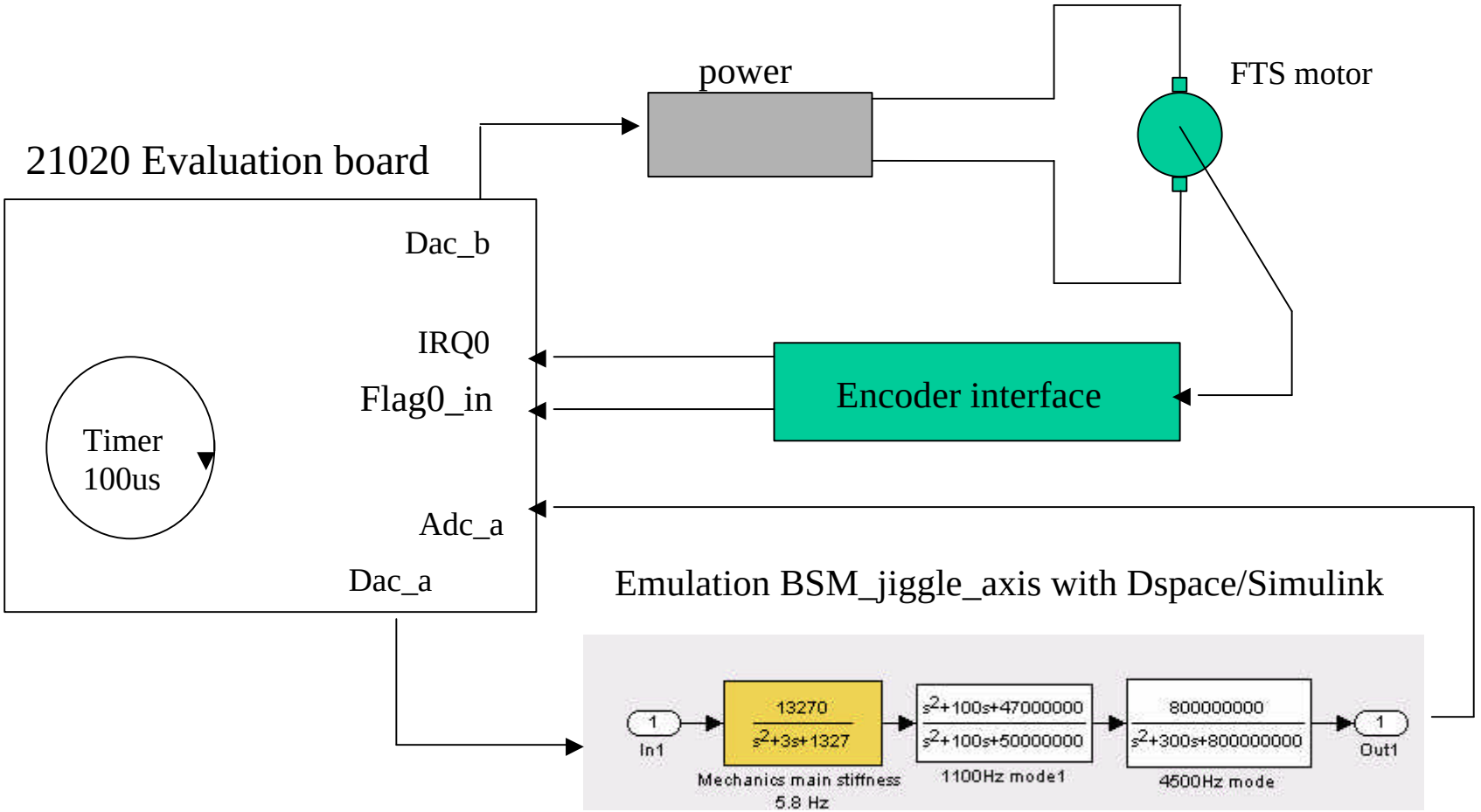
- The DSP software shall be written in 21020 assembly language without the use of a specific off-the-shelf real time operating kernel. The main tasks to be realized shall be called by a Master scheduler which is a routine interrupted by a software interrupt generated by the inner timer of the DSP.
- Mainly, the software shall not use other interrupt, excepted for the the following functions :
    - watchdog interrupt to recover from a loss of control of the DSP,
    - interrupt from a specific command from FPGA in case of emergency.
- Code uploading in the DSP is not foressen, the DSP beeing only used for control, in substitution of analogue electronics, with very poor load regarding communication / command interpreter. Code uploading would imply a very heavy software management task.

3 axis control : Mac Master Scheduler



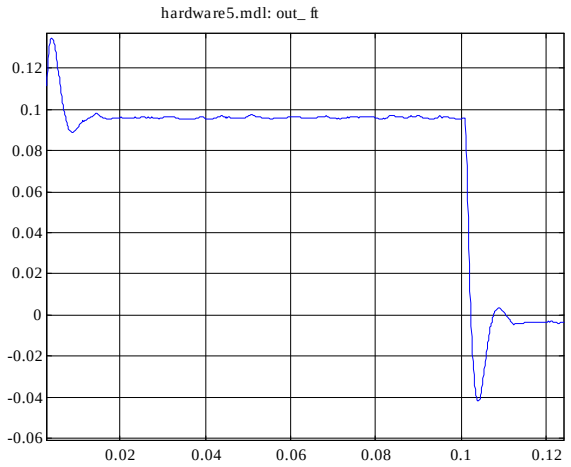
The 3 axis control tasks take 10% time.
The remaining time is used for other tasks (read command,…)

3 axis control : Evaluation of 21020 DSP Benchmarks



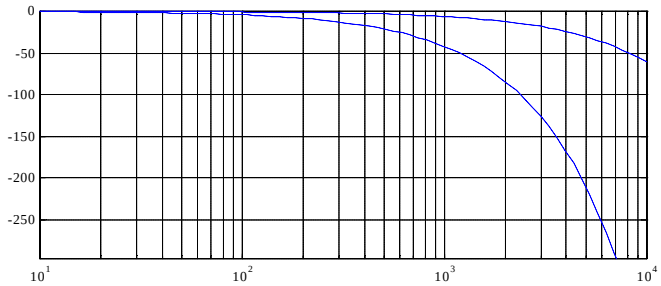
3 axis control : measurement on BSM jiggle axis emulation

- Step response



Without notches filter

- It 's difficult to implement BSM notch filters (1100Hz,4500Hz) because of DACs and ADCs pure delays (settling time)
- pure delays MAC board for BSM = 17us
- phasis fall for pur delay:



17us: 7° for 1KHz, 30° for 4KHz
100us: 40° for 1KHz,170° for 4KHz

3 axis control : CPU bench mark

Wide use of:
multiply + addition + fetch data in memory data + fetch data in memory program
4 instructions in one cycle

2nd order filter, PID: 6 cycles = 300ns

FTS Task: 6us

BSM_Jiggle_axis task:2us

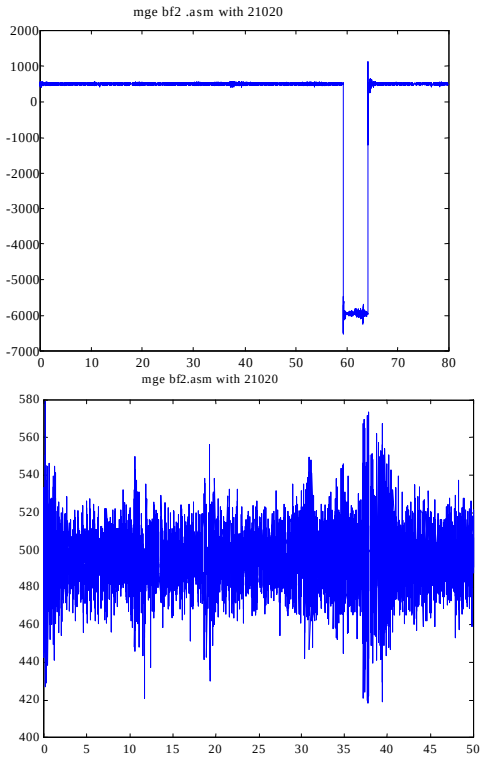
BSM_Chopper_axis task:2us

- 2nd order Filter routine

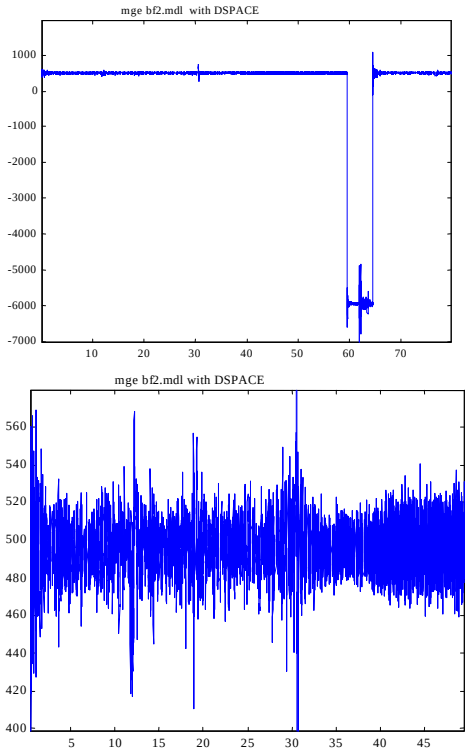
```
IIR2_Control:b1=b0;                                          /* #0 */
    f12=f12-f12,        f2=dm(i0,m1), f4=pm(i8,m8);          /* #1 */
    f12=f2*f4, f8=f8+f12, f3=dm(i0,m1), f4=pm(i8,m8);        /* #2 */
    f12=f3*f4, f8=f8+f12, dm(i1,m1)=f3, f4=pm(i8,m8);        /* #3 */
    f12=f2*f4, f8=f8+f12,           f4=pm(i8,m8);            /* #4 */
    f12=f3*f4, f8=f8+f12, dm(i1,m1)=f8 ;                     /* #5 */
  rts (db),     f8=f8+f12;                                   /* #6 */
  nop;
  nop;
```

3 axis control : Comparison measurement on GSFC speed filtered

- With Control from 21020 Evaluation Board

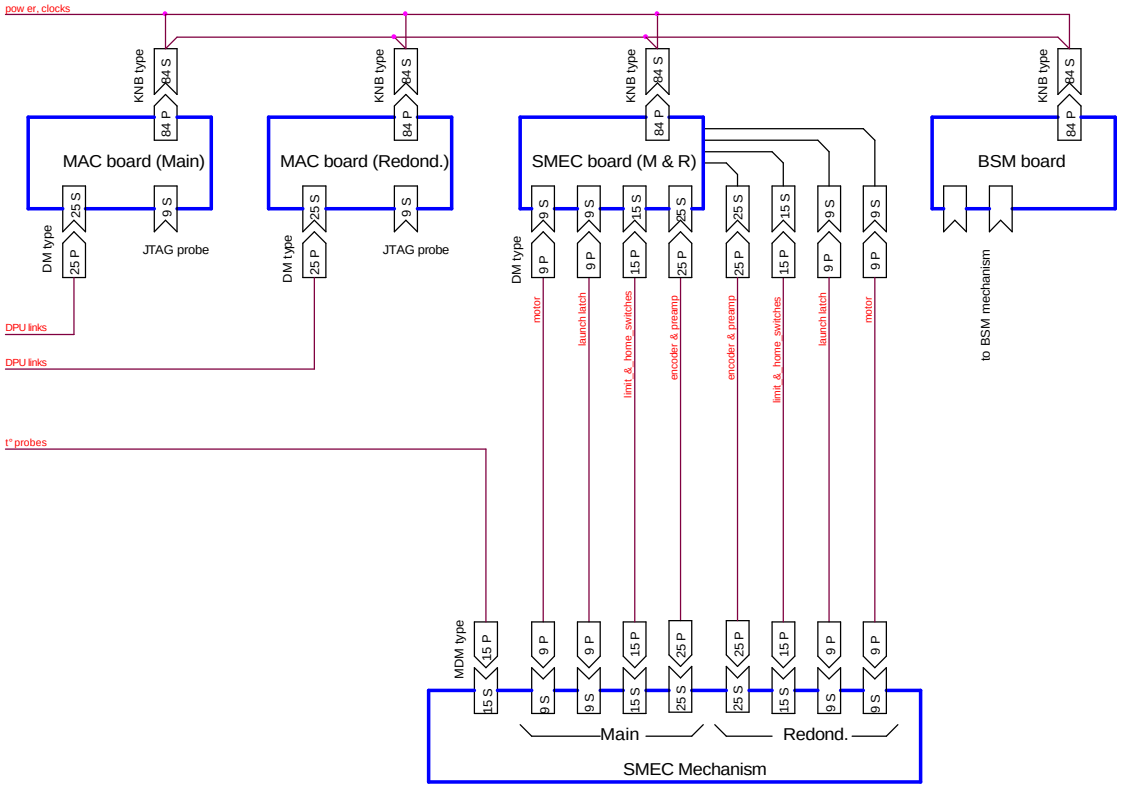


- With control from Dspace system



MCU ELECTRONICS overall architecture

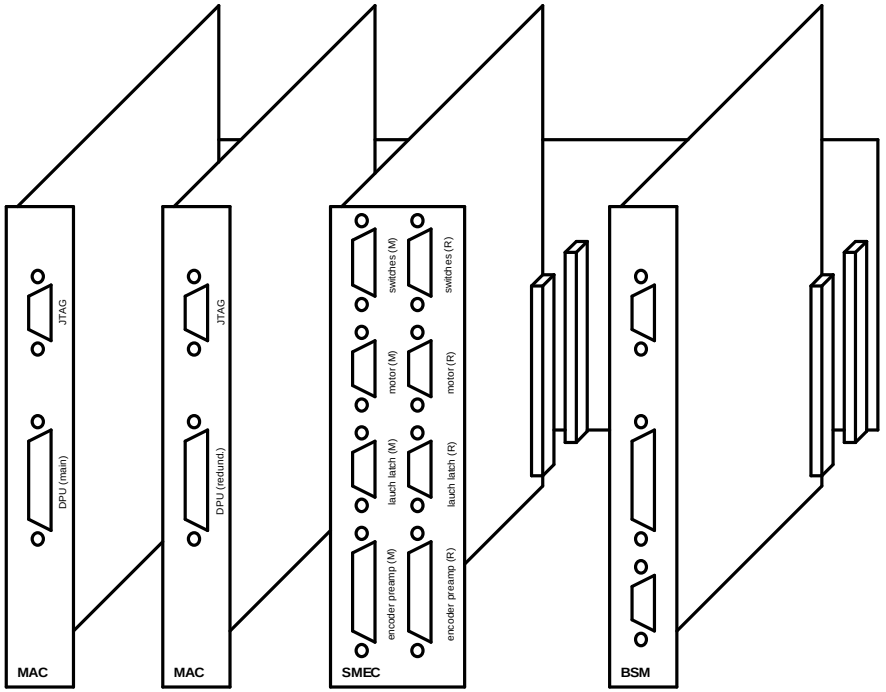
Backplane and connectors: are there imposed by Sap ? If yes what are the requirements ?



Laboratoire d'Astrophysique de Marseille		
Title: SPIRE/FTS - INTERCONNECTION DIAGRAM		
Size: A4	Document Number: LAM/ELE/FTS/GEN/00-06	Rev: 1.3
Date: 09-05-00	Sheet 1 of 1	

MCU MECHANICAL IMPLEMENTATION

- SMEC WE includes :
  - 2 Multi Axes Controllers (MAC) boards,
  - 1 SMEC board.
  - 1 BSM Board
- The 2 MAC boards, SMEC board and BSM board are plugged on the same mother board.
- Dimensions of the MAC and SMEC boards are 160 x 233.35 mm².



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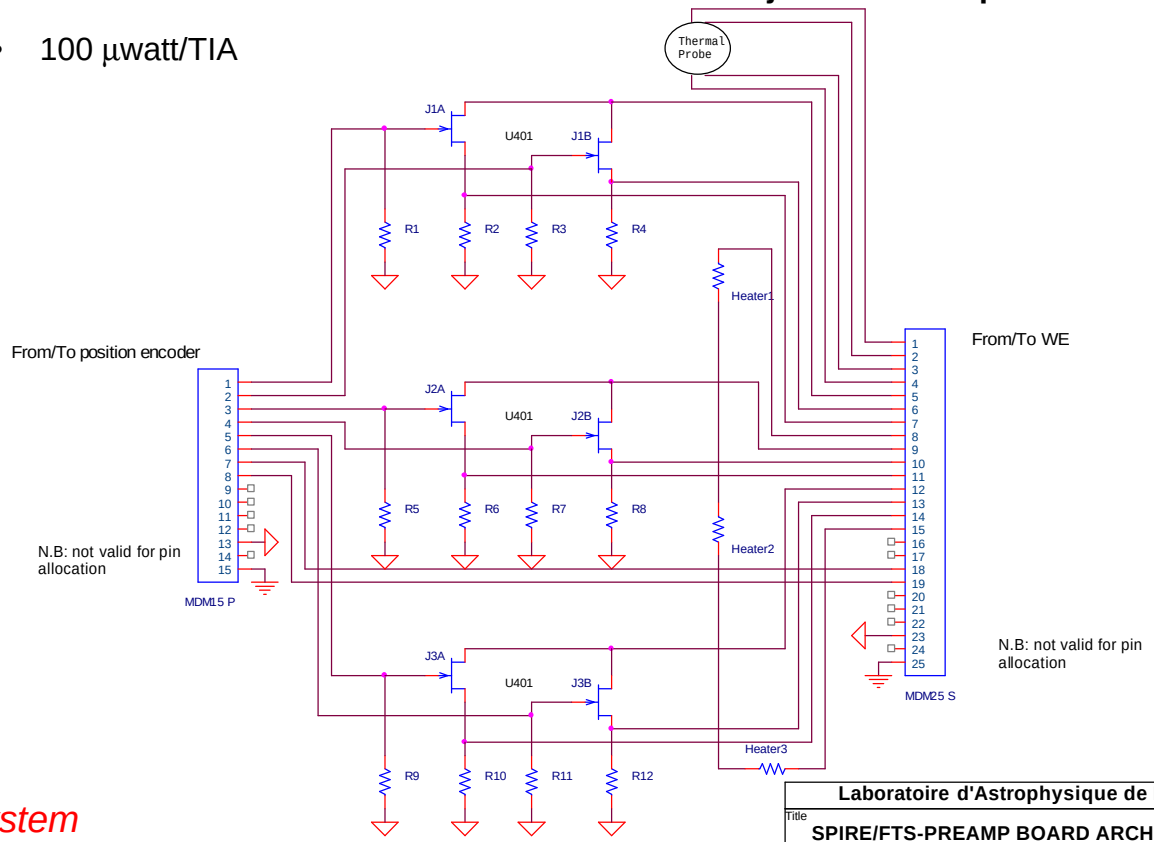
Title: SPIRE/FTS - MECHANICAL CRATE		
Size: A4	Document Number: LAM/ELE/FTS/GEN/00-08	Rev: 1.1
Date: 21-04-00	Sheet 1 of 1	

Position encoder preamp box

- The preamplifier box include the two preamplifiers for main and redundant channels. It is located in the SMEC mechanism, near the position encoder heads.
- 3 TIA (IRLAB Components) with inner thermal regulation (+ 3 redundant)
- **PB: Needs 20 mn to rize from 4K to 100 K => Major issue for operations**
- 100 µwatt/TIA



Laboratoire d'Astrophysique de Marseille		
Title: SPIRE/FTS-PREAMP BOARD ARCHITECTURE		
Size: A4	Document Number: LAM/ELE/FTS/AMP/00-05	Rev: 1.0

Mass (boards only)

Subsystem	Number	Nominal mass / unit (g)	Margin / unit (g)	Dispersion / unit (g)	Total max. mass (g)	Remarks
MAC module board	2	380	76	9	930	TBC
MAC module mechanical and thermal parts	2	TBD			TBD	
SMEC module board	1	420	84	10	514	TBC
SMEC module mechanical and thermal parts	1	TBD			TBD	
preamplifier board	2	40	8	1	98	TBC
TOTAL					**TBD**	

Power

Subsystem	Voltage	Average power	Peak power / time	Average / peak current	Voltage stability (including the drop in the lines)	Remarks
MAC board DSP and logic	+ 5 V	8000 mW (TBC)	13500 mW (TBC) t = 100 ms (TBC)	1.6 A / 2.7 A (TBC)	+/- 2.5%	• power peak happens during parameter change in EEPROM
MAC board analogue & data converters	± 15 V	2500 mW	2500 mW	90 mA on + 15 V 77 mA on – 15 V	+/- 2.5%	
SMEC board PWR Amplifier	+/-8 V (TBC)	80 mW on + 8V or 80 mW on - 8V (TBC)	800 mW on + 8V or 800 mW on - 8V t < 100 ms	10 mA 100 mA max (TBC)	+/- 5%	• voltage value depends of motor harness resistance at 300 K • power peak happens during acceleration of the mirror.
SMEC board analogue electronics	± 15 V	1500 mW	-	50 mA on + 15 V 50 mA on – 15 V	+/- 2.5%	
TOTAL		12080 mW	17500 mW			• power peaks on SMEC and MAC boards are nether at the same time.

MCU/SMEC Interfaces

I/F	Type	Nb. of cond.	I/O	Value	Constraints
Linear Motor Coil	analogue current	2	out	100 mA max. (TBC)	20 Ω load for total resistance harness as a maximal value for power dissipation
Optical Encoder	Sinusoidal low level signals provided and preamplified by 3 photodiodes delivering moire fringes signals	6	in	5 µA peak (TBC)	distance from position encoder to preamplifier as short as possible.
	analogue current delivered to LED	2	out	0.5 mA DC (TBC)	
	analogue current delivered to preamplifier	2	out	0.2 mA DC (TBC)	
	analogue current delivered to t° probe	2	out	10 µA DC (TBC)	
	analogue t° signals provided by t° probe	2	in	TBD mV	
	analogue current delivered to heater	2 (TBC)	out	0.5 mA peak (TBC)	
Home and Limit Position magnetoresistive sensors	analogue current delivered to resistors bridge	2 x 3 switches	out	0.5 mA (TBC)	
	analogue voltage delivered by resistors bridge	2 x 3 switches	in	TBD mV	

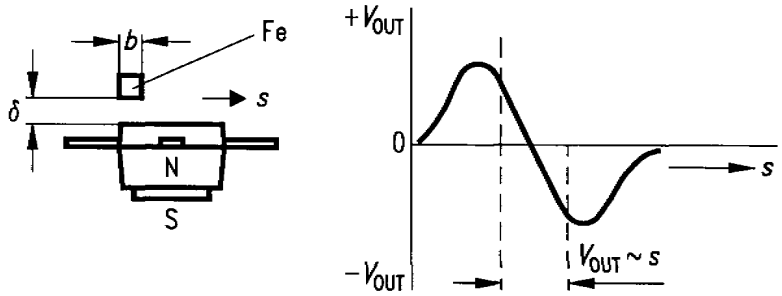
MCU/BSM Interfaces

I/F	Type	Nb.	I/O	Value	Constraints
Voice Coil Motor	analogue current	2	out	100 mA max TBC	
Magnetoresistive sensors		1	in		

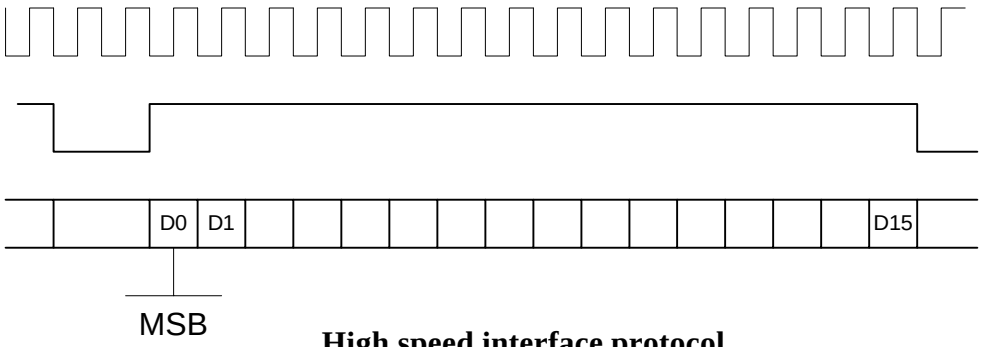
Position sensor specification :

- resistance at 300K : 2 x 100 Ω nominal
- small change at 4K
- excitation current : 1 mA DC
- dissipation : 0.5 mW (constant)
- output voltage : +-0.1 V
- Hysteresis : ~ 0.05° - corrected as part of control algorithm

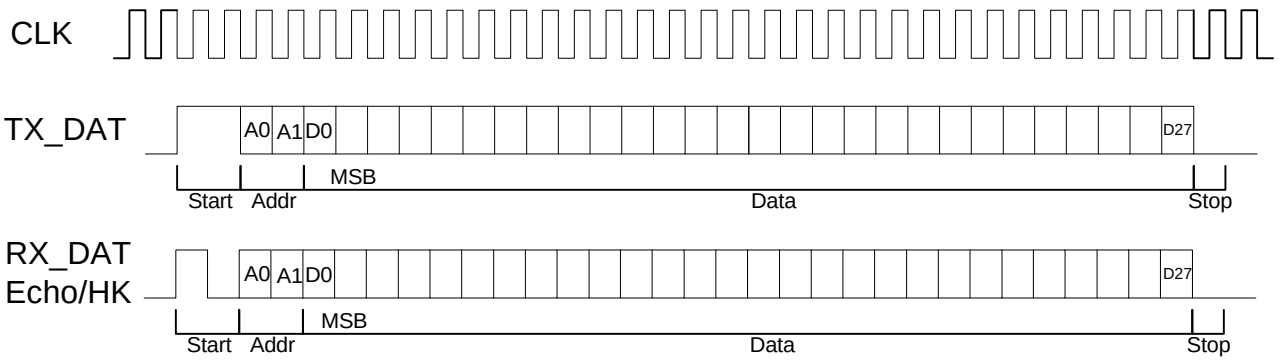
- Infineon (ex-Siemens) FP 212 L100-22 differential field plates sensing moving soft iron pieces
- The sensors are dual InSb/NiSb magnetoresistive elements, biased with a permanent magnet and forming part of a bridge circuit.



MCU/DPU Interface

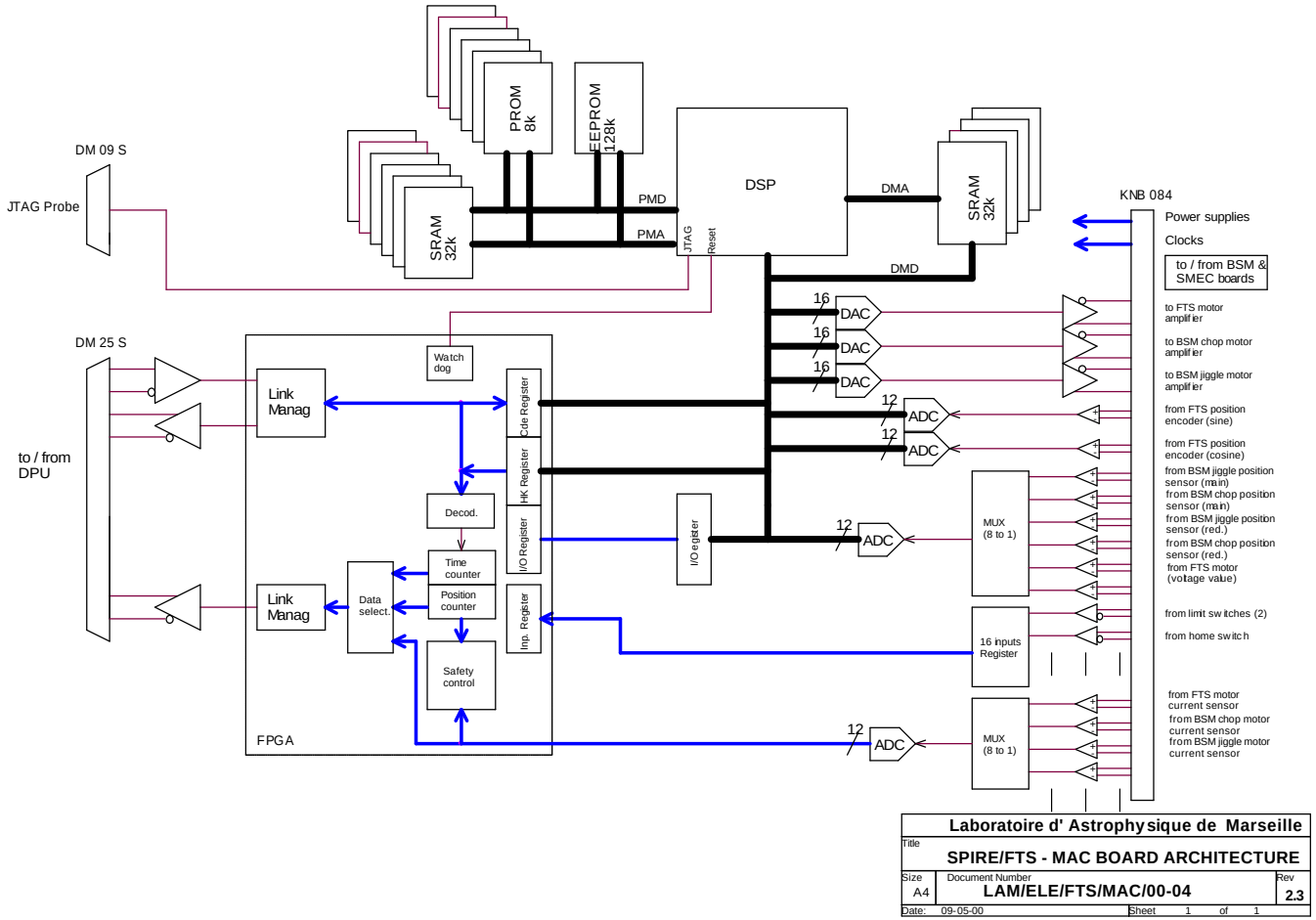


High speed interface protocol

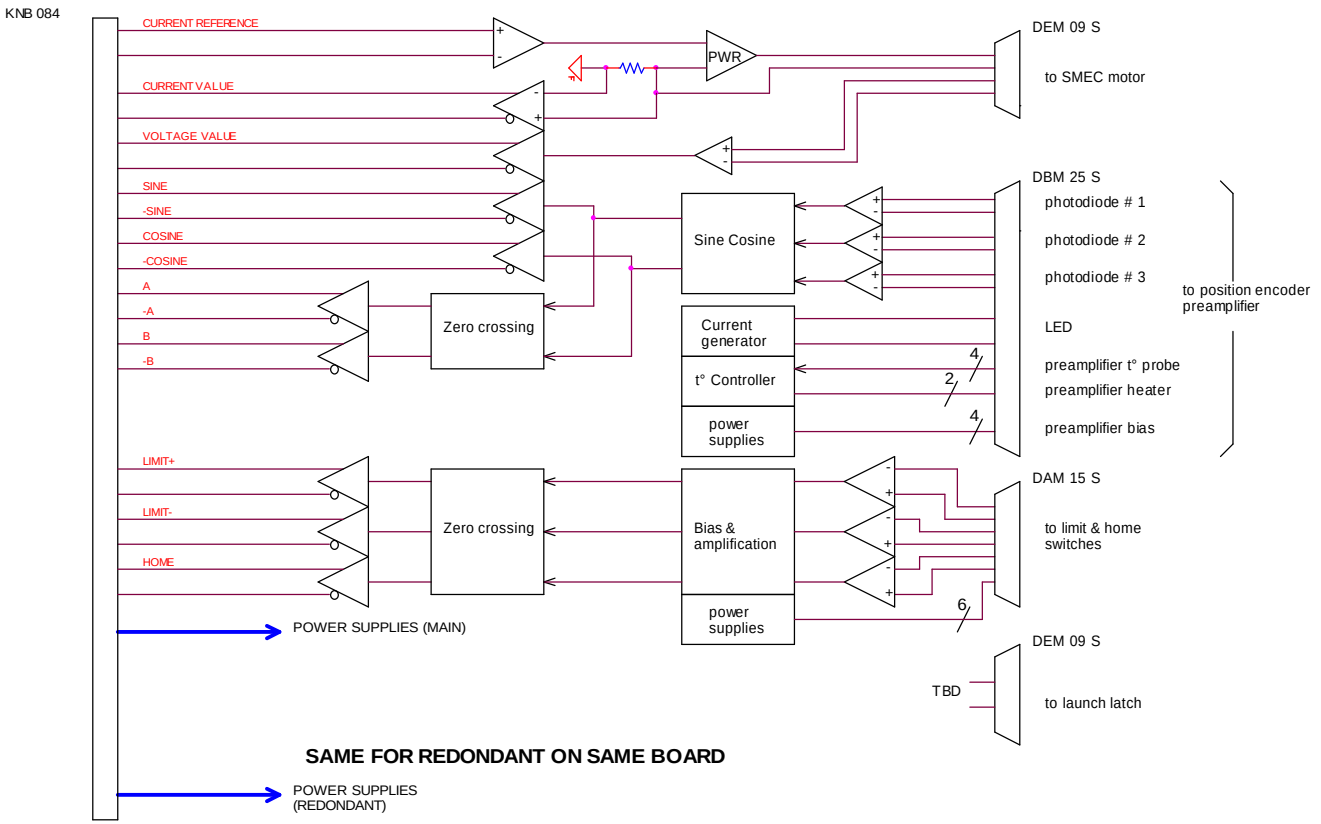


FSDPU/FSDRCU Low Speed Interface protocol

MAC Board


PROM 8k
EEPROM 128k
SRAM 32k
PMD
PMA
DSP
JTAG
Reset
DMA
SRAM 32k
KNB 084
Power supplies
Clocks
to / from BSM & SMEC boards
DM 09 S
JTAG Probe
DM 25 S
to / from DPU
Watch dog
Link Manag
Link Manag
Cde Register
HK Register
I/O Register
Inp. Register
Decod.
Time counter
Position counter
Safety control
Data select.
FPGA
I/O register
DMD
16
DAC
12
ADC
MUX (8 to 1)
16 inputs Register
to FTS motor amplifier
to BSM chop motor amplifier
to BSM jiggle motor amplifier
from FTS position encoder (sine)
from FTS position encoder (cosine)
from BSM jiggle position sensor (main)
from BSM chop position sensor (main)
from BSM jiggle position sensor (red.)
from BSM chop position sensor (red.)
from FTS motor (voltage value)
from limit switches (2)
from home switch
from FTS motor current sensor
from BSM chop motor current sensor
from BSM jiggle motor current sensor
Laboratoire d' Astrophysique de Marseille
Title
SPIRE/FTS - MAC BOARD ARCHITECTURE
Size
A4
Document Number
LAM/ELE/FTS/MAC/00-04
Rev
2.3
Date: 09-05-00
Sheet 1 of 1

SMEC Board



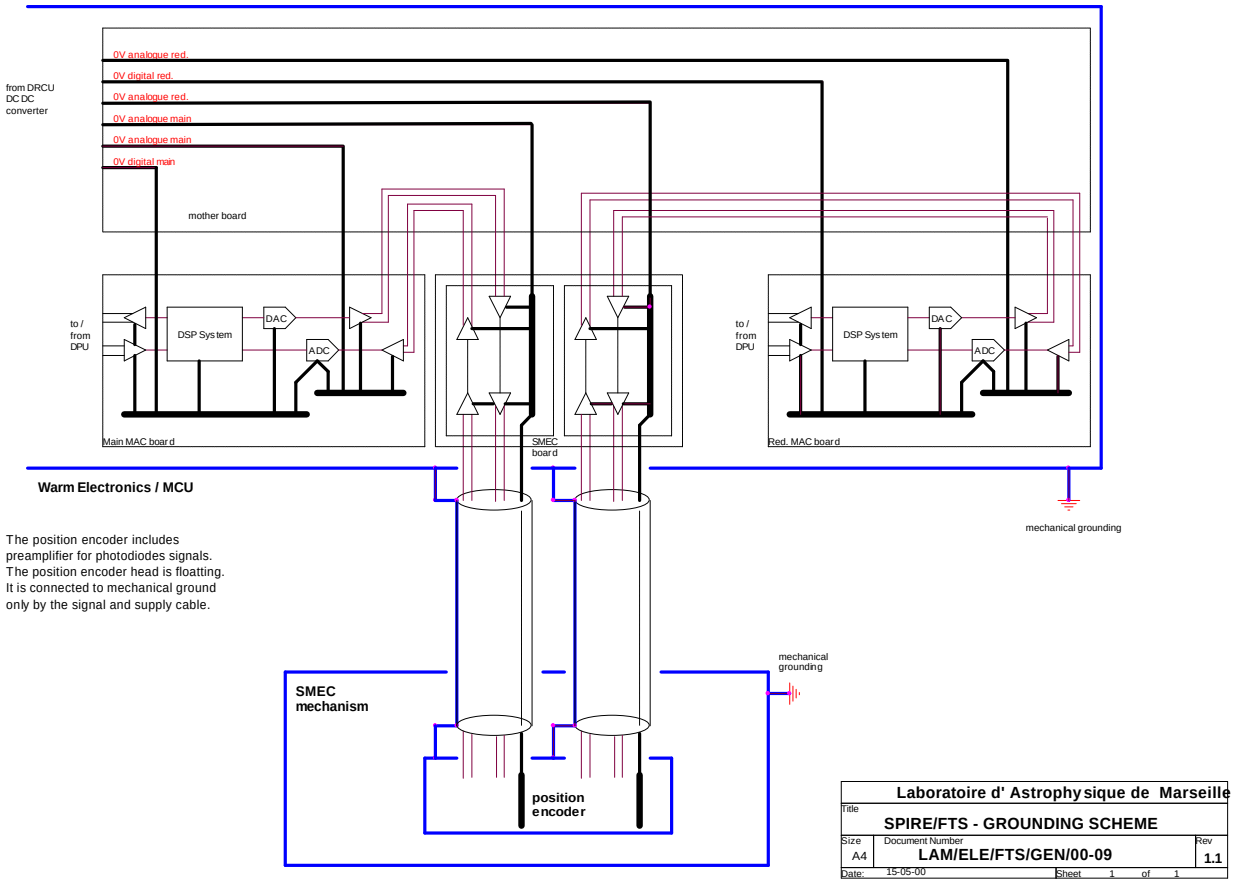
Laboratoire d' Astrophysique de Marseille		
Title: SPIRE/FTS - SMEC BOARD ARCHITECTURE		
Size: A4	Document Number: LAM/ELE/FTS/SME/00-07	Rev: 1.2
Date: 12-05-00	Sheet 1 of 1	

BSM Board

- Position sensor read-out :
  - Bridge circuit with switchable DC bias,
  - Instrumentation Amplifier eg LM108, AMP 01 or OP 27,
  - Multiplexer ADG 507 and 12 bit A/D converter eg AD 9221
- Motor drive
  - Complimentary bipolar transistor pair eg 2N 5153/4 or 2N2219 / 2N 2905
  - DAC 12/16 bits AD 7846
- Motor Current Measurement
  - series resistor and connection to A/D converter
  - same Instrument Amp as sensor one

GROUNDING

- *Motor PWR Analog ground to be added on the schematics*
- *The analog grounds not connected @ MCU level*
- *Analog/Digital grounds connected @ ADC level*
- *Analog ground not connected to mechanics*

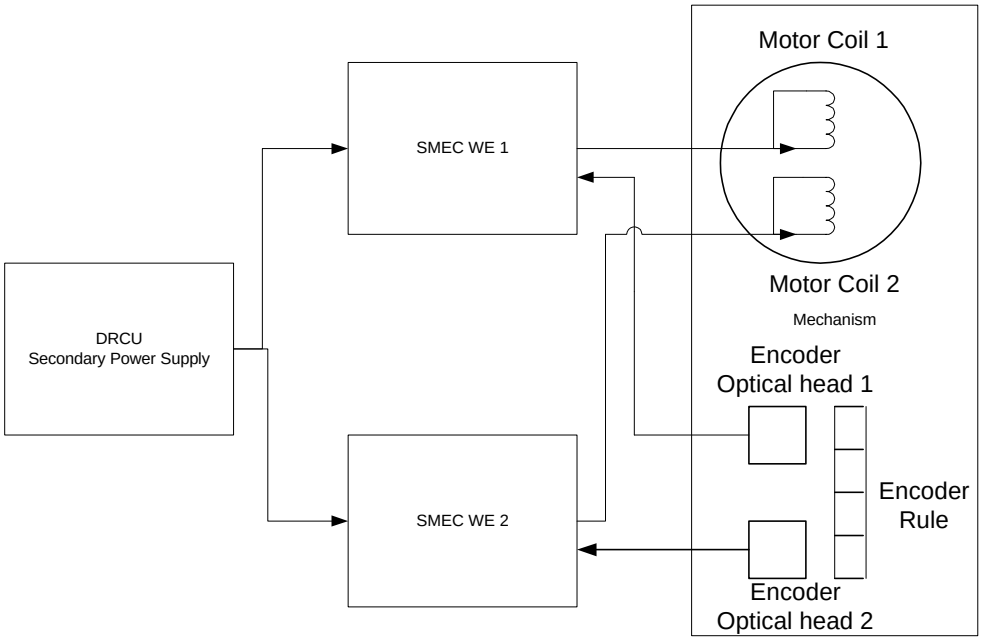


COMPONENTS

See the EEE part list for the complete set of components (doc ref LAM/ELE/FTS/QUA/000201).

REDUNDANCY

WE1.M1.OE1 + WE2.M2.OE2



FAILURE ANALYSIS

Subsystem/Component in failure	Event during a specific mode of operation	identification mean	Effect	Recovering Degraded mode
Interface electronics	No command can be received	the DPU has no command handshake	FTS WE out of control	
	Bad command/parameter	Checksum/No recognition of a command		Stop of the scan Status report Switch to stand-by mode waiting for another control mode operation
DSP and related interface components	Control algorithm diverging	software limits	Increase of the actuator command up to limitation	Stop of the scan Status report Switch to stand-by mode waiting for another control mode operation
	No control on the DSP	Watchdog		Emergency stop on watchdog action
Motor and related PWR amp	Short cut in the motor coil	Motor current measurement	Limitation of current value by the PWR amplifier	Use of the redundant board + motor coil.
Optical encoder and related acquisition electronics	Loss of some individual incremental pulses during closed loop operation	Difference between fiducial mark and position counter	Perturbation on the trajectory	Status report Adjust the position counter on next scan
	Total loss of incremental encoder pulses	id.	Error vs ramp reference increase -> Increase of the actuator command due to integral effect and position ramp increase -> Excessive motion speed up to speed limitation. -> Emergency stop.	Stop of the scan Status report Switch to stand-by mode waiting for another control mode operation
	Glitch on the absolute position counter (decreasing)	Additional position switch on the mechanics	The scan goes to hardware limits	Flyback operation and reset of the absolute position counter
	Glitch on the absolute position counter (increasing)	The scan ends before the nominal scan length parameter, and a difference between fiducial mark and position counter occurs at the end of flyback	The scientific scan is not achieved completely	Status report Readjust the position counter on next scan

DEGRADED MODES

Failure Mode	Effect	Remedy	Criticality
Chop Pos Sensor 1 fails	Cannot measure Ch1 position	Use C2 pos coil	No effect
Chop Pos Sensor 2 fails	Cannot measure Ch2 position	Use C1 pos coil	No effect
Chop Drive Coil 1 fails off	Cannot move from nominal position	Use C2 drive coil on its own	Longer rise-time – lose some efficiency
Chop Drive Coil 2 fails off	Cannot move from nominal position	Use C1 drive coil on its own	Longer rise-time – lose some efficiency
Chop Drive Coil 1 fails on	Cannot move from last position	Switch off BSM controller	Cannot chop or jiggle – only scan mode
Chop Drive Coil 2 fails on	Cannot move from last position	Switch off BSM controller	Cannot chop or jiggle – only scan mode
Both Pos Sensors fail	Cannot measure position	Run open loop	Reduced accuracy of chop or jiggle – or use scan mode
Both Drive coils fail off	Cannot move from nominal position	None – 2 point failure	Cannot chop or jiggle – only scan mode
Mechanism sticks	Cannot move from last position	None	Cannot chop or jiggle – only scan mode May lose some FOV

Test Equipements

- **WE Interface simulator**
  - EGSE Dedicated to be representative of the WE Interfaces. May be based on LABVIEW + interface board
  - Used for the control and monitor of the FTS Electronics during tests and commissionning
  - Not deliverable - For LAS internal use - Could be provided by CEA WE Group (Depends on date availability)
- **FTS Electronics simulator:**
  - EGSE dedicated to be representative of FTS Electronics behaviour vs. WE
  - Deliverable to CEA WE Group.
  - Could be composed with the delivered EM and a FTS Mechanism Simulator (TBC), or a simple board with 2 Communication FPGAs with simulated data or the EM board with DSP running in simulated mode.
- **FTS Mechanism simulator:**
  - EGSE Dedicated to simulate the mechanism behaviour vs. FTS electronics Use of a mathematical model compiled on a real-time simulator using MATLAB (Hardware-in-the-loop simulation)
  - Not deliverable. For LAS internal use.
  - One copy could be made to be delivered to CEA with the FTS Electronics simulator (TBC)

Development Summary

Activity	Hardware definition Flight model representativity	% realized	Milestone	
			Event	Date
Control system engineering Control system fast prototyping Measurement of data on test bench and servo performances assessment (speed stability)	Control electronics using dSpace.	75%	FTS PDR	06/2000
Control system of GSFC 2 mechanics with 21020 Evaluation board. BSM simulated by dSpace	Control electronics using evaluation board with limited interfaces	75%	internal development	10/2000
Detailed Electronics Design	Design of the EM electronics	50%	WE DDR	10-11/2000
Control system with 21020 Evaluation board + Interface board	Control electronics using evaluation board with complete interfaces and FPGAs	25% SMEC under manufacture	internal development	01/2001
DM development with MAC Board	Development of the MAC from elementary components (21020, memory,etc ..). Functions splitted on many single boards	/	internal development	03/2001
SMECm simulator	**Real time mathematical model of the mechanics running on dSpace with input/outputs using ADC/DAC**	**75%**	**Delivery to SAp**	**02/2001**
EM development	**MAC integrated on one board @flight dimension, interface and functions levels. <u>but</u> with Commercial components**		**1Delivery to SAp** 1 for lifetime tests 1 for internal needs	**09/2001**
QM1 MCU	**Commercial components (nodifference with EM? Need the agreement from ESA and long delay in case of military components)**	**/**	**Delivery to SAp**	**09/2001**
QM2 MCU	**Flight components**	**/**	**Delivery to SAp**	**07/2002**
PFM Development	**Flight components**		**Delivery to SAp**	**06/2003**

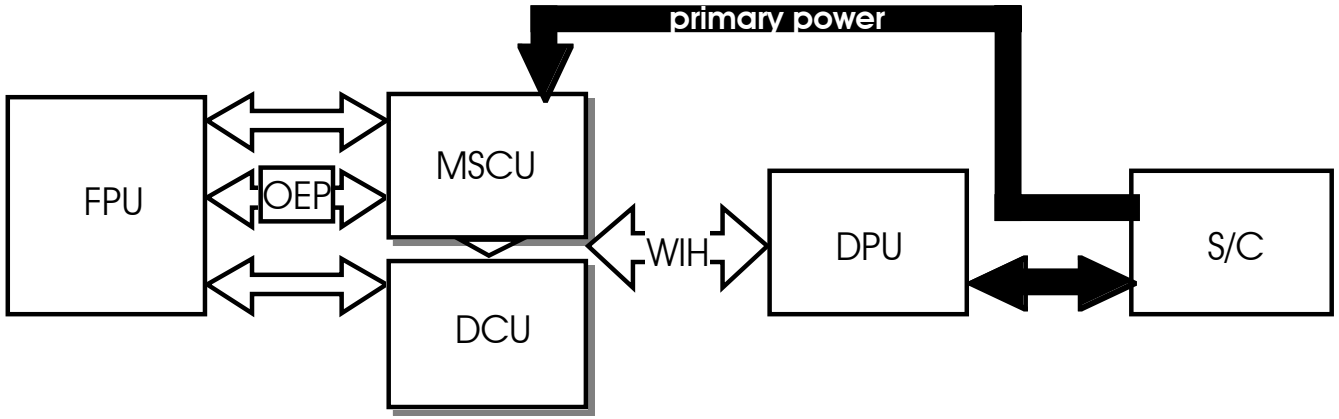
Additional Viewgraphs for the Warm Electronics and Operations System Summit

18 - 20 October 2000

Christophe Cara

Spire Electrical System

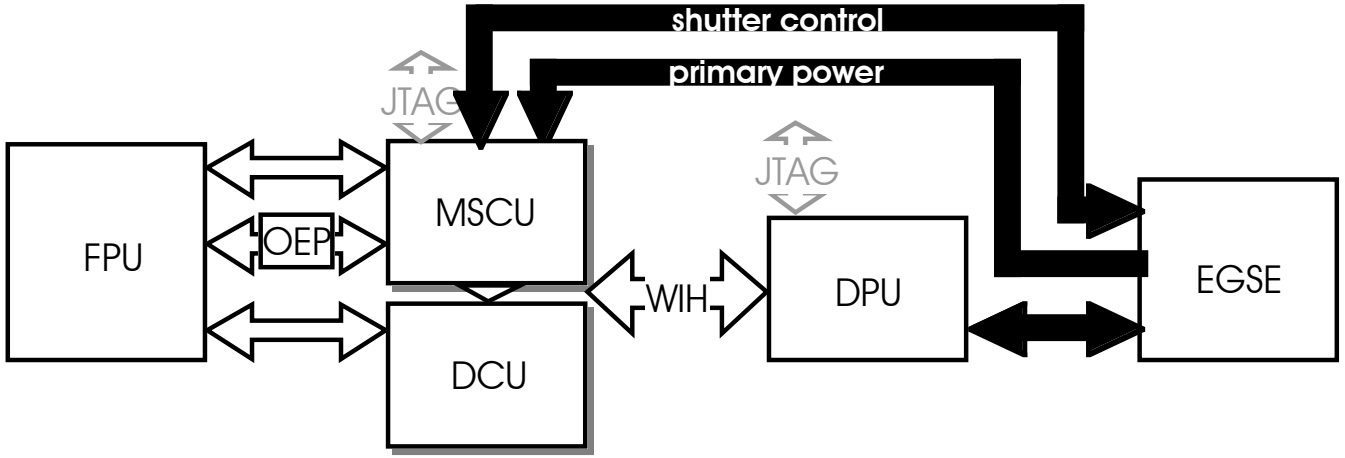
Flight Configuration



- **Warm Electronics :**
  - **DPU : Data Processing Unit**
  - **DCU : Detector Control Unit**
  - **MSCU : Mechanisms & Subsystem Control Unit**
  - **WIH : Warm Interconnect Harness**
  - **PEP : Position Encoder Preamplifier (OEP)**

Spire Electrical System

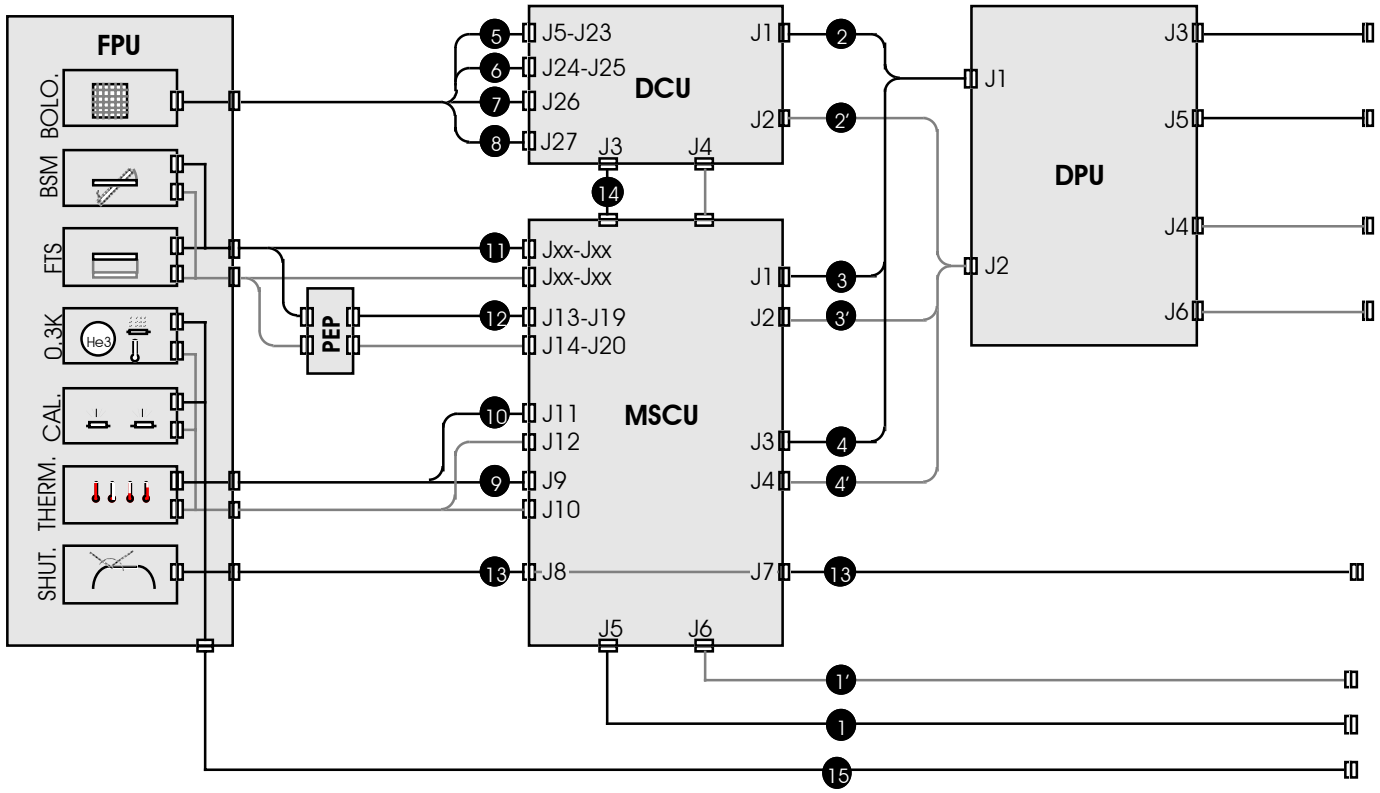
Ground Test Configuration



- **Flight Configuration plus :**
  - **Shutter to DRCU & DRCU to EGSE harnesses**
  - **DSPs JTAG connections (diagnostics+S/W updates)**

Spire Electrical System

Harnesses Detailed Configuration



1. DRCU Primary Power
2. DCU Cmd/Data
3. MCU Cmd/Data
4. SCU Cmd/Data
5. Ph. analogue channels
6. Sp. analogue channels
7. Thermometers analogue channels
8. Bolo. Bias + JFET supply (J40)
9. Thermometers
10. Cryocooler Heaters/Switches + Calibrators
11. FTS mechanism drivers/sensors
12. BSM mechanism drivers/sensors
13. Shutter mechanism drivers/sensors
14. DCU Seconary Power
15. FPU temperture channels

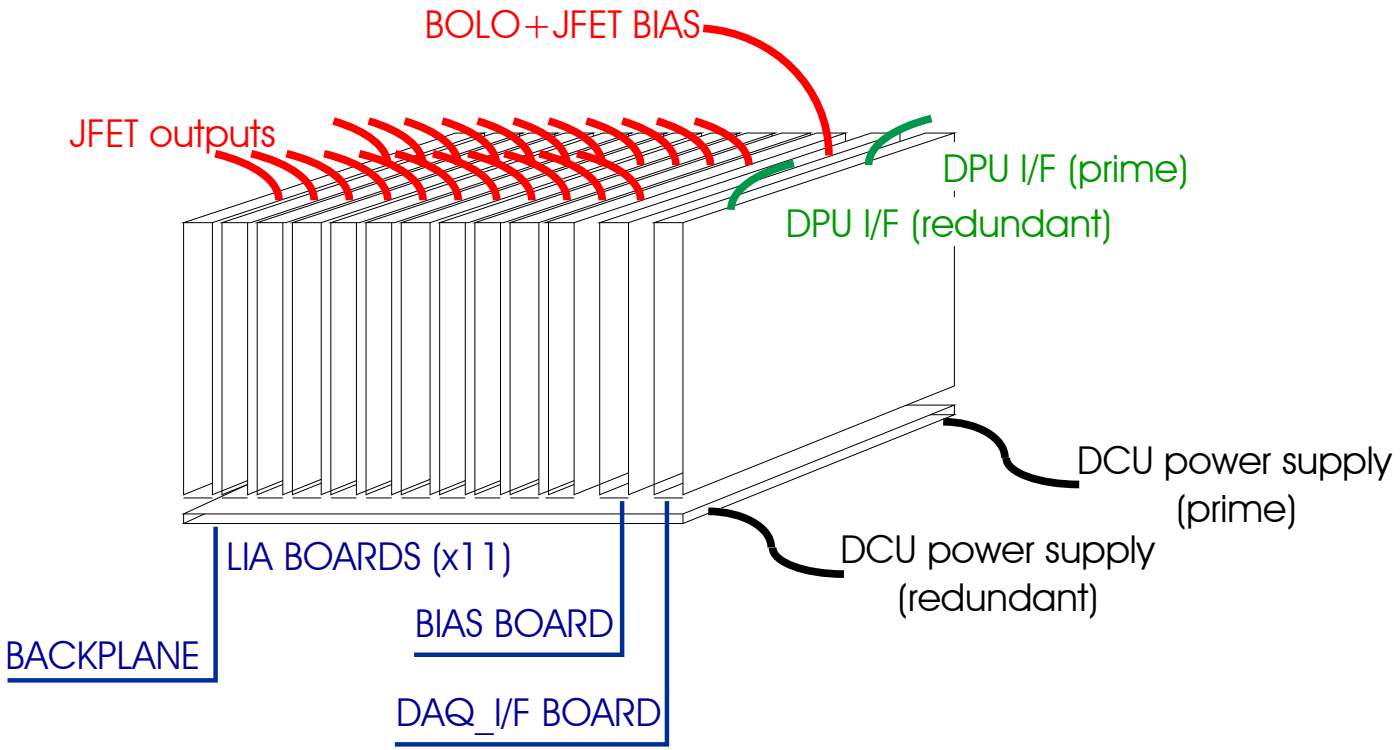
WE electrical interfaces (1)

- External interfaces
  - DPU / CDMS (digital)
    - IEEE 1553
    - ESA Packet Standard ICD
    - DPU ICD (Commands/Data/HK)
  - DPU / PDU (supply lines+analog)
    - SPIREIID-B (power budget)
    - FIRST IID-A (EMC+power bus)
  - DRCU / PDU (supply lines+analog)
    - SPIRE IID-B (power budget)
    - FIRST IID-A (EMC+power bus)

WE electrical interfaces (2)

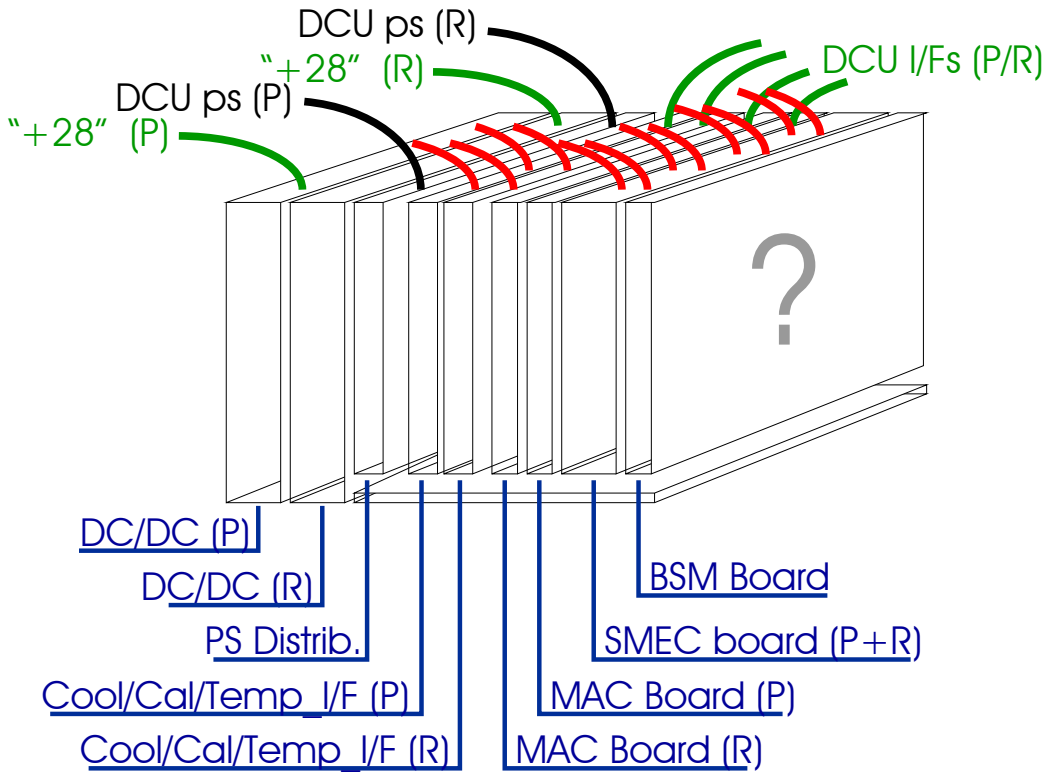
- Internal Interface
  - DPU / DRCU (digital)
    - DPU / DRCU Electrical ICD
    - FIRST IID–A (EMC) + EIA 422
  - DCU / SCU (supply lines)
    - DCU / SCU ICD (power budget, voltages, currents, ...)
    - FIRST IID–A (EMC)
  - MCU / SCU (supply lines)
    - DCU / SCU ICD (power budget, voltages, currents, ...)
  - DRCU / FPU (analog)
    - DCU–MCU–SCU / FPU ICDs
    - FIRST IID–A (EMC)

DRCU function implementation
DCU



For connectors details (pin-out, ...) see DRCU ICD

DRCU function implementation MSCU



For connectors details (pin-out, ...) see DRCU ICD

Sub-system Control

- DRCU sub-units implements H/W and low level S/W functions of sub-systems :
  - DPU to DRCU command interface allows :
    - Parameter settings,
    - Action triggering,
  - Instrument operation can be describe as successive parameter settings phases and action triggering phases.
  - I.e. : configuration of FTS mirror scan speed, length and then start for one scan.

Sub-system Control

- **Parameter settings :**
  - **Sub-unit specific parameters :**
    - **Bolometer bias amplitude**
    - **Bolometer bias frequency**
    - **Bolometer bias phase**
    - **JFET bias**
    - **On/off ADC offset**
    - **Bolometer data to be transferred in a frame**
    - **Number of frames to transfer (TBC)**

    - **FTS scan length**
    - **FTS scan speed**

Sub-system Control

- FTS scan speed
- FTS scan mode (open loop, encoder, back EMF)
- FTS position reference
- FTS telemetry mode

- BSM parameters : to be defined

- On/off temperature probe current generator (CERNOX)
- Pump heater current
- Switch heater currents (x2)
- Calibrator BB currents (x3)

Sub-system Control

- DRCU parameters :
  - On/off sub-system power supplies (by means of a SCU command) : part of autonomous safety function.

- Action triggering
  - Start FTS mirror scan (single)
  - Start bolometer frame transfer (single or multiple)

Sub-system Control

- **Broadcast command specific case :**
  - **A broadcast command affects more than one sub-system**
  - **Enables sub-system operation synchronization**

➡ **Action triggering commands are broadcast commands**

➡ **Starts FTS scan and detector sampling synchronously.**

Sub-system Control

- **Command verification :**
  - **Done by HK checking (by DPU S/W – sampled @ 16 Hz)**
  - **Command acknowledge indicates rejected command**
    - **Unknown code**
    - **Illegal command – i.e. : "*set_scan_length*" received when scanning**
    -
  - **MCU has defined "*get_parameter*" command type for engineering verification (step by step mirror motion)**

Sub-system Control

- **Unit synchronization**
  - Synchronization of the sub-systems is required to enable on-ground data processing (especially between mechanisms and detector).
  - Every sub-unit features a time counter whose content ($t_{s/u}$) is transmitted as a header of a data packet
  - Sub-unit time counters are simultaneously reset by means of a broadcast command
  - DPU samples its own internal counter when sending the command.

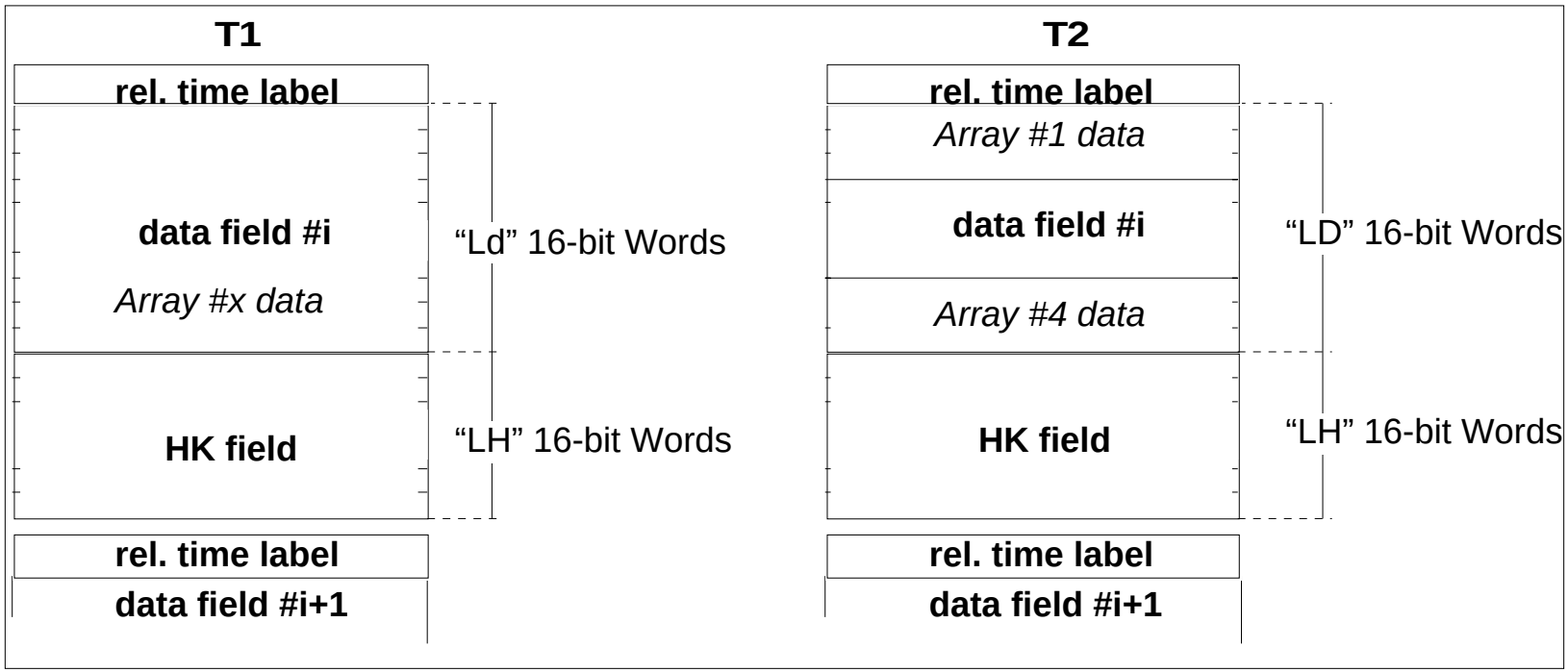
Data / HK rates

		Photometry			Spectrometry			Cooler Recycle		
S/U	Data	Amount	Rate	Size	Amount	Rate	Size	Amount	Rate	Size
DCU	detectors	288	16	16	56	80	16	0		16
	temperatures	8	16	16	8	16	16	0		16
	HK - *note 1*	20	16	8	20	16	8	20	16	8
SCU	temperatures	14	16	16	14	16	16	14	16	16
	sec. voltages	18	16	8	18	16	8	18	16	8
	currents - *note 2*	6	16	16	6	16	16	0		16
	HK - *note 3*	5	16	8	5	16	8	5	16	8
MCU	position rel. time	0		32	1	250	32	0		32
	current - *note 4*	0		32	1	250	32	0		32
	currents - *note 5*	2	16	32	2	16	32	0		32
	HK - *note 6*	5	16	32	5	16	32	5	16	32
Data Rates		**5624**			**6496**			**728**		
Bit Rates		**89984**			**103936**			**11648**		

Note 1 : 6 biases (8-bit) + 13 WE boards temperatures (8-bit)+status (8-bit)
Note 2 : 3 cooler heaters (16-bit) + 3 calibrators (16-bits)
Note 3 : 5 WE boards temperatures (8-bit)+status (8-bit)
Note 4 : 1 FTS coil (16-bit)
Note 5 : 2 BSM coils (16-bit)
Note 6 : 4 WE boards temperatures (8-bit)+status (8-bit)

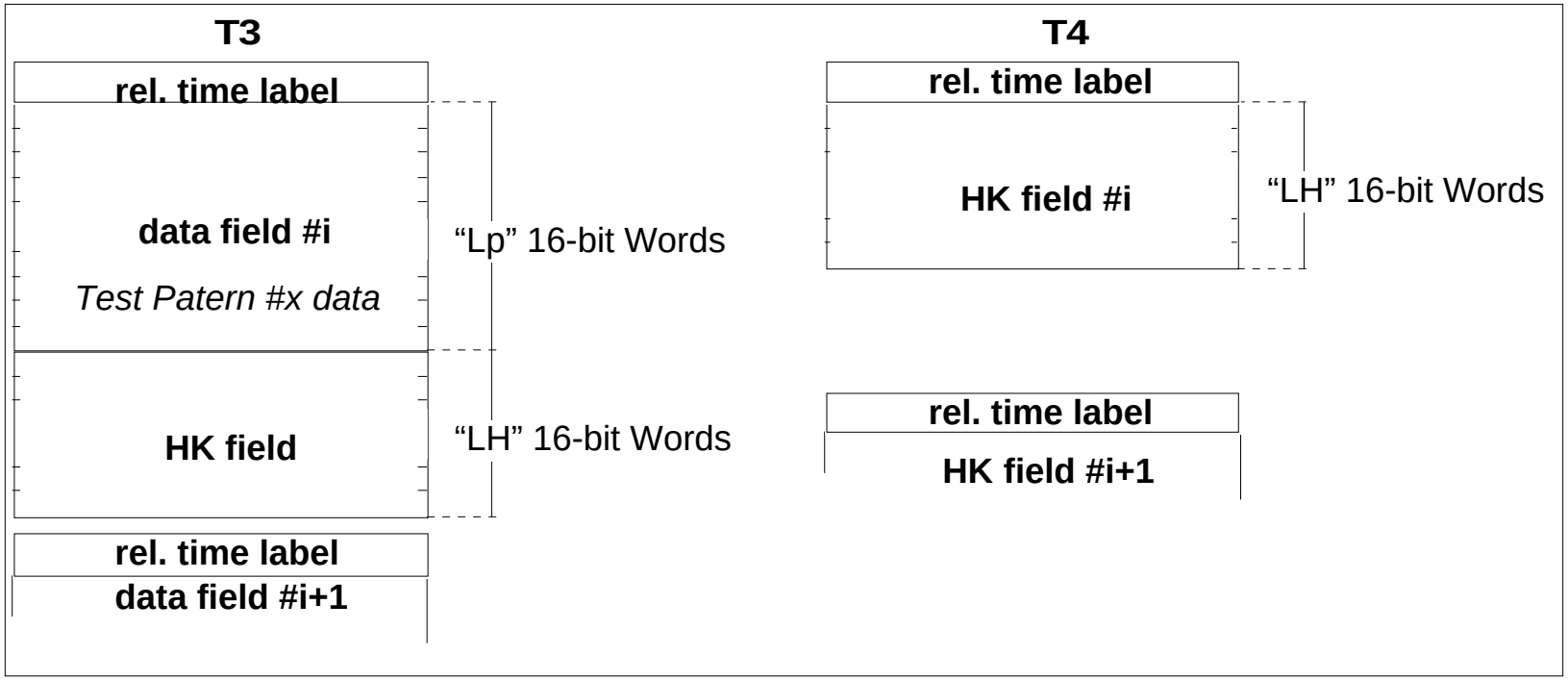
DCU Data frame description (1)

Bolometer + HK data

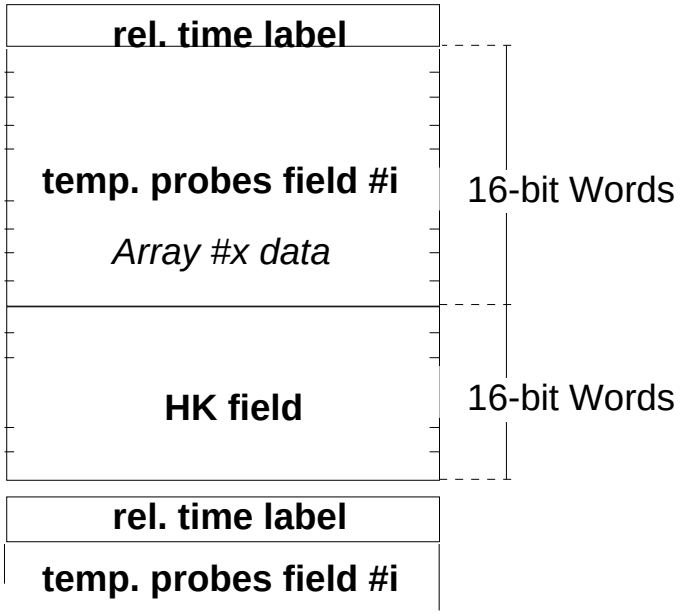


DCU Data frame description (2)

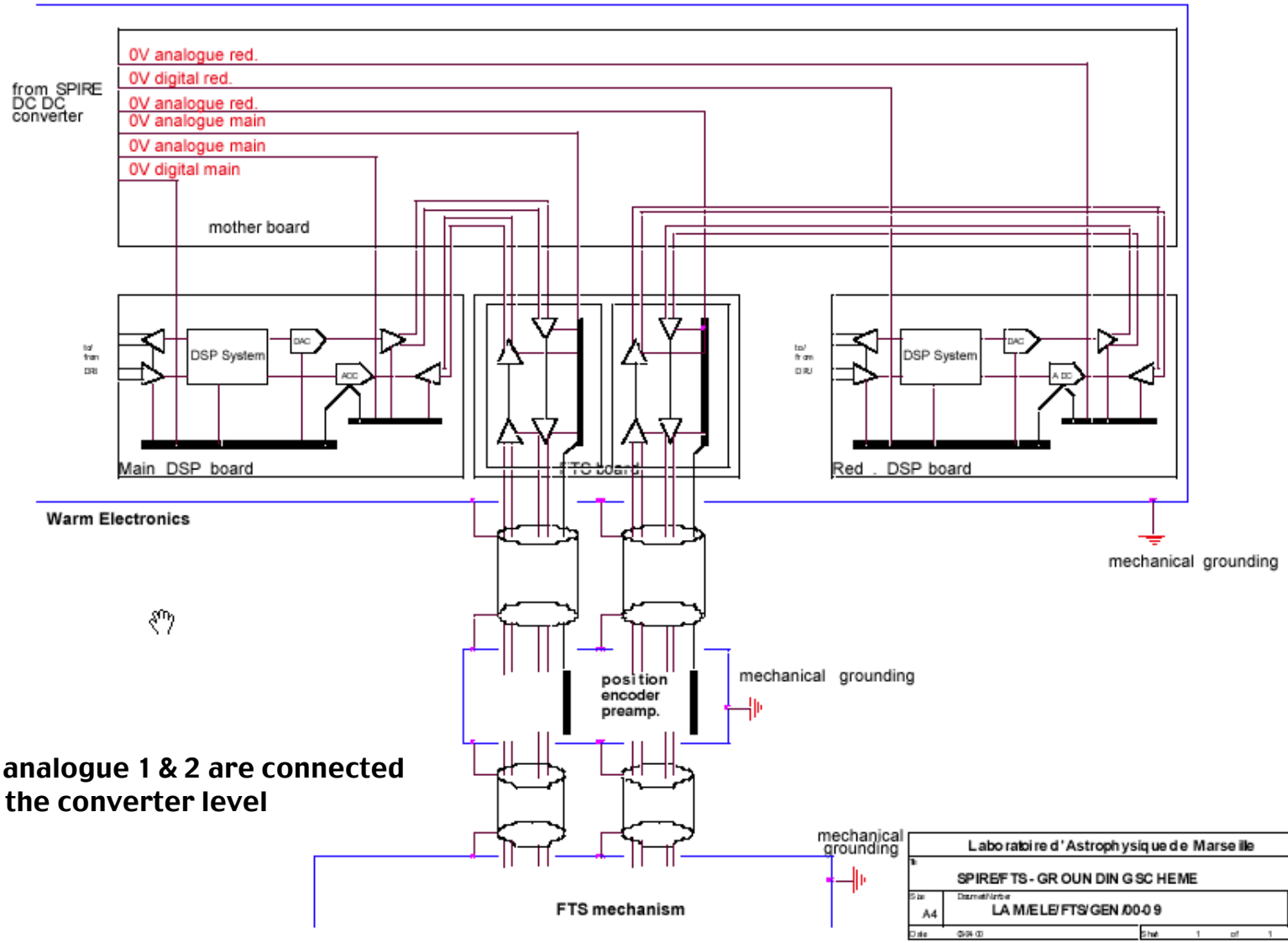
Test Pattern & HK only



SCU Data frame description

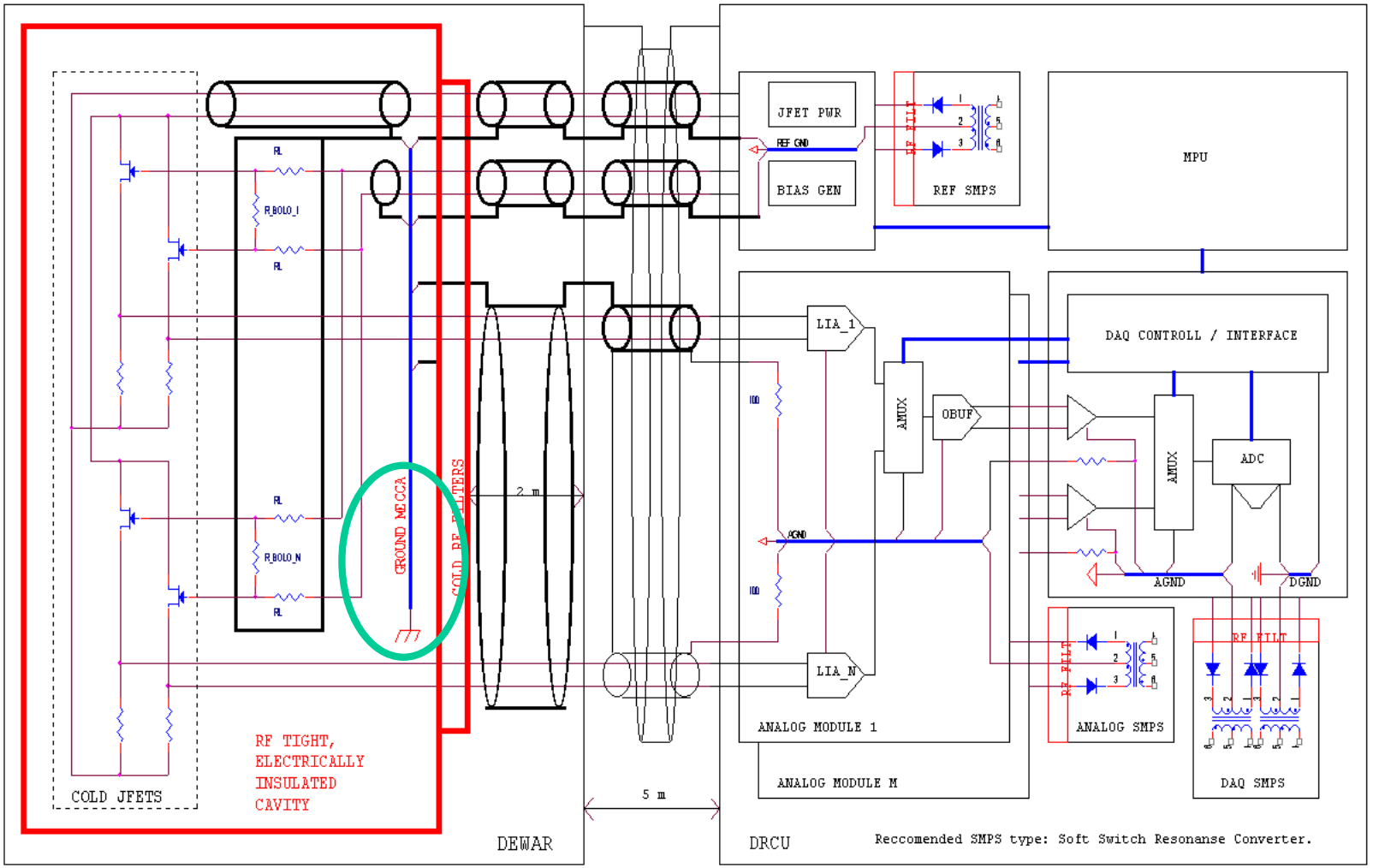


MCU grounding diagram



0V analogue 1 & 2 are connected at the converter level

DCU grounding diagram



NOTE:
Due to the high bolometer RF sensitivity, special care should be taken on proper RF filtering and RF tightness of the cold instrument, and on the RF filtering of the Switch-Mode Power Supply lines. A low-noise SMPS like the Soft Switch Resonanse Converter type is highly reccomended.

VIKTOR HRISTOV CalTECH		
Title: SPIRE READOUT GROUNDING SCHEME		
Size: B	Document Number: 0	Rev: 0
Date: Tuesday, April 11, 2000	Sheet 1 of 1	

Power Supply & Grounding

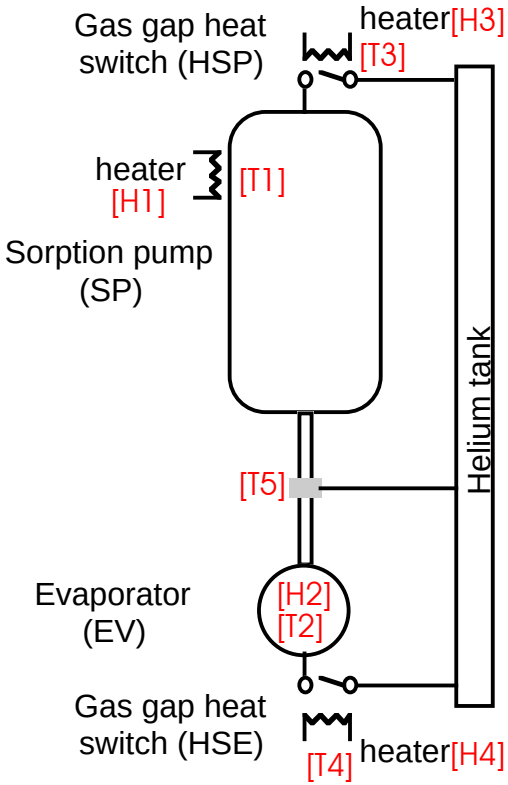
- **Summary :**

DCU	+Vdigital	connected to V_{daq} at ADC level
	+/- Vdaq	
	+/- Vanalog	connected to $V_{bias+jet}$ via 100 Ω
	+/- Vbias+jfet	
MCU	+Vdigital	connected to +/-Vanalog(mac) at ADC/DAC level
	+/-Vanalog(mac)	
	+/-Vanalog(smec)	connected to +/-Vanalog(mac) at DC/DC level
SCU	+Vdigital	common to +Vdidgital MCU
	+/-Vanalog	connected to +Vdigital at ADC/DAC level

Subsystem requirement on WE Cryocooler

- **Summary :**
  - Temperature measurement
  - Heater bias generation
  - Recycling sequencing algorithm
  - Temperature control loop algorithm

Subsystem requirement on WE Cryocooler

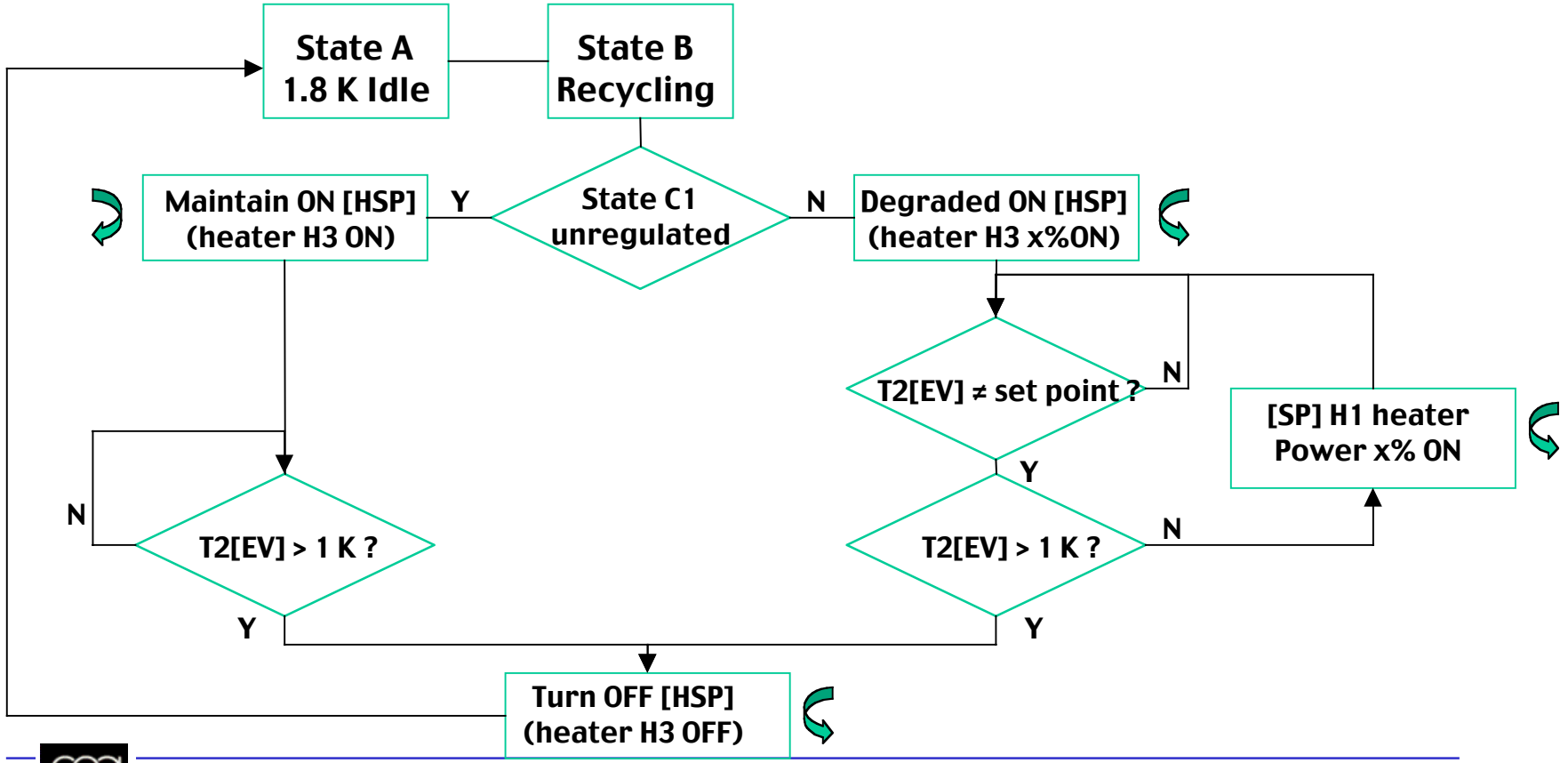


	Item	Range	Accuracy & Resolution	No of wires	Status
T1	Sorption pump temperature	1.5 K – 50 K	A ≤ 1 K R≤ 0.5 K	4	Required
H1	Sorption pump heater	0 – 500 mW		2	Required
T2	Evaporator thermometer	0.25 K – 10 K	A ≤ 5 mK R ≤ 0.1 mK	4	Required
H2	Evaporator heater	0 – 1 mW		2	Optionnal
T3	Miniature sorption pump thermometer on sorption pump	1.5 K – 25 K	A ≤ 1 K R ≤ 0.5 K	4	Required
H3	Miniature sorption pump heater on sorption pump	0 – 1 mW		2	Rquired
T4	Miniature sorption pump thermometer on evap. heat sw.	1.5 – 25 K	A ≤ 1 K R ≤ 0.5 K	4	Required
H4	Miniature sorption pump heater on evap. heat sw.	0 – 1 mW		2	Required
T5	Thermometer on thermal sw.	1.5 – 10 K	A ≤ 0.1 K R ≤ 0.1 K	4	Optionnal

Note : **All temp. Probes are now CERNOX type**
Sorption pump heater resistor = 400 Ω

Subsystem requirement on WE Cryocooler

- Control algorithm (including stabilization)



Subsystem requirement on WE Cryocooler

- **Standard Recycling**