FIRST/PLANK - EMC & POWER QUESTIONNAIRE FOR PAYLOADS

PAYLOAD NAME: FIRST/ SPIRE

REFERENCE PERSON: Colin Cunningham, UK Astronomy Technology Centre

Version: 1.0

Date : May 10, 2000

1. Power Interface Requirement

Function	Number of main lines required	Number of redundant lines required	LCL class eg 1,2,4,7A
+ 28 V FSDRC power	1	1	(109W/4A Trip-off limit)
+28 V FSDPU power	1	1	(28W/1A Trip-off limit)
Keep alive supply 7 – 9V	0	0	1W max per line

Note
The inrush current of the instrument should be limited to <TBD times the LCL peak value and of duration < TBD msec. The rate of change of the inrush current shall not exceed TBD/micro sec

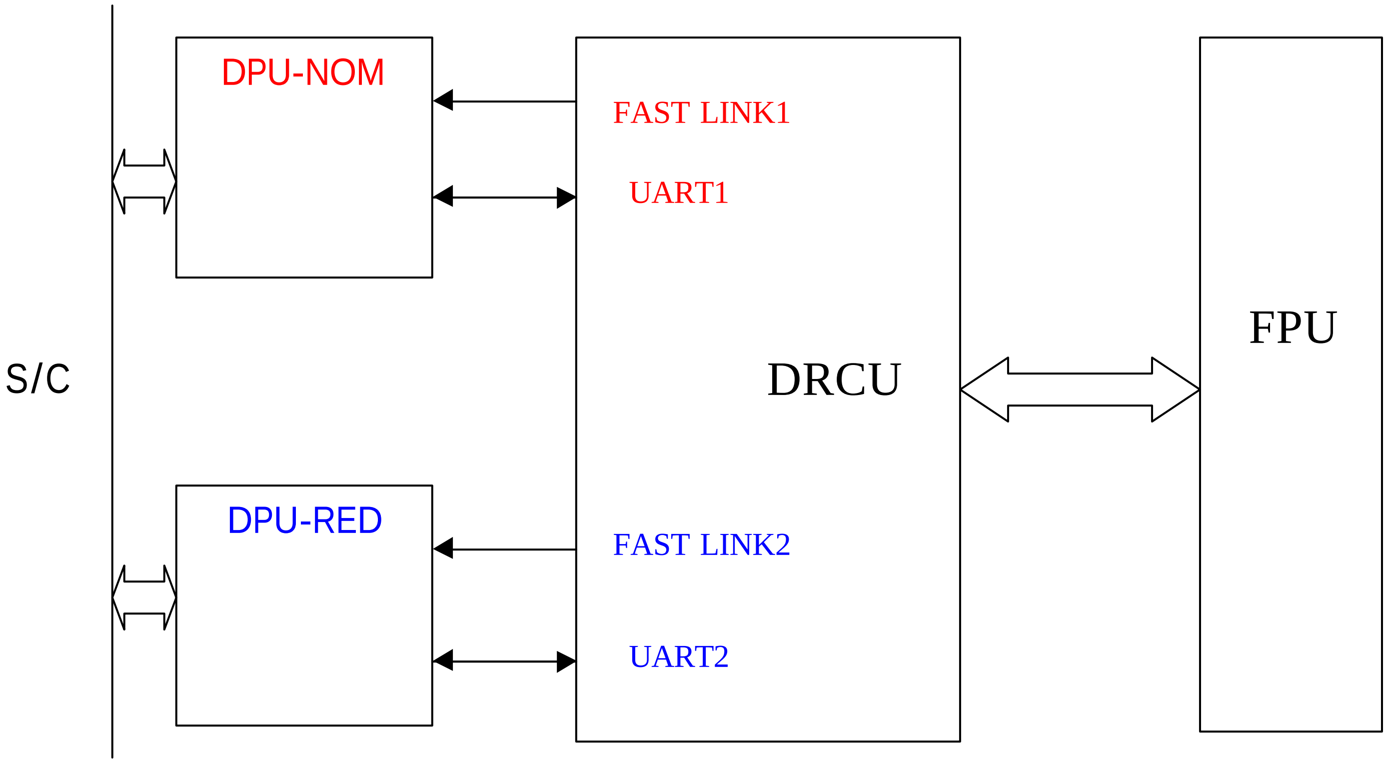
2. Instrument Power Distribution Block Diagram and Redundancy Approach

Please describe the expected instrument internal power distribution block diagram and the redundancy concept within the instrument.

3. Instrument Power Requirements

Experiment interface	Operational mode:	Average Power	Peak Power and duration
+28 FSDRCU Power	Photometer	71 W	TBD
+28 FSDRCU Power	Spectrometer	71W	TBD
+28 FSDRCU Power	Cooler Recycle	71W	TBD
+28 FSDPU Power	Photometer	10W	TBD
+28 FSDPU Power	Spectrometer	10W	TBD
+28 FSDPU Power	Cooler Recycle	10W	TBD

- System redundancy

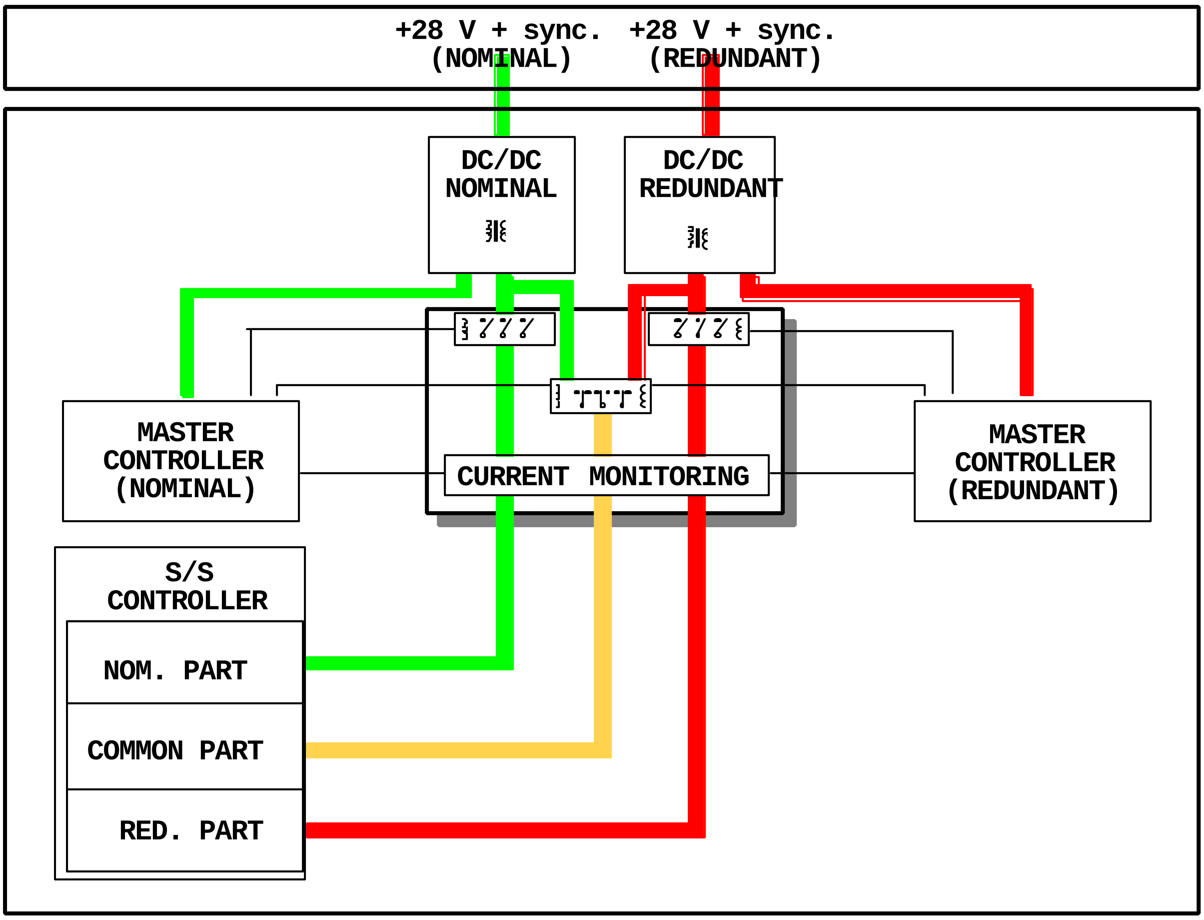


DC/DC converter synchronisation is required. The rationale is to ensure converters do not generate difference frequencies, which might be in the range of the low frequency high sensitivity detector signals, in the range 100Hz to 1KHz.

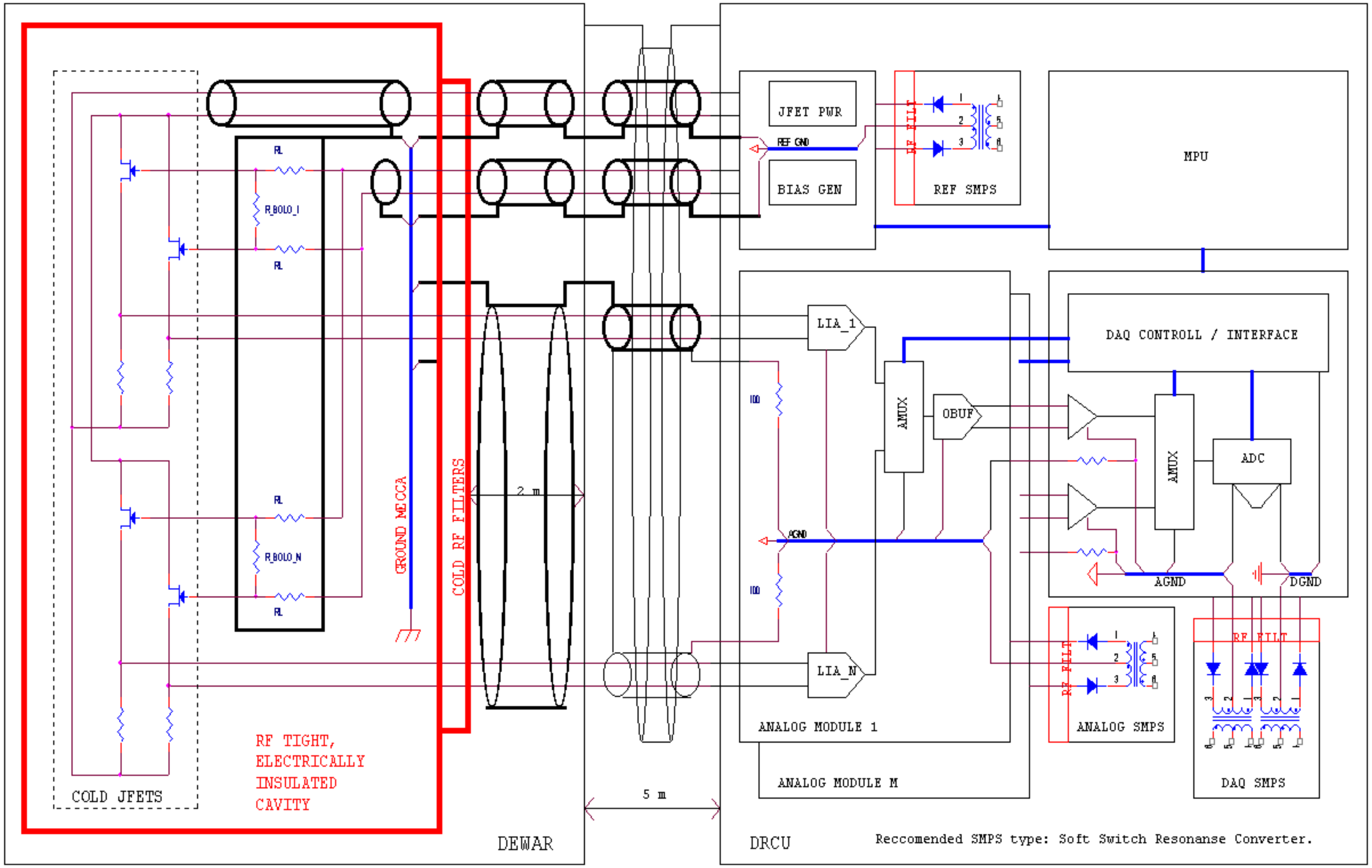
Top Level Redundancy

- DRCU and DPU are supplied with primary and redundant 28V power
- H/W redundancy within DRCU

– Master Controller, Interface Board and DC/DC converter are cold redundant
– Motherboard and Power Distribution Boards provide support for both nominal and redundant signals



4. Instrument Grounding Diagram



NOTE:
Due to the high bolometer RF sensitivity, special care should be taken on proper RF filtering and RF tightness of the cold instrument, and on the RF filtering of the Switch-Mode Power Supply lines. A low-noise SMPS like the Soft Switch Resonanse Converter type is highly reccomended.

VIKTOR HRISTOV CalTECH		
Title: SPIRE READOUT GROUNDING SCHEME		
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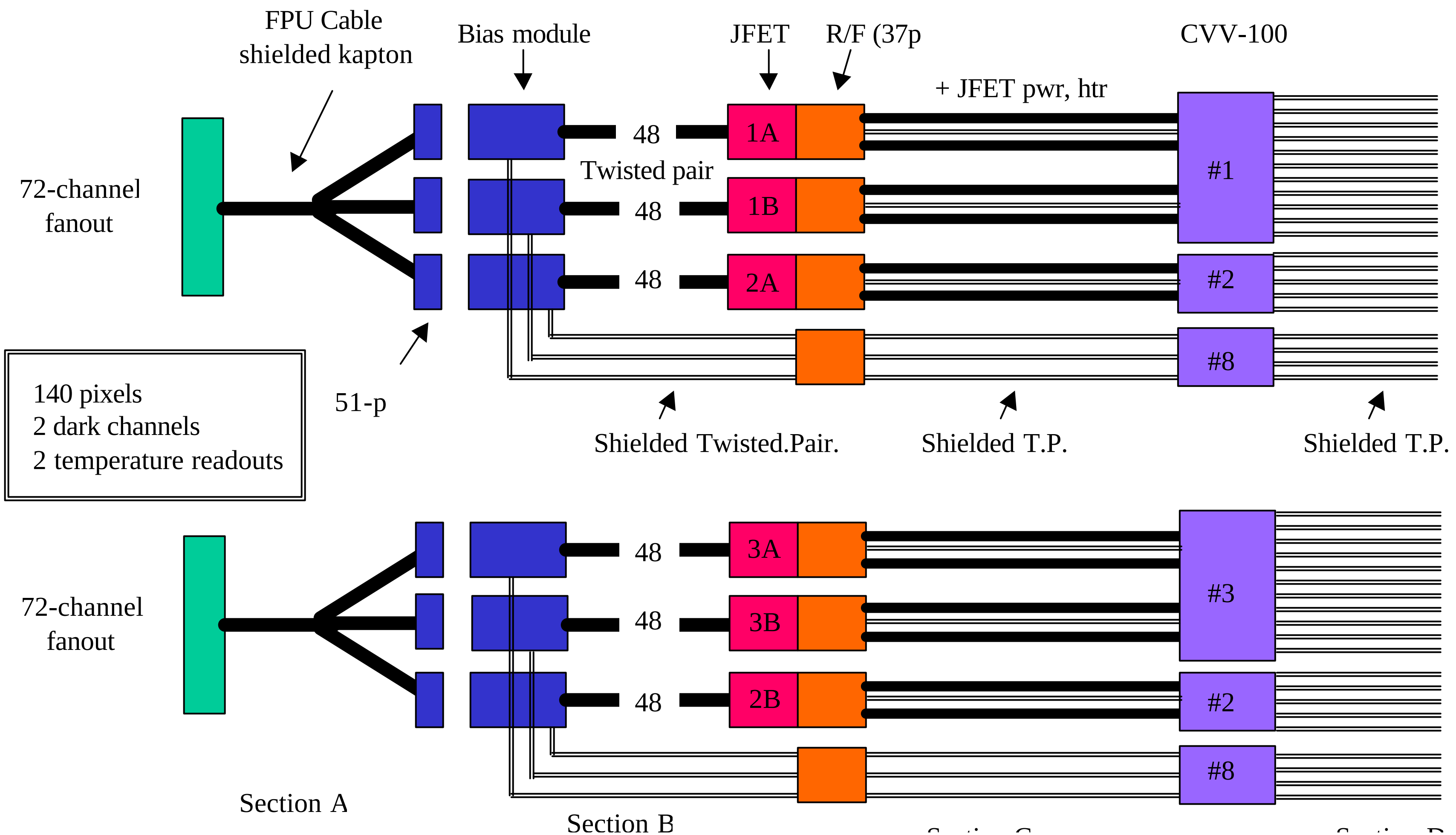
5.   Interconnecting Harness Block Diagram

FPU Harness: 250 um Photometer (Repeated for 4 other arrays)



Section	Length, m (TBC)	Temperature Range, K	Source resistance, ohms	Noise Floor, nV/rt Hz
A	0.1	0.3 - 2	5M	7
B	0.6	2 - 11	5M	7
C	2	11 - 120	6k	6
D	5	120 - 300	6k	6

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6. Instrument Susceptibilities

Please specify the frequencies and the levels for which you expect your instrument, or its parts/components, to be susceptible (Voltage and Current ripple, Electric Fields, Magnetic Fields, etc.). – all TBD

7. Instrument Emissions

Please specify the frequencies and the levels you expect your instrument will emit (Voltage and Current ripple, Electric Fields, Magnetic Fields, etc.). – all TBD

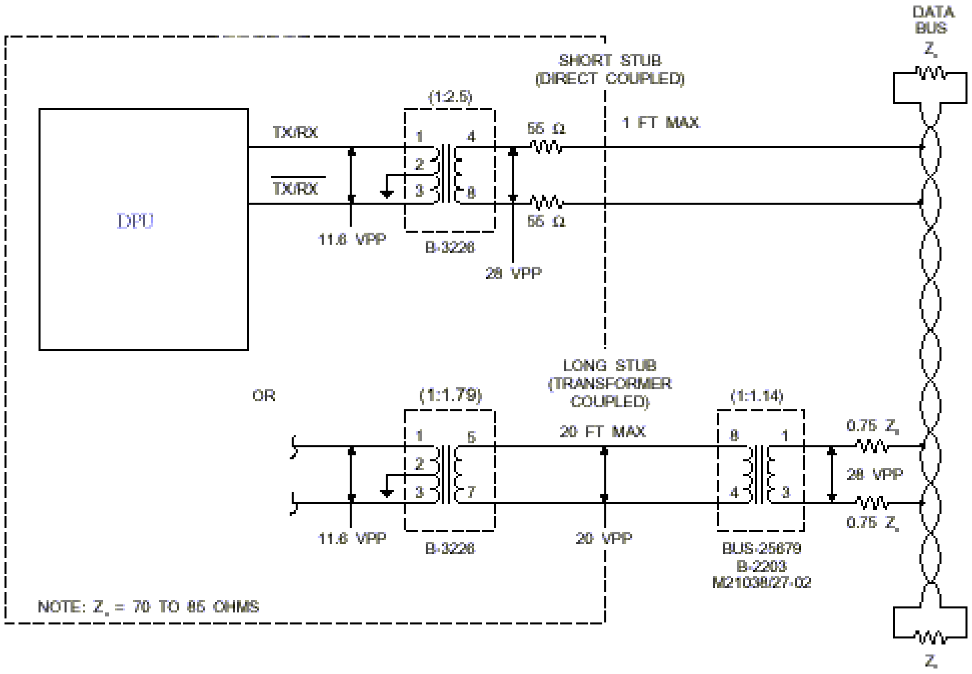
8. Instrument Frequency Plan

Frequency	Type of signal	Characteristics / Remarks
100 Hz & odd harmonics to 1KHz(TBC)	Detector Bias	Very sensitive – noise floor 7nV/rt Hz
10 MHz	A/D clock	TBD
20 MHz	DSP clock	TBD

9.   Detailed questions on EMC

A) Does your instrument require electrostatic or magneto-static cleanliness at spacecraft level?
Not that we know of at present

B) What is the topology of the electronic interfaces you are considering in the instrument design? (E.g. single ended-differential, balanced-differential, etc.). If available, please give an interface circuit diagram.
Detector signals to warm electronics DRCU are balanced differential.
Digital interface from DPU to S/C is to Mil STD 1553B



C) Do you believe your experiment be compliant to the ISO EMC requirements, which are presently assumed as a reference? Please try to establish a compliance matrix with the ISO EMC requirements.

TBD

D) Do you expect your experiment be vulnerable to Electrostatic Discharge (say 10 kV, 5.6 mJ)?

No more than conventional electronics.

E) Do you believe it is mandatory to use a static screen for the converters' transformers in order to minimise the winding capacitance and enhance AC de-coupling between primary and secondary power?

Very likely.

F) Do you expect your experiment be vulnerable to voltage common mode transients? Which peak value and time characteristics?

Yes – levels TBD.

G) What is the EMC verification concept you plan to implement in the development phases of your instrument?

Conducted EMC tests at subsystem and instrument verification levels.Details TBD. Radiated EMC testing is only valid in the S/C environment and as such is problematic.

H) What are the major concerns of your instrument from the EMC discipline point of view?

The noise floor is very low over 7 metres of wiring harness from 0.3K detectors to the warm electronics at 300K. There is no voltage amplification over all this length, although the source impedance is converted from 5 Mohm to 6 Kohm after 0.6 metres at the 11K stage.

Bolometers are thermal sensors, and as such sensitive to all types of energy interference from RF to mechanical vibration. Hence our concept is to RF filter every wire entering the Faraday shield formed by the 4K instrument enclosure.