SPIRE Spectrometer Mirror Mechanism Subsystem Development Plan

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Update

Date	Indice	Remarks
3 Feb 2000	1	Creation of the document
11 Feb 2000	2	Distributed to the project
1 May 2000	3	Distribution List revised LAS changed into LAM One more model : STM added Mechanical scheme added MCU concept added
24 May 2000	4	BSM included Dates revised
6 June 2000	5	CDR date updated
20 June 2000	6	BSM dates included Documentation planning included in the associated mpp file

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1. Scope of the document

This document describes the development plan of the FIRST/SPIRE Spectrometer mirror mechanism subsystem.
The development plan is based on the applicable documents cited in §2.
The format of this document is compliant with the CNES instructions applicable at LAM [AD3].

2. Documents

2.1. Applicable documents

	Title	Author	Reference	Date
AD1	SPIRE Spectrometer Mirror Mechanism Subsystem Specification	D.Pouliquen	LAS.PJT.SPI.SPT.200002 Ind 4	9 May 2000
AD2	SPIRE Development plan	K.King	TBU	
AD3	Guide pour les projets scientifiques	CNES	DTS/AQ/QP 98-083	June 1998
AD4	SPIRE BSM Development plan	C.Cunningham	DRAFT 2	June 2000
AD5	DRCU Development plan	JL Augères		May 2000

2.2. Reference documents

	Title	Author	Reference	Date
RD1	Intrument Requirements Document	B.M.Swinyard	SPIRE-RAL-PRJ-000034 Iss .30	May 2000
RD2	Instrument Development Plan	K.King	SPIRE WE Review viewgraphs	6 Dec 1999

2.3. Glossary

AD	Applicable Document	JPL	Jet Propulsion Laboratory
BSM	Beam Steering Mirror	LAM	Laboratoire d'Astrophysique de Marseille
BSMm	BSM cryogenic mechanism	MCU	Mechanism Control Unit
CEA	Commissariat à l'Energie Atomique	MGSE	Mechanical Ground Support Equipment
CDR	Critical Design Review	MSSL	Mullard Space Science Laboratory
CNES	Centre National des Etudes Spatiales	NA	Not Applicable
CoG	Center of Gravity	OGSE	Optical Ground Support Equipment
CQM	Cryogenic Qualification Model	PDR	Preliminary Design Review
DDR	Detailed Design Review	PFM	Prototype Flight Model
DESPA	Département des Etudes SPAtiales	RAL	Rutherford Appleton Laboratory
DM	Development Model	RD	Reference Document
DPU	Digital Processing Unit	SMEC	Spectrometer mirror MEChanism
DRCU	Digital Read-out and Control Unit	SMECm	SMEC cryogenic mechanism
DSP	Digital Signal Processor	SMECp	SMEC cold preamplifier
EGSE	Electrical Ground Support Equipment	SPIRE	Spectral and Photometric Imaging REceiver
EM	Electrical Model	STM	Structural Model
FIRST	Far InfraRed Submillimeter Telescope	TBC	To Be Confirmed
FPU	Focal Plane Unit	TBD	To Be Defined
FS	Flight Spare model	TBU	To Be Updated
FTS	Fourier Transform Spectrometer	TBW	To Be Written
GSFC	Goddard Space and Flight Center	WE	Warm Electronics

3. Description of the spectrometer mirror mechanism subsystem

The Spectrometer mirror MEChanism subsystem (SMEC) is a major part of the SPIRE Spectrometer. It is in charge of the movement of the rooftop mirrors inside the SPIRE spectrometer.
The critical performances of SMEC [AD1] are the mirror velocity and its stability, the mirror movement around its travel axis and the required accuracy of the mirror position measurements.

The SMEC is made of 3 main parts :

- **The cryogenic mechanism** (SMECm)

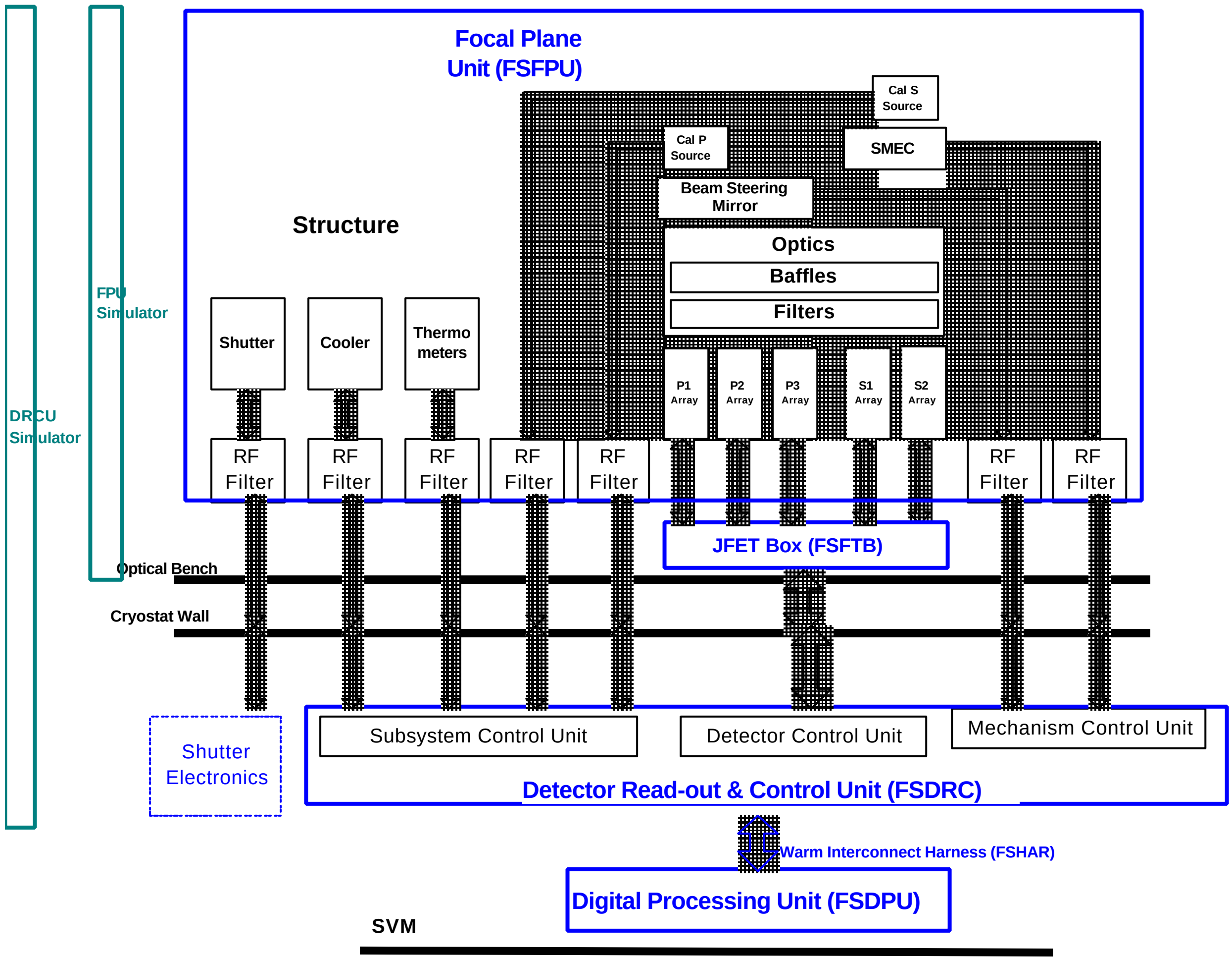
The SMECm is the mechanism which moves the mirrors, The mirrors are considered a part of SMECm.
Basically, the movement of the mirrors is a translation only, obtained through the action of a linear actuator.
The position of the mirrors along their travel is measured by an incremental optical sensor coupled to a rule.
The mechanical design is based on the GSFC design for a balloon project. A base plate supports the mechanism and is mounted on the SPIRE Optical Bench (Structure). On the baseplate are mounted the fixed part of the actuator and the optical encoder. A moving plate supports the rooftop mirrors and the rule for the optical encoder. The base plate and the mirror moving plate are linked by four "legs". Each leg has two arms, one arm linking the base plate and the intermediate moving plate, the other linking the intermediate moving plate and the mirror moving plate. The articulations at both extremities of the legs use flex pivots. The stiffness of the articulation is very low to keep the actuator power consumption within the specified limits. Consequently, for SPIRE, a launch latch item is added to allow the mechanism to sustain the launch vibrations without damage. The latch is placed between the baseplate and the mirror moving plate.

- **The preamplifier** (SMECp)

Due to the loss of current on the output signals of the optical encoders when they are cooled down to 4K, a preamplifier is necessary (TBC). The electronic components (JFETs, etc..) are implemented on a card integrated in a separate box on the SPIRE structure. The temperature of the components is set around 100K.

- **The Mechanisms Control Unit** (MCU)

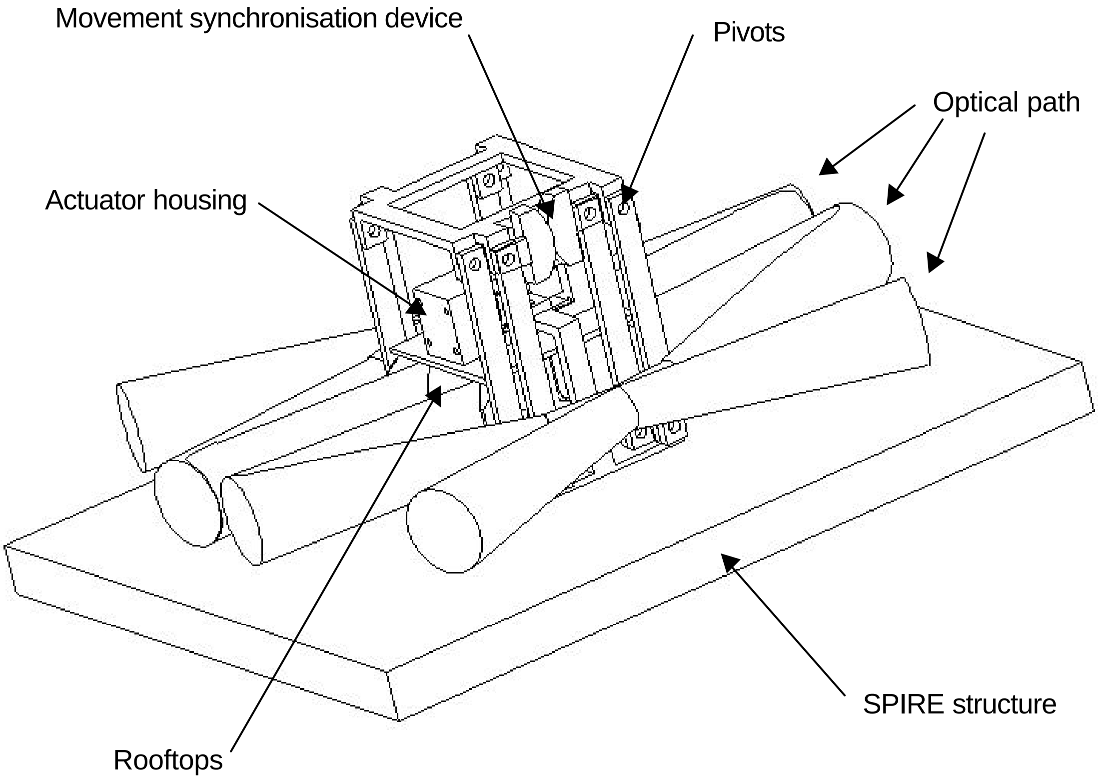
The SMEC warm electronic comprises the SMEC analog electronic i.e. the power amplifier for the actuator, the position acquisition electronics and interface unit and the limit position sensors conditioning. The main and redundant circuitry are implemented on one board.
This board is a part of the Mechanism Control Unit (MCU) which comprises the SMEC board, the BSM board and the Multi Axis Controller (MAC) board which houses the interface electronics (FPGA) and the mechanism control electronics (DSP based). The MAC board takes charge of the commands sent by SPIRE Digital Processing Unit (DPU) via the Digital Read-out Control Unit (DRCU), controls the movement of the mechanisms via the relevant analog board, delivers the position measurements and transmits the housekeeping data to SPIRE DPU via the DRCU.
The power is provided by the DRCU in which the MCU is integrated.



SPIRE Block Diagram

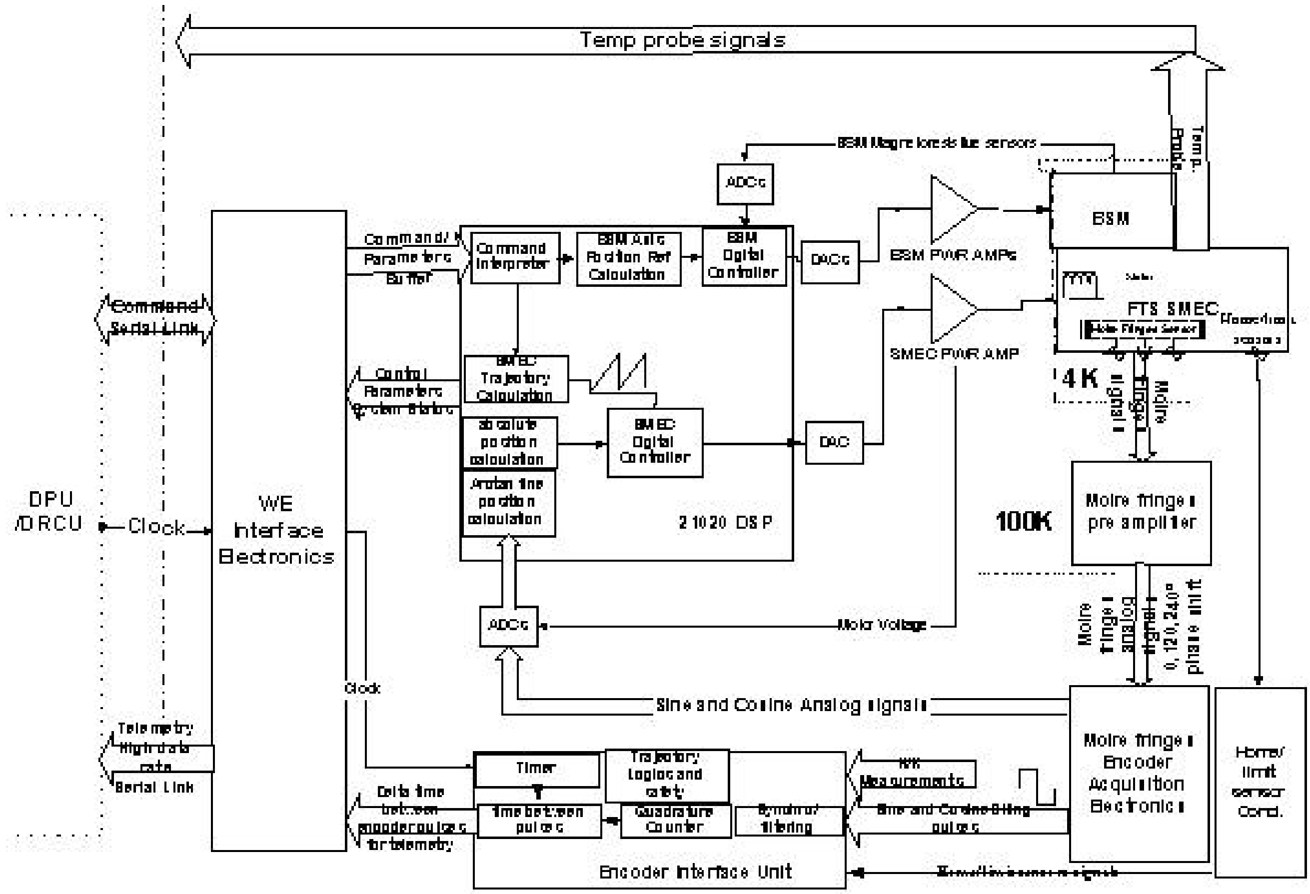
This diagram shows the links between the SMEC, the BSM, the MCU, the DRCU and the DPU.

View of the GSFC mechanism
The optical path has been symbolized for show.



MCU schematics

The 21020 DSP is the heart of the control system. It controls both the SMEC and the BSM FPU subsystems. It is integrated in the DRCU.



4. Constraints

4.1. Development constraints

4.1.1. Technical constraints

Note : the figures hereafter are for information only. The applicable figures are in [AD1] which refers to [RD1]

The main performances specifications are:

- The mirror travel is +/-3.2 mm, -3.2/35.2 mm is a goal.
- The mirror speed is nominally 0.5 mm/s with a 0.01mm/s rms stability filtered with a TBD filter on the travel over a 24 hours period.
- The speed value should be selectable from 0.2 to 1mm/s, up to 2mm/s is desirable.
- The mirrors tilt along travel axis = TBD arcminutes / TBD mm
- The measurement specification of the accuracy of the mirror position is 0.1µm over a 6.4mm travel, 0.3µm elsewhere.
- The measurement resolution of the mirror position is 0.5µm over the complete travel.

The main technical constraints are :

- SPIRE lifetime on orbit = 4.25 years
- SPIRE spectrometer lifetime on orbit = 9 months
- SMECm operating temperature = 4K
- SMECm power = less than 7.4 mW
- SMECm mass = 1.2 kg including 20% margin and excluding mirrors
- SMECm CoG position = TBD
- SMECm volume = TBD mm3
- SMECm and MCU level of radiations = TBD
- SMECm vibrations level = TBD at 4K
- SMECm shock level = TBD at 4K
- Format of the MCU electronic cards = double Europe
- Cleanliness = TBD

During its lifetime,

The SMEC is :

- designed under LAM responsibility.
- manufactured under LAM responsibility, part at LAM, part in the industry.
- qualified/accepted and calibrated under LAM responsibility, part at LAM, part at RAL (cryovibrations), part in the industry (EMI-EMC). The qualification/acceptance program includes thermal cycling, warm and cold vibrations, life testing, EMI-EMC. The calibration program verifies the performance requirements.

The SMECm is :

- transported to RAL under LAM responsibility.
- integrated at RAL in the SPIRE FPU Structure under joint RAL, MSSL and LAM responsibility.

The SMECp is :

- transported to RAL under LAM responsibility
- integrated in the JPL JFET Box under joint RAL, JPL and LAM responsibility.

The SPIRE-FPU is to undergo the project qualification/acceptance program under RAL responsibility.

The MCU is:

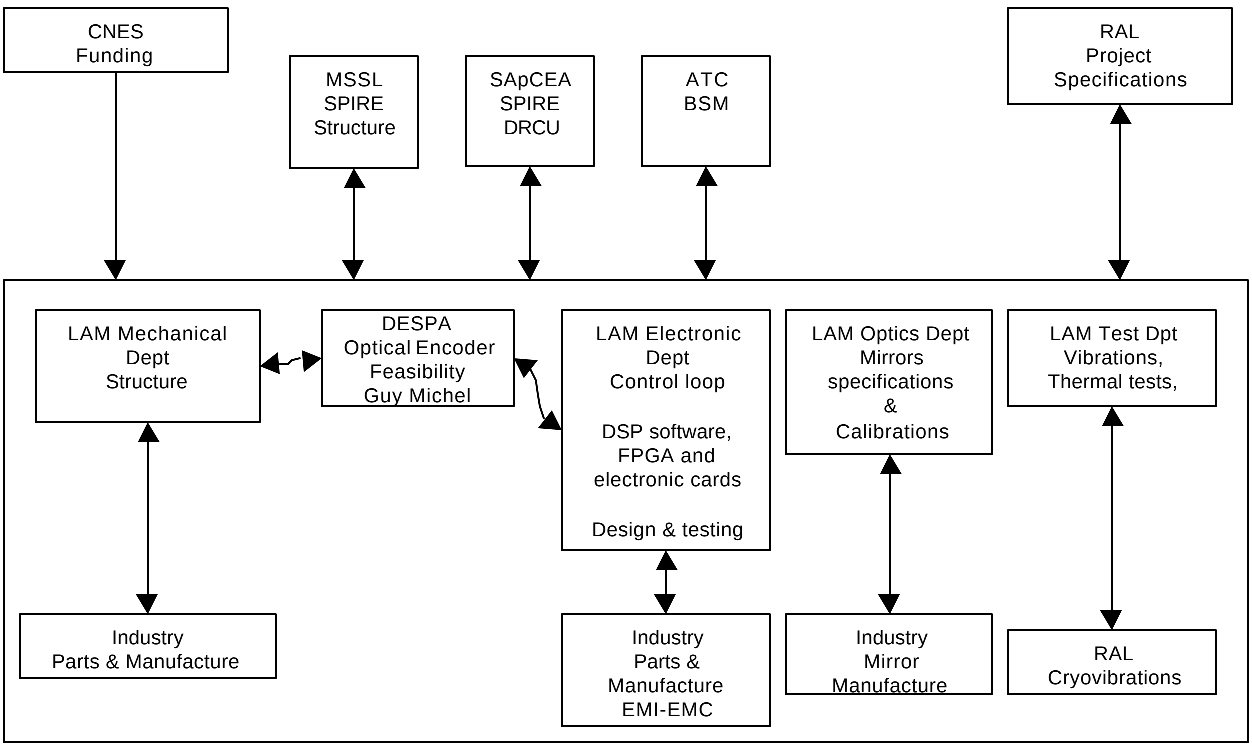
- designed under LAM responsibility.
- manufactured under LAM responsibility, part at LAM, part in the industry.
- qualified/accepted under LAM responsibility, part at LAM, part at CEA. The qualification/acceptance program includes thermal cycling, warm vibrations, EMI-EMC, tests with the SMECm, the BSMm and their associated boards.
- transported to CEA-Sap under LAM responsibility.
- integrated at CEA-Sap in the SPIRE DRCU (part of the SPIRE WE) under CEA Sap responsibility.

The SPIRE-WE is to undergo the project qualification/acceptance program under CEA-Sap responsibility.

The SPIRE WE and the SPIRE FPU are integrated under RAL responsibility and undergo the project calibration program under RAL responsibility.
SPIRE is delivered to ESA under RAL responsibility.
SPIRE is integrated in the FIRST satellite under ESA responsibility.
SPIRE CQM is to undergo the ESA test program under ESA responsibility.
SPIRE PFM is to undergo the ESA Acceptance program.
On the launch pad, before launching, the SPIRE FPU is cooled down to its operating temperature and launched cold.
SPIRE FS is prepared in the event of SPIRE PFM failure.

4.1.2. Organisation

LAM is responsible for the SMEC, (SMECm plus SMECp) and for the MCU which comprises the MAC board, the SMEC board and the BSM board.
Under LAM responsibility, DESPA is responsible for the optical encoder feasibility. Once the feasibility is demonstrated, LAM designs the necessary modifications and qualifies the optical encoder for the space and cryogenic SPIRE application. The encoders are manufactured in the industry and by LAM.
LAM designs the electronics of the subsystem and builds the relevant breadboards. The electronics manufacture is subcontracted to the industry.
ATC is responsible for the Beam Steering Mirror Cryomechanism whose control loop is implemented in the MCU by LAM. ATC is responsible for the end to end performances of the BSM.
JPL is responsible for the JFET box inside which the SMECp is implemented.
Sap-CEA is responsible for SPIRE DRCU inside which the MCU is implemented.
MSSL is responsible for the structure inside which the SMECm is integrated.



4.1.3. Calendar constraints

The main SPIRE project rendez-vous are [RD2]:

Milestone	Date
PDR	Jun 2000
DDR - Interface review	Oct 2000
DDR - BSM & SMEC	Jan 2001 (TBC)
LAM delivers the SMECm/p Simulator to CEA	Sep 2001
LAM delivers the MCU-EM to CEA	Dec 2001
SMECm and BSMm CQM delivery to SPIRE	Apr 2002
LAM delivers the MCU-QM1 to CEA	Juil 2002
LAM delivers the MCU-QM2 to CEA	Jan 2003
CDR	Dec 2002
RAL delivers SPIRE CQM to ESA	Apr 2003
LAM delivers the MCU-PFM to CEA	Sep 2003
LAM delivers SMECm/p and BSMm PFM to RAL	Mar 2004
RAL delivers SPIRE PFM to ESA	Nov 2004
LAM delivers SMECm/p and BSMm FS to RAL	May 2005
RAL delivers SPIRE FS to ESA	Dec 2005
FIRST launch	2007

4.2. Risk analysis

In this document, the risk analysis concerns only the risks conducting to this development plan not being completed.

Risk	Impact	Preventive action	Note
FIRST Microvibrations level and spectrum	Problem meeting performance requirements	Know the level and spectrum ASAP	This level has a direct impact on the speed stability. Must be included during design
Optical encoder qualification failure	Delay in design Problem meeting performance requirements	None	If it turns out that it is not possible to qualify the optical encoder for the flight, a new position sensor will have to be found and a delay in the delivery dates will occur. This delay is due to the fact that LAM cannot provide the manpower and the budget that would be necessary to conduct the development of a baseline solution along with a back-up solution. As the optical encoder is the only one that meets the performance specifications, inevitably, the new one will not meet all of them and a trade-off will have to be made at system level. A possible candidate would be an LVDT.
Flex Pivot problems (parasitic resonances, life tests)	Delay, Power consumption increase	Provision for different types of pivots	Replace flex pivots by more rigid pivots. => increase in power consumption
New distribution of work among the consortium members	This development plan is not applicable any more.	None	If the project redefines the distribution of work and LAM has not to provide what is described in this plan with the described organisation, this plan will no longer be applicable and the whole LAM participation in

			SPIRE will be re-discussed with CNES, CEA and RAL.

4.3. Redundancy

- **Redundancy philosophy**

The redundancy philosophy adopted for SPIRE is to duplicate every part that would be a single point failure.
The MCU incorporates two complete sets of MAC cards with identical functions and the SMEC and BSM are fully redunded on their cards.
The SMECp incorporates two complete sets of cards with identical functions.
The SMECm incorporates two optical encoders and two actuator windings.
Every temperature measurement is duplicated.
From the system point of view, there are two separate electronic assemblies. No crossswitching of components is implemented at SMEC level. The switch from one assembly to the other is made at the DRCU level.

- **Launch latch**

The launch latch is made up of two identical items, mounted in series. If one fails, the other is able to free the mechanism.
In the event of the launch latch not unlocking after launch (i.e. both latches fail), the SPIRE spectrometer would be completely lost. To prevent that, the possibility to have a reduced travel (6.4 mm) around the ZPD point is studied. This travel is not latched during the launch. This is a backup mode.
This possibility is currently under study and decision will be made by DDR.

5. Work description

5.1. Development and model philosophy

The model philosophy is compliant with the SPIRE project requirements and meets the LAM development needs.

5.1.1. Preliminary Design (*Phase B*)

The mechanical design is based on the GSFC design. The first resonance frequencies and the mass are verified by fem analysis. As a means of cross checking, a very low level sine test is performed on the GSFC prototype.
A launch latch mechanism principle is studied.
An actuator type is chosen.
The optical encoder is a critical part and a qualification program has to be established. To establish a start point for the qualification program, a series of cryogenic tests is conducted to check the survivability of the encoder and to measure its output signal at cryogenic temperature.
The tests leads to the SMECp specifications and the establishment of the list of components to be used for the flight in the optical encoder. These components include optical, electronic and mechanic ones.
The control loop design is verified by simulation and with a DSPACE system associated with mechanical mockups. The speed range and the speed stability are verified. The position accuracy is checked with a reference LASER source. The mockup is equiped with an actuator and the ground version of the SMECm PFM optical encoder and its stiffness is similar to the one expected on SMECm PFM.
The typical tests are defined. The typical tests are to be used through the life of the subsystem to check that it stays within the specifications. The typical tests are to be applied to the mechanism, the preamplifier and the warm electronic.
The interfaces with SPIRE WE are defined during this step.

The preliminary design is presented at the Preliminary Design Review. The PDR freezes the technical specifications and the interfaces.

5.1.2. Procurement of long delay components

Once the preliminary design has been validated by the PDR, the procurement for long delay components is initiated, if money is available. These components include actuators, flex pivots, cryogenic connectors, JFET's, etc.. to be mounted on the MCU, the SMECm and the SMECp CQM, PFM and FS.
The optical encoder critical components are procured. Those one cannot find in flight grade are individually tested. The tests are to demonstrate that these components are suitable for the flight. The tests concern the electronic components. They consist in warm tests for accelerated aging and cold tests. Radiation tests or analysis are conducted. No vibrations are conducted at that component level.

5.1.3. Detailed design and CQM manufacture (*Phase C/D*)

The detailed design encompasses all the functions of the subsystem. A draft of the on-board software is written.
The design is verified by more detailed modelisation where necessary.
Before the DDR, a launch latch mechanism mock-up is built to prove by tests that the design is flyable. The tests are warm vibrations, thermal cycles and operation at cryogenic temperature.

The detailed design is presented at the Detailed Design Review (mid October 2000). The DDR must have happened before CQM manufacture can begin. The typical tests are now frozen.

To verify the design, a complete qualification and lifetests are to be conducted (see §5) on the various models listed below.

Purpose	Model	Flight representativity	Difference w.r.t. flight	Comment
To verify the mechanical design verification (vibrations, carriage titls)	SMECm-STM	CoG, mass, dimensions, interfaces	No active component except non redunded launch latch	Also used for the SPIRE Structure tests
To verify the lifetime of SMECm components	SMECm-DM	Full, except…	… redundancies replaced with mass dummies	Copy of the SMECm-CQM
To verify the electronic design	SMECp-DM	Full, except…	.. redundancies replaced with mass dummies	Used with MCU and SMECm simulators.
To verify the electronic design	MCU-DM	Dimensions, interfaces, functions	Commercial components, no redundancy	Used with BSM, SMECp and SMECm simulators.
To secure the DRCU development	MCU-EM	Dimensions, interface, functions	Commercial components, no redundancy	Copy of the MCU-DM.
To qualify the SPIRE-FPU	SMECm-CQM SMECp-CQM MCU-QM1	Full, except… Full, except… Dimensions, interface, functions	… redundancies replaced with mass dummies Flight representative components only, no redundancy	The first complete SMEC subsystem.(except redundancies), tested with BSM-CQM
To qualify the SPIRE-WE	MCU-QM2	Dimensions, interfaces, functions, Redundancy	Flight representative components only	

For the verification of the SMEC, a DRCU simulator and an OGSE are to be developed. The DRCU simulator provides the DRCU/MCU interfaces including the power supply. The OGSE is used to check optically the mirror displacement.
For the verification of the MCU, a BSM simulator and a SMECm/p simulator are needed which simulate the relevant BSMm parameters and SMECm and SMECp parameters as seen from the BSM and the SMEC boards inside the MCU.
For the verification of SMECm, the SMECm EGSE allows for control and measurement of the mechanism during tests.
All the simulators and tools are needed since all subsystems are to be tested at approximately the same time.
After the SMEC-CQM delivery, the SPIRE CQM is tested at project level.
The results of the qualification tests are to be presented at the SPIRE CDR which is the start point of the PFM and FS manufacture.
Then, the SPIRE CQM is delivered to ESA for cryogenic tests of the FIRST payload.

5.1.4. Flight design modifications and PFM/FS manufacture

Following the SMEC lifetests and SPIRE CQM tests, some modifications may have to be implemented in the design.
The design changes are to be implemented in the flight design and be validated using the SMEC-DM and BSM-DM.
The MCU-PFM and the MCU-FS are then manufactured and undergo the acceptance tests.
The SMEC-PFM is then manufactured and undergoes the performance verification (associated with the BSMm-PFM and MCU-PFM) and acceptance tests.
The SMEC-FS is a duplicate of the SMEC-PFM and is manufactured at the same time as the SMEC-PFM. The SMEC-FS undergoes the performance verification (associated with the BSMm-PFM and MCU-PFM) and acceptance tests after the SMEC-PFM.
The SMECm-FS and SMECp-FS could be the SMECm-CQM and SMECp-CQM refurbished to flight level. This is TBC as it depends on ESA that the back delivery of the CQM arrives on time. For the moment, it is planned to manufacture a full new SMEC-FS.

5.2. Verification plan

The verification plan must be compliant with the project verification plan [AD2, RD1] and must fulfill the SMEC development needs.

In the tables below,

X =	a real test is realised
A =	an analysis is conducted
NA =	Non applicable

Basic performances are controlled during environmental testings. This control is based upon the typical test, defined during phase A, and allways performed following the same procedure.
300K vibrations are conducted at LAM.
Cryovibrations are conducted at RAL.
Vacuum cycles, soak cycles, thermal cycles (temperature >=20K) are conducted at LAM.
Lifetime tests are conducted at LAM.
EMI/EMC tests are conducted at INTESPACE.
Microphonics tests are conducted at TBD.
Performance tests are conducted at LAM.

5.2.1. SMECm

	SMECm-DM	SMECm-STM	SMECm-CQM	SMECm-PFM	SMECm-FS
Interface control	X	X	X	X	X
Mass mesasurement	X	X	X	X	X
CoG measurement	X	X	X	X	X
Launch latch test	X	X	X	X	X
Stiffness check	X	X	X	X	X
Carriage tilts measurement	X	X	X	X	X
Travel measurement	X	X(****)	X	X	X
Vibrations 300K	X	X	X	X	X
Vibrations 4K		X	X	X	X
Power Consumption measurement	X		X	X	X
Thermal/Vacuum cycle	X		X	X	X
Functional 4K test			X	X	X
Bakeout	X	X	X	X	X
Lifetime	X				
Radiation tolerance			A(**)	A(**)	A(**)
Microphonics			X(***)	X(***)	
EMI / EMC			A(*)	X(*)	A(*)

(*) : EMI/EMC tests are to be conducted on the PFM only if design changes have occurred.
(**) : The radiation tolerance is verified by analysis only, taking into account the materials involved.
(***) : Microphonic tests are to be conducted at the SPIRE FPU level only.
(****) : done to check that the possible travel is the expected one. No real actuator implemented.

5.2.2. SMECp

	SMECp-DM	SMECp-CQM	SMECp-PFM	SMECp-FS
Dimensions measurement	X	X	X	X
Vibrations 300K	A	X	X	X
Vibrations 100K (TBC)		X	X	X
Power Consumption mearurement		X	X	X
Bake out		X	X	X
Thermal/Vacuum cycle		X	X	X
Thermal Range		X	X	X
Thermal stability		X	X	X
Lifetime		A		
Radiation tolerance	A (**)	A(**)	A (**)	A (**)
EMI / EMC	A	X	(*)	(*)

(*) : As EMI/EMC is verified on the CQM, no further verification are conducted on the subsequent models.
(**) : The radiation tolerance is verified by analysis only, taking into account the materials involved.

5.2.3. MCU

	MCU-DM	MCU-EM	MCU-QM1	MCU-QM2	MCU-PFM	MCU-FS
Interface checks	X	X	X	X	X	X
Power Consumption measurement	X	X	X	X	X	X
Vibrations 300K	NA	NA	NA	X	X	X
Soak/Cycle	NA	NA	NA	X	X	X
Radiation tolerance	A(**)	A(**)	A(**)	A(**)	A (**)	A (**)
Thermal Range	A	A	NA	X	X	X
Thermal stability	A	A	NA	X	X	X
EMI / EMC	A(*)	A(*)	A(*)	A(*)	A(*)	A(*)

(*) : EMI-EMC is verified by analysis at subsystem level and verified by tests once integrated in SPIRE WE.
(**) : The radiation tolerance is verified by analysis only, taking into account the materials and the components involved.
(***) : Lifetime duration is verified by analysis only taking into account the materials and the components involved.

5.2.4. SMEC

At the spectrometer mirror mechanism subsystem level, the performances are thoroughly verified.
They are checked both at 300K and at its operating temperatures.

In every operational modes,	SMEC-DM	SMEC-STM	SMEC-CQM	SMEC-PFM	SMEC-FS
Travel range	X	NA	X	X	X
Speed range	X	NA	X	X	X
Speed stability	X	NA	X	X	X
Position measurement accuracy	X	NA	X	X	X
Mirror movement (tilts)	X	NA	X	X	X
Travel/Speed calibration	X	NA	X	X	X
Power consumption	X	NA	X	X	X

5.2.5. BSM

For the BSM board, the verification is included in the MCU verification.
The verification of the BSMm is done first at ATC (see the BSM development plan) and with SMEC once integrated with the MCU. Details are TBD

5.3. Ground associated equipment

The ground equipments are used to develop and test one item without the presence of the others.
Only the equipements needed for SMEC development are listed.
The simulators replace one or more items.
The tools are used to operate, check or integrate an item.
Most simulators are PC based as it is the most flexible and economical solution.

5.3.1. Simulators

Simulator	Used for…	Functions
DRCU Simulator	…the control and monitoring of the MCU during tests and commissionning	Replaces DRCU Receives position data, synchro signals and temperature signals. Simulates Interfaces: Serial, Parallel, Analog and Synch. Bus Supplies power. Sends commands.
SMECm/p Simulator	…MCU development and testing and …SMECp development and testing and …post DRCU / MCU integration testing.	Replaces SMECm and/or SMECp.(at will) Receives actuator current values. Simulates the main parameters of the real SMECm : resonance frequencies, stiffness, noises. Delivers simulated thermometer values and simulated preamplified or non-preamplified optical encoder signals

5.3.2. Tools

Tool	Used for …	Functions
SMECm EGSE	… SMECm and SMECp development and testing	Replaces MCU. Can be plugged in the SMECm simulator for SMECp testing purposes. Receives commands : travel range, speed value. Is able to control and monitor SMECm and SMECp Sends actuator current analog values, powers the temperature sensors and the optical encoder Receives and processes temperature, actuator current, synchro signals and preamplified or non-preamplified position measurements. Sums up the operational time.
SMECm AT	…mirror cinematic checking and …mirror alignment w.r.t. SMECm baseplate	Measures travel range, mirror position, mirror tilt around travel axis.
SMECm OGSE	…SMECm alignment in SPIRE spectrometer structure	Allows SMECm position control and adjustement inside SPIRE spectrometer structure.
SMECm MGSE	…SMECm Integration in the SPIRE spectrometer structure or in any test equipment	Allows SMECm handling during its integration in a structure.

5.3.3. Additional equipment

6. Development calendar

			Dates	Notes
Dvlpt		Mechanical development and STM	Jun 2000 - Jun 2001	Begins after PDR
	STM	Delivery	Beginning Jun 2001	
	MCU Electronic	Development	Jun 2000 - Jun 2001	
	SMECm DM	Manufacture, Qualification, Calibration, lifetests	Jun 2001 - Sep 2002	
CQM	MCU & SMECm	Manufacture, qualification & calibration	Mar 2001 - Feb 2002	
	BSM Board	Design, manufacture & tests	Apr - Oct 2001	
	BSMm CQM	Delivery to LAM	Feb 2002	BSM Development plan [AD4]
	SMEC+BSM	Tests	Feb - Apr 2002	
		Delivery to RAL and CEA	Beginning Apr 2002	
CDR			Dec 2002	
PFM & FS	MCU & SMEC	Manufacture	Feb 2002 - Apr 2003	Manufacture will begin before CDR and modifs will be made after CDR Dependant on the CDR date
	MCU PFM	Acceptance tests	Jun - Jul 2003	Using BSMm+SMECm DM or simulators
	MCU PFM	Delivery to CEA	Sep 2003	
	MCU FS	Acceptance tests	Apr - May 2003	Using BSMm+SMECm DM or simulators
	SMEC PFM	Acceptance & calibration	Apr - Oct 2003	
	BSM PFM	Delivery to LAM	Jun 2003	BSM Development plan [AD4]
	PFM SMEC + BSM	Tests	Oct - Dec 2003	Using MCU FS
	SMEC + BSM PFM	Delivery to RAL	Beginning Feb 2004	14 months after CDR
	SMEC FS	Acceptance & calibration	Dec 2003 - May 2004	Begins after end of PFM
	BSM FS	Delivery to LAM	Aug 2003	BSM Development plan [AD4]
	SMEC + BSM FS	Tests	May - Jun 2004	Using MCU FS
	SMEC + BSM FS	Delivery to RAL	Beginning Oct 2004	8 months after end of PFM
	MCU FS	Delivery to CEA	Beginning Oct 2004	

Detailed planning in file SMEC_DevpPlan_20000620.mpp.

7. Description of deliverables

7.1. Deliverable models

7.1.1. MCU models

Model	Flight representativity	Difference with flight	Deliverables	Delivered to
EM	Dimensions, interface, functions	No redundancy, commercial components, power consumption	1	CEA
QM1	Dimensions, interface, functions	No redundancy, flight equivalent components	1	CEA
QM2	Dimensions, interface, functions,	Flight equivalent components	1	CEA

	redundancy			
PFM	100%	None	1	CEA
FS	100%	None	1	CEA

7.1.2. SMECp models

Model	Flight representativity	Difference with flight	Deliverables	Delivered to
CQM	100%, except…	… no redundancy	1	RAL
PFM	100%	None	1	RAL
FS	100%	None	1	RAL

7.1.3. SMECm models

LAM will deliver the BSMm at the same time as the SMECm models (Not applicable to the STM)

Model	Flight representativity	Difference with flight	Deliverables	Delivered to
STM	25% (Mass, CoG, Stiffnesses)	No active components, only mass dummies	1	MSSL
CQM	100%, except…	… no redundancy, only mass dummies	1	RAL
PFM	100%	None	1	RAL
FS	100%	None	1	RAL

7.2. Associated equipment

The associated equipment is for integration and alignement.

Model	Use/Function	Associated with	Deliverable
MCU SIM	Controls the MCU/DRCU interfaces Simulates the MCU as seen from the DRCU	Any SPIRE WE model	1 to CEA
MECm SIM	Simulates the electrical interfaces of the SMECm and BSMm during MCU integration into DRCU	Any deliverable MCU	1 to CEA, 1 to RAL
SMECm EGSE	SMECm control and monitor during integration and before and after transportation	Any deliverable SMECm and SMECp	1 to RAL
SMECm MGSE	SMECm integration in the SPIRE Structure	Any deliverable SMECm	1 to MSSL (for the STM) and 3 to RAL (1 with the CQM, 1 with the PFM, 1 with the FS)
SMECm OGSE	SMECm alignment after integration in SPIRE structure	Any deliverable SMECm	1 to RAL(TBC)

7.3. Associated documentation

The documentation is TBD.