Herschel

DPU/ICU Subsystem Development Plan

Document Ref.: SPIRE-IFS-PRJ-000469

Issue: 1.4

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Document Status Sheet:

Document Title: Herschel DPU/ICU Subsystem Development Plan			
Issue	Revision	Date	Reason for Change
Draft 1		23 May 2000	First draft
Issue1		30 October 2000	Issue 1
Issue 1.1		30 January 2001	Different plannings and miscell.
Issue 1.2		2 April 2001	After ICU PDR (HIFI) and DPU PDR (PACS)
Issue 1.3		23 October 2001	After CDR1&2 at CGS
Issue 1.4		20 February 2002	For IBDR

Document Change Record :

Document Title: Herschel DPU/ICU Subsystem Development Plan	
Document Reference Number: SPIRE-IFS-PRJ-000469	
Document Issue/Revision Number: Issue 1.4	
Section	Reason For Change
3.1	Overall DPU/ICU block diagram
4.1	HIFI CDR date
7	HW calendar and SW calendar
9	Corrections of plannings after contract ASI-CGS signature
ISSUE 1.2	
All sections	Updated/revised after ICU PDR (HIFI) and DPU PDR (PACS)
Issue 1.3	
Sect. 2.2	Updated Reference Documents
Sect 2.3	Updated Acronyms
Sect. 5.1	Updated
Sect. 5.3	Some AVM OBS features added; EQM updated
Sect. 9	Updated Schedules
Issue 1.4	
Sect. 2	Updated
Sect. 9	Updated Schedules
Sect. 4.1	Updated

Sect. 5.1	Updated
Sect. 5.2	Updated
Sect. 5.4.5	Updated
Sect. 5.4.7	Note 4 modified
Sect. 5.5.5	Updated
Sect. 7.1	Updated
Sect. 7.2	Updated
Sect. 8.2	Updated
Sect. 9.1	Updated
Sect. 9.2	Updated
Sect. 9.3	Updated
Sect. 9.4	Updated
Sect. 9.5	Updated

1 Scope of the document

This document describes the development plan of the Herschel Data Processing Unit/Instrument Control Unit hardware and software:

PACS DPU

HIFI ICU

SPIRE DPU

The development plan is based on the applicable documents listed in paragraph #2.

2 Documents

2.1 Applicable documents

AD1	Herschel/Planck Instrument Interface Document Part A	PT-IID-A-04624
AD2	Herschel/Planck Instrument Interface Document Part B – Instrument “PACS”	PT-PACS-02126
AD3	Herschel/Planck Instrument Interface Document Part B – Instrument “HIFI”	PT-HIFI-02125
AD4	Herschel/Planck Instrument Interface Document Part B- Instrument “SPIRE”	PT-SPIRE-02124
AD5	PACS Design Development and Verification Plan	PACS-ME-PL-002
AD6	HIFI Instrument Development and Verification plan	SRON-U/HIFI/PL/2000-010
AD7	SPIRE Instrument Development plan	SPIRE-RAL-PRJ-000035
AD8	HIFI ICU Subsystem Specification Document	IFSI/ICU/SP/2000-001
AD9	SPIRE DPU Subsystem Specification Document	SPIRE-IFS-PRJ-000462
AD10	PACS DPU Subsystem Specification Document	PACS-CR-GS-006

AD11	HIFI Interface Control Document	SRON-G/HIFI/SP/1999-001
AD12	SPIRE DPU Interface Control Document	SPIRE-IFS-PRJ-000650
AD13	PACS Hardware Specification/Interface Control Document	PACS-xx-xx-001
AD14	DPU/ICU On Board Software User Requirements Document PACS	PACS-CR-RD-001
AD15	DPU/ICU On Board Software User Requirements Document HIFI	IFSI/OBS/SP/2000-001
AD16	DPU/ICU On Board Software User Requirements Document SPIRE	SPIRE-IFS-PRJ-000444
AD17	HIFI Instrument Specification	SRON-G/HIFI/SP/1998-001
AD18	PACS Instrument Specification Document	
AD19	SPIRE Instrument Requirements Document	SPIRE-RAL-PRJ-000034
AD20	DPU/ICU Product Assurance Plan	IFSI/ICU/PL/1999-001
AD21	DPU/ICU On Board Software Product Assurance Plan	IFSI/OBS/PL/2000-001
AD22	Herschel/Planck Packet Structure Interface Control Document	SCI-PT-ICD-7527
AD23	F/P CDMS Interface Test Requirements Specifications	SRON-U/HIFI-SP-2000-5
AD24	DPU/ICU Spacecraft Interface Acceptance Test Plan	CNR.IFSI.2001TR04 Draft 0.1
AD25	DPU/ICU WBS	IFSI/ICU/PL/2001-001

2.2 Reference documents

RD1	HSO DPU/ICU Switch-ON Procedure	CNR.IFSI.2001TR01
RD2	HSO DPU/ICU Power Budget	CNR.IFSI.1001TR03
RD3	HSO DPU/ICU Spacecraft Interface Acceptance Test Plan	CNR.IFSI.1001TR04

2.3 Acronyms

AD	Architectural Design
Adx	Applicable Document N. x
ASCII	American Standard Code for Information Interchange
ATP	Authorization To Proceed
AVM	Avionic Model
CASE	Computer Aided Software Engineering
CDMS	Central Data Management System
CDMU	Central Data Management Unit
CDR	Critical Design Review
CGS	Carlo Gavazzi Space
CNR	Consiglio Nazionale delle Ricerche
CPP	Co-ordinated Parts Procurement
CPU	Control Processing Unit
DDD	Detailed Design Document

DPU	Digital Processing Unit
DRB	Delivery Review Board
DRCU	Detector Readout Control Unit
EEPROM	Electrically Erasable Programmable Read Only Memory
EGSE	Electronic Ground Support Equipment
ESA	European Space Agency
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
FCU	Focal plane Control Unit
FIRST	Far InfraRed and Submillimeter Telescope
HIFI	Heterodyne Instrument for FIRST
HK	HouseKeeping
HRS	High Resolution Spectrometer
HSO	Herschel Space Observatory
HW	HardWare
IBDR	Instrument Baseline Design Review
ICD	Interface Control Document
ICDR	Instrument Critical Design Review
ICU	Instrument Control Unit
IHDR	Instrument Hardware Design Review
I/F	InterFace
IFSI	Istituto di Fisica dello Spazio Interplanetario
ISVR	Instrument Science Verification Review
NCR	Non Conformance Report

OBS	On-Board Software
PACS	Photoconductor Array Camera and Spectrometer
PA	Product Assurance
PDR	\Preliminary Design Review
PROM	Programmable Read Only Memory
QA	Quality Assurance
RDX	Reference Document X
RID	Review Item Discrepancy
S/C	Spacecraft
S/S	Subsystem
SCCS	Source Code Control System
SCR	Software Change Request
SPIRE	Spectral and Photometric Imaging Receiver
SPR	Software Problem Report
SPU	Signal Processing Unit
SR	Software Requirement
SSD	Software Specification Document
SVVP	Software Verification and Validation Plan
SW	SoftWare
TBC	To Be Confirmed
TBD	To Be Defined
TRB	Test Review Board
TRR	Test Readiness Review
TRRB	Test Readiness Review Board

TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
UR	User Requirement
URD	UR Document
WBS	Wide Band Spectrometer
WBS	Work Breakdown Structure
WP	Work Package

3 Description of the DPU/ICU subsystem

The DPU/ICU is based on a 20 MHz clock TEMIC TSC21020, that is a Digital Signal Processing (DSP) developed by Analogue Devices and manufactured and qualified for flight use by TEMIC.

The DSP implements a Harvard architecture, i.e. the data bus (32 bit) and the program bus (48 bit) are completely separated, so increasing the execution speed.

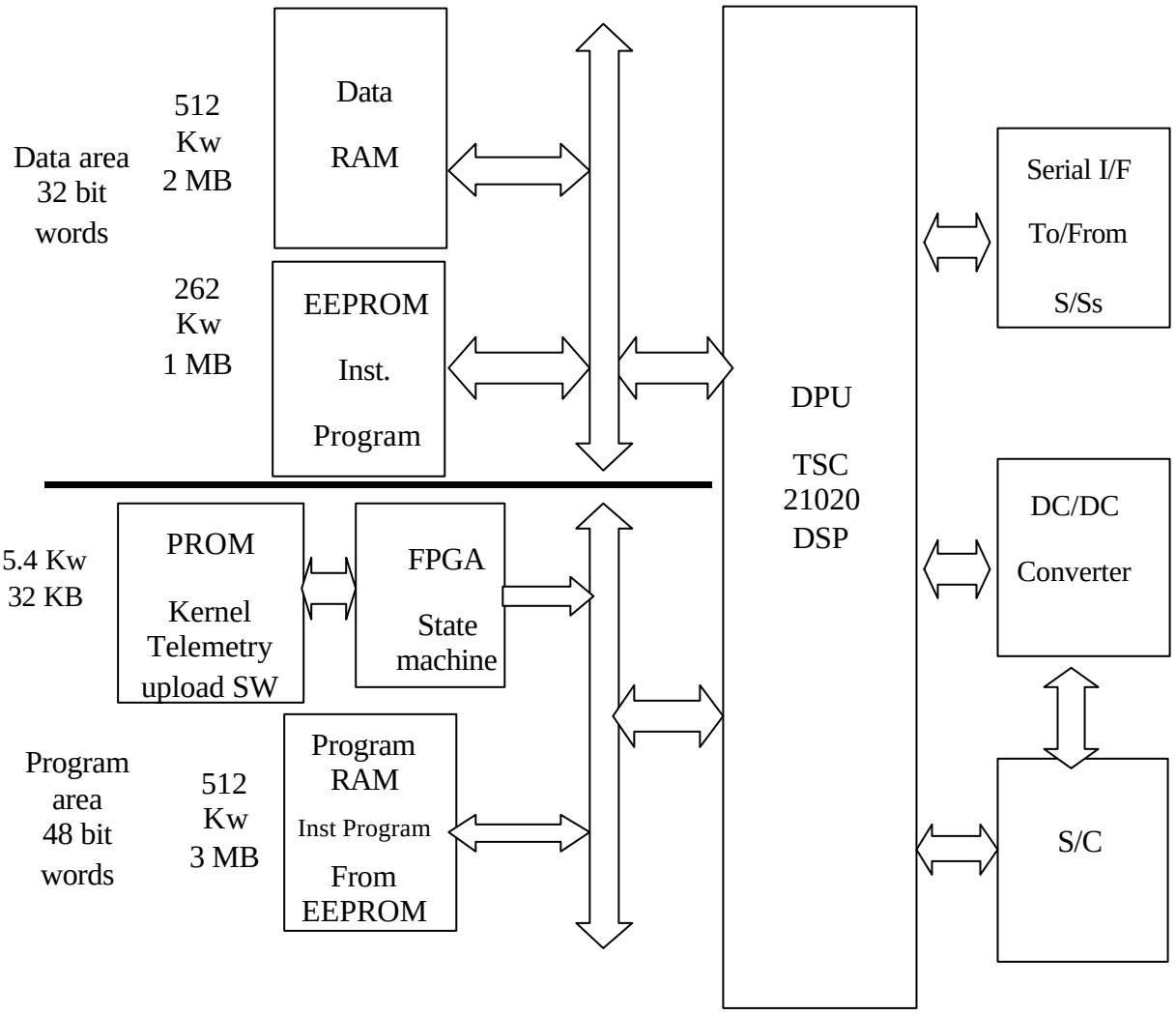
The program area is implemented with PROMs, EEPROMs and RAM. The PROM stores the initial boot loader and emergency recovery modules. At switch on a state machine, implemented in a FPGA, while keeping the DSP in a reset state, copies the PROM content in a suitable program area, the DSP reset is then removed and the basic program runs. After a series of tests (see RD1) the EEPROM content is copied in a suitable program area and the application program starts.

Part of the program area may be used as data memory.

The DPU/ICU includes a DC/DC converter with internal synchronization to supply internal circuitry, and to supply FCU S/S in HIFI.

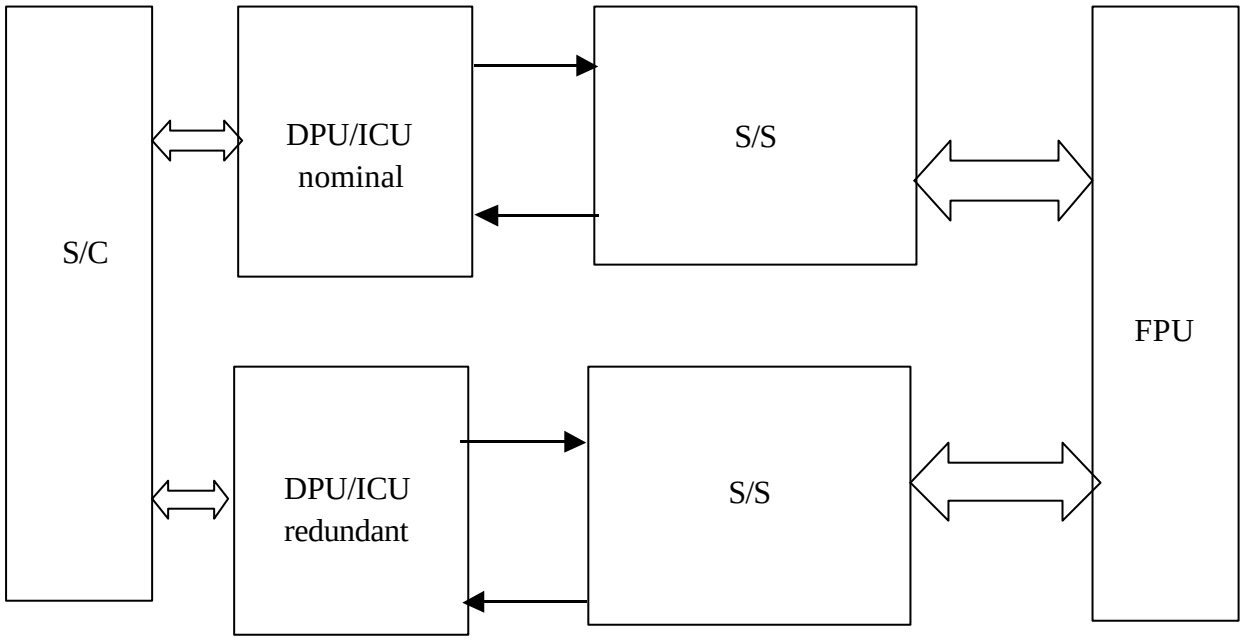
3.1 Overall DPU/ICU block diagram

The following diagram shows the main DPU/ICU blocks and the memory dimensions.



3.2 Redundancy concept

The top level DPU/ICU redundancy concept is shown in the following diagram:



The DPU/ICU box contains two complete units in cold redundancy states. The S/C nominal/redundant 28V power bus controls the switching between the two units.

3.3 DPU/ICU Product Tree

CI IDENTIFICATION	NAME	DELIVERABLE MODELS			
		A	Q	F	S
xxx-DPU/ICU	DPU/ICU Unit	X	X	X	
xxx –DPU/ICU-EL	DPU/ICU Electronics	X	X	X	
xxx -DPU/ICU-EL-1	Boards	X	X	X	
xxx -DPU/ICU-EL-1.1	CPU board Prime	X	X	X	*
xxx -DPU/ICU-EL-1.2	CPU board Redundant		X	X	*
xxx -DPU/ICU-EL-1.3	Interface Board Prime	X	X	X	
xxx -DPU/ICU-EL-1.4	Interface Board Redundant		X	X	X
xxx -DPU/ICU-EL-1.5	DC/DC Conv. Board for DPU/ICU (one conv.)	X			
xxx -DPU/ICU-EL-1.6	DC/DC Conv. Board for ICU and HIFI FCU (2 conv.)	X			
xxx -DPU/ICU-EL-1.7	DC/DC Conv. Board for DPU (one conv.) or for HIFI (2 conv.)		X	X	*
xxx -DPU/ICU-EL-1.8	DC/DC Conv. Board for DPU (one conv.) or for HIFI (2 conv.)		X	X	X
xxx -DPU/ICU-EL-1.9	Motherboard	X	X	X	*
xxx -DPU/ICU-MS	Mechanical Box	X	X	X	

xxx -DPU/ICU-HWSE	Transport Container	X	X	X	
xxx -DPU/ICU-OBS	On Board Software	X	X	X	

N.B1: As far as the Flight Spare items are concerned, for the three Herschel instruments there will be:

- two motherboards for the three instruments
- One CPU board for HIFI and SPIRE
- One CPU board for PACS
- One interface board for PACS
- One interface board for HIFI/SPIRE
- One DC/DC converter board with only the DPU converter for PACS and SPIRE
- One DC/DC converter board with the ICU and the HIFI FCU converters

NB2: The item xxx -DPU/ICU-EL-1.6 for the HIFI AVM will consist in a single board, i.e. **for (all) the AVMs there will be no redundancy.**

NB3: Each box (QM and FM) will contain:

1 motherboard

2 CPU boards

2 Interface Boards

2 DC/DC converters Boards and for these:

- HIFI boards will each have two converters (for ICU and FCU)
- SPIRE and PACS boards will have each 1 converter only (for the DPU)

4 Constraints

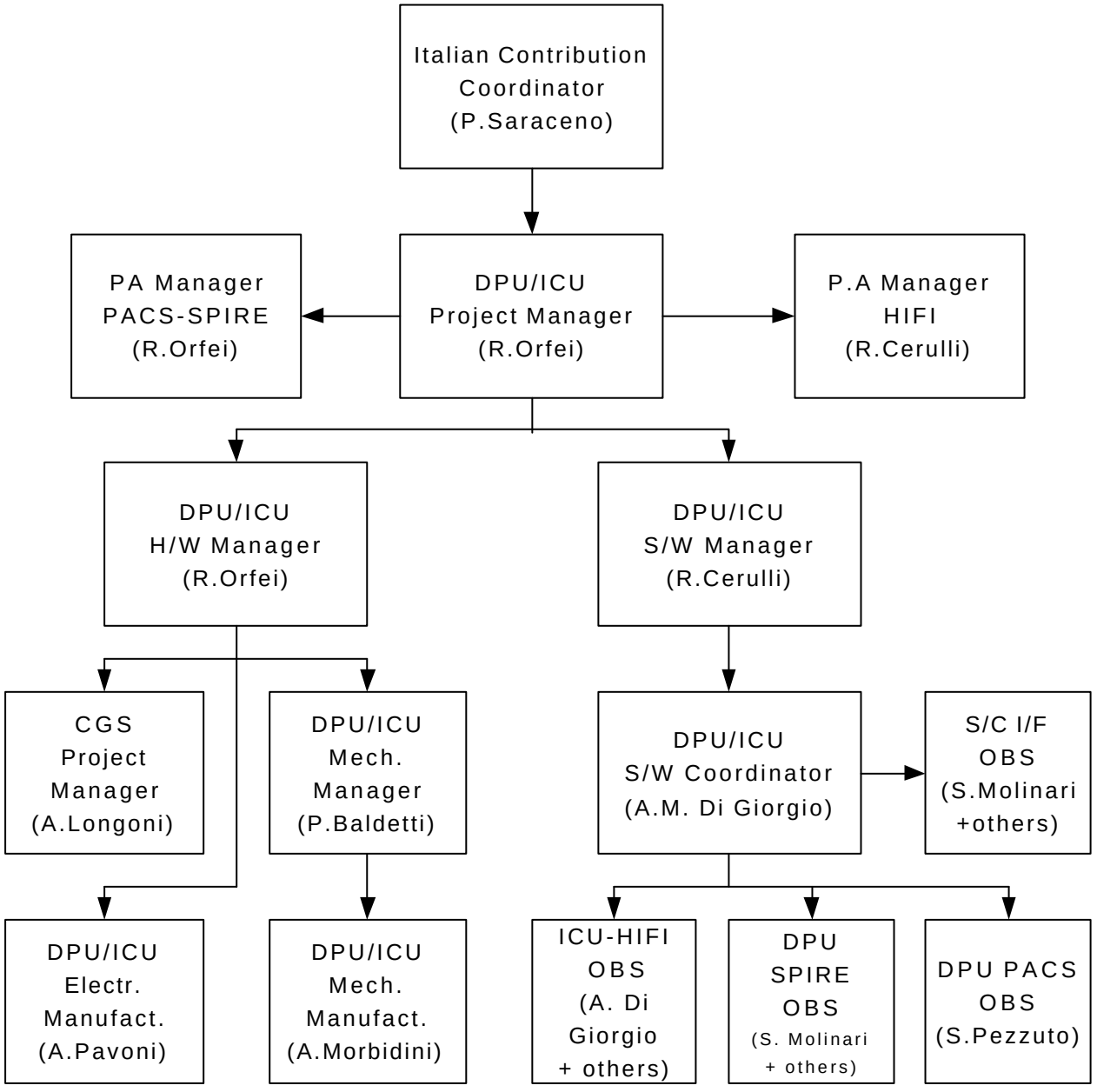
4.1 Calendar constraints

The main Herschel project constraints as far as the DPU/ICUs are concerned are:

ACTIVITY	PACS	HIFI	SPIRE
DPU/ICU PDR/IIDR	1-03-2001	22-02-01	26-06-2000
DPU/ICU IBDR	27-02-2002	14-03-2002	5-03-2002
AVM delivery to consortium	15-03-2002	29-03-2002	26-04-2002
CDR	Dec 02	01-02-03	Dec 02
AVM delivery to ESA	Apr 03	Apr 03	Apr 03
EQM delivery to consortium	7-11-2002	18-12-2002	21-01-2003
PFM delivery to consortium	29-9-2003	02-01-2004	05-03-2004
PFM delivery to ESA	Jul 04	Jul 04	Nov 04
FS delivery to consortium	NA	NA	NA
FS delivery to ESA	Dec 05	Dec 05	Dec 05
Herschel launch	1st quart. 2007	1st quart. 2007	1st quart. 2007

5 HW Work description

5.1 IFSI Management Structure



5.2 Carlo Gavazzi Space Management Structure

Name	Function
Angelo Longoni	Project Manager
Flavio Facchin	Project Controller
E. Francini	PA & Safety Manager
Sergio Legramandi	PA & Safety
Luca Tunesi	System Engineer
Massimo Vitta	Hardware Engineer
M. La Bella	Power Engineer
Maria Lucia Tampellini	Software Design
Alberto Dell'Acqua	Manufacturing

5.3 Development and model philosophy

All the DPU/ICU electronic boards, together with the boot software, will be manufactured by CGS under a contract with ASI-IFSI and implementing the specifications for the boards design and manufacturing and for the PROM software provided by IFSI. IFSI will:

- design and manufacture the mechanical box,
- integrate the electronic boards with the box and the front wall mounted connectors,
- design and test the application software,
- perform all tests including the environmental tests.

The following units will be manufactured, tested and delivered:

AVM

This unit is electrically, mechanically and thermally representative of the flight unit, but without redundancy. It will use standard commercial components.

The AVM OBS will be upgradable via EGSE and capable to test the S/C I/F and the available S/S simulators.

EQM

This unit is electrically, mechanically and thermally representative of the flight unit, including redundancy. It will be built in accordance with the DPU/ICU product assurance plan except the EEE components quality level. The components will be as far as possible representative of the FM with respect to fit, form and function and at least at MIL-C quality level. This unit will undergo the full qualification tests.

PFM

This model is the flight unit and is built to the full extend of the DPU/ICU product assurance plan. This unit will undergo the environmental acceptance tests.

FS

These are just spare boards to be submitted to acceptance test. The FS is built to the same standard as FM. The boards will be stored in conformal coated condition.

5.4 Verification plan

The verification plan must be compliant with the project verification plans [AD5-7] and must fulfil the DPU/ICU development needs.

5.4.1 Definition

The verification is the assessment of Verification Categories to establish that the design and the implemented product are qualified. This means that each DPU/ICU realised “as built” in compliance with the Final Configuration Model baseline (“as designed”) is compliant with the Model Requirements Specification (“as required” baseline).

The following Verification Categories are taken into consideration:

- Testing
- Analysis
- Simulation
- Inspection
- Similarity
- Review of design.

The Verification process is extremely complex and for a number of reasons careful and balanced judgement shall be exercised:

the categories are not independent. Inspection gives input to other categories. Testing requires analysis for its definition as well as to interpret and to extend its results.

It is difficult to get good representative environments for testing, to define test levels and duration to verify critical features while not over-testing others.

It is difficult to represent well the hardware in analysis and simulation.

Analysis and testing should be well balanced both within and between different levels in the Product Tree.

Careful trade-off should always be made to economise as much as possible on hardware and on exposure, should the hardware be re-used.

Verification is a co-operative task of the whole System Engineering teams.

The Verification Campaign shall be initiated at the beginning of the Development Program, prior to producing and testing hardware, the term Design Justification may be used and relevant documentation may be used as Qualification/Verification evidence in the final campaign.

5.4.2 Formal aspects

A Design Verification Matrix shall be established in which for each item in the Subsystem Specification Document it is indicated which of the above Verification Categories are applicable.

The Verification process shall be under Configuration Control from the early stages of the development program.

A Verification Control Matrix shall be used to maintain traceability between the documented Verification Status evidence and the Subsystem Specification Document.

5.4.3 Mechanical Verification

For testing the reference is to the relevant sections of IID-A. Vibration tests will be carried out at TBD facilities.

5.4.4 Thermal Verification

For testing the reference is to the relevant sections of IID-A. Thermal vacuum tests will be carried out at TBD facilities.

5.4.5 Electrical and Software Verification

For hardware testing the reference is to the relevant sections of AD1-AD4, AD8-AD13, AD17-AD19, AD22-AD24.

A Functional Test Sequence will verify that all functions are tested before the delivery first to Consortia and then to ESA. A reduced functional test, testing key functions, will be defined for the Integrated System Tests. A quick version of this test, the Short Integrated System Test, will be developed to check the instruments health. A Short Functional Test based on HK parameters only will be defined in compliance with AD1.

Software Verification will comply with AD1 , AD14-AD16, AD22-AD24.

5.4.6 EMC Verification

For testing the reference is to the relevant sections of IID-A. EMC tests will be carried out at TBD facilities.

5.4.7 Radiation Environment Verification

No specific radiation tests will be carried out as all components will be selected to be able to withstand the radiation environment and procured through the CPP.

In the following table the test matrix of the various units is presented:

TYPE OF TEST	AVM	EQM	FM	FS
Functional Test	X	X	X	X (note2)
Performance Test	X	X	X	X (note2)
Interface Drawing Verification	X *	X	X	NA
Electrical Interface Tests	X	X	X	X
Vibrations Tests	NA	Q	A	A
Thermal-.Vacuum Test	NA	Q	A	A
Radiation tolerance	NA	NA	note 1	note 1
EMI / EMC	NA (note 4)	Q (note 3)	Partly (TBD)	NA
ESD	NA	X	NA	NA

(* NA but implemented also for AVM).

Items that will be in the Interface Drawing:
- Box dimensions and envelope.
- Mass; Moment of Inertia; Centre of Gravity
- Feet and connectors positions..
- Flatness of the mounting surface.
- Box and connectors identification.
- Connectors definitions.
- Box surface treatment including α and ε values (*NA for AVM).

Note 1: Radiation is included in EEE component selection and S/C sector analysis.
Note 2: Tests on PCB level only.
Note 3: Meaningful EMI/EMC tests should be carried out with sub systems or subsystems simulators.
Note 4: on the AVM only conducted emission tests will be carried out.

X = a test is carried out.

Q = Qualification levels and duration.

A = Acceptance levels and duration.

5.5 Ground associated equipment

The ground equipment are used to develop and test one item without the presence of the others.

Only the equipment needed for DPU/ICU development are listed.

The simulators replace one or more items connected to the DPU/ICU.

The tools are used to operate, check or integrate an item.

Most simulators are PC based as it is the most flexible and economic solution.

The simulators indicated in the following table are meant to be used at DPU/ICU test level, but they will also be used at the instrument integration site for integrity check after transport.

The IFSI subsystems simulators will be as simple as possible and will include only the HIFI and SPIRE subsystems simulators to test electrical interfaces and basic software interfaces.

No CDMS interface simulator will be built as this will be provided by the Consortia prior to the delivery of the boards from CGS to IFSI. The Consortia provided CDMS simulator will be used for electrical interface tests and basic exchange of information between DPU/ICU and the CDMS through the STD MIL 1553B hardware and software protocol.

5.5.1 Electrical tools

For the electrical tests laboratory instruments will be used like multimeteres, oscilloscopes, logic state analysers, etc. The EMC/EMI tests on power supply lines will be carried out both at IFSI and at TBD facility.

5.5.2 Software tools

For the software development and testing the following tools will be used:

- Axiomsys CASE tool
- ADSP C runtime library
- Virtuoso OS
- ADSP compatible development board (SIGMA 2000 PC board supporting the Virtuoso O.S.)
- C language development environment
- Configuration management tool
- 21020 In Circuit Emulator.

5.5.3 Subsystems Simulators

Simulator	Used for…	Functions	Provided by
DRCU Simulator	..simulating the MCE, SCE and DCE S/S of SPIRE.	Replaces DRCU Receives commands and sends science and HK data	SPIRE project
MEC/DEC and SPU Simulators	..simulating the PACS S/S behaviour.	Replaces PACS MEC/DEC and SPU. Receives commands and sends HK data	PACS project (only S/W)
HIFI S/S Simulators	..simulating the HIFI S/S interfaces. During the instrument level testing, HIFI S/S simulators will be provided (or the actual S/S).	Replaces HIFI S/S interfaces at ICU level tests.	IFSI project

5.5.4 S/C Tools

Tool	Used for …	Functions	Provided by
CDMS I/F (Part of EGSE)	… DPU/ICU SW testing	Simulates the S/C HW and SW I/F both at DPU/ICU level test and at instrument integration test.	PACS-HIFI-SPIRE projects
EGSE	DPU/ICU full S/W testing	Implements all functions needed to command the instruments and to interpret the telemetry data	PACS-HIFI-SPIRE projects

5.5.5 Transport container

All models will be transported by an IFSI representative in an aluminum box with suitable shock adsorbing material. The QM and FM will be in a sealed plastic conductive bag with silica-gel.

6 SW Work description

In the following table the schedule of all the activities foreseen for the software development is reported.

WP	Description
1	OBS
1.1	Spacecraft I/F
1.2	Subsystem I/F
1.3	OBS Controller
1.4	Data Packetiser
1.5	Health autonomy modules
1.6	AVM issue
1.7	PFM issue
1.8	Documentation
1.9	Support Activities
1.9.1	Virtuoso OS
1.9.2	Test modules

There is one main WP (OBS), shortly described in the following. All the other work packages shall be considered as a breakdown of all the activities related to it. They are described in detail in AD22.

6.1 On Board Software (OBS)

6.1.1 Objectives

To provide the computer board the functionality to manage each instrument.

6.1.2 WP description

Development of the DPU/ICU OBS.

Design activities: user requirements definition, logical model design, software requirements definition, architectural design. (WP 1.3, 1.8)

Coding activities: detailed design and code development. (WP 1.3, 1.5, 1.8)

Testing activities: unit tests, integration tests, acceptance tests. Subsystems' interfaces simulators development. SVVP definition. Test reports generation.

7 Development calendar

In the following tables the DPU/ICU milestones are shown both for hardware and software:

7.1 HW calendar

Description	**PACS**	**HIFI**	**SPIRE**
DPU/ICU PDR	01/03/2001	22/02/2001	26/06/2000
AVM boards to IFSI (from CGSpace)	05/11/01	19/02/02	19/02/02
EGSE delivery to IFSI (1 unit, 3 SW)	16/01/02	16/01/02	16/01/02
PACS S/S simulators	07/03/02	-	-
HIFI S/S simulators	-	17/09/01	-
SPIRE DRCU simulator	-	-	28/02/02
AVM delivery to consortium	**15/03/02**	**29/03/02**	**26/04/02**
EQM boards to IFSI (from CGSpace)	01/07/02	05/08/02	10/09/02
EQM environmental tests	Sept.-Oct. 02	Nov.-Dec. 02	Dec 02-Jan03
EQM delivery to consortium	**07/11/02**	**18/12/02**	**21/01/03**
DPU/ICU CDR	12/9/2002	11/09/02	2/12/2002
Burn of flight PROMs	27/05/03	23/06/03	26/08/03
FM boards to IFSI (from CGSpace)	16/06/03	14/07/03	15/09/03
FM environmental tests	Aug-Sep 03	Nov-Dec 03	Jan-Feb 04
FM delivery to consortium	**29/09/03**	**02/01/04**	**05/03/04**
FS boards to IFSI (from CGSpace)	10/11/03	10/11/03	10/11/03
FS environmental tests	Jan 04	Jan 04	Jan 04
FS boards ready for consortia	24/02/04	24/02/04	24/02/04

7.2 SW calendar

Description	**PACS**	**HIFI**	**SPIRE**
S/W Requirements Review	02/04/2001	02/04/2001	02/04/2001
S/W Architecture Design Review	02/04/2001	02/04/2001	02/04/2001
S/W Intermediate Review	03/07/01	17/7/01	09/01/02
AVM S/W TRR	08/03/02	22/03/02	19/04/02
AVM S/W Delivery Review	**15/03/02**	**29/03/02**	**26/04/02**
S/W 2nd Review	10/04/02	24/04/02	11/07/02
PFM S/W TRR	16/09/03	22/12/03	23/02/04
PFM S/W Delivery Review	**29/09/03**	**02/01/04**	**05/03/04**
AVM S/W Documentation	at AVM issue	at AVM issue	at AVM issue
PFM S/W Documentation	at PFM issue	at PFM issue	at PFM issue

8 Description of Receivables, Deliverables and Services

8.1 Receivables

IFSI expects to receive the following items:

ITEM	**FROM**	**DATE**
CDMS (S/C Interface) simulator	PACS (note 1)	16/01/02
EGSE (with SCOS 2000)	PACS (note 1)	16/01/02
DRCU Simulator	SPIRE	28/02/02
SPU Subsystem I/F S/W Simulator	PACS SPU	07/03/02
DEC/MEC Subsystem I/F S/W Simulator	PACS DEC/MEC	07/03/02

Note 1: The same system will be used for the three instruments.

8.2 Deliverables

IFSI is expected to deliver the following items:

ITEM	**PACS**	**HIFI**	**SPIRE**
DPU S/W Simulator for SPU	07/03/02	-	-
DPU S/W Simulator for DEC/MEC	07/03/02	-	-
AVM	**15/03/02**	**29/03/02**	**26/04/02**
AVM Software	15/03/02	29/03/02	26/04/02
AVM S/W Documentation	28/02/02	11/03/02	16/04/02
EQM	**07/11/02**	**18/12/02**	**21/01/03**
FM	**29/09/03**	**02/01/04**	**05/03/04**
FM Software	29/09/03	02/01/04	05/03/04
FM S/W Documentation	29/09/03	02/01/04	05/03/04

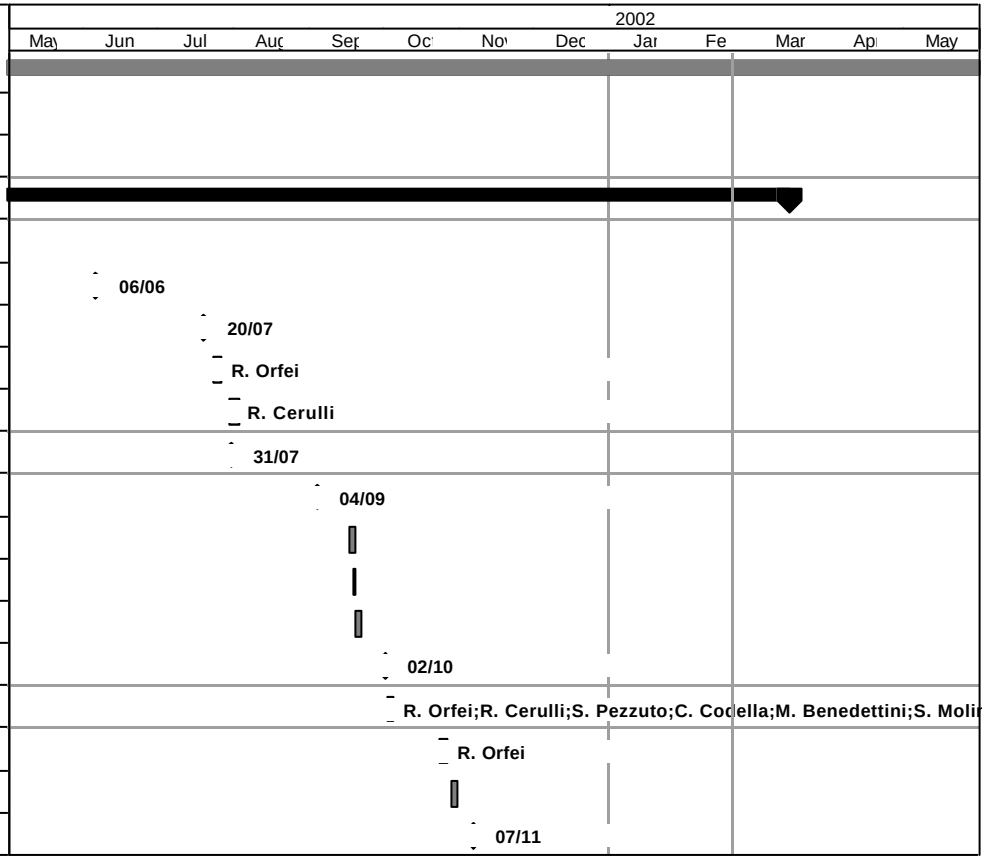
8.3 Services

IFSI will support the other Consortia partners during hardware and software integrations to solve both hardware and software problems.

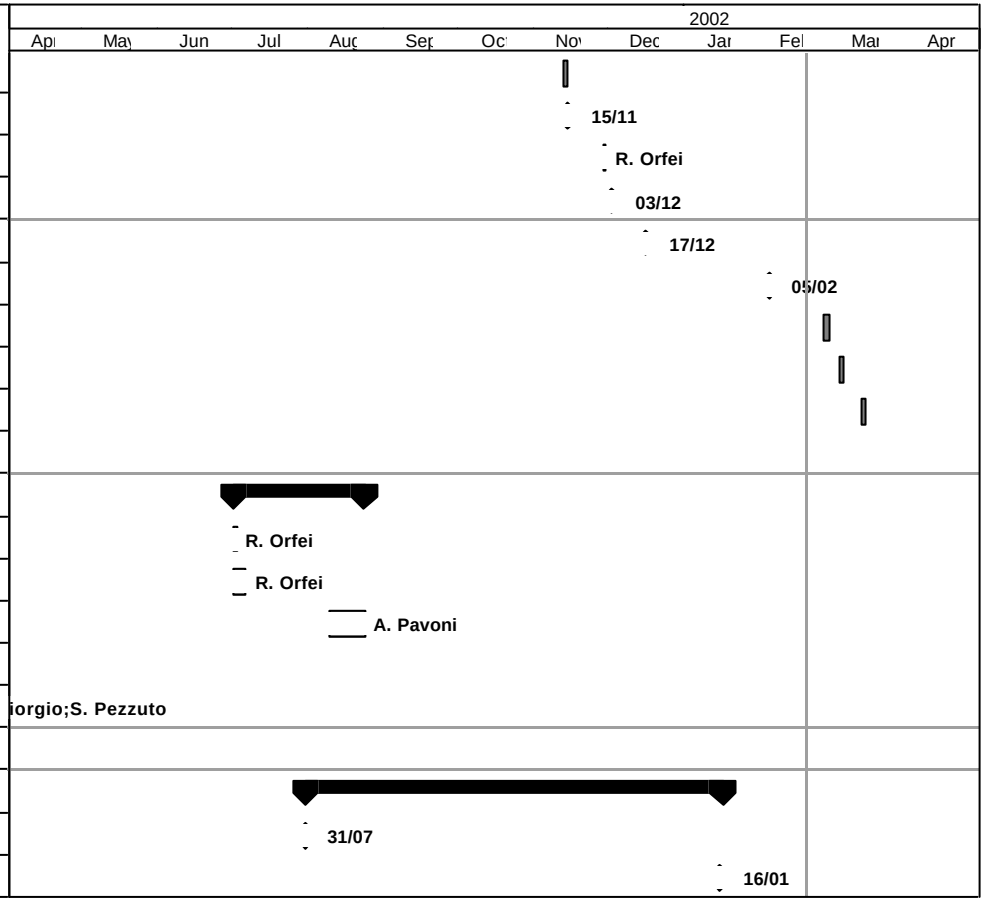
9 Schedules

9.1 General

ID	Task Name	Duration	Start	Finish
0	**Herschel DPU-ICU_WP**	**1477 days**	**Mon 20/07/98**	**Tue 16/03/04**
1	**DPU/ICU design**	**50 wks**	**Mon 20/07/98**	**Fri 02/07/99**
5	**DPU/ICU ITT**	**73,6 wks**	**Mon 05/07/99**	**Wed 29/11/00**
10	**Meetings & Reviews with CGS**	**64,6 wks**	**Wed 20/12/00**	**Fri 15/03/02**
11	PDR1 at CGS	0 wks	Wed 20/12/00	Wed 20/12/00
12	PDR2 & CDR1 at CGS	1 day	Wed 06/06/01	Wed 06/06/01
13	CDR2 at CGS	1 day	Fri 20/07/01	Fri 20/07/01
14	CPPA # 11	3 days	Tue 24/07/01	Thu 26/07/01
15	SPIRE OBS at RAL	4 days	Mon 30/07/01	Thu 02/08/01
16	2nd Progress Meeting at CGS	1 day	Tue 31/07/01	Tue 31/07/01
17	3rd Progress Meeting at CGS	1 day	Tue 04/09/01	Tue 04/09/01
18	HIFI Mgmt Meet. Warshaw	3 days	Mon 17/09/01	Wed 19/09/01
19	CPPA # 12	1 day	Wed 19/09/01	Wed 19/09/01
20	PACS CM #14 Garching	2 days	Thu 20/09/01	Fri 21/09/01
21	4th Progress Meeting at CGS	1 day	Tue 02/10/01	Tue 02/10/01
22	OBS # 7 at IFSI	2 days	Wed 03/10/01	Thu 04/10/01
23	CPPA # 13	3 days	Wed 24/10/01	Fri 26/10/01
24	HIFI EMC Des. Implem. Assess.	2 days	Mon 29/10/01	Tue 30/10/01
25	**5th Progress Meet. at CGS**	1 day	Wed 07/11/01	Wed 07/11/01

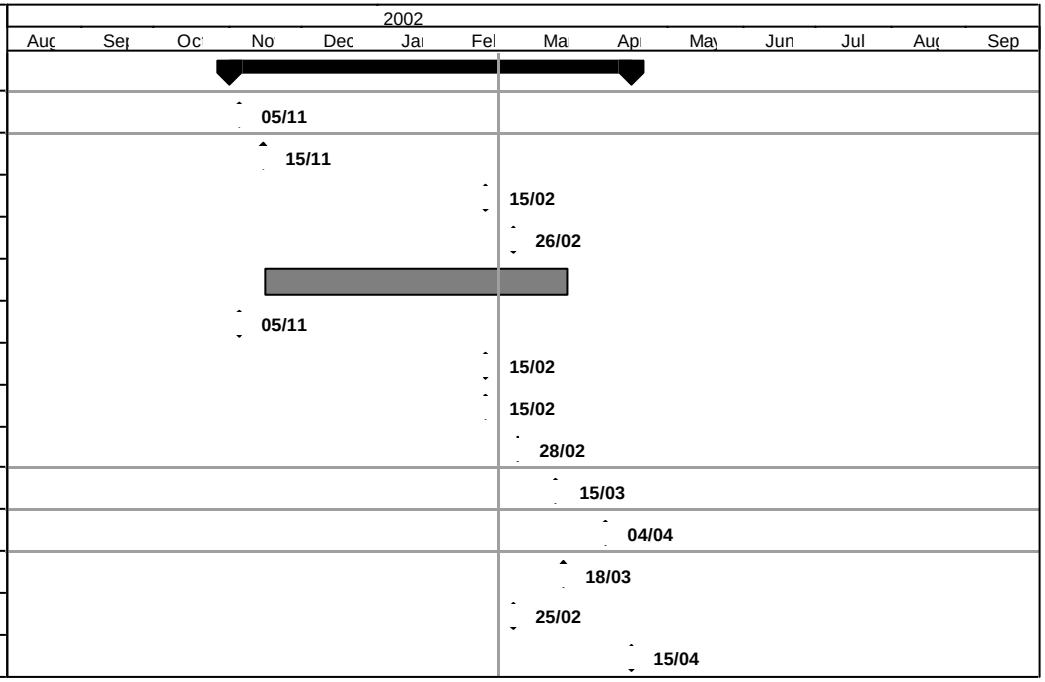


ID	Task Name	Duration	Start	Finish
26	HIFI AIV Readin. Assess.	2 days	Tue 13/11/01	Wed 14/11/01
27	Progress Meeting 5	0 days	Thu 15/11/01	Thu 15/11/01
28	CPPA # 14	1 day	Thu 29/11/01	Thu 29/11/01
29	**6th Progress Meet. at CGS**	1 day	Mon 03/12/01	Mon 03/12/01
30	Progress Meeting 6	0 days	Mon 17/12/01	Mon 17/12/01
31	Progress Meeting 7	2 days	Tue 05/02/02	Wed 06/02/02
32	PACS IBDR	2 days	Wed 27/02/02	Thu 28/02/02
33	SPIRE IBDR	2 days	Tue 05/03/02	Wed 06/03/02
34	HIFI IBDR	2 days	Thu 14/03/02	Fri 15/03/02
35				
36	**DPU/ICU Procurement/mfg**	**7,8 wks**	**Mon 02/07/01**	**Thu 23/08/01**
37	Herschel Wires Procurement	1 day	Mon 02/07/01	Mon 02/07/01
38	AVM/EQM Connec. Procur.	1 wk	Mon 02/07/01	Fri 06/07/01
39	Break-out Box Mftrg	2 wks	Fri 10/08/01	Thu 23/08/01
40	**SW Support activities**	**48,2 wks**	**Wed 01/03/00**	**Wed 31/01/01**
41	Virtuoso OS	48 wks	Wed 01/03/00	Tue 30/01/01
42	Decision on OS use	0,2 wks	Wed 31/01/01	Wed 31/01/01
43	**S/C CDMS Simulators**	**24,4 wks**	**Tue 31/07/01**	**Wed 16/01/02**
44	(S/C I/F) Simul. Proto SW at IFSI	0,2 wks	Tue 31/07/01	Tue 31/07/01
45	EGSE (with SCOS 2000)	0,2 wks	Wed 16/01/02	Wed 16/01/02

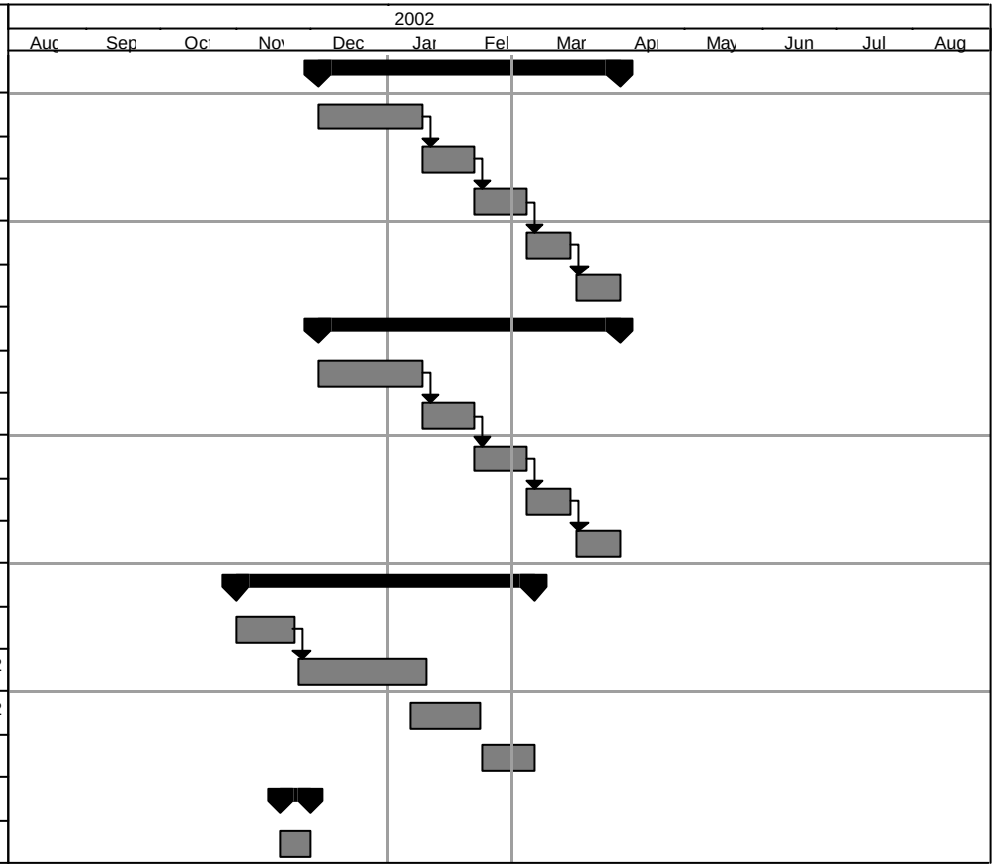


9.2 Carlo Gavazzi Space

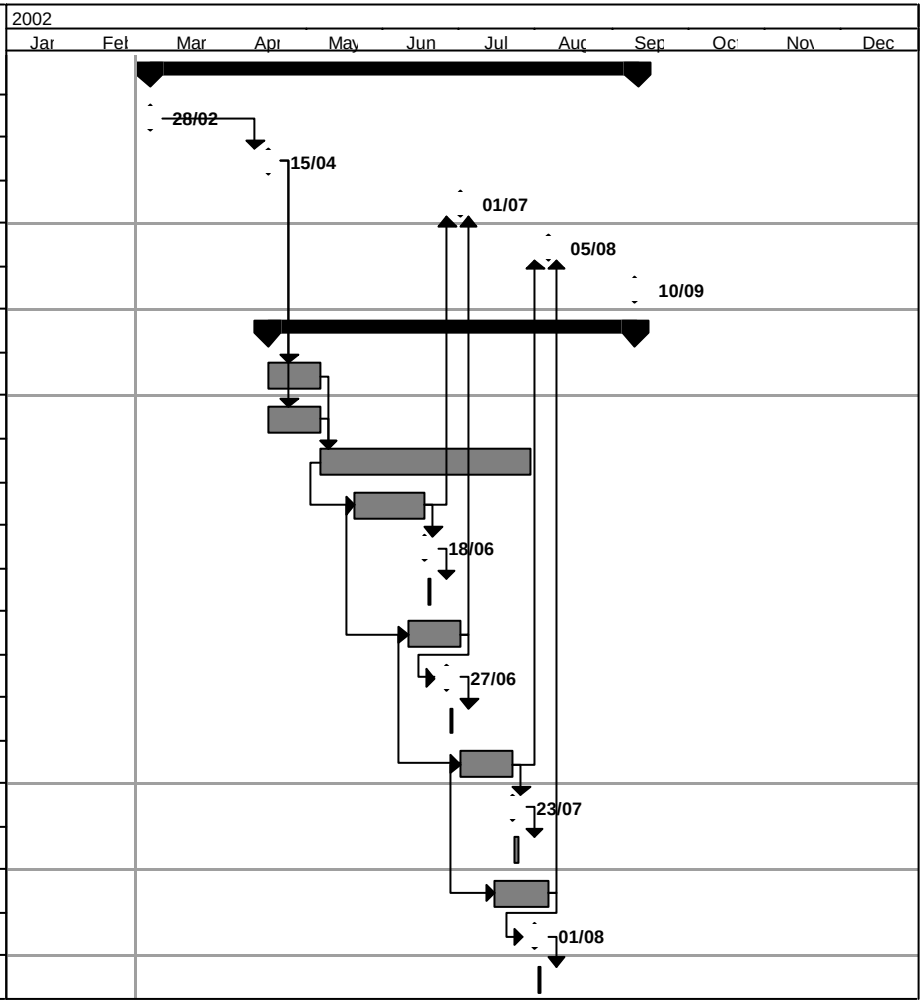
ID	Task Name	Duration	Start	Finish
47	**CGS AVM DPU-ICU HW & SW**	**23,6 wks**	**Thu 01/11/01**	**Mon 15/04/02**
48	S/W Basic Functions delivery	0 days	Mon 05/11/01	Mon 05/11/01
49	S/W PKT TM TC Delivery	0 days	Thu 15/11/01	Thu 15/11/01
50	SW Partial Delivery	0,2 wks	Fri 15/02/02	Fri 15/02/02
51	S/W Final Delivery	0 days	Tue 26/02/02	Tue 26/02/02
52	Availability of IFSI Simulator	88 days	Fri 16/11/01	Tue 19/03/02
53	EM S/N 01 Delivery (PACS/HIFI SD)	0 days	Mon 05/11/01	Mon 05/11/01
54	EM S/N 02 Delivery (HIFI/PACS SD)	0 days	Fri 15/02/02	Fri 15/02/02
55	EM S/N 03 Delivery (SPIRE SD)	0 days	Fri 15/02/02	Fri 15/02/02
56	EM S/N 04 Delivery (HIFI SD)	0 days	Thu 28/02/02	Thu 28/02/02
57	EM S/N 05 Delivery (PACS SD)	0 days	Fri 15/03/02	Fri 15/03/02
58	EM S/N 06 Delivery (SPIRE SD)	0 days	Thu 04/04/02	Thu 04/04/02
59	EM DC/DC S/N 01 Delivery (HIFI)	0 days	Mon 18/03/02	Mon 18/03/02
60	EM DC/DC S/N 02 Delivery (PACS)	0 days	Mon 25/02/02	Mon 25/02/02
61	EM DC/DC S/N 03 Delivery (SPIRE)	0 days	Mon 15/04/02	Mon 15/04/02



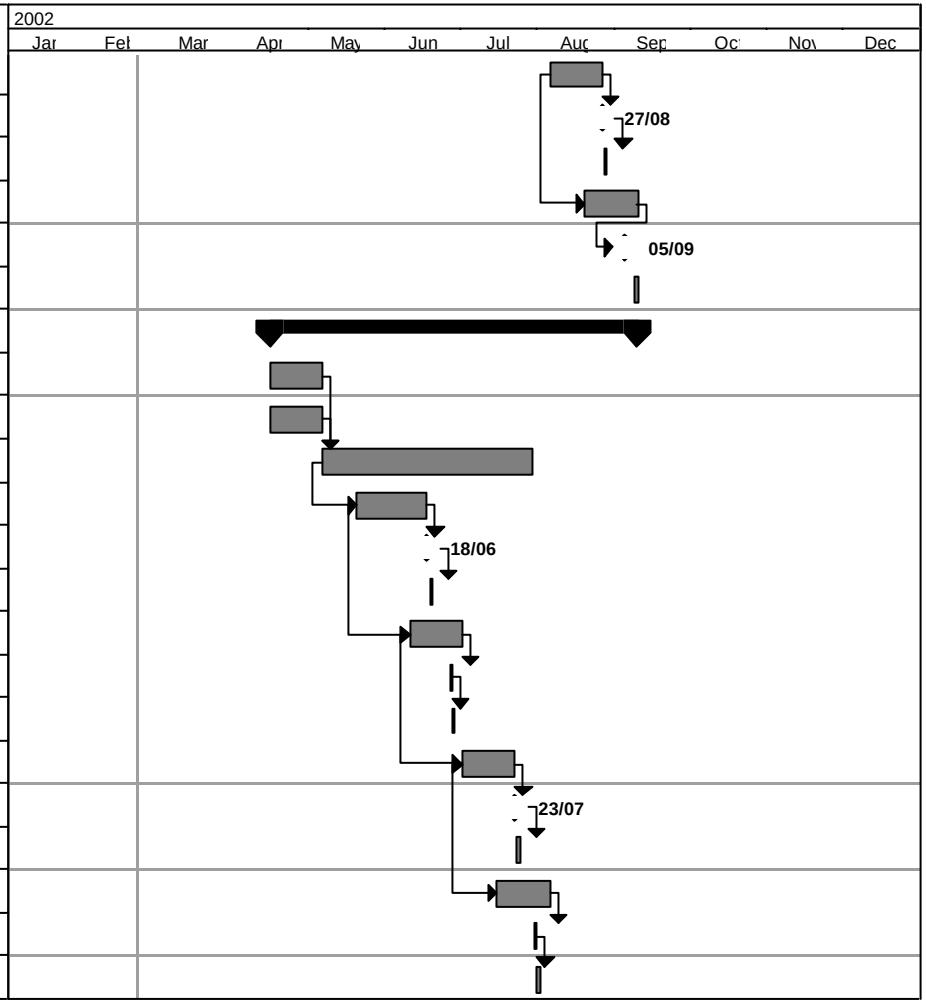
ID	Task Name	Duration	Start	Finish
62	**CPU BOARD**	**17,6 wks**	**Tue 04/12/01**	**Thu 04/04/02**
63	Board Testing (S/N 02 PACS)	30 days	Tue 04/12/01	Mon 14/01/02
64	Board Testing (S/N 03 HIFI)	15 days	Tue 15/01/02	Mon 04/02/02
65	Board Testing (S/N 04 HIFI)	15 days	Tue 05/02/02	Mon 25/02/02
66	Board Testing (S/N 05 SPIRE)	14 days	Tue 26/02/02	Fri 15/03/02
67	Board Testing (S/N 06 SPIRE)	14 days	Mon 18/03/02	Thu 04/04/02
68	**PL I/F BOARD**	**17,6 wks**	**Tue 04/12/01**	**Thu 04/04/02**
69	Board Testing (S/N 02 HIFI)	30 days	Tue 04/12/01	Mon 14/01/02
70	Board Testing (S/N 03 PACS)	15 days	Tue 15/01/02	Mon 04/02/02
71	Board Testing (S/N 04 PACS)	15 days	Tue 05/02/02	Mon 25/02/02
72	Board Testing (S/N 05 SPIRE)	14 days	Tue 26/02/02	Fri 15/03/02
73	Board Testing (S/N 06 SPIRE)	14 days	Mon 18/03/02	Thu 04/04/02
74	**DC/DC CONVERTER BOARD**	**17,2 wks**	**Thu 01/11/01**	**Thu 28/02/02**
75	Boards Assembling	17 days	Thu 01/11/01	Fri 23/11/01
76	Board Testing (S/N 01 PACS)	38 days	Mon 26/11/01	Wed 16/01/02
77	Board Testing (S/N 02 HIFI)	20 days	Thu 10/01/02	Wed 06/02/02
78	Board Testing (S/N 03 SPIRE)	15 days	Fri 08/02/02	Thu 28/02/02
79	**MOTHERBOARD**	**2 wks**	**Mon 19/11/01**	**Fri 30/11/01**
80	Board Testing (S/N 04, 05 and 06)	10 days	Mon 19/11/01	Fri 30/11/01



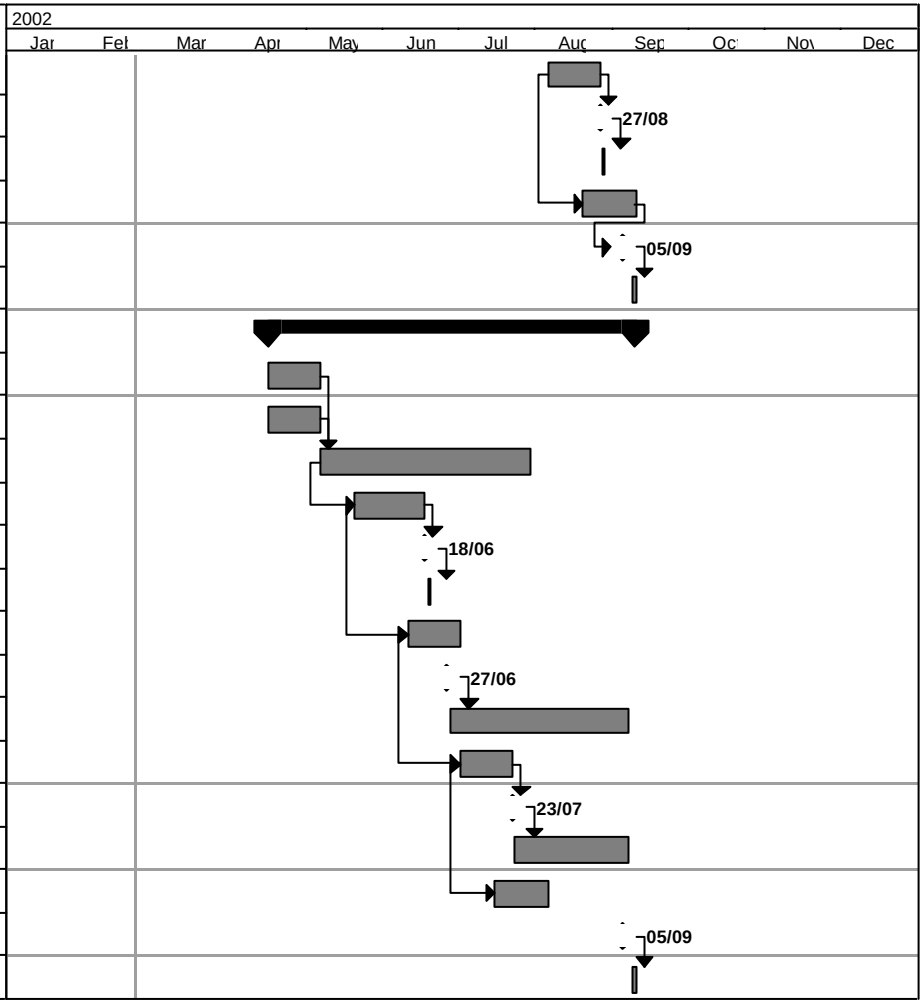
ID	Task Name	Duration	Start	Finish
82	**CGS EQM DPU-ICU HW**	**27,8 wks**	**Thu 28/02/02**	**Tue 10/09/02**
83	IFSI Authorization To Proceed	0,2 wks	Thu 28/02/02	Thu 28/02/02
84	Documentation Upgrading	0 days	Mon 15/04/02	Mon 15/04/02
85	EQM SN01 Delivery (PACS)	0 days	Mon 01/07/02	Mon 01/07/02
86	EQM SN02 Delivery (HIFI)	0 days	Mon 05/08/02	Mon 05/08/02
87	EQM SN03 Delivery (SPIRE)	1 day	Tue 10/09/02	Tue 10/09/02
88	**CPU BOARD**	**21 wks**	**Tue 16/04/02**	**Mon 09/09/02**
89	PCB Manufacturing	15 days	Tue 16/04/02	Mon 06/05/02
90	Kitting	15 days	Tue 16/04/02	Mon 06/05/02
91	Boards Assembling	60 days	Tue 07/05/02	Mon 29/07/02
92	Board Testing (S/N 01 PACS)	20 days	Tue 21/05/02	Mon 17/06/02
93	KIP	1 day	Tue 18/06/02	Tue 18/06/02
94	Conformal coating	1 day	Wed 19/06/02	Wed 19/06/02
95	Board Testing (S/N 02 PACS)	15 days	Tue 11/06/02	Mon 01/07/02
96	KIP	0,2 wks	Thu 27/06/02	Thu 27/06/02
97	Conformal coating	0,2 wks	Fri 28/06/02	Fri 28/06/02
98	Board Testing (S/N 03 HIFI)	15 days	Tue 02/07/02	Mon 22/07/02
99	KIP	0,2 wks	Tue 23/07/02	Tue 23/07/02
100	Conformal coating	0,2 wks	Wed 24/07/02	Wed 24/07/02
101	Board Testing (S/N 04 HIFI)	15 days	Tue 16/07/02	Mon 05/08/02
102	KIP	0,2 wks	Thu 01/08/02	Thu 01/08/02
103	Conformal coating	0,2 wks	Fri 02/08/02	Fri 02/08/02



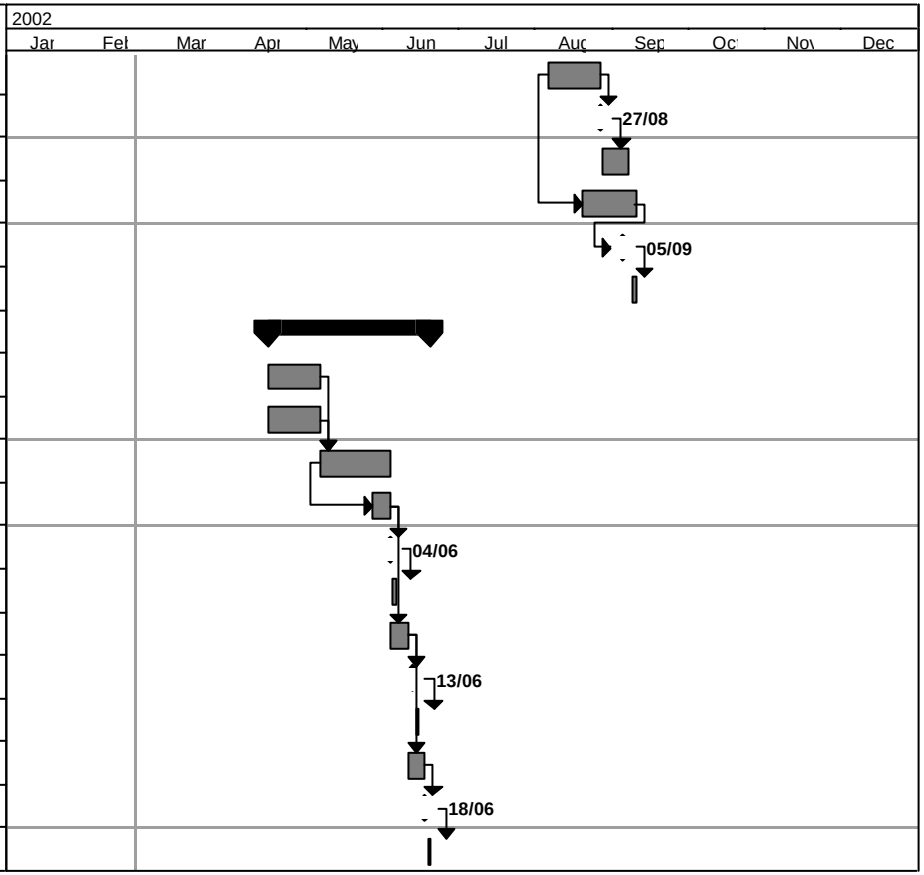
ID	Task Name	Duration	Start	Finish
104	Board Testing (S/N 05 SPIRE)	15 days	Tue 06/08/02	Mon 26/08/02
105	KIP	0,2 wks	Tue 27/08/02	Tue 27/08/02
106	Conformal coating	0,2 wks	Wed 28/08/02	Wed 28/08/02
107	Board Testing (S/N 06 SPIRE)	15 days	Tue 20/08/02	Mon 09/09/02
108	KIP	0,2 wks	Thu 05/09/02	Thu 05/09/02
109	Conformal coating	0,2 wks	Mon 09/09/02	Mon 09/09/02
110	**PL I/F BOARD**	**21 wks**	**Tue 16/04/02**	**Mon 09/09/02**
111	PCB Manufacturing	15 days	Tue 16/04/02	Mon 06/05/02
112	Kitting	15 days	Tue 16/04/02	Mon 06/05/02
113	Boards Assembling	60 days	Tue 07/05/02	Mon 29/07/02
114	Board Testing (S/N 01 PACS)	20 days	Tue 21/05/02	Mon 17/06/02
115	KIP	0,2 wks	Tue 18/06/02	Tue 18/06/02
116	Conformal coating	0,2 wks	Wed 19/06/02	Wed 19/06/02
117	Board Testing (S/N 02 PACS)	15 days	Tue 11/06/02	Mon 01/07/02
118	KIP	0,2 wks	Thu 27/06/02	Thu 27/06/02
119	Conformal coating	0,2 wks	Fri 28/06/02	Fri 28/06/02
120	Board Testing (S/N 03 HIFI)	15 days	Tue 02/07/02	Mon 22/07/02
121	KIP	0,2 wks	Tue 23/07/02	Tue 23/07/02
122	Conformal coating	0,2 wks	Wed 24/07/02	Wed 24/07/02
123	Board Testing (S/N 04 HIFI)	15 days	Tue 16/07/02	Mon 05/08/02
124	KIP	0,2 wks	Wed 31/07/02	Wed 31/07/02
125	Conformal coating	0,2 wks	Thu 01/08/02	Thu 01/08/02



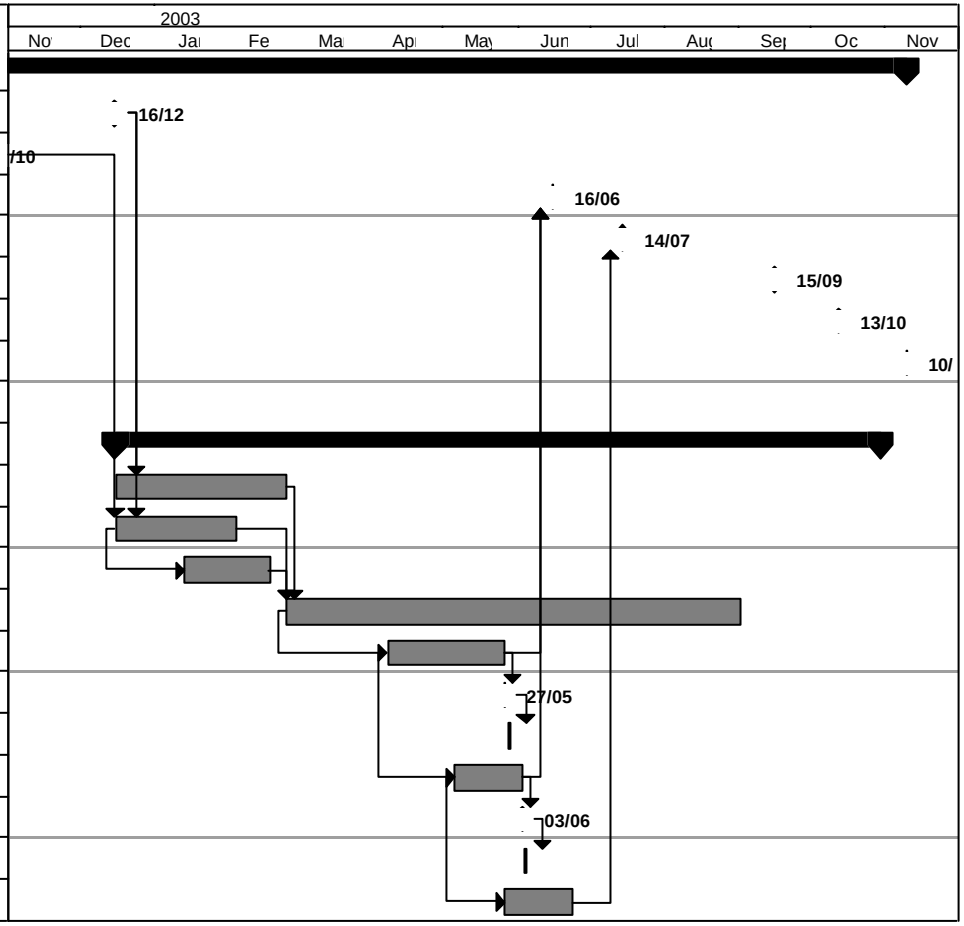
ID	Task Name	Duration	Start	Finish
126	Board Testing (S/N 05 SPIRE)	15 days	Tue 06/08/02	Mon 26/08/02
127	KIP	0,2 wks	Tue 27/08/02	Tue 27/08/02
128	Conformal coating	0,2 wks	Wed 28/08/02	Wed 28/08/02
129	Board Testing (S/N 06 SPIRE)	15 days	Tue 20/08/02	Mon 09/09/02
130	KIP	0,2 wks	Thu 05/09/02	Thu 05/09/02
131	Conformal coating	0,2 wks	Mon 09/09/02	Mon 09/09/02
132	**DC/DC CONVERTER BOARD**	**21 wks**	**Tue 16/04/02**	**Mon 09/09/02**
133	PCB Manufacturing	15 days	Tue 16/04/02	Mon 06/05/02
134	Kitting	15 days	Tue 16/04/02	Mon 06/05/02
135	Boards Assembling	60 days	Tue 07/05/02	Mon 29/07/02
136	Board Testing (S/N 01 PACS)	20 days	Tue 21/05/02	Mon 17/06/02
137	KIP	0,2 wks	Tue 18/06/02	Tue 18/06/02
138	Conformal coating	1 day	Wed 19/06/02	Wed 19/06/02
139	Board Testing (S/N 02 PACS)	15 days	Tue 11/06/02	Mon 01/07/02
140	KIP	0,2 wks	Thu 27/06/02	Thu 27/06/02
141	Conformal coating	10,2 wks	Fri 28/06/02	Fri 06/09/02
142	Board Testing (S/N 03 HIFI)	15 days	Tue 02/07/02	Mon 22/07/02
143	KIP	0,2 wks	Tue 23/07/02	Tue 23/07/02
144	Conformal coating	6,6 wks	Wed 24/07/02	Fri 06/09/02
145	Board Testing (S/N 04 HIFI)	15 days	Tue 16/07/02	Mon 05/08/02
146	KIP	0,2 wks	Thu 05/09/02	Thu 05/09/02
147	Conformal coating	0,2 wks	Mon 09/09/02	Mon 09/09/02



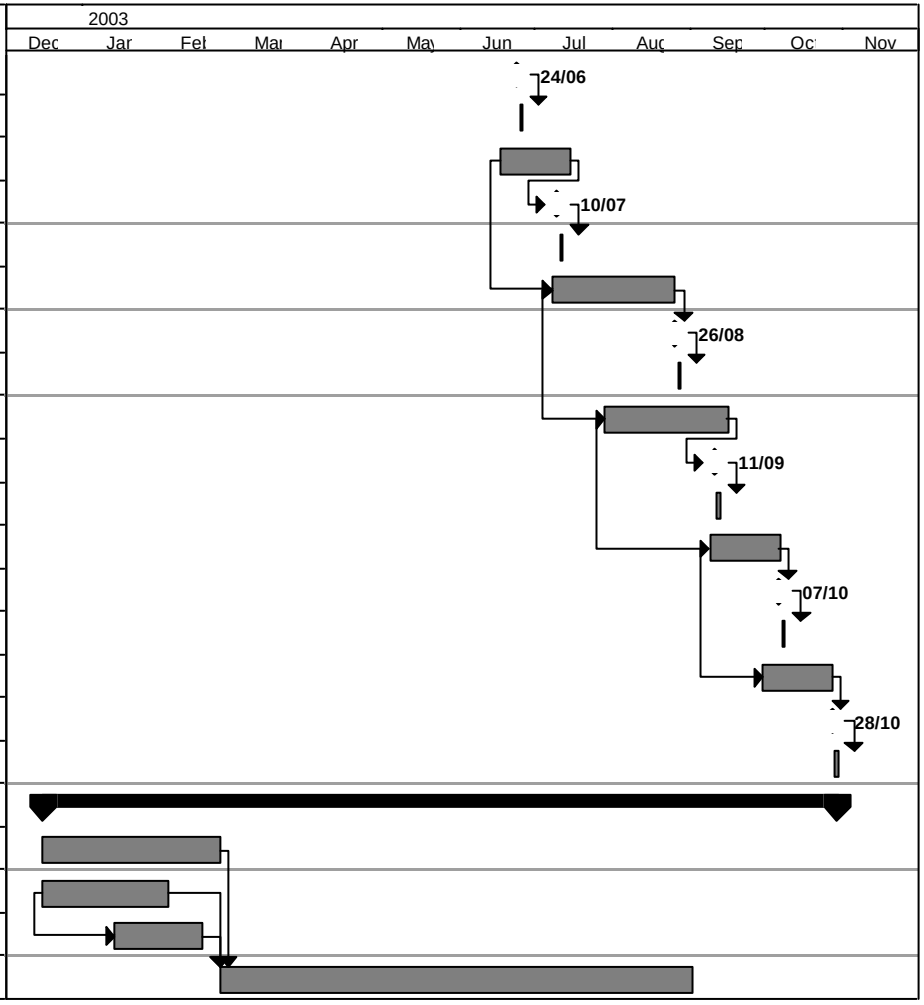
ID	Task Name	Duration	Start	Finish
148	Board Testing (S/N 05 SPIRE)	15 days	Tue 06/08/02	Mon 26/08/02
149	KIP	0,2 wks	Tue 27/08/02	Tue 27/08/02
150	Conformal coating	1,6 wks	Wed 28/08/02	Fri 06/09/02
151	Board Testing (S/N 06 SPIRE)	15 days	Tue 20/08/02	Mon 09/09/02
152	KIP	0,2 wks	Thu 05/09/02	Thu 05/09/02
153	Conformal coating	0,2 wks	Mon 09/09/02	Mon 09/09/02
154	**MOTHERBOARD**	**9,4 wks**	**Tue 16/04/02**	**Wed 19/06/02**
155	PCB Manufacturing	15 days	Tue 16/04/02	Mon 06/05/02
156	Kitting	15 days	Tue 16/04/02	Mon 06/05/02
157	Boards Assembling	20 days	Tue 07/05/02	Mon 03/06/02
158	Board Testing (S/N 01 PACS)	5 days	Tue 28/05/02	Mon 03/06/02
159	KIP	0,2 wks	Tue 04/06/02	Tue 04/06/02
160	Conformal coating	1 day	Wed 05/06/02	Wed 05/06/02
161	Board Testing (S/N 02 HIFI)	5 days	Tue 04/06/02	Mon 10/06/02
162	KIP	0,2 wks	Thu 13/06/02	Thu 13/06/02
163	Conformal coating	1 day	Fri 14/06/02	Fri 14/06/02
164	Board Testing (S/N 03 SPIRE)	5 days	Tue 11/06/02	Mon 17/06/02
165	KIP	0,2 wks	Tue 18/06/02	Tue 18/06/02
166	Conformal coating	1 day	Wed 19/06/02	Wed 19/06/02



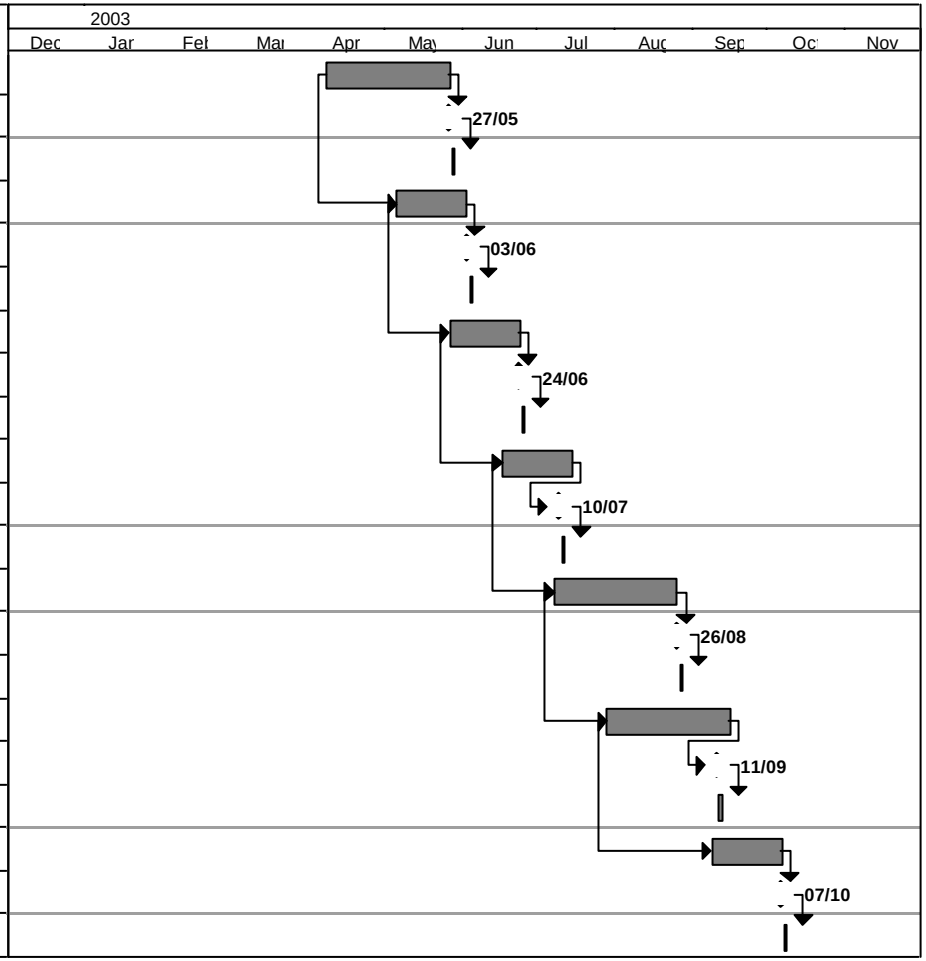
ID	Task Name	Duration	Start	Finish
168	**CGS FM DPU-ICU HW**	**55,6 wks**	**Wed 16/10/02**	**Mon 10/11/03**
169	IFSI Authorization to Proceed FM	0 days	Mon 16/12/02	Mon 16/12/02
170	FM compon. from TL&TR at CGS	0 days	Wed 16/10/02	Wed 16/1[illegible]
171	FM SN01 Delivery (PACS)	0 days	Mon 16/06/03	Mon 16/06/03
172	FM SN02 Delivery (HIFI)	0 days	Mon 14/07/03	Mon 14/07/03
173	FM SN03 Delivery (SPIRE)	0 days	Mon 15/09/03	Mon 15/09/03
174	FS SN01 Delivery	0 days	Mon 13/10/03	Mon 13/10/03
175	FS SN 01 Delivery	0 days	Mon 10/11/03	Mon 10/11/03
176				
177	**CPU BOARD**	**45,6 wks**	**Mon 16/12/02**	**Wed 29/10/03**
178	PCB Manufacturing	51 days	Mon 16/12/02	Mon 24/02/03
179	Kitting	36 days	Mon 16/12/02	Mon 03/02/03
180	Components pre-tinning	25 days	Tue 14/01/03	Mon 17/02/03
181	Boards Assembling	135 days	Tue 25/02/03	Mon 01/09/03
182	Board Testing (S/N 01 PACS)	35 days	Tue 08/04/03	Mon 26/05/03
183	KIP	0,2 wks	Tue 27/05/03	Tue 27/05/03
184	Conformal coating	1 day	Wed 28/05/03	Wed 28/05/03
185	Board Testing (S/N 02 PACS)	20 days	Tue 06/05/03	Mon 02/06/03
186	KIP	0,2 wks	Tue 03/06/03	Tue 03/06/03
187	Conformal coating	1 day	Wed 04/06/03	Wed 04/06/03
188	Board Testing (S/N 03 HIFI)	20 days	Tue 27/05/03	Mon 23/06/03



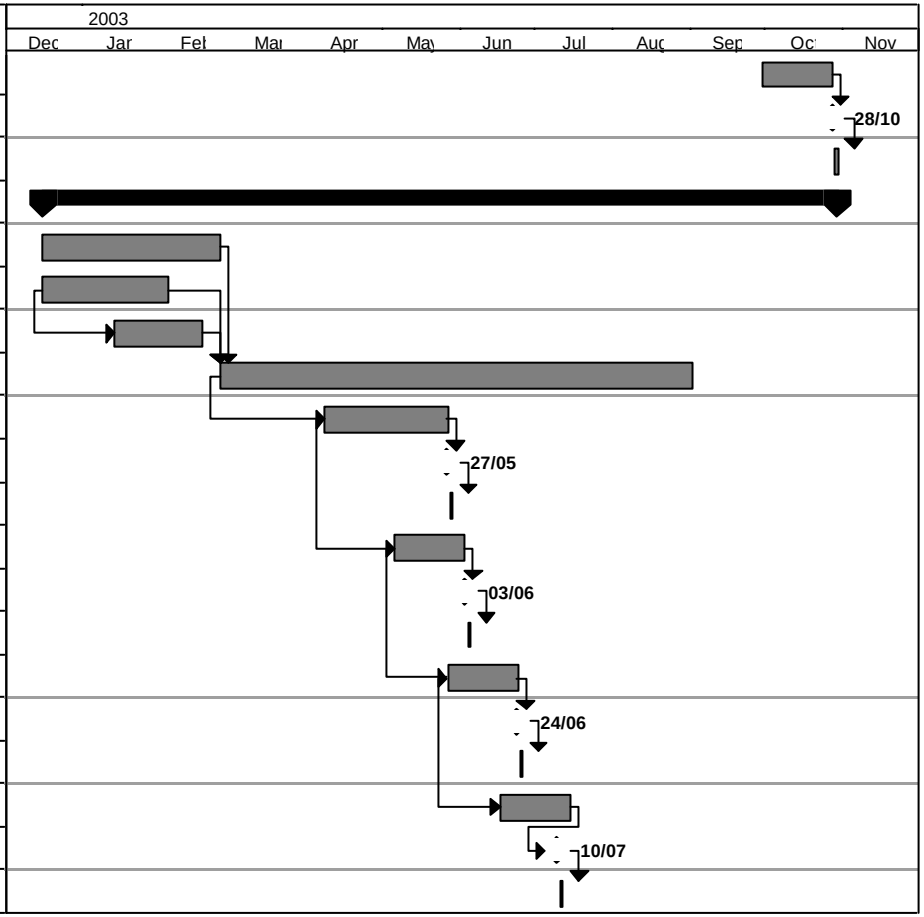
ID	Task Name	Duration	Start	Finish
189	KIP	0,2 wks	Tue 24/06/03	Tue 24/06/03
190	Conformal coating	1 day	Wed 25/06/03	Wed 25/06/03
191	Board Testing (S/N 04 HIFI)	20 days	Tue 17/06/03	Mon 14/07/03
192	KIP	0,2 wks	Thu 10/07/03	Thu 10/07/03
193	Conformal coating	1 day	Fri 11/07/03	Fri 11/07/03
194	Board Testing (S/N 05 SPIRE)	35 days	Tue 08/07/03	Mon 25/08/03
195	KIP	0,2 wks	Tue 26/08/03	Tue 26/08/03
196	Conformal coating	1 day	Wed 27/08/03	Wed 27/08/03
197	Board Testing (S/N 06 SPIRE)	35 days	Tue 29/07/03	Mon 15/09/03
198	KIP	0,2 wks	Thu 11/09/03	Thu 11/09/03
199	Conformal coating	1 day	Fri 12/09/03	Fri 12/09/03
200	Board Testing (S/N 07 Spare)	20 days	Tue 09/09/03	Mon 06/10/03
201	KIP	0,2 wks	Tue 07/10/03	Tue 07/10/03
202	Conformal coating	1 day	Wed 08/10/03	Wed 08/10/03
203	Board Testing (S/N 08 Spare)	20 days	Tue 30/09/03	Mon 27/10/03
204	KIP	0,2 wks	Tue 28/10/03	Tue 28/10/03
205	Conformal coating	1 day	Wed 29/10/03	Wed 29/10/03
206	**PL I/F BOARD**	**45,6 wks**	**Mon 16/12/02**	**Wed 29/10/03**
207	PCB Manufacturing	51 days	Mon 16/12/02	Mon 24/02/03
208	Kitting	36 days	Mon 16/12/02	Mon 03/02/03
209	Components pre-tinning	25 days	Tue 14/01/03	Mon 17/02/03
210	Boards Assembling	135 days	Tue 25/02/03	Mon 01/09/03



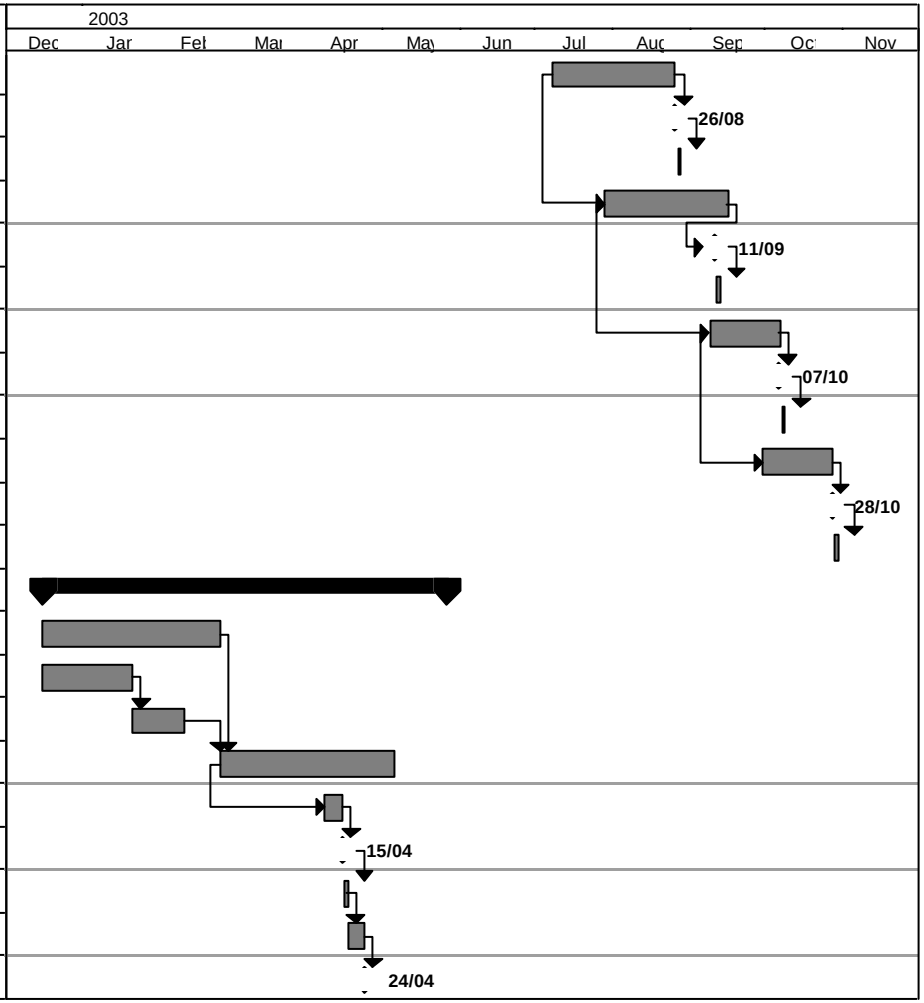
ID	Task Name	Duration	Start	Finish
211	Board Testing (S/N 01 PACS)	35 days	Tue 08/04/03	Mon 26/05/03
212	KIP	0,2 wks	Tue 27/05/03	Tue 27/05/03
213	Conformal coating	1 day	Wed 28/05/03	Wed 28/05/03
214	Board Testing (S/N 02 PACS)	20 days	Tue 06/05/03	Mon 02/06/03
215	KIP	0,2 wks	Tue 03/06/03	Tue 03/06/03
216	Conformal coating	1 day	Wed 04/06/03	Wed 04/06/03
217	Board Testing (S/N 03 HIFI)	20 days	Tue 27/05/03	Mon 23/06/03
218	KIP	0,2 wks	Tue 24/06/03	Tue 24/06/03
219	Conformal coating	1 day	Wed 25/06/03	Wed 25/06/03
220	Board Testing (S/N 04 HIFI)	20 days	Tue 17/06/03	Mon 14/07/03
221	KIP	0,2 wks	Thu 10/07/03	Thu 10/07/03
222	Conformal coating	1 day	Fri 11/07/03	Fri 11/07/03
223	Board Testing (S/N 05 SPIRE)	35 days	Tue 08/07/03	Mon 25/08/03
224	KIP	0,2 wks	Tue 26/08/03	Tue 26/08/03
225	Conformal coating	1 day	Wed 27/08/03	Wed 27/08/03
226	Board Testing (S/N 06 SPIRE)	35 days	Tue 29/07/03	Mon 15/09/03
227	KIP	0,2 wks	Thu 11/09/03	Thu 11/09/03
228	Conformal coating	1 day	Fri 12/09/03	Fri 12/09/03
229	Board Testing (S/N 07 Spare)	20 days	Tue 09/09/03	Mon 06/10/03
230	KIP	0,2 wks	Tue 07/10/03	Tue 07/10/03
231	Conformal coating	1 day	Wed 08/10/03	Wed 08/10/03



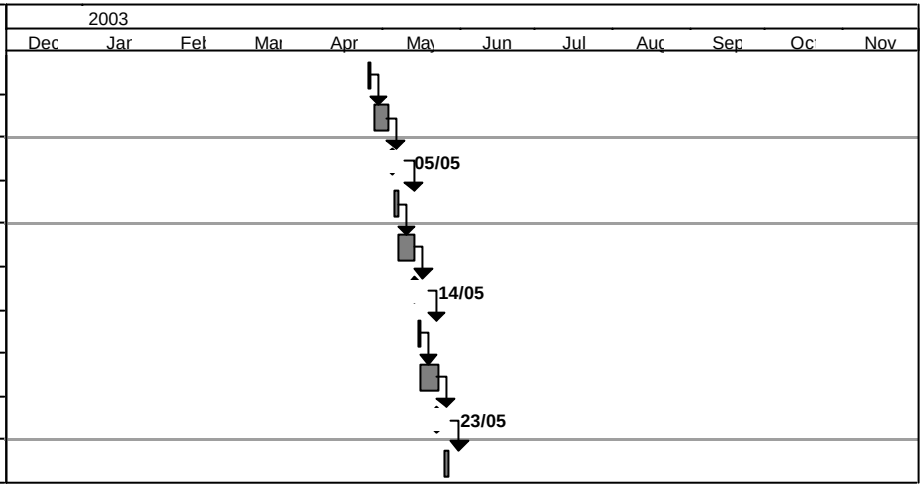
ID	Task Name	Duration	Start	Finish
232	Board Testing (S/N 08 Spare)	20 days	Tue 30/09/03	Mon 27/10/03
233	KIP	0,2 wks	Tue 28/10/03	Tue 28/10/03
234	Conformal coating	1 day	Wed 29/10/03	Wed 29/10/03
235	**DC/DC CONVERTER BOARD**	**45,6 wks**	**Mon 16/12/02**	**Wed 29/10/03**
236	PCB Manufacturing	51 days	Mon 16/12/02	Mon 24/02/03
237	Kitting	36 days	Mon 16/12/02	Mon 03/02/03
238	Components pre-tinning	25 days	Tue 14/01/03	Mon 17/02/03
239	Boards Assembling	135 days	Tue 25/02/03	Mon 01/09/03
240	Board Testing (S/N 01 PACS)	35 days	Tue 08/04/03	Mon 26/05/03
241	KIP	0,2 wks	Tue 27/05/03	Tue 27/05/03
242	Conformal coating	1 day	Wed 28/05/03	Wed 28/05/03
243	Board Testing (S/N 02 PACS)	20 days	Tue 06/05/03	Mon 02/06/03
244	KIP	0,2 wks	Tue 03/06/03	Tue 03/06/03
245	Conformal coating	1 day	Wed 04/06/03	Wed 04/06/03
246	Board Testing (S/N 03 HIFI)	20 days	Tue 27/05/03	Mon 23/06/03
247	KIP	0,2 wks	Tue 24/06/03	Tue 24/06/03
248	Conformal coating	1 day	Wed 25/06/03	Wed 25/06/03
249	Board Testing (S/N 04 HIFI)	20 days	Tue 17/06/03	Mon 14/07/03
250	KIP	0,2 wks	Thu 10/07/03	Thu 10/07/03
251	Conformal coating	1 day	Fri 11/07/03	Fri 11/07/03



ID	Task Name	Duration	Start	Finish
252	Board Testing (S/N 05 SPIRE)	35 days	Tue 08/07/03	Mon 25/08/03
253	KIP	0,2 wks	Tue 26/08/03	Tue 26/08/03
254	Conformal coating	1 day	Wed 27/08/03	Wed 27/08/03
255	Board Testing (S/N 06 SPIRE)	35 days	Tue 29/07/03	Mon 15/09/03
256	KIP	0,2 wks	Thu 11/09/03	Thu 11/09/03
257	Conformal coating	1 day	Fri 12/09/03	Fri 12/09/03
258	Board Testing (S/N 07 Spare)	20 days	Tue 09/09/03	Mon 06/10/03
259	KIP	0,2 wks	Tue 07/10/03	Tue 07/10/03
260	Conformal coating	1 day	Wed 08/10/03	Wed 08/10/03
261	Board Testing (S/N 08 Spare)	20 days	Tue 30/09/03	Mon 27/10/03
262	KIP	0,2 wks	Tue 28/10/03	Tue 28/10/03
263	Conformal coating	1 day	Wed 29/10/03	Wed 29/10/03
264	**MOTHERBOARD**	**23,2 wks**	**Mon 16/12/02**	**Mon 26/05/03**
265	PCB Manufacturing	51 days	Mon 16/12/02	Mon 24/02/03
266	Kitting	26 days	Mon 16/12/02	Mon 20/01/03
267	Components pre-tinning	15 days	Tue 21/01/03	Mon 10/02/03
268	Boards Assembling	50 days	Tue 25/02/03	Mon 05/05/03
269	Board Testing (S/N 01 PACS)	5 days	Tue 08/04/03	Mon 14/04/03
270	KIP	0,2 wks	Tue 15/04/03	Tue 15/04/03
271	Conformal coating	1 day	Wed 16/04/03	Wed 16/04/03
272	Board Testing (S/N 02 HIFI)	5 days	Thu 17/04/03	Wed 23/04/03
273	KIP	0,2 wks	Thu 24/04/03	Thu 24/04/03

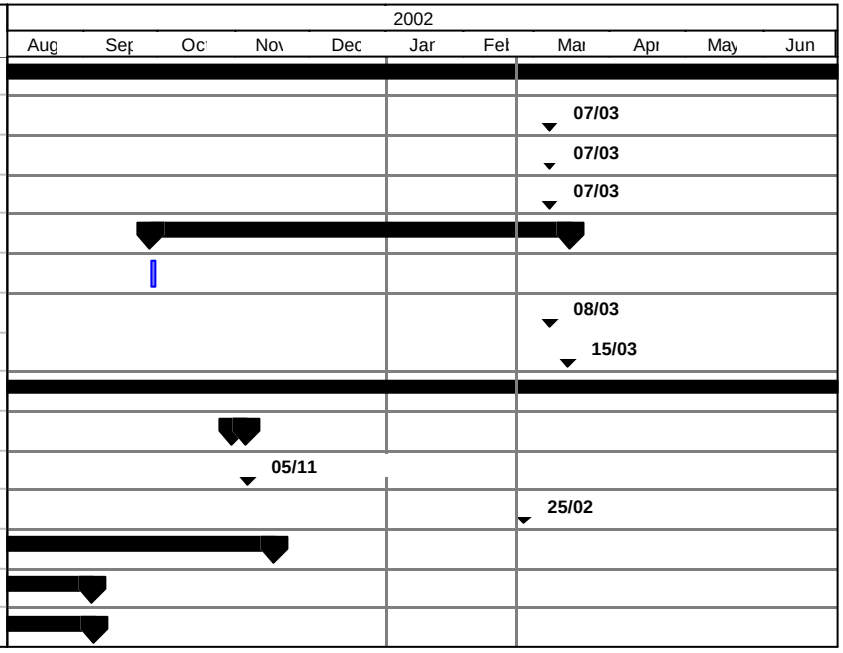


ID	Task Name	Duration	Start	Finish
274	Conformal coating	1 day	Fri 25/04/03	Fri 25/04/03
275	Board Testing (S/N 03 SPIRE)	5 days	Mon 28/04/03	Fri 02/05/03
276	KIP	0,2 wks	Mon 05/05/03	Mon 05/05/03
277	Conformal coating	1 day	Tue 06/05/03	Tue 06/05/03
278	Board Testing (S/N 04 Spare)	5 days	Wed 07/05/03	Tue 13/05/03
279	KIP	0,2 wks	Wed 14/05/03	Wed 14/05/03
280	Conformal coating	1 day	Thu 15/05/03	Thu 15/05/03
281	Board Testing (S/N 05 Spare)	5 days	Fri 16/05/03	Thu 22/05/03
282	KIP	0,2 wks	Fri 23/05/03	Fri 23/05/03
283	Conformal coating	1 day	Mon 26/05/03	Mon 26/05/03

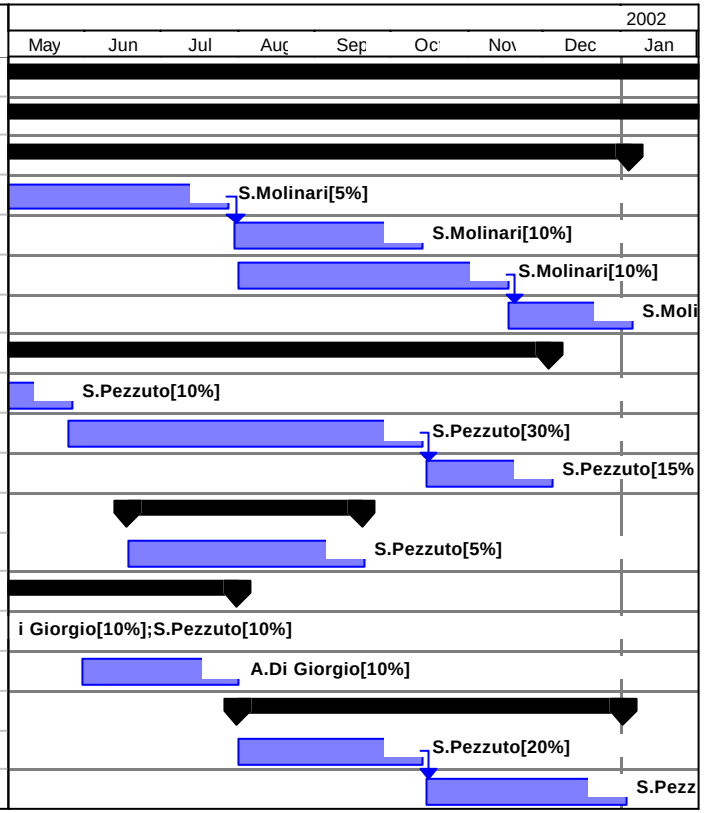


9.3 PACS

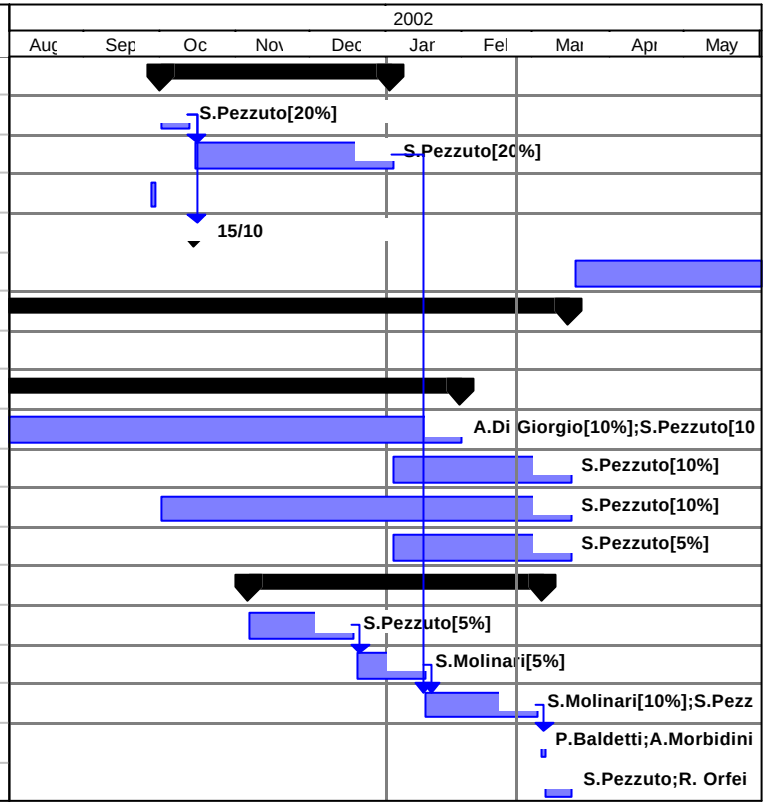
ID	Task Name	Duration	Start	Finish
285	**PACS_WP**	**152,8 wks**	**Wed 05/07/00**	**Mon 09/06/03**
286	**PACS Simulators**	**0 wks**	**Thu 07/03/02**	**Thu 07/03/02**
287	SPU S/W Simul. at IFSI	0 wks	Thu 07/03/02	Thu 07/03/02
288	DEC/MEC S/W Simul. at IFSI	0 wks	Thu 07/03/02	Thu 07/03/02
289	**Reviews**	**24,2 wks**	**Fri 28/09/01**	**Fri 15/03/02**
290	Req/Arch design	1 day	Fri 28/09/01	Fri 28/09/01
291	AVM TRR	1 day	Fri 08/03/02	Fri 08/03/02
292	AVM Delivery	1 day	Fri 15/03/02	Fri 15/03/02
293	**PACS AVM**	**152,8 wks**	**Wed 05/07/00**	**Mon 09/06/03**
294	**PACS Acceptance Tests at CGS**	**0,8 wks**	**Wed 31/10/01**	**Mon 05/11/01**
299	CPU+I/F+MB Boards at IFSI	0 wks	Mon 05/11/01	Mon 05/11/01
300	DC/DC Board at IFSI	0 wks	Mon 25/02/02	Mon 25/02/02
301	**PACS Board Assembly**	**19,2 wks**	**Fri 06/07/01**	**Fri 16/11/01**
306	**PACS PC & Room/Settings**	**8,6 wks**	**Fri 06/07/01**	**Tue 04/09/01**
312	**PACS S/C-Sim <=> DPU-Sim Test**	**5,2 wks**	**Wed 01/08/01**	**Wed 05/09/01**



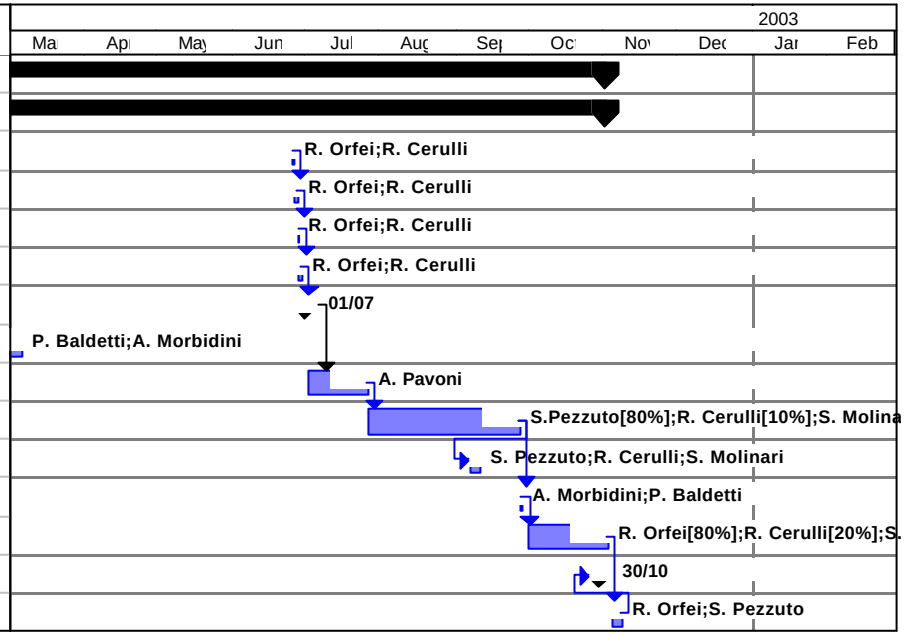
ID	Task Name	Duration	Start	Finish
316	**PACS OBS**	**152,8 wks**	**Wed 05/07/00**	**Mon 09/06/03**
317	**PACS OBS Development**	**126,8 wks**	**Wed 03/01/01**	**Mon 09/06/03**
318	**S/C I/F task**	**48,8 wks**	**Tue 30/01/01**	**Fri 04/01/02**
319	S/C I/F study & S/W design	129 days	Tue 30/01/01	Fri 27/07/01
320	S/C I/F task dvlpmt & integr.with VIRTUOSO	55 days	Mon 30/07/01	Fri 12/10/01
321	S/C I/F task development under Windows	78 days	Tue 31/07/01	Thu 15/11/01
322	S/C I/F task testing	36 days	Fri 16/11/01	Fri 04/01/02
323	**S/S I/F Tasks**	**36 wks**	**Tue 27/03/01**	**Mon 03/12/01**
324	S/S I/F study & S/W des.	44 days	Tue 27/03/01	Fri 25/05/01
325	S/S I/F task dvlpmt& integr.	101 days	Fri 25/05/01	Fri 12/10/01
326	S/S I/F task testing	36 days	Mon 15/10/01	Mon 03/12/01
327	**DPU OBS simulators**	**13,6 wks**	**Mon 18/06/01**	**Wed 19/09/01**
328	DPU S/Ss simulators	68 days	Mon 18/06/01	Wed 19/09/01
329	**OBS Controller Prototype**	**30 wks**	**Wed 03/01/01**	**Tue 31/07/01**
330	OBS Contr. Requ. study & task arch.	75 days	Wed 03/01/01	Tue 17/04/(
331	Pototype development	45 days	Wed 30/05/01	Tue 31/07/01
332	**OBS Controller**	**22,4 wks**	**Tue 31/07/01**	**Wed 02/01/02**
333	OBS Controller development & integr.	54 days	Tue 31/07/01	Fri 12/10/01
334	OBS Controller testing	58 days	Mon 15/10/01	Wed 02/01/02



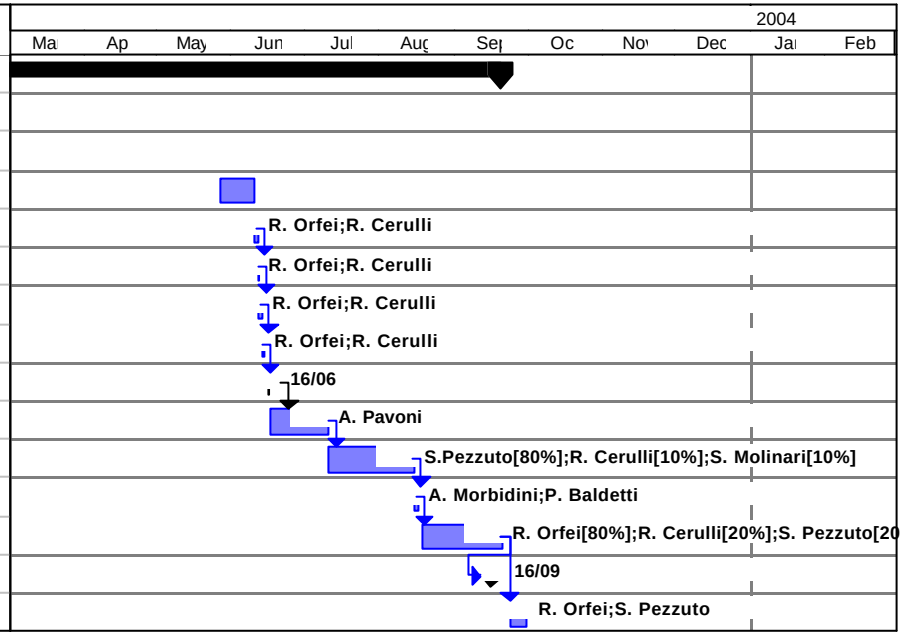
ID	Task Name	Duration	Start	Finish
335	**S/Ss Monitoring**	**13,6 wks**	**Mon 01/10/01**	**Wed 02/01/02**
336	S/S monitoring development & integr.	10 days	Mon 01/10/01	Fri 12/10/01
337	S/S monit. testing	58 days	Mon 15/10/01	Wed 02/01/02
338	OBS Architecture ready - AD Review	1 day	Fri 28/09/01	Fri 28/09/01
339	AVM issue 0	0,2 wks	Mon 15/10/01	Mon 15/10/01
340	PFM development	321 days	Mon 18/03/02	Mon 09/06/03
341	**SW Documentation**	**88,6 wks**	**Wed 05/07/00**	**Fri 15/03/02**
342	URD - User Requir. Doc	130 days	Wed 05/07/00	Tue 02/01/01
343	**SSD - SW Spec. Doc**	**56,4 wks**	**Tue 02/01/01**	**Wed 30/01/02**
344	Architecture	282 days	Tue 02/01/01	Wed 30/01/02
345	OBS DDD - Detail design doc	52 days	Thu 03/01/02	Fri 15/03/02
346	SVVP-SW Val &Ver. Plan	120 days	Mon 01/10/01	Fri 15/03/02
347	OBS User Manual Draft	52 days	Thu 03/01/02	Fri 15/03/02
348	**DPU-OBS Integraftion**	**17,2 wks**	**Tue 06/11/01**	**Tue 05/03/02**
349	J-TAG DPU <=> S/S-Sim Test	30 days	Tue 06/11/01	Mon 17/12/01
350	J-TAG DPU <=> S/C-Sim Test	19 days	Thu 20/12/01	Tue 15/01/02
351	EGSE DPU-OBS Test	33 days	Wed 16/01/02	Fri 01/03/02
352	Box Assembly	2 days	Mon 04/03/02	Tue 05/03/02
353	**PACS AVM delivery to MPE**	1,69 wks	Tue 05/03/02	Fri 15/03/02



ID	Task Name	Duration	Start	Finish
355	**PACS EQM**	**38,6 wks**	**Wed 06/02/02**	**Fri 01/11/02**
356	**PACS EQM Acceptance Tests at CGS**	**38,6 wks**	**Wed 06/02/02**	**Fri 01/11/02**
357	Electrical Tests	1 day	Tue 25/06/02	Tue 25/06/02
358	S/C I/F Signals	0,2 wks	Wed 26/06/02	Wed 26/06/02
359	S/S I/F Signals	1 day	Thu 27/06/02	Thu 27/06/02
360	SW Tests	1 day	Fri 28/06/02	Fri 28/06/02
361	CPU+I/F+DC/DC + MB Boards at IFSI	1 day	Mon 01/07/02	Mon 01/07/02
362	Mechanical mfg	4 wks	Wed 06/02/02	Tue 05/03/0
363	Cabling	18 days	Tue 02/07/02	Thu 25/07/02
364	DPU-OBS Integration	9 wks	Fri 26/07/02	Thu 26/09/02
365	S/W Review	2 days	Fri 06/09/02	Mon 09/09/02
366	Box Assembly	1 day	Fri 27/09/02	Fri 27/09/02
367	Envir. Tests	5 wks	Mon 30/09/02	Fri 01/11/02
368	TRRB HW & SW and DRB	0,2 wks	Wed 30/10/02	Wed 30/10/02
369	**PACS EQM Delivery to MPE**	0,8 wks	Mon 04/11/02	Thu 07/11/02

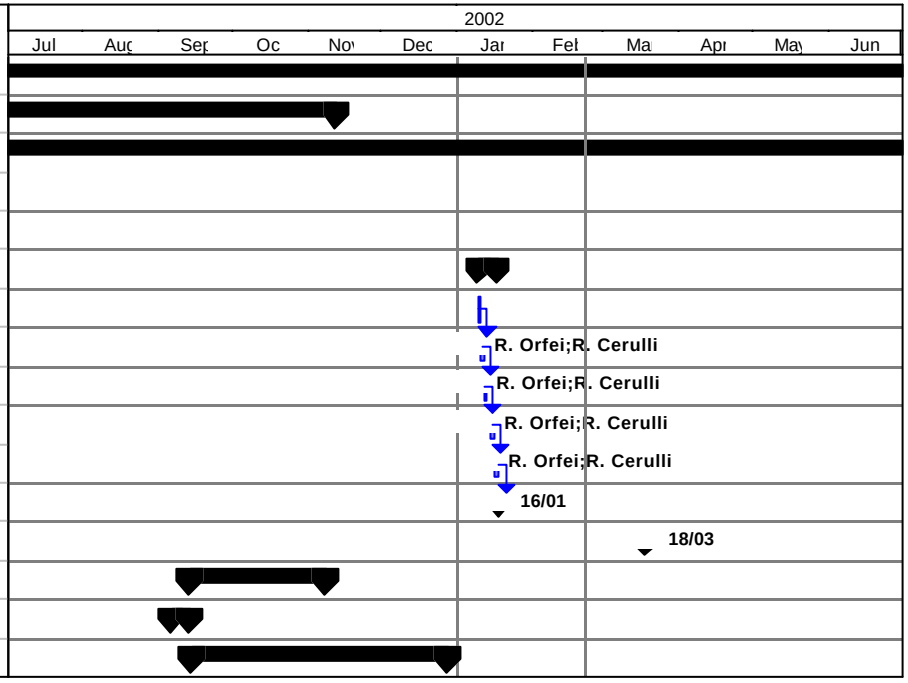


ID	Task Name	Duration	Start	Finish
371	**PACS FM**	**80,6 wks**	**Wed 06/03/02**	**Fri 19/09/03**
372	DPU CDR	0,2 wks	Thu 12/09/02	Thu 12/09/02
373	Mechanical mfg	4 wks	Wed 06/03/02	Tue 02/04/02
374	Burn of Flight PROMs	2 wks	Tue 27/05/03	Mon 09/06/03
375	Electrical Tests	1 day	Tue 10/06/03	Tue 10/06/03
376	S/C I/F Signals	1 day	Wed 11/06/03	Wed 11/06/03
377	S/S I/F Signals	1 day	Thu 12/06/03	Thu 12/06/03
378	SW Tests	1 day	Fri 13/06/03	Fri 13/06/03
379	CPU+I/F+DC/DC Conv. MB Boards at IFSI	1 day	Mon 16/06/03	Mon 16/06/03
380	Cabling	18 days	Tue 17/06/03	Thu 10/07/03
381	DPU-OBS Integration	5 wks	Fri 11/07/03	Thu 14/08/03
382	Box Assembly	1 day	Fri 15/08/03	Fri 15/08/03
383	Envir. Tests	5 wks	Mon 18/08/03	Fri 19/09/03
384	TRRB HW & SW and DRB	0,2 wks	Tue 16/09/03	Tue 16/09/03
385	**PACS FM Delivery to MPE**	1 wk	Tue 23/09/03	Mon 29/09/03

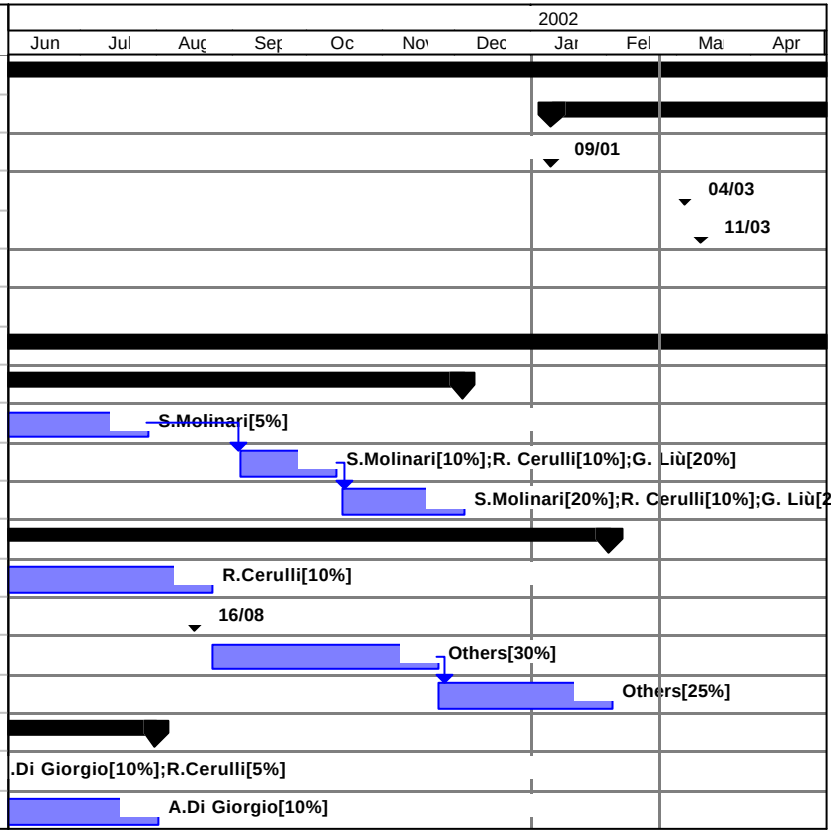


9.4 HIFI

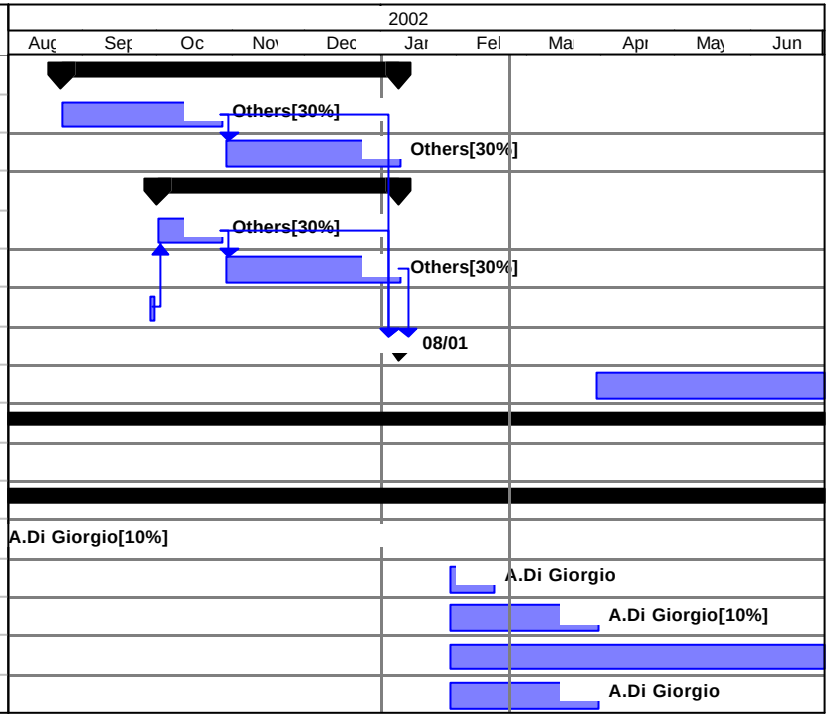
ID	Task Name	Duration	Start	Finish
387	**HIFI_WP**	**186,6 wks**	**Wed 07/06/00**	**Fri 02/01/04**
388	**HIFI Simulators**	**23,2 wks**	**Mon 04/06/01**	**Mon 12/11/01**
390	**HIFI AVM**	**185,8 wks**	**Wed 07/06/00**	**Mon 29/12/03**
391	ICU PDR	0,2 wks	Thu 22/02/01	Thu 22/02/01
392	Instrument PDR	0,2 wks	Fri 27/04/01	Fri 27/04/01
393	**HIFI Acceptance Tests at CGS**	**1,2 wks**	**Wed 09/01/02**	**Wed 16/01/02**
394	Acceptance Doc. Agreement	1 day	Wed 09/01/02	Wed 09/01/02
395	Electrical Tests	1 day	Thu 10/01/02	Thu 10/01/02
396	S/C I/F Signals	1 day	Fri 11/01/02	Fri 11/01/02
397	S/S I/F Signals	1 day	Mon 14/01/02	Mon 14/01/02
398	PROM & EEPROM S/W Test	2 days	Tue 15/01/02	Wed 16/01/02
399	CPU+I/F+MB Boards at IFSI	0 wks	Wed 16/01/02	Wed 16/01/02
400	DC/DC Board at IFSI	0,2 wks	Mon 18/03/02	Mon 18/03/02
401	**HIFI Boards Assembly**	**8,2 wks**	**Thu 13/09/01**	**Thu 08/11/01**
406	**HIFI PC Settings**	**1,2 wks**	**Thu 06/09/01**	**Thu 13/09/01**
409	**HIFI S/C-Sim <=> ICU-Sim Test**	**15 wks**	**Fri 14/09/01**	**Thu 27/12/01**



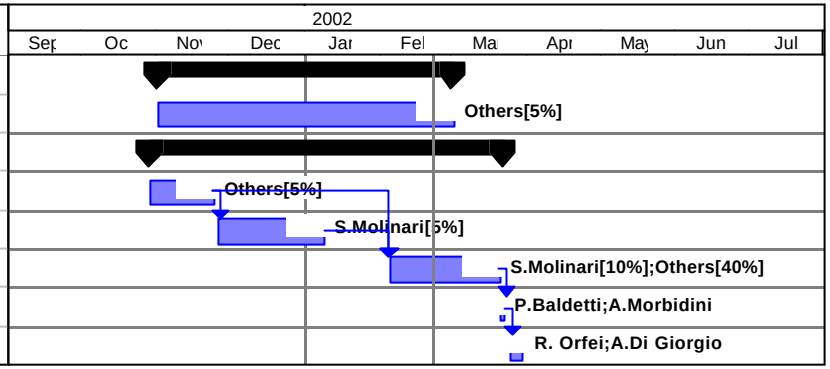
ID	Task Name	Duration	Start	Finish
412	**HIFI OBS**	**185,8 wks**	**Wed 07/06/00**	**Mon 29/12/03**
413	**Reviews**	**102,8 wks**	**Wed 09/01/02**	**Mon 29/12/03**
414	Req/Arch design	2 days	Wed 09/01/02	Thu 10/01/02
415	AVM TRR	0,2 wks	Mon 04/03/02	Mon 04/03/02
416	AVM Delivery	0,2 wks	Mon 11/03/02	Mon 11/03/02
417	PFM TRR	0,2 wks	Mon 22/12/03	Mon 22/12/03
418	PFM delivery	0,2 wks	Mon 29/12/03	Mon 29/12/03
419	**HIFI OBS Development**	**155,8 wks**	**Wed 03/01/01**	**Mon 29/12/03**
420	**HIFI S/C I/F task**	**44 wks**	**Tue 30/01/01**	**Mon 03/12/01**
421	S/C I/F study and S/W design	129 days	Tue 30/01/01	Fri 27/07/01
422	S/C I/F task development	30 days	Mon 03/09/01	Fri 12/10/01
423	S/C I/F task integr. and testing	36 days	Mon 15/10/01	Mon 03/12/01
424	**HIFI S/S I/F Tasks**	**52,4 wks**	**Thu 01/02/01**	**Fri 01/02/02**
425	S/S I/F study and S/W design	145 days	Thu 01/02/01	Wed 22/08/01
426	**Command req.s frozen**	1 day	Thu 16/08/01	Thu 16/08/01
427	S/S I/F tasks development	66 days	Thu 23/08/01	Thu 22/11/01
428	S/S I/F task integr. and testing	51 days	Fri 23/11/01	Fri 01/02/02
429	**HIFI OBS Controller Prototype**	**30 wks**	**Wed 03/01/01**	**Tue 31/07/01**
430	Requir. study & task arch.	100 days	Wed 03/01/01	Tue 22/05
431	prototype development	45 days	Wed 30/05/01	Tue 31/07/01



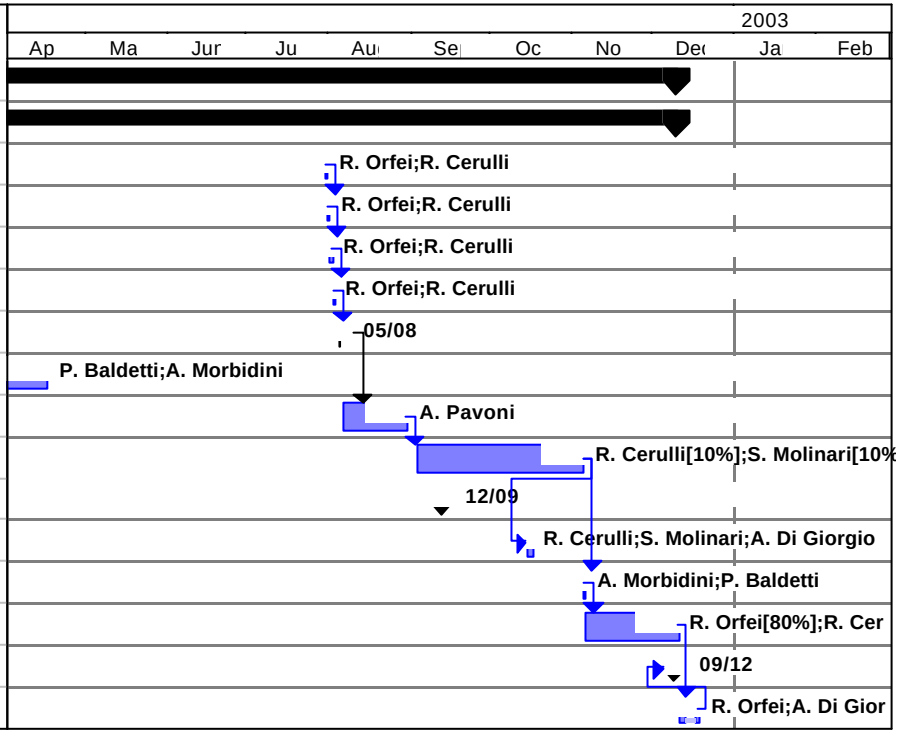
ID	Task Name	Duration	Start	Finish
432	**HIFI OBS Controller**	**19,6 wks**	**Thu 23/08/01**	**Mon 07/01/02**
433	OBS Controller development	47 days	Thu 23/08/01	Fri 26/10/01
434	OBS Controller integr. & testing	51 days	Mon 29/10/01	Mon 07/01/02
435	**HIFI S/Ss Monitoring**	**14,2 wks**	**Mon 01/10/01**	**Mon 07/01/02**
436	S/S monitoring development	20 days	Mon 01/10/01	Fri 26/10/01
437	S/S monit. integr. and testing	51 days	Mon 29/10/01	Mon 07/01/02
438	HIFI OBS Arch. ready - AD Review	1 day	Fri 28/09/01	Fri 28/09/01
439	AVM issue0	0,2 wks	Tue 08/01/02	Tue 08/01/02
440	PFM development	91,4 wks	Fri 29/03/02	Mon 29/12/03
441	**HIFI SW Documentation**	**185,8 wks**	**Wed 07/06/00**	**Mon 29/12/03**
442	URD - User Requir. Doc	130 days	Wed 05/07/00	Tue 02/01/01
443	**HIFI SSD - SW spec. Doc**	**185,8 wks**	**Wed 07/06/00**	**Mon 29/12/03**
444	Draft Architecture & SR	298 days	Wed 07/06/00	Fri 27/07/
445	Full document	14 days	Mon 28/01/02	Thu 14/02/02
446	DDD - Detail design doc	45 days	Mon 28/01/02	Fri 29/03/02
447	OBS User Manual	501 days	Mon 28/01/02	Mon 29/12/03
448	SVVP - SW Val. & Ver. Plan	9 wks	Mon 28/01/02	Fri 29/03/02



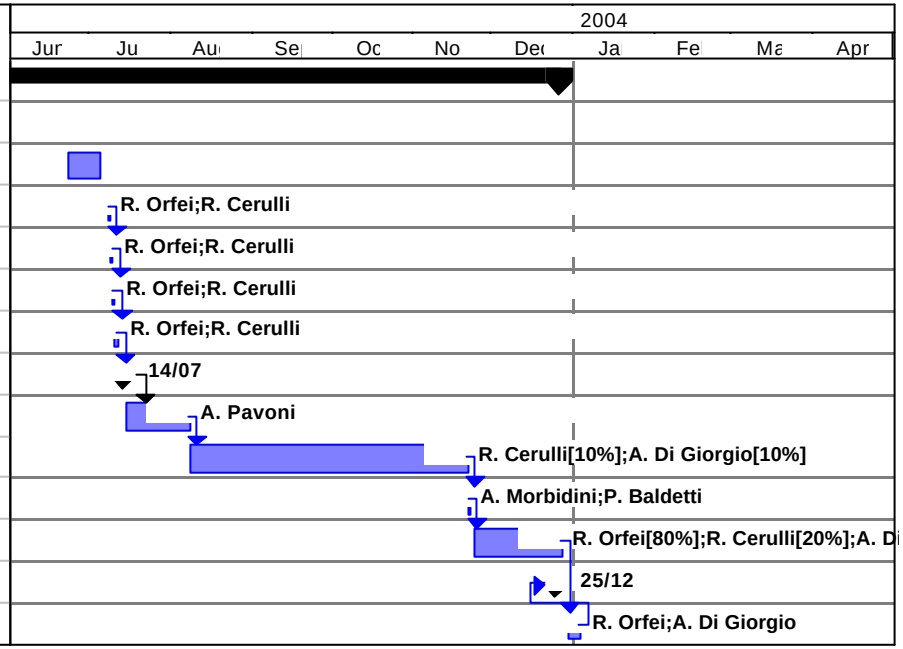
ID	Task Name	Duration	Start	Finish
449	**HIFI Support activities**	**17,4 wks**	**Thu 01/11/01**	**Fri 01/03/02**
450	Testing tools developm.	87 days	Thu 01/11/01	Fri 01/03/02
451	**HIFI ICU-OBS Integraftion**	**21 wks**	**Mon 29/10/01**	**Fri 22/03/02**
452	J-TAG ICU <-> S/S-Sim Test	20 days	Mon 29/10/01	Fri 23/11/01
453	J-TAG ICU <-> S/C-Sim Test	31 days	Mon 26/11/01	Mon 07/01/02
454	HIFI EGSE ICU-OBS Test	33 days	Mon 04/02/02	Wed 20/03/02
455	Box Assembly	2 days	Thu 21/03/02	Fri 22/03/02
456	**HIFI AVM delivery to SRON**	1 wk	Mon 25/03/02	Fri 29/03/02



ID	Task Name	Duration	Start
458	**HIFI EQM**	**38,2 wks**	**Tue 19/03/02**
459	**HIFI EQM Acceptance Tests at CGS**	**38,2 wks**	**Tue 19/03/02**
460	Electrical Tests	1 day	Tue 30/07/02
461	S/C I/F Signals	0,2 wks	Wed 31/07/02
462	S/S I/F Signals	1 day	Thu 01/08/02
463	SW Tests	1 day	Fri 02/08/02
464	CPU+I/F+DC/DC Conv. MB Boards at IFSI	1 day	Mon 05/08/02
465	Mechanical mfg	4 wks	Tue 19/03/02
466	Cabling	18 days	Tue 06/08/02
467	DPU-OBS Integration	9 wks	Tue 03/09/02
468	ICU CDR	0,2 wks	Thu 12/09/02
469	S/W Review	2 days	Tue 15/10/02
470	Box Assembly	1 day	Tue 05/11/02
471	Envir. Tests	5 wks	Wed 06/11/02
472	TRRB HW & SW and DRB	0,2 wks	Mon 09/12/02
473	**HIFI EQM delivery to SRON**	0,8 wks	Wed 11/12/02

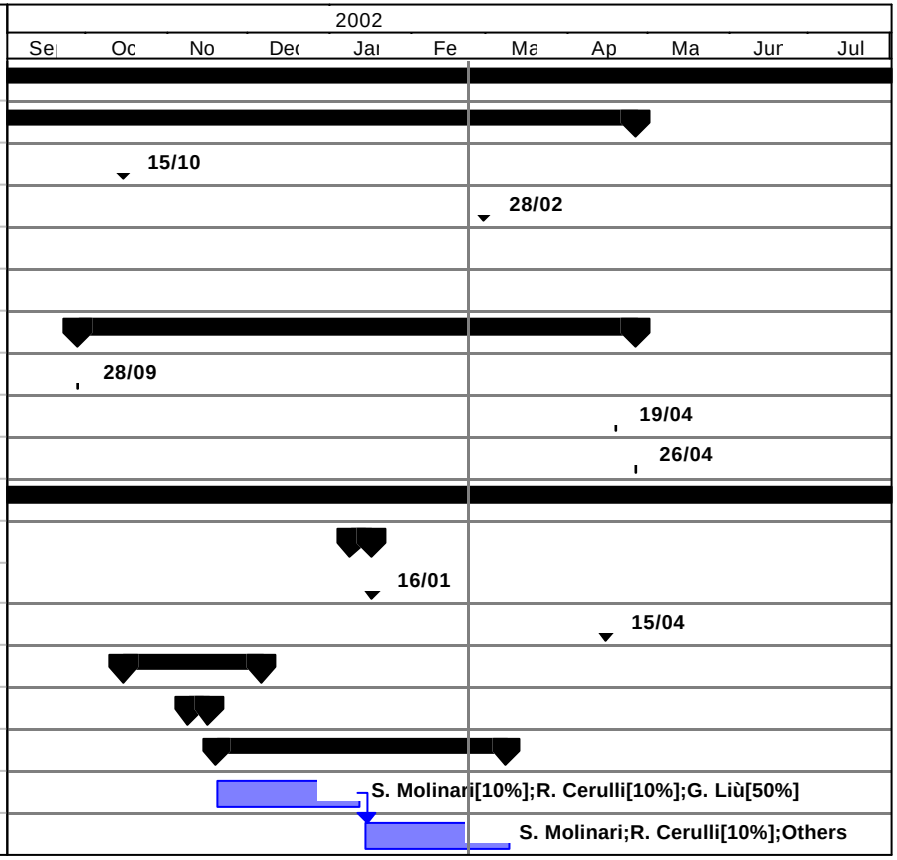


ID	Task Name	Duration	Start
475	**HIFI FM**	**88,8 wks**	**Tue 16/04/02**
476	Mechanical mfg	4 wks	Tue 16/04/02
477	Burn of Flight PROMs	2 wks	Mon 23/06/03
478	Electrical Tests	1 day	Tue 08/07/03
479	S/C I/F Signals	1 day	Wed 09/07/03
480	S/S I/F Signals	1 day	Thu 10/07/03
481	SW Tests	1 day	Fri 11/07/03
482	CPU+I/F+DC/DC Conv. MB Boards at IFSI	1 day	Mon 14/07/03
483	Cabling	18 days	Tue 15/07/03
484	DPU-OBS Integration	15 wks	Fri 08/08/03
485	Box Assembly	1 day	Fri 21/11/03
486	Envir. Tests	5 wks	Mon 24/11/03
487	TRRB HW & SW and DRB	0,15 wks	Thu 25/12/03
488	**HIFI FM delivery to SRON**	1 wk	Mon 29/12/03

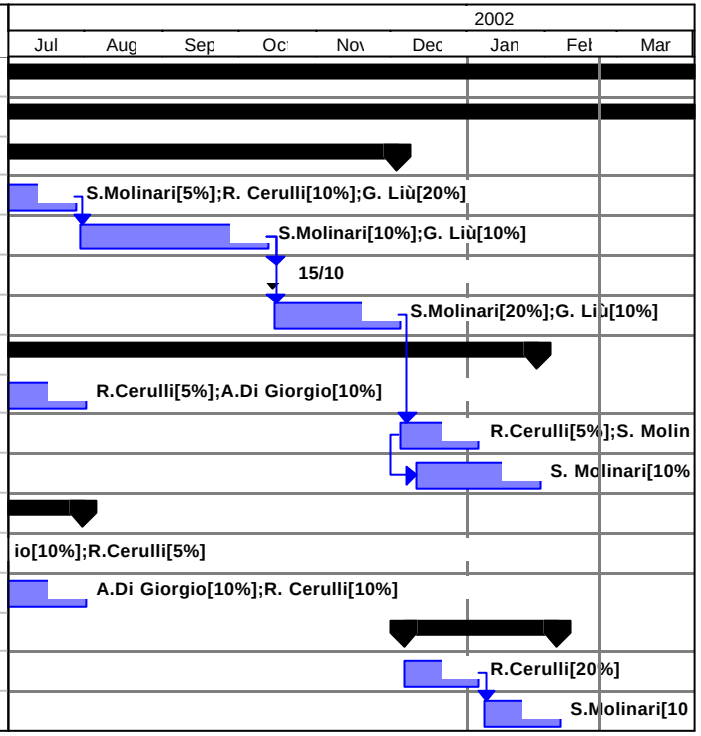


9.5 SPIRE

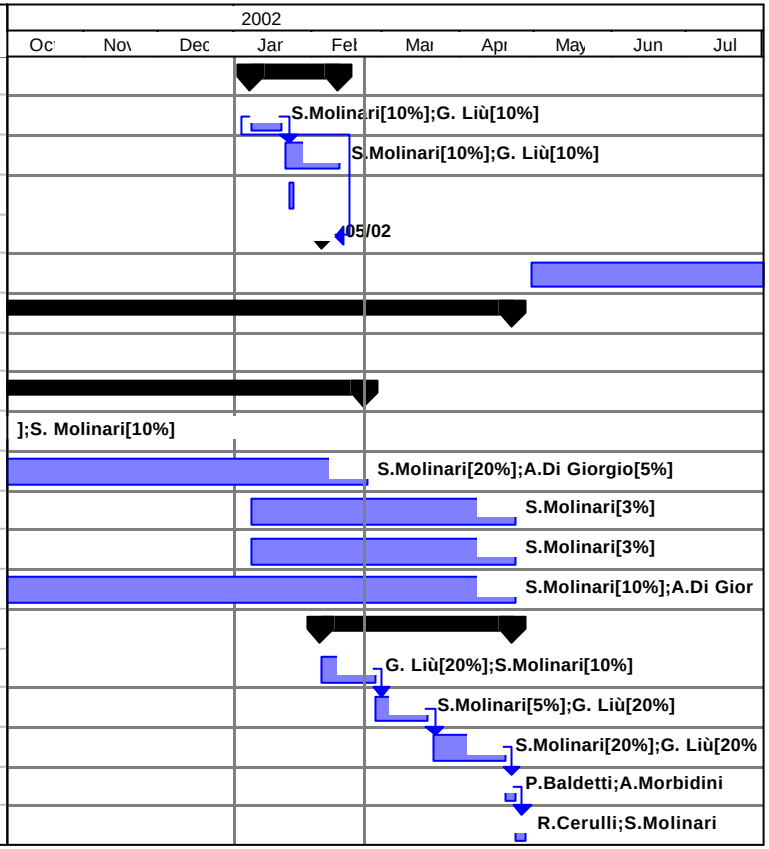
ID	Task Name	Duration	Start
490	**SPIRE_WP**	**194,4 wks**	**Mon 26/06/00**
491	**SPIRE Simulators**	**96 wks**	**Mon 26/06/00**
492	S/S Simulator (IFSI)	0 wks	Mon 15/10/01
493	DRCU Simulator at IFSI	0 wks	Thu 28/02/02
494	DPU PDR	0,2 wks	Mon 26/06/00
495	SPIRE PDR	0,2 wks	Mon 23/04/01
496	**Reviews**	**30,2 wks**	**Fri 28/09/01**
497	Req/Arch design	0,2 wks	Fri 28/09/01
498	AVM TRR	0,2 wks	Fri 19/04/02
499	AVM Delivery	0,2 wks	Fri 26/04/02
500	**SPIRE AVM**	**193 wks**	**Wed 05/07/00**
501	**SPIRE Acceptance Tests at CGS**	**1,2 wks**	**Wed 09/01/02**
507	CPU+I/F+MB Boards at IFSI	0 wks	Wed 16/01/02
508	DC/DC Board at IFSI	0,2 wks	Mon 15/04/02
509	**SPIRE Boards Assembly**	**7,8 wks**	**Mon 15/10/01**
514	**SPIRE PC Settings**	**1,2 wks**	**Fri 09/11/01**
517	**SPIRE S/C-Sim <=> DPU-Sim Test**	**16 wks**	**Mon 19/11/01**
518	S/C-Sim Test	8 wks	Mon 19/11/01
519	RT-(PC-WIN98)<=> S/C-Sim Test	8 wks	Mon 14/01/02



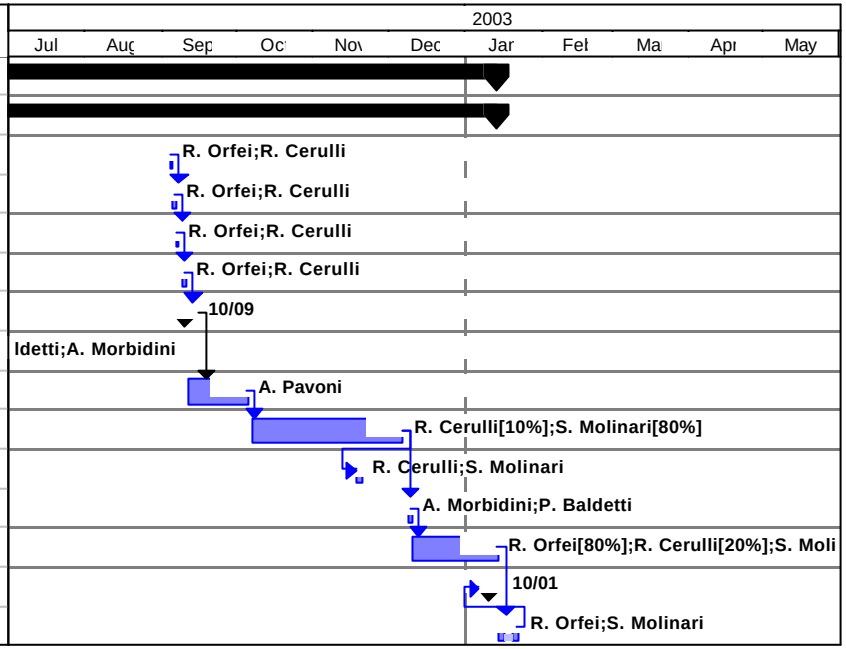
ID	Task Name	Duration	Start	Finish
520	**SPIRE OBS**	**193 wks**	**Wed 05/07/00**	**Tue 16/03/04**
521	**SPIRE OBS Development**	**182 wks**	**Wed 20/09/00**	**Tue 16/03/04**
522	**SPIRE S/C I/F task**	**44 wks**	**Tue 30/01/01**	**Mon 03/12/01**
523	S/C I/F study and S/W design	129 days	Tue 30/01/01	Fri 27/07/01
524	S/C I/F task dvpmt & Integr. with VIRTUOSO	55 days	Mon 30/07/01	Fri 12/10/01
525	SPIRE commanding req.s frozen	1 day	Mon 15/10/01	Mon 15/10/01
526	S/C I/F task integr. and testing	36 days	Mon 15/10/01	Mon 03/12/01
527	**SPIRE S/S I/F Tasks**	**53,2 wks**	**Mon 22/01/01**	**Mon 28/01/02**
528	SPIRE S/S I/F study and S/W design	137 days	Mon 22/01/01	Tue 31/07/01
529	HIFI S/S I/F tasks adaptation	24 days	Tue 04/12/01	Fri 04/01/02
530	SPIRE S/S I/F task integr. and testing	35 days	Tue 11/12/01	Mon 28/01/02
531	**SPIRE OBS Controller Prototype**	**45 wks**	**Wed 20/09/00**	**Tue 31/07/01**
532	Requirements study & task arch.	100 days	Wed 03/01/01	Tue 22/05/
533	prototype development	45 wks	Wed 20/09/00	Tue 31/07/01
534	**SPIRE OBS Controller**	**8,8 wks**	**Thu 06/12/01**	**Tue 05/02/02**
535	SPIRE OBS Controller development	22 days	Thu 06/12/01	Fri 04/01/02
536	SPIRE OBS Controller integr. & testing	22 days	Mon 07/01/02	Tue 05/02/02



ID	Task Name	Duration	Start	Finish
537	**SPIRE S/Ss Monitoring**	**5,2 wks**	**Mon 07/01/02**	**Mon 11/02/02**
538	SPIRE S/S monitoring development	10 days	Mon 07/01/02	Fri 18/01/02
539	SPIRE S/S monit. integr. and testing	16 days	Mon 21/01/02	Mon 11/02/02
540	SPIRE OBS Arch. ready - AD Review	1 day	Wed 23/01/02	Wed 23/01/02
541	SPIRE AVM issue0	0,2 wks	Tue 05/02/02	Tue 05/02/02
542	SPIRE PFM development	98,4 wks	Mon 29/04/02	Tue 16/03/04
543	**SW Documentation**	**93,8 wks**	**Wed 05/07/00**	**Mon 22/04/02**
544	SPIRE URD - User Requir. Doc	130 days	Wed 05/07/00	Tue 02/01/01
545	**SPIRE SSD - SW spec. Doc**	**59,8 wks**	**Tue 02/01/01**	**Fri 22/02/02**
546	SPIRE Draft Architecture & SR	151 days	Tue 02/01/01	Tue 31/07/(
547	SPIRE SSD Full document	148 days	Wed 01/08/01	Fri 22/02/02
548	SPIRE OBS DDD - Detail design doc	76 days	Mon 07/01/02	Mon 22/04/02
549	SPIRE OBS User Manual Draft	76 days	Mon 07/01/02	Mon 22/04/02
550	SPIRE OBS SVVP - SW Val. & Ver. Plan	60,8 wks	Wed 21/02/01	Mon 22/04/02
551	**SPIRE AVM DPU-OBS Integration**	**11,2 wks**	**Mon 04/02/02**	**Mon 22/04/02**
552	J-TAG DPU <=> SPIRE S/S-Sim Test	15,5 days	Mon 04/02/02	Mon 25/02/02
553	J-TAG DPU <=> S/C-Sim Test	15,5 days	Mon 25/02/02	Mon 18/03/02
554	EGSE SPIRE DPU-OBS Test	21 days	Thu 21/03/02	Thu 18/04/02
555	Box Assembly	2 days	Fri 19/04/02	Mon 22/04/02
556	**SPIRE AVM delivery to RAL**	4 days	Tue 23/04/02	Fri 26/04/02



ID	Task Name	Duration	Start	Finish
558	**SPIRE EQM**	**35 wks**	**Tue 14/05/02**	**Mon 13/01/03**
559	**SPIRE EQM Acceptance Tests at CGS**	**35 wks**	**Tue 14/05/02**	**Mon 13/01/03**
560	Electrical Tests	1 day	Wed 04/09/02	Wed 04/09/02
561	S/C I/F Signals	0,2 wks	Thu 05/09/02	Thu 05/09/02
562	S/S I/F Signals	1 day	Fri 06/09/02	Fri 06/09/02
563	SW Tests	1 day	Mon 09/09/02	Mon 09/09/02
564	CPU+I/F+DC/DC+ MB Boards at IFSI	1 day	Tue 10/09/02	Tue 10/09/02
565	Mechanical mfg	4 wks	Tue 14/05/02	Mon 10/06/
566	Cabling	18 days	Wed 11/09/02	Fri 04/10/02
567	DPU-OBS Integration	9 wks	Mon 07/10/02	Fri 06/12/02
568	S/W Review	2 days	Mon 18/11/02	Tue 19/11/02
569	Box Assembly	1 day	Mon 09/12/02	Mon 09/12/02
570	Envir. Tests	5 wks	Tue 10/12/02	Mon 13/01/03
571	TRRB HW & SW and DRB	0,2 wks	Fri 10/01/03	Mon 13/01/03
572	**SPIRE EQM delivery to RAL**	0,8 wks	Tue 14/01/03	Tue 21/01/03



ID	Task Name	Duration	Start	Finish
574	**SPIRE FM**	**89,8 wks**	**Tue 11/06/02**	**Fri 27/02/04**
575	DPU CDR	0,2 wks	Mon 02/12/02	Mon 02/12/02
576	Mechanical mfg	4 wks	Tue 11/06/02	Mon 08/07/02
577	Burn of Flight PROMs	2 wks	Tue 26/08/03	Mon 08/09/03
578	Electrical Tests	1 day	Tue 09/09/03	Tue 09/09/03
579	S/C I/F Signals	1 day	Wed 10/09/03	Wed 10/09/03
580	S/S I/F Signals	1 day	Thu 11/09/03	Thu 11/09/03
581	SW Tests	1 day	Fri 12/09/03	Fri 12/09/03
582	CPU+I/F+DC/DC+ MB Boards at IFSI	1 day	Mon 15/09/03	Mon 15/09/03
583	Cabling	18 days	Tue 16/09/03	Thu 09/10/03
584	DPU-OBS Integration	15 wks	Fri 10/10/03	Thu 22/01/04
585	Box Assembly	1 day	Fri 23/01/04	Fri 23/01/04
586	Envir. Tests	5 wks	Mon 26/01/04	Fri 27/02/04
587	PFM S/W TRR	0,2 wks	Mon 23/02/04	Mon 23/02/04
588	**SPIRE FM delivery to RAL**	1 wk	Mon 01/03/04	Fri 05/03/04