

	Herschel Space Observatory DPU/ICU Subsystem Development Plan	Ref.: IFSI/ICU/PL/2000-001 Issue: 1.2 Date: 13/06/00
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Herschel Space Observatory

DPU/ICU Subsystem Development Plan

Document Ref.: IFSI/ICU/PL/2000-001

Issue: 1.2

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Issue 1.1		30 January 2001	Different plannings and miscell.
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4.1	HIFI CDR date
7	HW calendar and SW calendar
9	Corrections of plannings after contract ASI-CGS signature
ISSUE 1.2	
All sections	Updated/revised after ICU PDR (HIFI) and DPU PDR (PACS)

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1 Scope of the document

This document describes the development plan of the HSO Data Processing Unit hardware and software:

PACS DPU

HIFI ICU

SPIRE DPU

The development plan is based on the applicable documents cited in paragraph #2.

2 Documents

2.1 Applicable documents

AD1	FIRST/Planck Instrument Interface Document Part A	PT-IID-A-04624
AD2	FIRST/Planck Instrument Interface Document Part B – Instrument “	PT-PACS-02126
AD3	FIRST/Planck Instrument Interface Document Part B – Instrument “HIFI”	PT-HIFI-02125
AD4	FIRST/Planck Instrument Interface Document Part B- Instrument “SPIRE”	PT-SPIRE-02124
AD5	PACS Design Development and Verification Plan	PACS-ME-PL-002
AD6	HIFI Instrument Development and Verification plan	SRON-U/HIFI/PL/2000-010
AD7	SPIRE Instrument Development plan	SPIRE-RAL-PRJ-000035
AD8	ICU Subsystem Specification Document	IFSI/ICU/SP/2000-001
AD9	SPIRE DPU Subsystem Specification Document	SPIRE-IFS-PRJ-000462
AD10	PACS DPU Subsystem Specification Document	PACS-CR-GS-006
AD11	HIFI Interface Control Document	SRON-G/HIFI/SP/1999-001
AD12	DPU/ICU On Board Software User Requirements Document PACS	PACS-CR-RD-001
AD13	DPU/ICU On Board Software User Requirements Document HIFI	IFSI/OBS/SP/2000-001
AD14	DPU/ICU On Board Software User Requirements Document SPIRE	SPIRE-IFS-PRJ-000444

AD15	HIFI Instrument Specification	SRON-G/HIFI/SP/1998-001
AD16	PACS Instrument Specification Document	
AD17	SPIRE Instrument Requirements Document	SPIRE-RAL-PRJ-000034
AD18	DPU/ICU Product Assurance Plan	IFSI/ICU/PL/1999-001
AD19	DPU/ICU On Board Software Product Assurance Plan	IFSI/OBS/PL/2000-001
AD20	FIRST/Planck Packet Structure Interface Control Document	SCI-PT-ICD-7527
AD21	F/P CDMS Interface Test Requirements Specifications	SRON-U/HIFI-SP-2000-5
AD22	DPU/ICU WBS	IFSI/ICU/PL/2001-001

2.2 Reference documents

Reference Document	Name	Number
RD1	HSO DPU/ICU Switch-ON Procedure	CNR.IFSI.2001TR01

2.3 Acronyms

AD	Architectural Design
ADx	Applicable Document N. x
ASCII	American Standard Code for Information Interchange
ATP	Acceptance Test Plan
AVM	Avionic Model
CASE	Computer Aided Software Engineering
CDMS	Command and Data Management System
CDR	Critical Design Review
CGS	Carlo Gavazzi Space
CNR	Consiglio Nazionale delle Ricerche
CPU	Control Processing Unit
DDD	Detailed Design Document
DPU	Digital Processing Unit
DRCU	Detector Readout Control Unit
EEPROM	Electrically Erasable Programmable Read Only Memory
EGSE	Electronic Ground Support Equipment
ESA	European Space Agency
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
FCU	Focal plane Control Unit
FIRST	Far InfraRed and Submillimeter Telescope
HIFI	Heterodyne Instrument for FIRST

HK	HouseKeeping
HSO	Herschel Space Observatory
HW	HardWare
IBDR	Instrument Baseline Design Review
ICD	Interface Control Document
ICDR	Instrument Critical Design Review
ICU	Instrument Control Unit
IHDR	Instrument Hardware Design Review
I/F	Interface
IFSI	Istituto di Fisica dello Spazio Interplanetario
ISVR	Instrument Science Verification Review
NCR	Non Conformance report
OBS	On-Board Software
PACS	Photoconductor Array Camera and Spectrometer
PA	Product Assurance
PDR	\Preliminary Design Review
PROM	Programmable Read Only Memory
QA	Quality Assurance
RID	Review Item Discrepancy
S/C	Spacecraft
S/S	Subsystem
SCCS	Source Code Control System
SCR	Software Change Request
SPIRE	Spectral and Photometric Imaging Receiver
SPR	Software Problem Report
SPU	Signal Processing Unit

SR	Software Requirement
SSD	Software Specification Document
SVVP	Software Verification and Validation Plan
SW	SoftWare
TBC	To Be Confirmed
TBD	To Be Defined
TRB	Test Review Board
TRR	Test Readiness Review
TBW	To Be Written
UR	User Requirement
URD	UR Document
WP	Work Package

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3 Description of the DPU/ICU subsystem

The DPU/ICU is based on a 20 MHz clock TEMIC TSC21020, that is a Digital Signal Processing (DSP) developed by Analogue Devices and manufactured and qualified for flight use by TEMIC.

The DSP implements a Harvard architecture, i.e. the data bus (32 bit) and the program bus (48 bit) are completely separated, so increasing the execution speed.

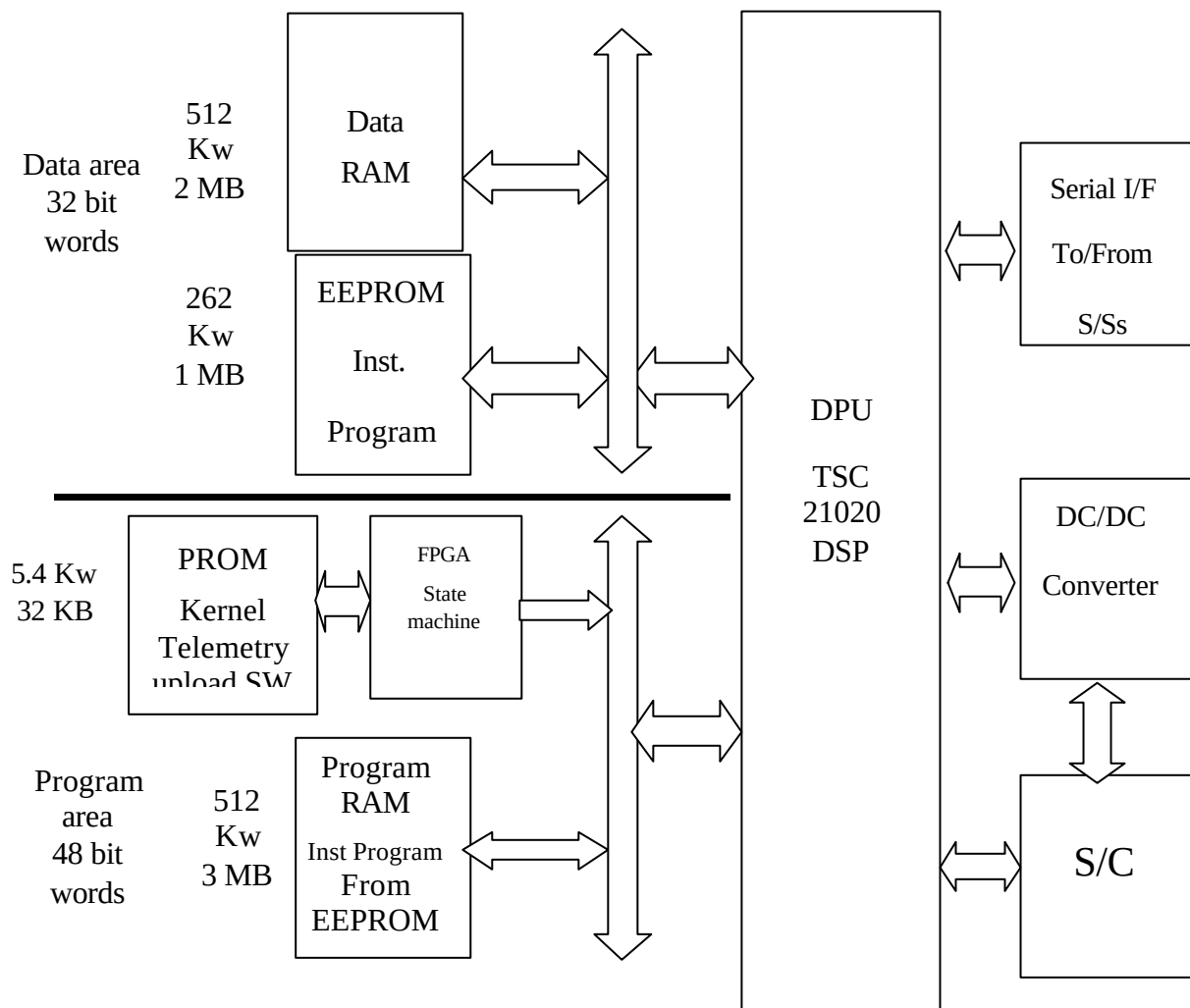
The program area is implemented with PROMs, EEPROMs and RAM. The PROM stores the initial boot loader and emergency recovery modules. At switch on a state machine, implemented in a FPGA, while keeping the DSP in a reset state, copies the PROM content in a suitable program area, the DSP reset is then removed and the basic program runs. After a series of tests (see RD1) the EEPROM content is copied in a suitable program area and the application program starts.

The program area may be used as data memory.

The DPU/ICU includes a synchronized DC/DC converter to supply internal circuitry, and to supply FCU S/S in HIFI.

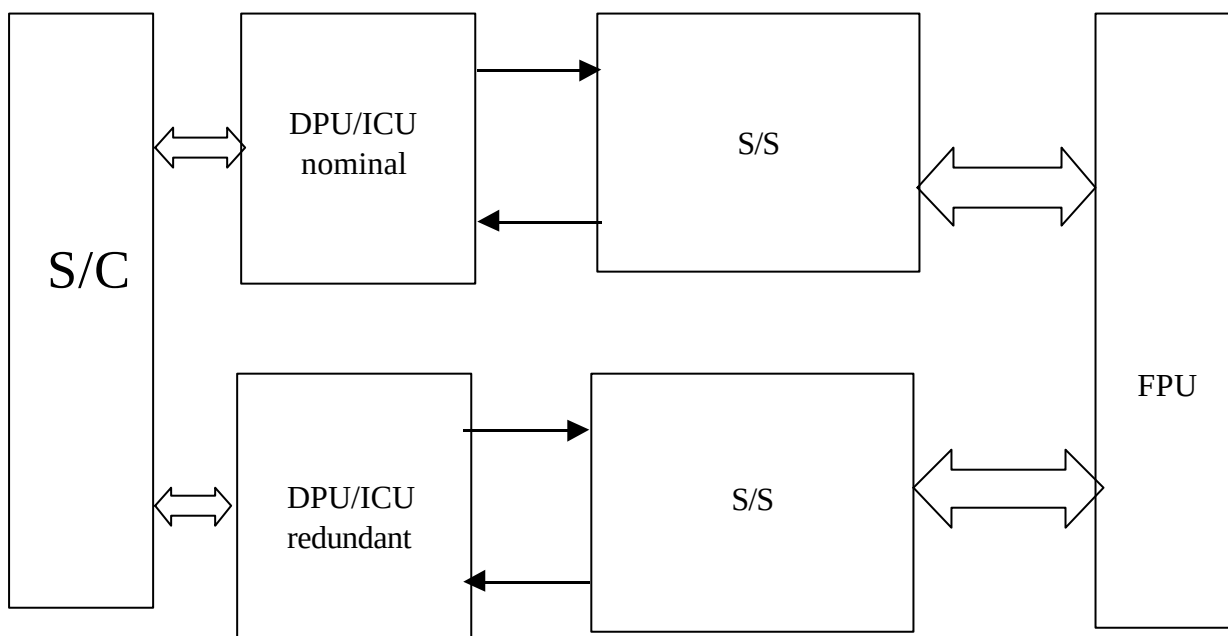
3.1 Overall DPU/ICU block diagram

The following diagram shows the main DPU/ICU blocks and the memory dimensions.



3.2 Redundancy concept

The top level DPU/ICU redundancy concept is shown in the following diagram:



The DPU/ICU box contains two complete units in cold redundancy states. The S/C nominal/redundant 28V power bus controls the switching between the two units.

3.3 DPU/ICU Product Tree

CI IDENTIFICATION	NAME	DELIVERABLE MODELS			
		A	Q	F	S
xxx-DPU/ICU	DPU/ICU Unit	X	X	X	
xxx -DPU/ICU-EL	DPU/ICU Electronics	X	X	X	
xxx -DPU/ICU-EL-1	Boards	X	X	X	
xxx -DPU/ICU-EL-1.1	CPU board Prime	X	X	X	*
xxx -DPU/ICU-EL-1.2	CPU board Redundant		X	X	*
xxx -DPU/ICU-EL-1.3	Interface Board Prime	X	X	X	
xxx -DPU/ICU-EL-1.4	InterfaceBoard Redundant		X	X	X
xxx -DPU/ICU-EL-1.5	DC/DC Conv. Board for DPU/ICU (one conv.)	X			
xxx -DPU/ICU-EL-1.6	DC/DC Conv. Board for ICU and HIFI FCU (2 conv.)	X			
xxx -DPU/ICU-EL-1.7	DC/DC Conv. Board for DPU (one conv.) or for HIFI (2 conv.)		X	X	*
xxx -DPU/ICU-EL-1.8	DC/DC Conv. Board for DPU (one conv.) or for HIFI (2 conv.)		X	X	X
xxx -DPU/ICU-EL-1.9	Motherboard	X	X	X	*
xxx -DPU/ICU-MS	Mechanical Box	X	X	X	

xxx -DPU/ICU-HWSE	Transport Container	X	X	X	
xxx -DPU/ICU-OBS	On Board Software	X	X	X	

N.B1: As far as the Flight Spare items are concerned, for the three Herschel instruments there will be:

- two motherboards for the three instruments
- one CPU board for HIFI and SPIRE
- one CPU board for PACS
- One interface board for PACS/SPIRE
- One interface board for HIFI
- one DC/DC converter board with only the DPU/ICU converter for PACS and SPIRE
- one DC/DC converter board with the DPU/ICU and the HIFI FCU converters

NB2: The item xxx -DPU/ICU-EL-1.6 for the HIFI AVM will consist in a single board, i.e. for (all) the AVMs there will be no redundancy.

NB3: Each box (QM and FM) will contain:

- 1 motherboard
- 2 CPU boards
- 2 Interface Boards
- 2 DC/DC converters Boards and for these:
 - HIFI boards will each have two converters (for ICU and FCU)
 - SPIRE and PACS boards will have each 1 converter only (for the DPU)

4 Constraints

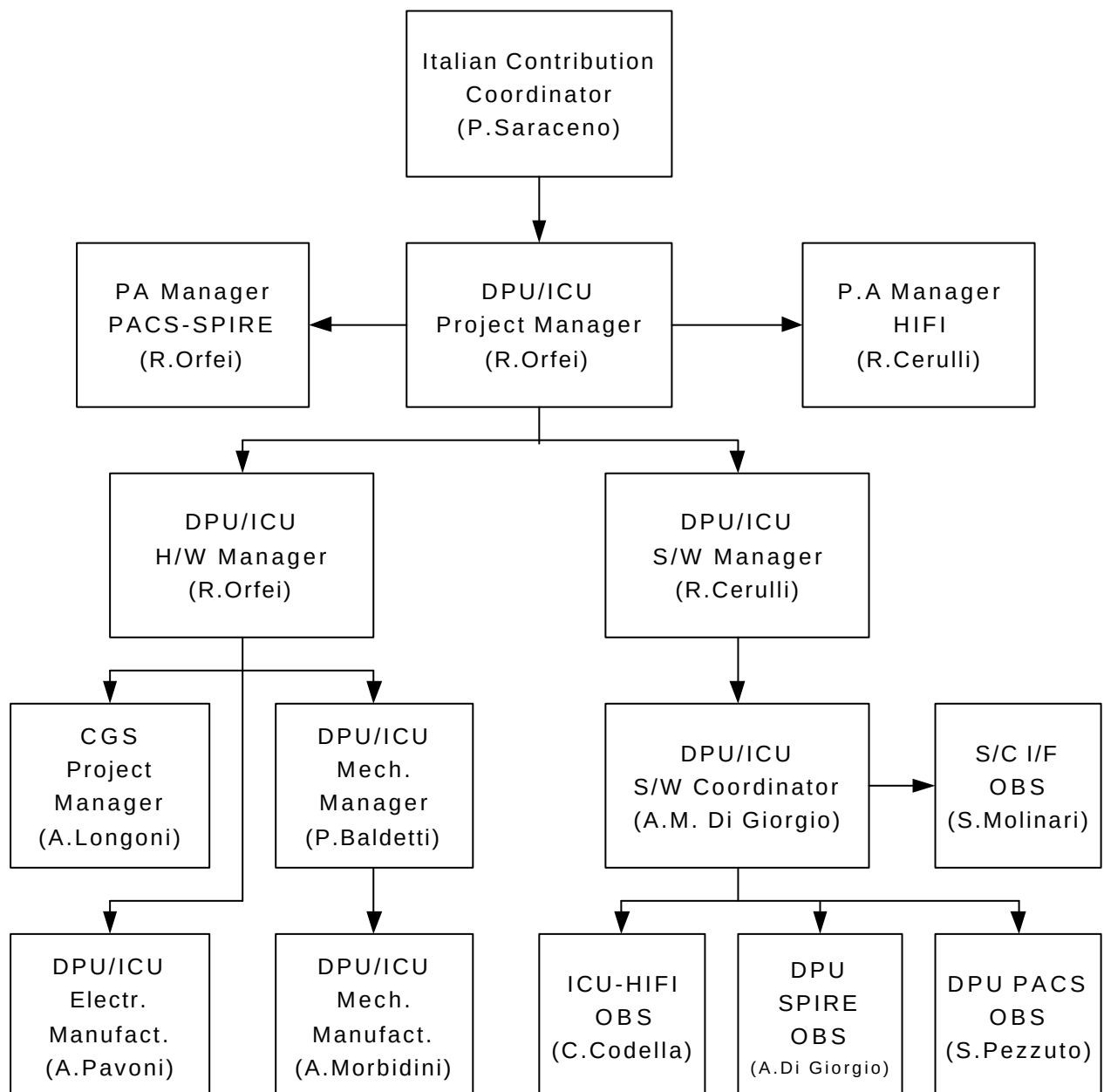
4.1 Calendar constraints

The main HSO project constraints as far as the DPU/ICUs are concerned are:

ACTIVITY	PACS	HIFI	SPIRE
DPU/ICU PDR/IIDR	1-2 March 01	22-02-01	26 June 00
AVM delivery to consortium	Dec 01	Jan 02	Feb 02
CDR	Dec 02	01-02-03	Dec 02
AVM delivery to ESA	Apr 03	Apr 03	Apr 03
EQM delivery to consortium	May 02	Sept 02	Nov 02
PFM delivery to consortium	Sept 03	Jan 04	Mar 04
PFM delivery to ESA	Jul 04	Jul 04	Nov 04
FS delivery to consortium	NA	NA	NA
FS delivery to ESA	Dec 05	Dec 05	Dec 05
HSO launch	1st quart. 2007	1st quart. 2007	1st quart. 2007

5 HW Work description

5.1 IFSI Management Structure



5.2 Carlo Gavazzi Space Management Structure

Name	Function
Angelo Longoni	Project Manager
Flavio Facchin	Project Controller
Ermanno Della Nave	PA & Safety Manager
Sergio Legramandi	PA & Safety
Luca Tunesi	System Engineer
Massimo Vitta	Hardware Engineer
Roberto Grossi	Power Engineer
Maria Lucia Tampellini	Software Design
Alberto Dell'Acqua	Manufacturing

5.3 Development and model philosophy

All the DPU/ICU electronic boards will be manufactured by CGS under a contract with ASI-IFSI and implementing the specifications for the boards design and manufacturing and for the PROM software provided by IFSI. IFSI will:

- design and manufacture the mechanical box,
- integrate the electronic boards with the box and the front wall mounted connectors,
- design and test the application software,
- perform all tests including the environmental tests.

The following units will be manufactured, tested and delivered:

AVM

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This unit is electrically, mechanically and thermally representative of the flight unit, but without redundancy. It will use standard commercial components.

EQM

This unit is electrically, mechanically and thermally representative of the flight unit, including redundancy. It will be built in accordance with the DPU/ICU product assurance plan except the EEE components quality level. The components will be as far as possible representative of the FM with respect to fit, form and function . This unit will undergo the full qualification tests.

PFM

This model is the flight unit and is built to the full extend of the DPU/ICU product assurance plan. This unit will undergo the environmental acceptance tests.

FS

These are just spare boards to be submitted to acceptance test. The FS is built to the same standard as FM. The boards will be stored in conformal coated condition.

5.4 Verification plan

The verification plan must be compliant with the project verification plans [AD5-7] and must fulfil the DPU/ICU development needs.

5.4.1 Definition

The verification is the assessment of Verification Categories to establish that the design and the implemented product are qualified. This means that each DPU/ICU realized “as built” in compliance with the Final Configuration Model baseline (“as designed”) is compliant with the Model Requirements Spacification (“as required” baseline).

The following Verification Categories are taken into consideration:

- Testing
- Analysis
- Simulation

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- Inspection
- Similarity
- Review of design.

The Verification process is extremely complex and for a number of reasons careful and balanced judgement shall be exercised:

- the categories are not independent. Inspection gives input to other categories. Testing requires analysis for its definition as well as to interpret and to extend its results.
- It is difficult to get good representative environments for testing, to define test levels and duration to verify critical features while not over-testing others.
- It is difficult to represent well the hardware in analysis and simulation.
- Analysis and testing should be well balanced both within and between different levels in the Product Tree.
- Careful trade-off should always be made to economize as much as possible on hardware and on exposure, should the hardware be re-used.

Verification is a co-operative task of the whole System Engineering teams.

The Verification Campaign shall be initiated at the beginning of the Development Program, prior to producing and testing hardware, the term Design Justification may be used and relevant documentation may be used as Qualification/Verification evidence in the final campaign.

5.4.2 Formal aspects

A Design Verification Matrix shall be established in which for each item in the Subsystem Specification Document it is indicated which of the above Verification Categories are applicable.

The Verification process shall be under Configuration Control from the early stages of the development program.

A Verification Control Matrix shall be used to maintain traceability between the documented Verification Status evidence and the Subsystem Specification Document.

5.4.3 Mechanical Verification

For testing the reference is to the relevant sections of IID-A. Vibration tests will be carried out at TBD facilities.

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5.4.4 Thermal Verification

For testing the reference is to the relevant sections of IID-A. Thermal vacuum tests will be carried out at TBD facilities.

5.4.5 Electrical and Software Verification

For hardware testing the reference is to the relevant sections of AD1-AD4, AD8-AD11, AD15-AD17, AD20 and AD21

A Functional Test Sequence will verify that all functions are tested before the delivery first to Consortia and then to ESA. A reduced functional test, testing key functions, will be defined for the Integrated System Tests. A quick version of this test, the Short Integrated System Test, will be developed to check the instruments health. A Short Functional Test based on HK parameters only will be defined in compliance with AD1.

Software Verification will comply with AD1 , AD12, AD13, AD14, AD19, AD20 and AD21.

5.4.6 EMC Verification

For testing the reference is to the relevant sections of IID-A. EMC tests will be carried out at TBD facilities.

5.4.7 Radiation Environment Verification

No specific radiation tests will be carried out as all components will be selected to be able to withstand the radiation environment.

In the following table the test matrix is presented:

	AVM	EQM	FM	FS
Functional Test	X	X	X	X (note2)
Performance Test	X	X	X	X (note2)
Interface Drawing Verification	X *	X	X	NA
Electrical Interface Tests	X	X	X	X
Vibrations Tests	NA	Q	A	A
Thermal-.Vacuum Test	NA	Q	A	A
Radiation tolerance	NA	NA	note 1	note 1
EMI / EMC	NA (note 4)	Q (note 3)	Partly (TBD)	NA
ESD	NA	X	NA	NA

(* NA but implemented also for AVM).

Items that will be in the Interface Drawing:

- Box dimensions and envelope.
- Mass; Moment of Inertia; Centre of Gravity
- Feet and connectors positions..
- Flatness of the mounting surface.
- Box and connectors identification.
- Connectors definitions.
- Box surface treatment including α and ϵ values (*NA for AVM).

Note 1: Radiation is included in EEE component selection and S/C sector analysis.

Note 2: Tests on PCB level only.

Note 3: Meaningful EMI/EMC tests should be carried out with subsystems or subsystems simulators.

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Note 4: on the AVM conducted emission and susceptibility tests (TBC) will be carried out.

X= a test is carried out.

Q= Qualification levels and duration.

A= Acceptance levels and duration.

5.5 Ground associated equipment

The ground equipment are used to develop and test one item without the presence of the others. Only the equipment needed for DPU/ICU development are listed.

The simulators replace one or more items connected to the DPU/ICU.

The tools are used to operate, check or integrate an item.

Most simulators are PC based as it is the most flexible and economic solution.

The simulators indicated in the following table are meant to be used at DPU/ICU test level, but they will also be used at the instrument integration site for integrity check after transport.

The IFSI subsystems simulators will be as simple as possible and will include only the HIFI, SPIRE and PACS subsystems simulators to test electrical interfaces and basic software interfaces.

No CDMS interface simulator will be built as this will be provided by the Consortia prior to the delivery of the boards from CGS to IFSI. The Consortia provided CDMS simulator will be used for electrical interface tests and basic exchange of information between DPU/ICU and the CDMS through the STD MIL 1553B hardware and software protocol.

5.5.1 Electrical tools

For the electrical tests laboratory instruments will be used like multimetres, oscilloscopes, logic state analysers, etc. The EMC/EMI tests on power supply lines will be carried out both at IFSI and at TBD facility.

5.5.2 Software tools

For the software development and testing the following tools will be used:

- Axiomsys CASE tool
- ADSP C runtime library
- Virtuoso OS

- ADSP compatible development board (SIGMA 2000 PC board supporting the Virtuoso O.S.)
- C language development environment
- Configuration management tool
- 21020 In Circuit Emulator.

5.5.3 Subsystems Simulators

Simulator	Used for...	Functions	Provided by
DRCU Simulator	..simulating the MCE, SCE and DCE S/S of SPIRE.	Replaces DRCU Receives commands and sends science and HK data	SPIRE project
MEC/DEC and SPU Simulators	..simulating the PACS S/S behaviour.	Replaces PACS MEC/DEC and SPU. Receives commands and sends HK data	PACS project (only S/W)
HIFI S/S Simulators	..simulating the HIFI S/S interfaces. During the instrument level testing, HIFI S/S simulators will be provided (or the actual S/S).	Replaces HIFI S/S interfaces at ICU level tests.	IFSI project

5.5.4 S/C Tools

Tool	Used for ...	Functions	Provided by
CDMS I/F (Part of EGSE)	... DPU/ICU SW testing	Simulates the S/C HW and SW I/F both at DPU/ICU level test and at instrument integration test.	PACS-HIFI-SPIRE projects
EGSE	DPU/ICU full S/W testing	Implements all functions needed to command the instruments and to interpret the telemetry data	PACS-HIFI-SPIRE projects

5.5.5 Transport container

All models will be transported by an IFSI representative in an aluminum box with suitable shock adsorbing material. The QM and FM will be in a sealed plastic conductive bag with silica-gel. The FM will be bolt on an aluminum plate and inside a protective box, with holes to access the connectors savers.

6 SW Work description

In the following table the schedule of all the activities foreseen for the software development is reported.

WP	Description
1	OBS
1.1	Spacecraft I/F
1.2	Subsystem I/F
1.3	OBS Controller
1.4	Data Packetiser
1.5	Health autonomy modules
1.6	AVM issue
1.7	PFM issue
1.8	Documentation
1.9	Support Activities
1.9.1	Virtuoso OS
1.9.2	Test modules

There is one main WP (OBS), shortly described in the following. All the other work packages shall be considered as a breakdown of all the activities related to it. They are described in detail in AD22.

6.1 On Board Software (OBS)

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6.1.1 Objectives

To provide the computer board the functionality to manage each instrument.

6.1.2 WP description

Development of the DPU/ICU OBS.

- Design activities: user requirements definition, logical model design, software requirements definition, architectural design. (WP 1.3, 1.8)
- Coding activities: detailed design and code development. (WP 1.3, 1.5, 1.8)

Testing activities: unit tests, integration tests, acceptance tests. Subsystems' interfaces simulators development. SVVP definition. Test reports generation.

7 Development calendar

In the following tables the DPU/ICU milestones are shown both for hardware and software:

7.1 HW calendar

Description	PACS	HIFI	SPIRE
DPU/ICU PDR	01/03/2001	22/02/2001	26/06/2000
AVM boards to IFSI (from CGSpace)	02/07/01	30/07/01	01/10/01
EGSE delivery to IFSI (1 unit, 3 SW)	28/06/01	28/06/01	28/06/01
PACS S/S simulators	Jun 01	-	-
HIFI S/S simulators	-	Jun 01	-
SPIRE DRCU simulator	-	-	Jun 01
AVM delivery to consortium	24/12/01	11/01/02	02/04/02
EQM boards to IFSI (from CGSpace)	01/03/02	29/03/02	22/04/02
EQM environmental tests	May 02	Jun 02	Sept 02
EQM delivery to consortium	26/06/02	01/09/02	02/01/2003
DPU/ICU CDR	12/9/2002	02/05/02	2/12/2002
Burn of flight PROMs	02/06/03	30/06/03	01/09/03
FM boards to IFSI (from CGSpace)	16/06/03	14/07/03	15/09/03
FM environmental tests	Aug 03	Sep 03	Nov 03
FM delivery to consortium	23/09/03	02/01/04	01/03/04
FS boards to IFSI (from CGSpace)	10/11/03	10/11/03	10/11/03
FS environmental tests	Jan 04	Jan 04	Jan 04
FS boards ready for consortia	24/02/04	24/02/04	24/02/04

7.2 SW calendar

Description	PACS	HIFI	SPIRE
S/W Requirements Review	02/04/2001	02/04/2001	02/04/2001
S/W Architecture Design Review	02/04/2001	02/04/2001	02/04/2001
S/W Intermediate Review	03/07/01	17/7/01	03/10/01
AVM S/W TRR	17/12/01	04/01/02	26/03/02
AVM S/W Delivery Review	24/12/01	11/01/02	02/04/02
S/W 2 nd Review	10/04/02	24/04/02	11/07/02
PFM S/W TRR	16/09/03	22/12/03	23/02/04
PFM S/W Delivery Review	23/09/03	02/01/04	01/03/04
AVM S/W Documentation	at AVM issue	at AVM issue	at AVM issue
PFM S/W Documentation	at PFM issue	at PFM issue	at PFM issue

8 Description of Receivables, Deliverables and Services

8.1 Receivables

IFSI expects to receive the following items:

ITEM	FROM	DATE
CDMS (S/C Interface) simulator	PACS (note 1)	15/06/01
EGSE (with SCOS 2000)	PACS (note 1)	28/06/01
DRCU Simulator	SPIRE	28/06/01
SPU Subsystem I/F S/W Simulator	PACS SPU	15/06/01
DEC/MEC Subsystem I/F S/W Simulator	PACS DEC/MEC	15/06/01

Note 1: The same system will be used for the three instruments.

8.2 Deliverables

IFSI is expected to deliver the following items:

ITEM	PACS	HIFI	SPIRE
DPU S/W Simulator for SPU	15/06/01	-	-
DPU S/W Simulator for DEC/MEC	15/06/01	-	-
AVM	24/12/01	11/01/02	02/04/02
AVM Software	24/12/01	11/01/02	02/04/02
AVM S/W Documentation	24/12/01	11/01/02	02/04/02
EQM	26/06/02	01/09/02	01/01/03
FM	23/09/03	01/01/04	01/03/04
FM Software	23/09/03	01/01/04	01/03/04
FM S/W Documentation	23/09/03	01/01/04	01/03/04

8.3 Services

IFSI will support the other Consortia partners during hardware and software integrations to solve both hardware and software problems.



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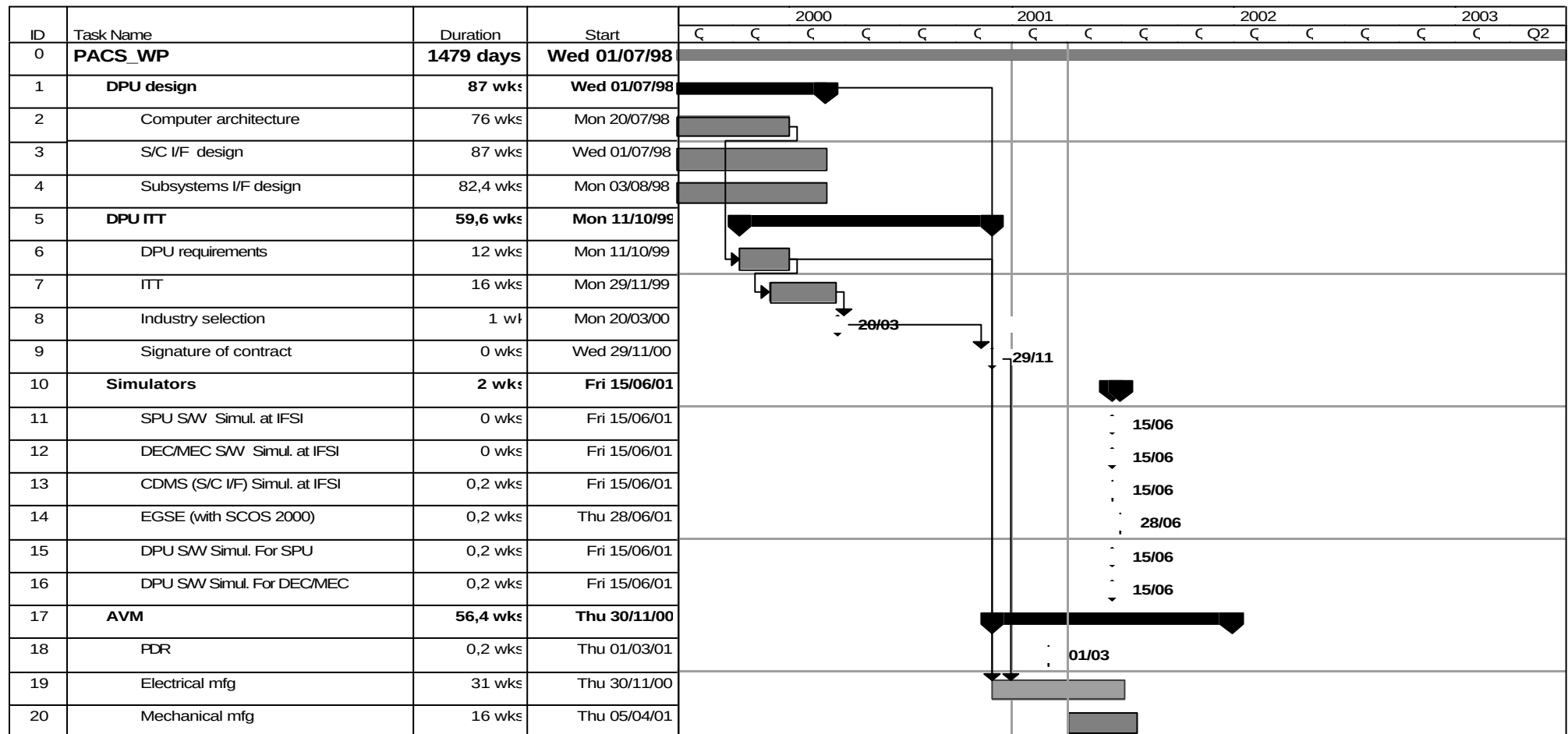
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9 Schedules

9.1 PACS





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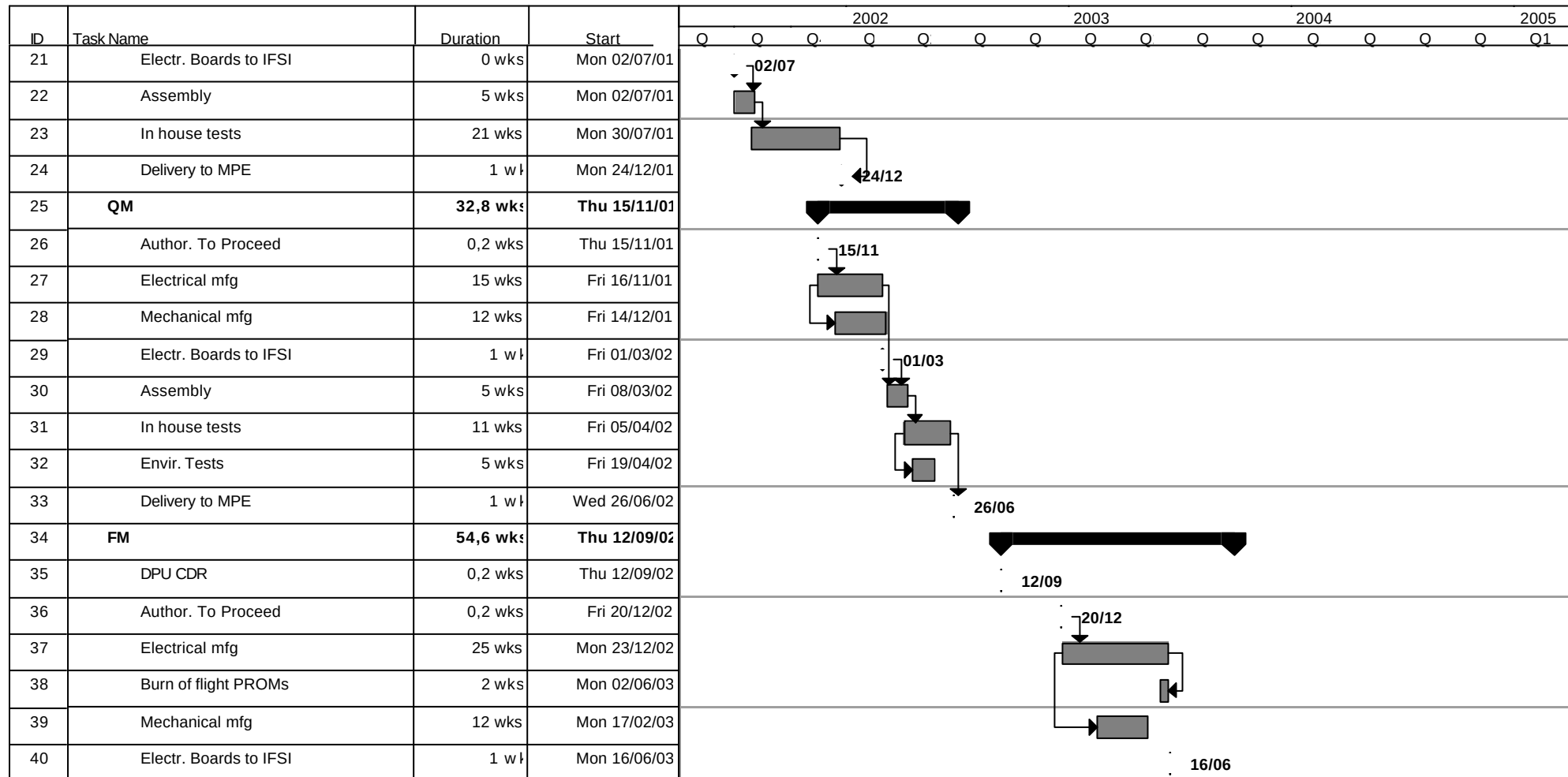
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ID	Task Name	Duration	Start	2002				2003				2004				2005
				C	C	C	C	C	C	C	C	C	C	C	C	Q1
41	Assembly	4 wks	Mon 23/06/03													
42	In house tests	10 wks	Mon 14/07/03													
43	Envir. Tests	5 wks	Mon 04/08/03													
44	Delivery to MPE	1 wks	Tue 23/09/03													
45	FS	37 wks	Tue 17/06/03													
46	Electrical mfg	21 wks	Tue 17/06/03													
47	Electr. Boards to IFSI	0,2 wks	Mon 10/11/03													
48	In house tests	16 wks	Tue 11/11/03													
49	Envir. Tests	5 wks	Tue 13/01/04													
50	Ready for Delivery	1 wks	Tue 24/02/04													



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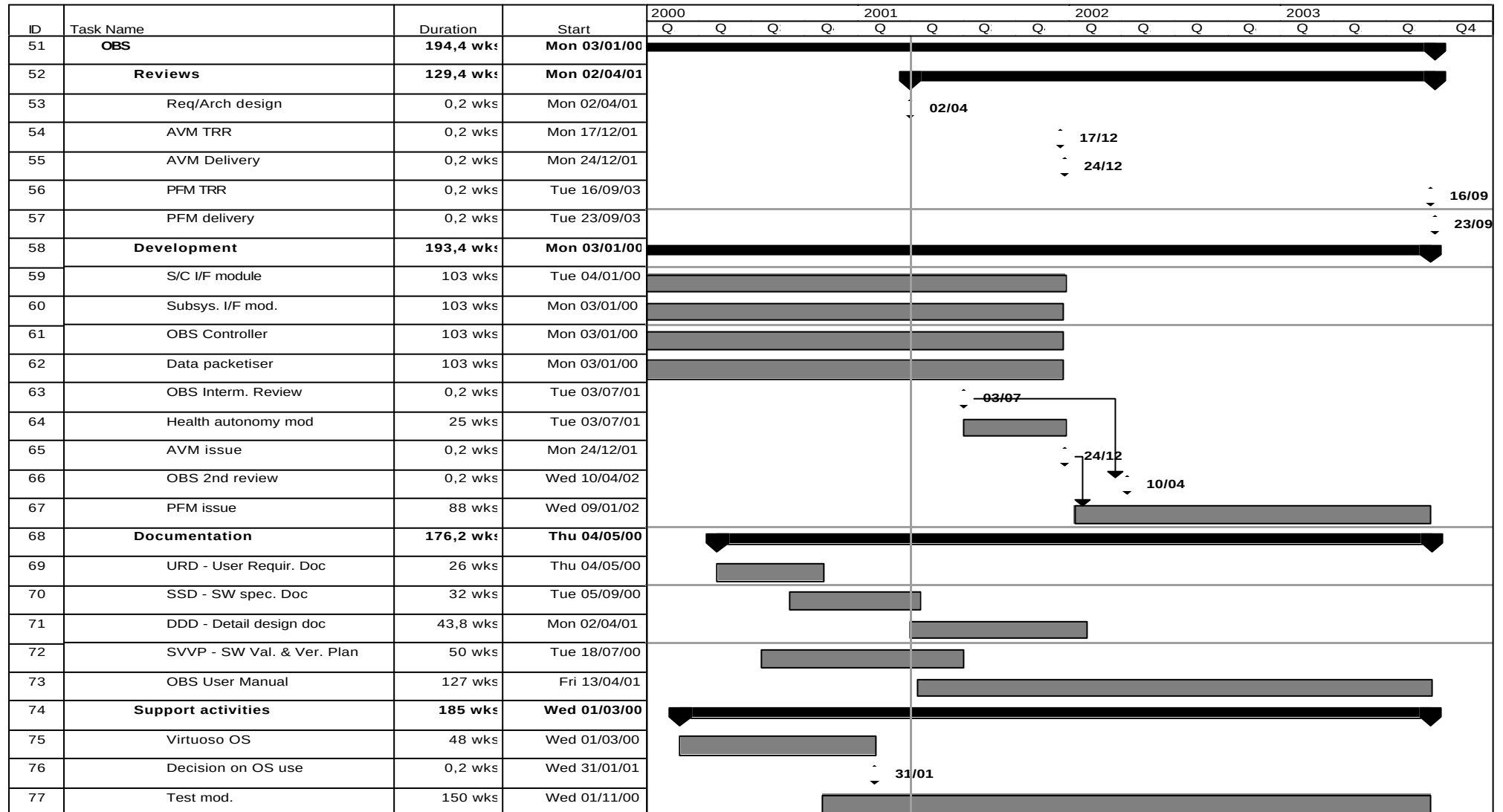
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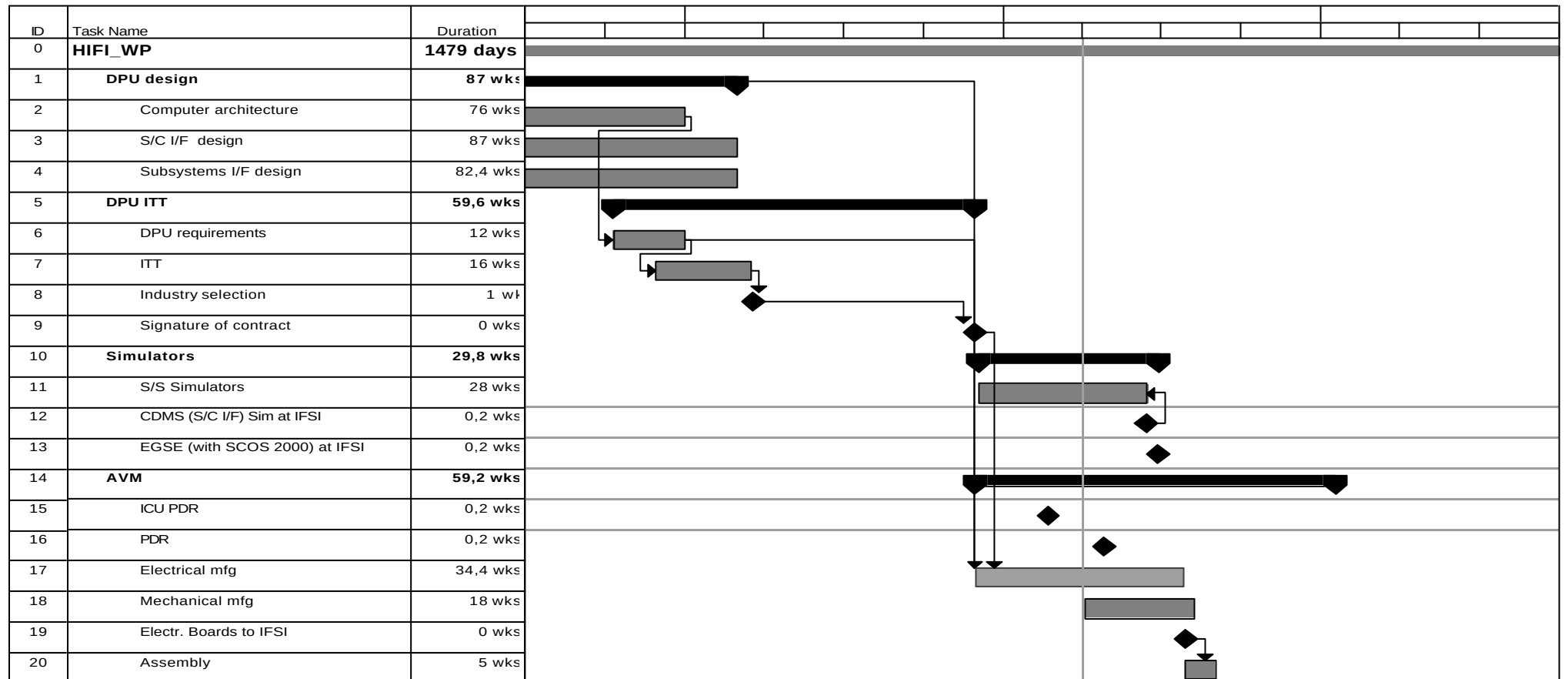
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9.2 HIFI





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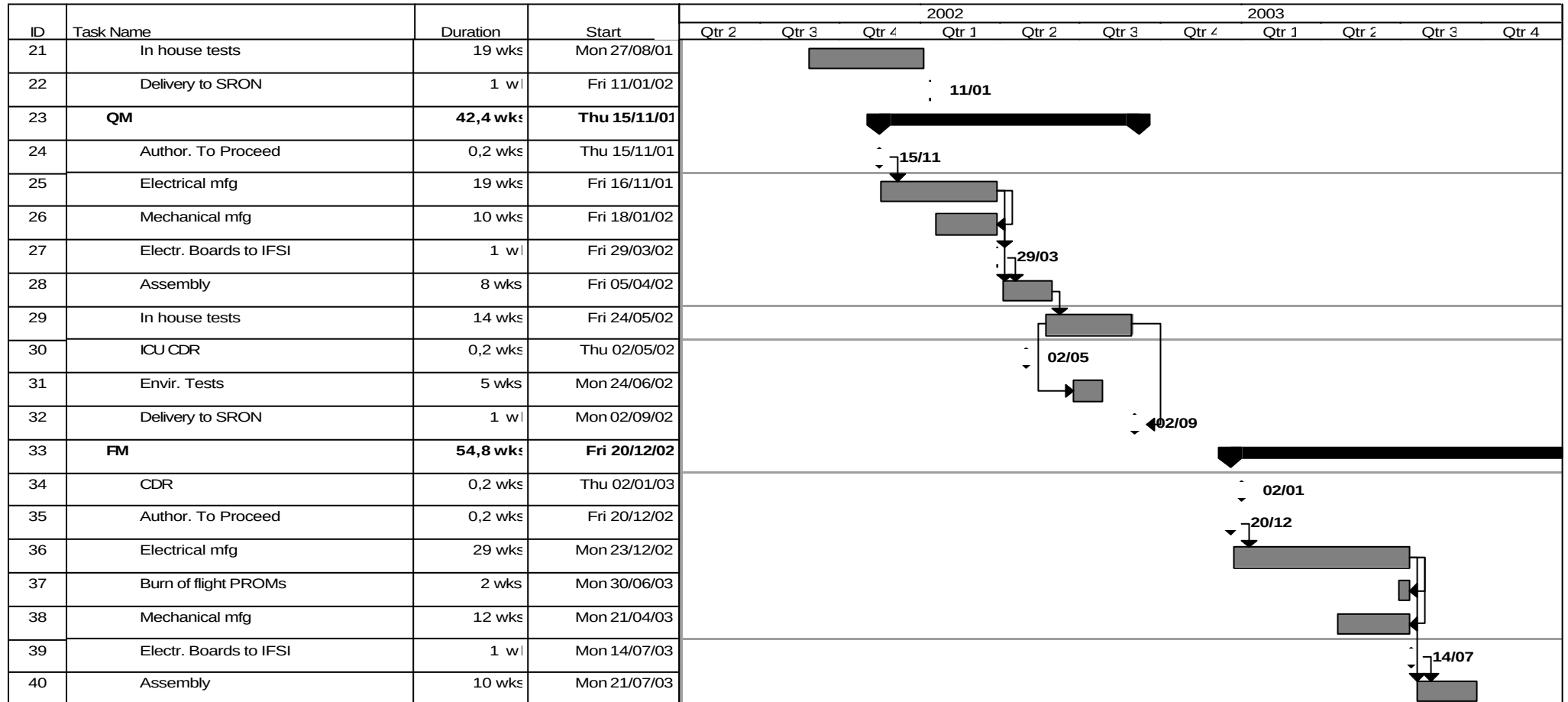
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ID	Task Name	Duration	Start	2003				2004				2005			
				Qtr 3	Qtr 4	Qtr 1	Qtr 2	Qtr 3	Qtr 4	Qtr 1	Qtr 2	Qtr 3	Qtr 4	Qtr 1	
41	In house tests	14,6 wks	Mon 22/09/03												
42	Envir. Tests	5 wks	Fri 10/10/03												
43	Delivery to SRON	1 wk	Thu 01/01/04												
44	FS	37 wks	Tue 17/06/03												
45	Electrical mfg	21 wks	Tue 17/06/03												
46	Electr. Boards to IFSI	0,2 wks	Mon 10/11/03												
47	In house tests	16 wks	Tue 11/11/03												
48	Envir. Tests	5 wks	Tue 13/01/04												
49	Ready for Delivery	1 wk	Tue 24/02/04												



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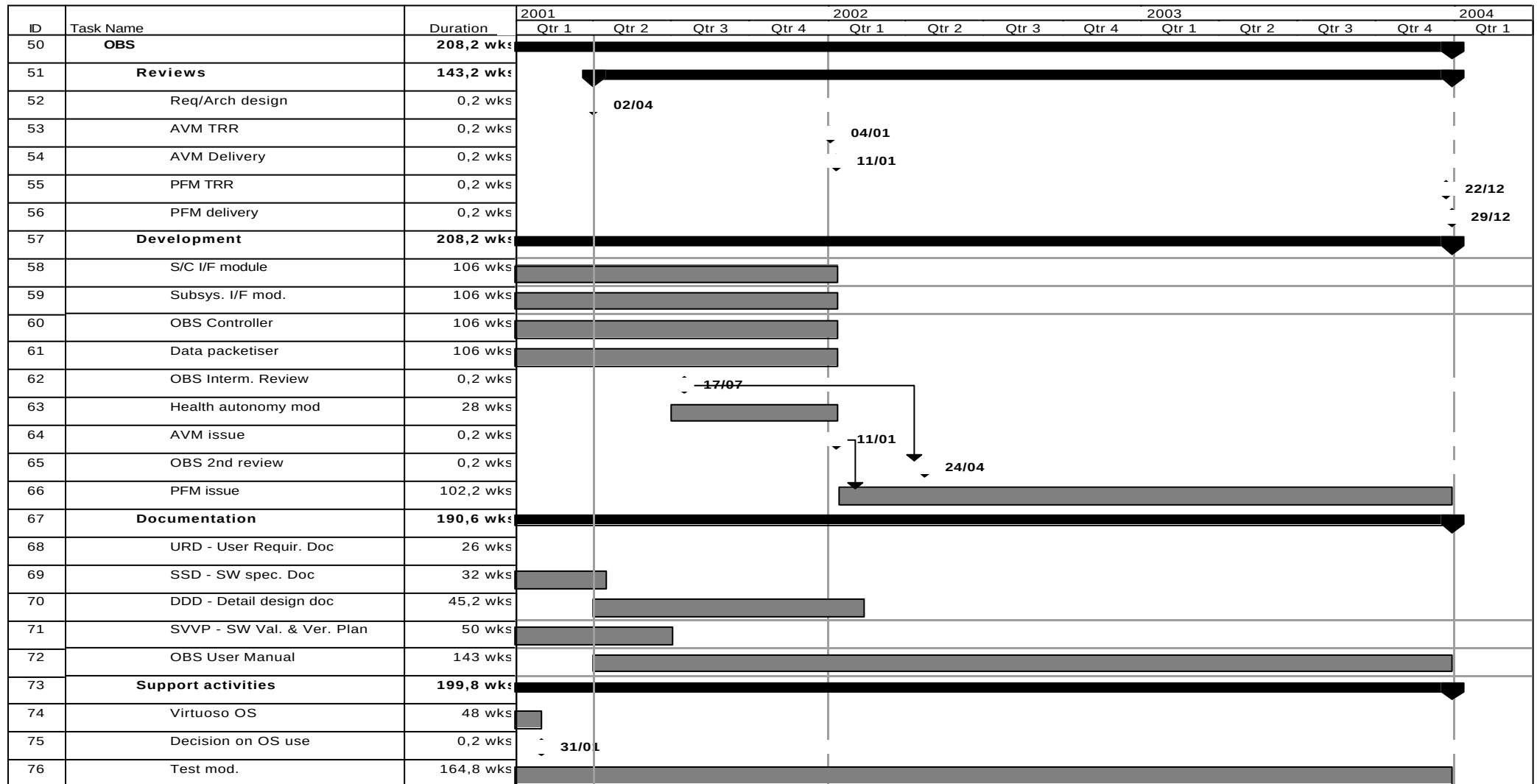
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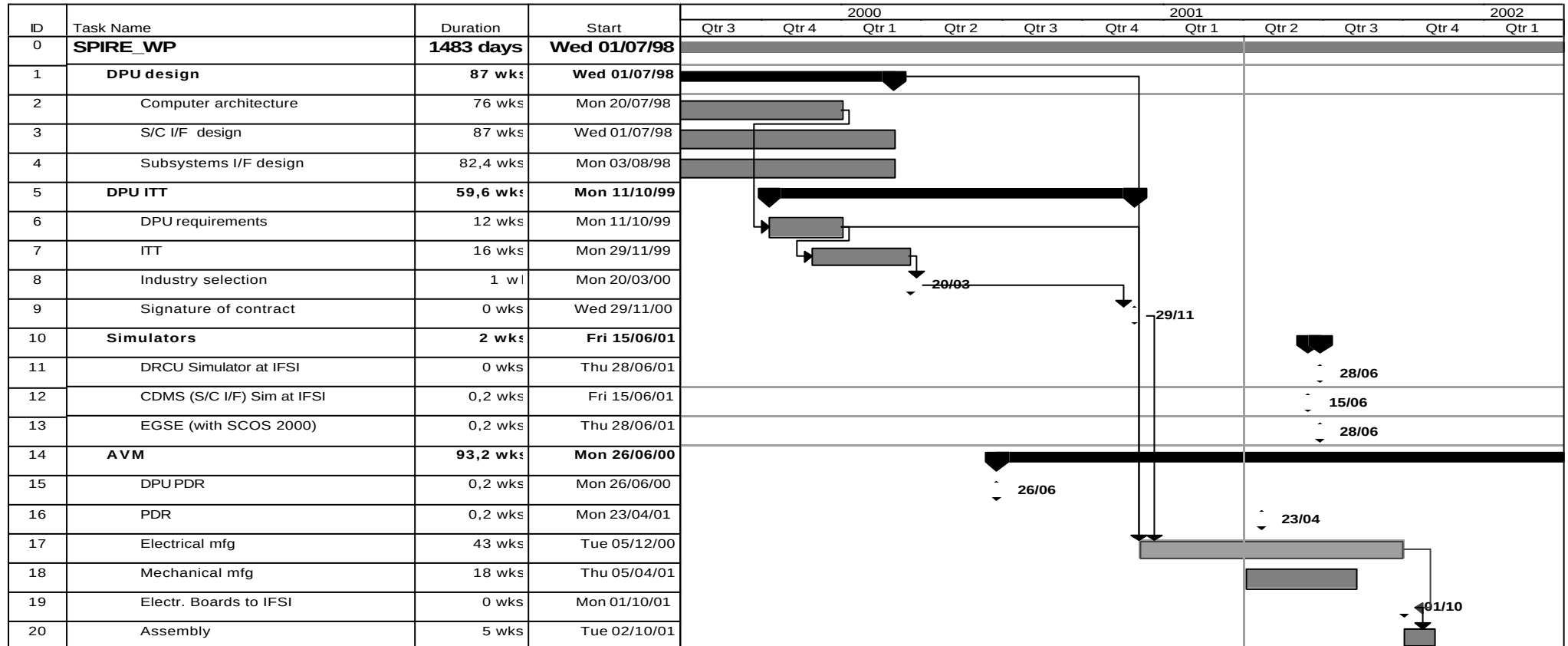
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9.3 SPIRE





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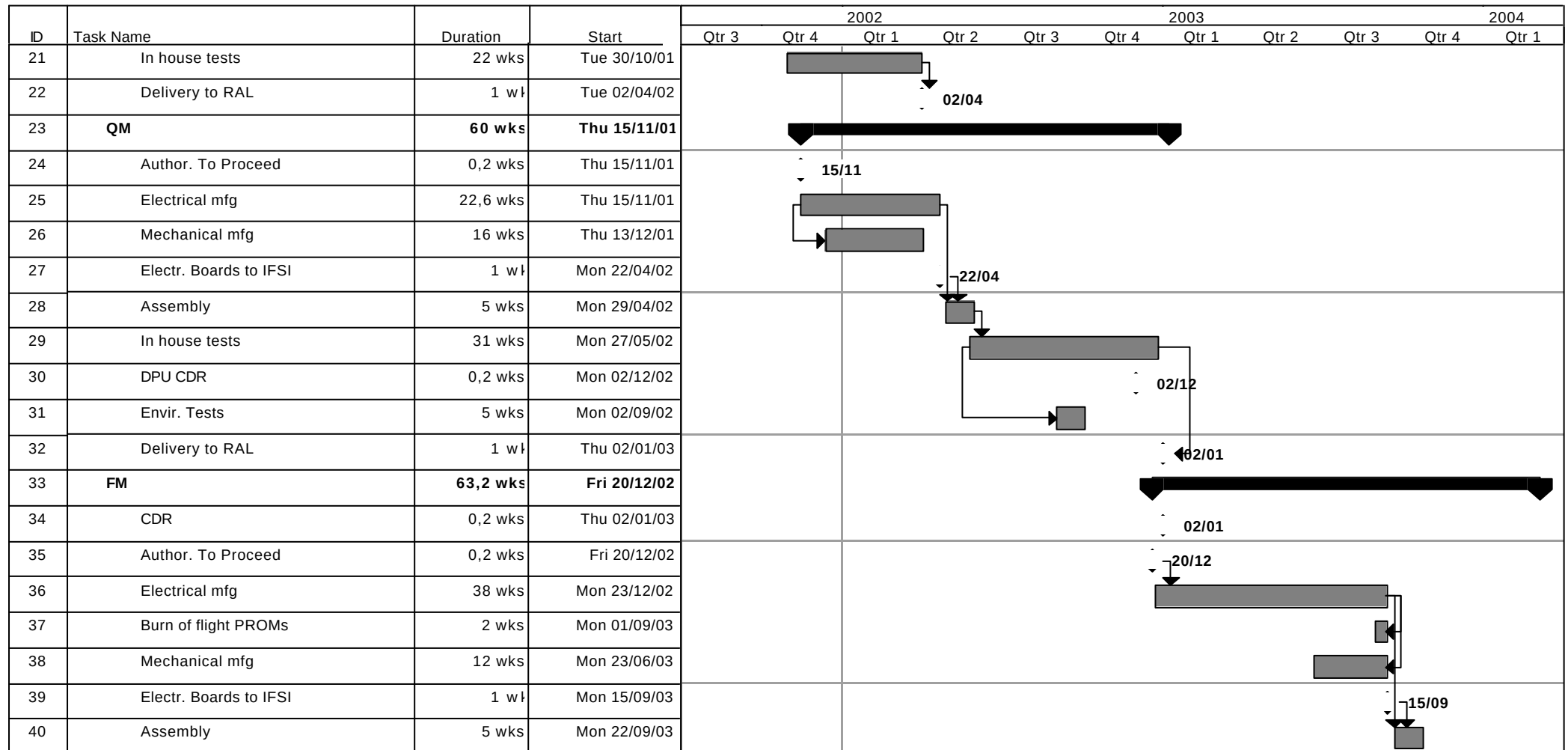
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ID	Task Name	Duration										
50	OBS	217,4 wks										
51	Reviews	152,2 wks										
52	Req/Arch design	0,2 wks										
53	AVM TRR	0,2 wks										
54	AVM Delivery	0,2 wks										
55	PFM TRR	0,2 wks										
56	PFM delivery	0,2 wks										
57	Development	217,4 wks										
58	S/C I/F module	116,8 wks										
59	Subsys. I/F mod.	117 wks										
60	OBS Controller	117 wks										
61	Data packetiser	117 wks										
62	OBS Intern. Review	0,2 wks										
63	Health autonomy mod	39 wks										
64	AVM issue	0,2 wks										
65	OBS 2nd review	0,2 wks										
66	PFM issue	100 wks										
67	Documentation	199,6 wks										
68	URD - User Requir. Doc	26 wks										
69	SSD - SW spec. Doc	32 wks										
70	DDD - Detail design doc	56,4 wks										
71	SVVP - SW Val. & Ver. Plan	50 wks										
72	OBS User Manual	152 wks										
73	Support activities	208,8 wks										
74	Virtuoso OS	48 wks										
75	Decision on OS use	0,2 wks										
76	Test mod.	172 wks										



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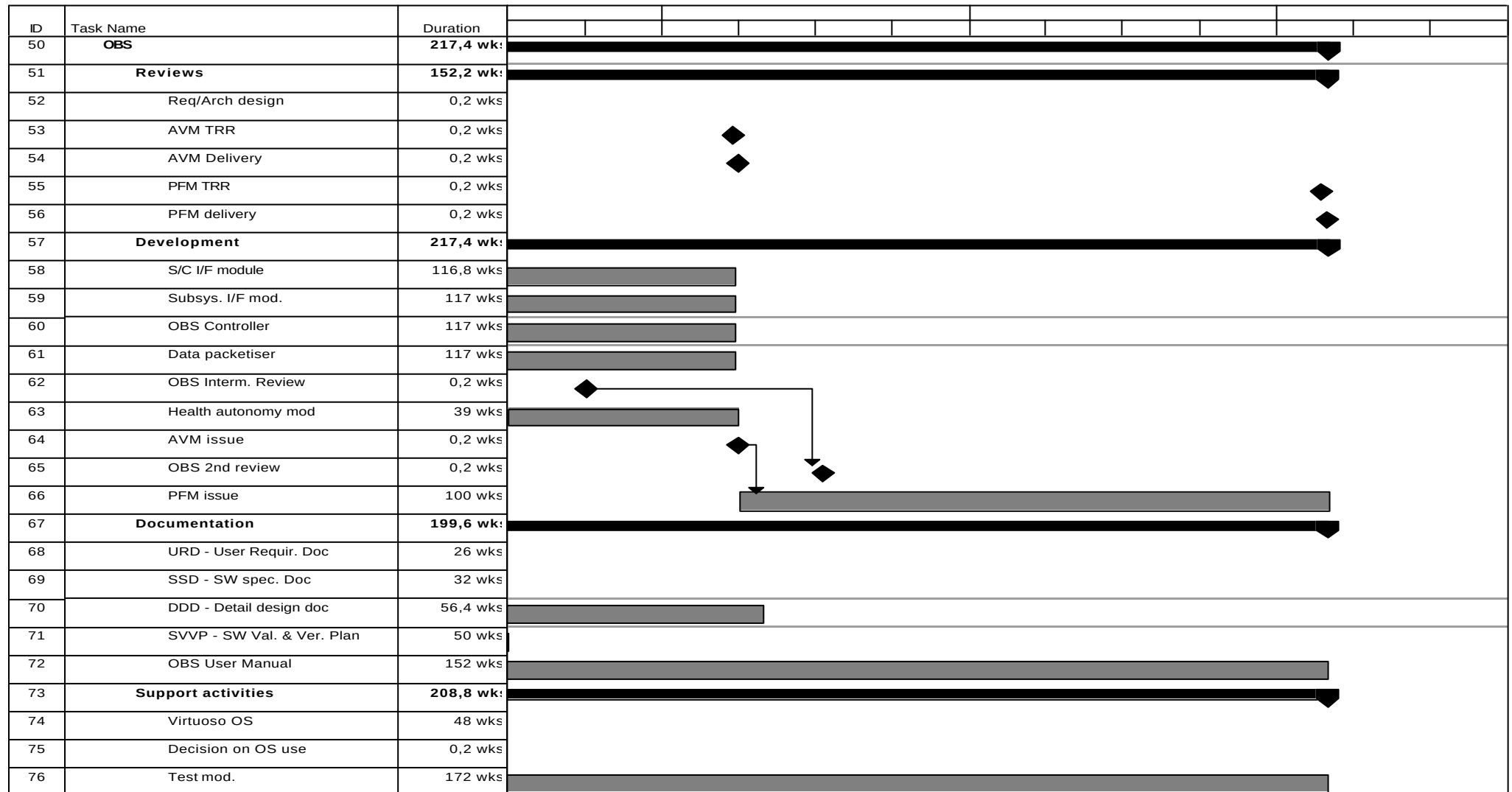
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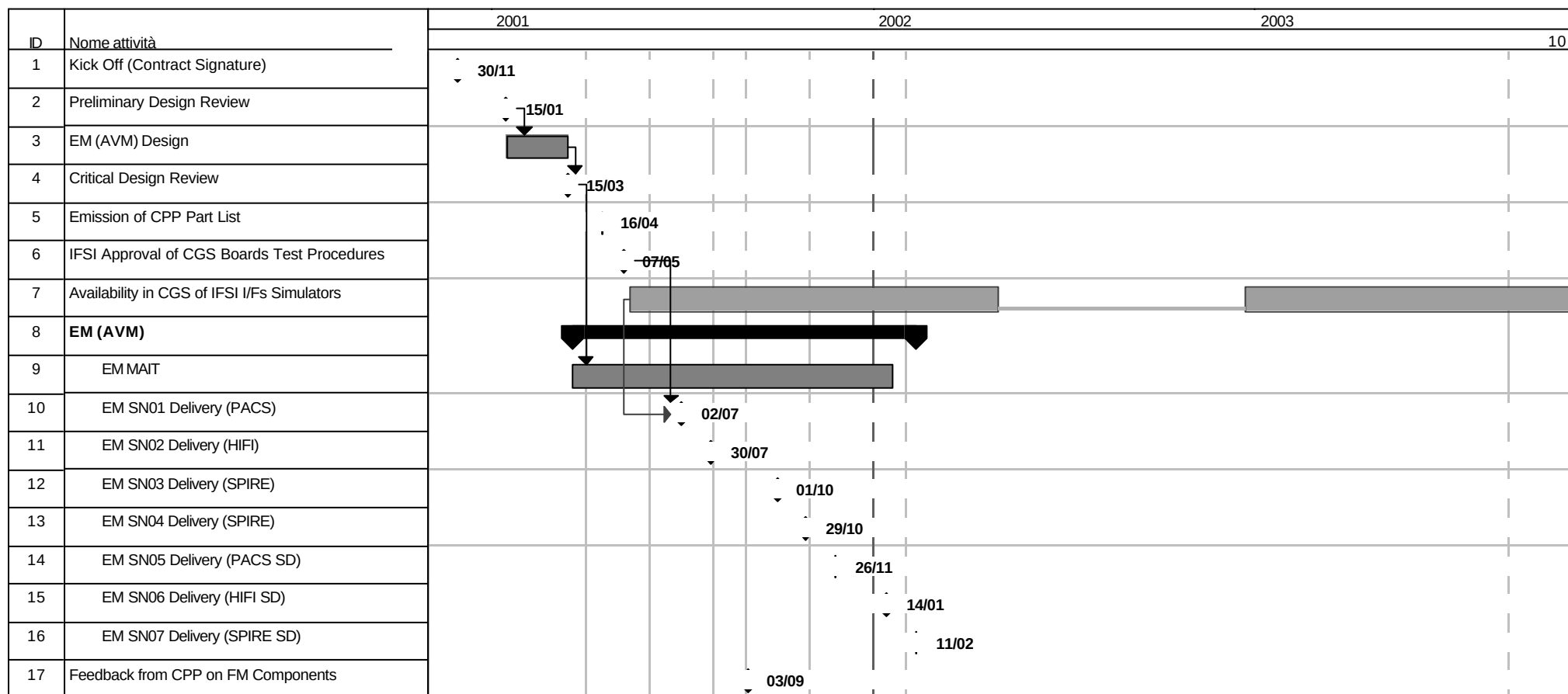
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9.4 Carlo Gavazzi Space





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