FIRST SPIRE

DPU Subsystem Specification Document

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1 Introduction

1.1 Purpose of the document

The Istituto di Fisica per lo Spazio Interplanetario (IFSI) of the Italian Consiglio Nazionale delle Ricerche (CNR) is responsible for the design and manufacturing of the three Digital Processing Units/Instrument Control Units for the three instruments to be flown on board of the ESA satellite FIRST: HIFI, PACS and SPIRE.
This specification defines the requirements applied to the performances, the design and the qualification of the SPIRE Digital Processing Unit (FSDPU subsystem). It is applicable to the AVM, the QM, the PFM and the FS.
The DPU On Board Software specification is given in the DPU/ICU OBS User Requirements Document and DPU/ICU OBS Software Specification Document.

1.2 Acronyms and Abbreviations

1.2.1 Acronyms

AD	Architectural Design
ATP	Acceptance Test Plan
AVM	Avionic Model
CNR	Consiglio Nazionale delle Ricerche
CPU	Control Processing Unit
CDMS	Computer Data Management System
CPP	Common parts Procurement
CQM	Cryogenic Qualification Model
DDD	Detailed Design Document
DPU	Digital Processing Unit
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	ElectroMagnetic Compatibility
EMI	ElectroMagnetic Interference
ESA	European Space Agency
FIRST	Far InfraRed and Submillimeter Telescope
HIFI	Heterodyne Instrument for FIRST
HK	HouseKeeping
HW	HardWare
IBDR	Instrument Baseline Design Review
ICD	Interface Control Document
ICDR	Instrument Critical Design Review
ICU	Instrument Control Unit
IHDR	Instrument Hardware Design Review
IFSI	Istituto di Fisica dello Spazio Interplanetario
ISVR	Instrument Science Verification Review
NA	Not Applicable

OBS	On-Board Software
PA	Product Assurance
PACS	Photoconductor Array Camera and Spectrometer
PROM	Programmable Read Only Memory
RAM	Random Access Memory
SCC	SpaceCraft Components
SEU	Single Event Upset
SPIRE	Spectral and Photometric Imaging REceiver
SVM	Service Module
SW	Software
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TVT	Thermal Vacuum Test

1.3 References

1.3.1 Applicable Documents

Document Reference	**Name**	**Number/version/date**
AD1	SPIRE Instrument Requirements Document	SPIRE/RAL/N/0034 Draft 0.3 May 2000
AD2	FIRST/Planck Instrument Interface Document Part A	PT-IID-A-04624 Draft 0.3 15 May 2000
AD3	FIRST/Planck Instrument Interface Document Part B Instrument "SPIRE"	PT-SPIRE-02124 Issue 0.4 15 May 2000

1.3.2 Reference Documents

Document Reference	**Name**	**Number/version**
RD1	FIRST SPIRE DPU-DRCU Interfaces	SP-RCI-18.5.00 Draft 1 18 May 2000

1.4 Overview of the document

TBW

2 Subsystem Description

The DPU of the SPIRE Instrument (FSDPU) interfaces with the Data readout and Control Unit subsystem (FSDRC) and with the S/C telemetry, telecommand (the on board CDMS, Command and Data Management system) and power systems. In Figure 2-1 the block diagram showing the interfaces of the FSDPU is presented, including the cryo-harness.

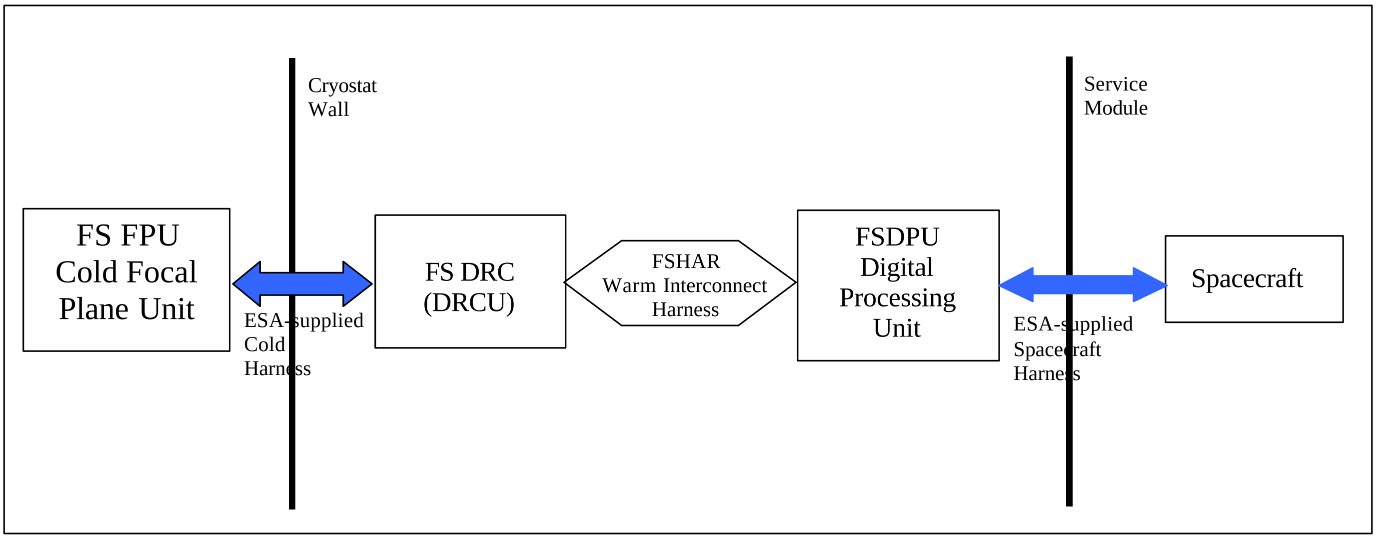

Figure 2-1 SPIRE sub-system block diagram

The interface with the FSDRC will be composed by three high speed data links (for science and housekeeping data collection) and one low speed serial bus with three output buffers (for command transmission and housekeeping data collection).
The interface with the spacecraft shall be able to handle a baseline data rate of 100 kbps, with burst mode transmission up to 300 kbps. The interface shall be compliant with the MIL-STD-1553B standard, with the FSDPU acting as a remote terminal and the CDMS as the bus controller.
In the following section a more detailed description of the DPU architecture and the proposed interfaces is given.

2.1 Design

In Figure 2-2 the SPIRE DPU high level block diagram is shown: the FSDPU box is fully hardware redundant, with one DPU ON and the other in cold redundance. Each of the two redunded computers has its own DC/DC converter, CPU, memory and interfaces both to spacecraft and to the subsystems. Only the Avionic Models (see section 2.3) will have no redundancy, neither for the DC/DC converter, nor for the on board computer.
The two main blocks of each of the two redunded DPUs are related with the CPU board and the Spacecraft and subsystems interface board.

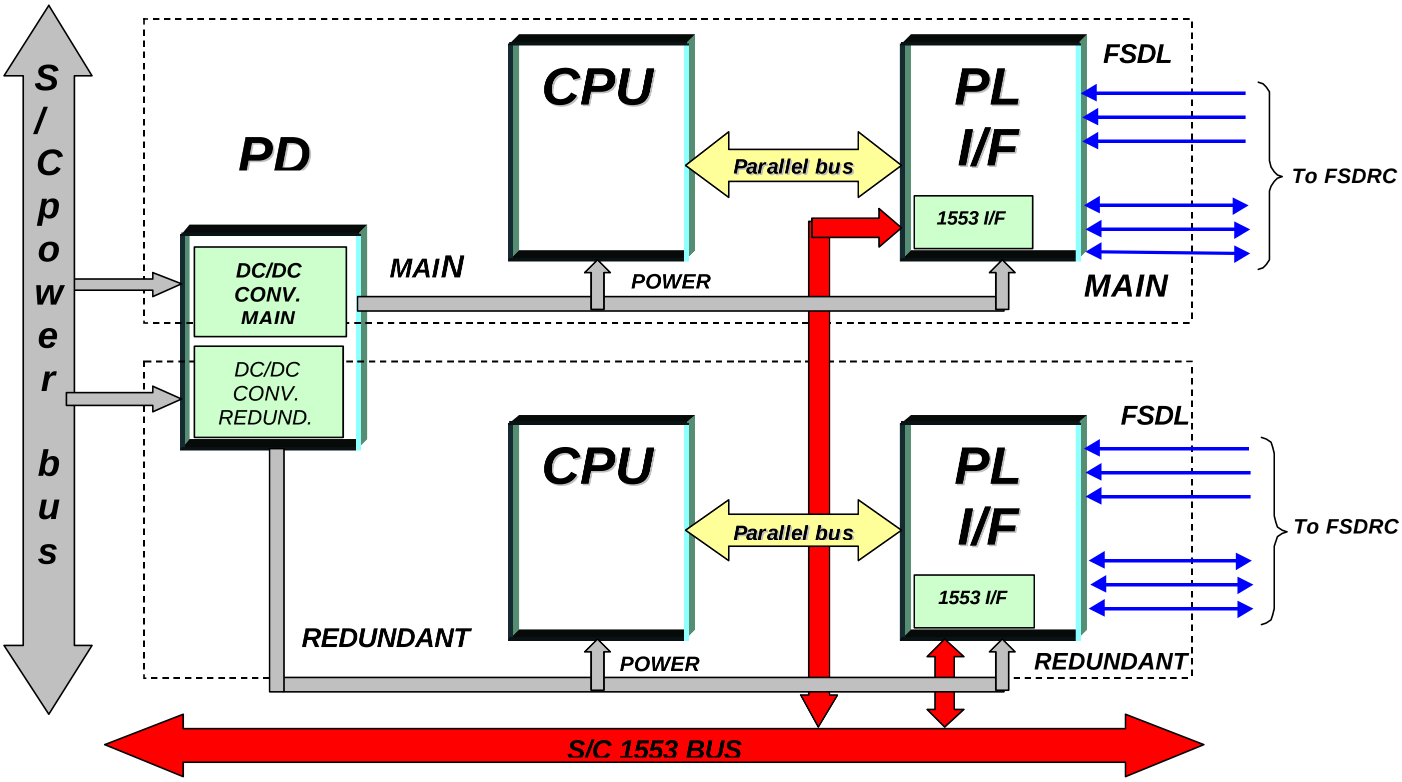

Figure 2-2 DPU high level block diagram

The FSDPU subsystem will include a synchronised DC/DC converter with a nominal input DC voltage of 28 V and the overall characteristics in agreement with AD2. In figure 2-3 a block diagram of the DC/DC converter is shown.

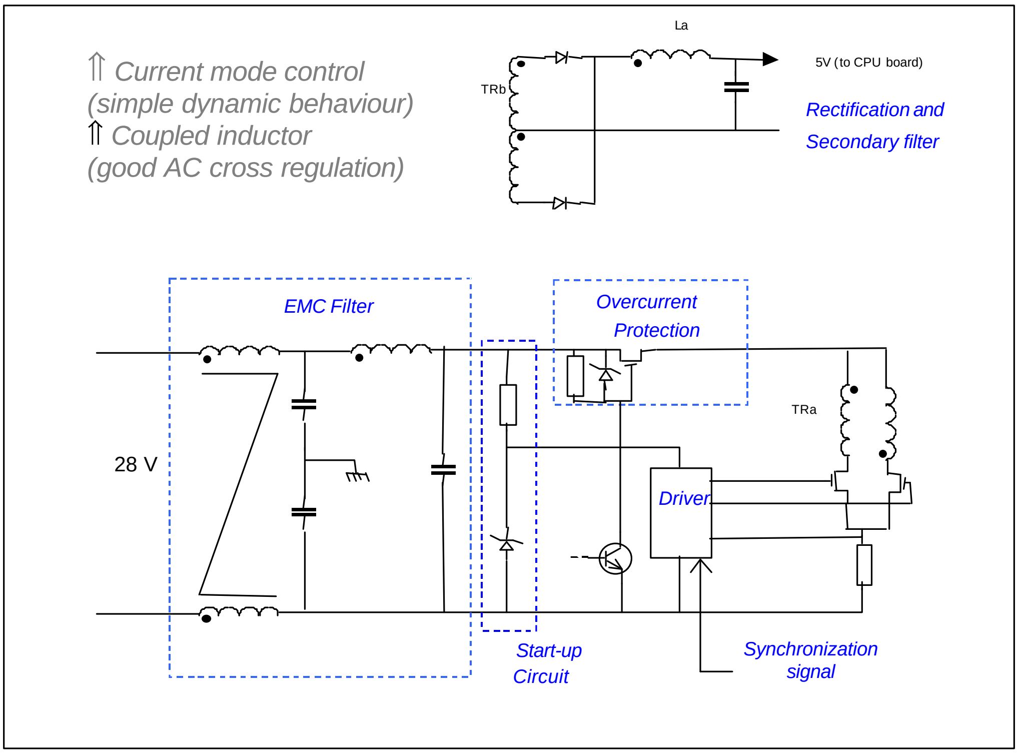

Figure 2-3 DC/DC Converter scheme.

For commonality purposes, in order to reduce the overall costs, the adopted CPU is the TEMIC TSC21020, that is a Digital Signal Processor (DSP) unit developed by Analogue Devices and implemented for flight use by TEMIC.

The CPU board will be based on this chip (20 MHz clock), with:

- an appropriate timer for time management and synchronisation purposes
- a watch-dog system (TBC)
- Rad Tolerant memories and components
- an EDAC hardware system for on line correction of single errors. If the memory SEU rate is such to guarantee no more than one bit error per year, the EDAC will not be implemented so allowing the CPU maximum speed.

In Figure 2-4 the main blocks of the CPU board are shown.

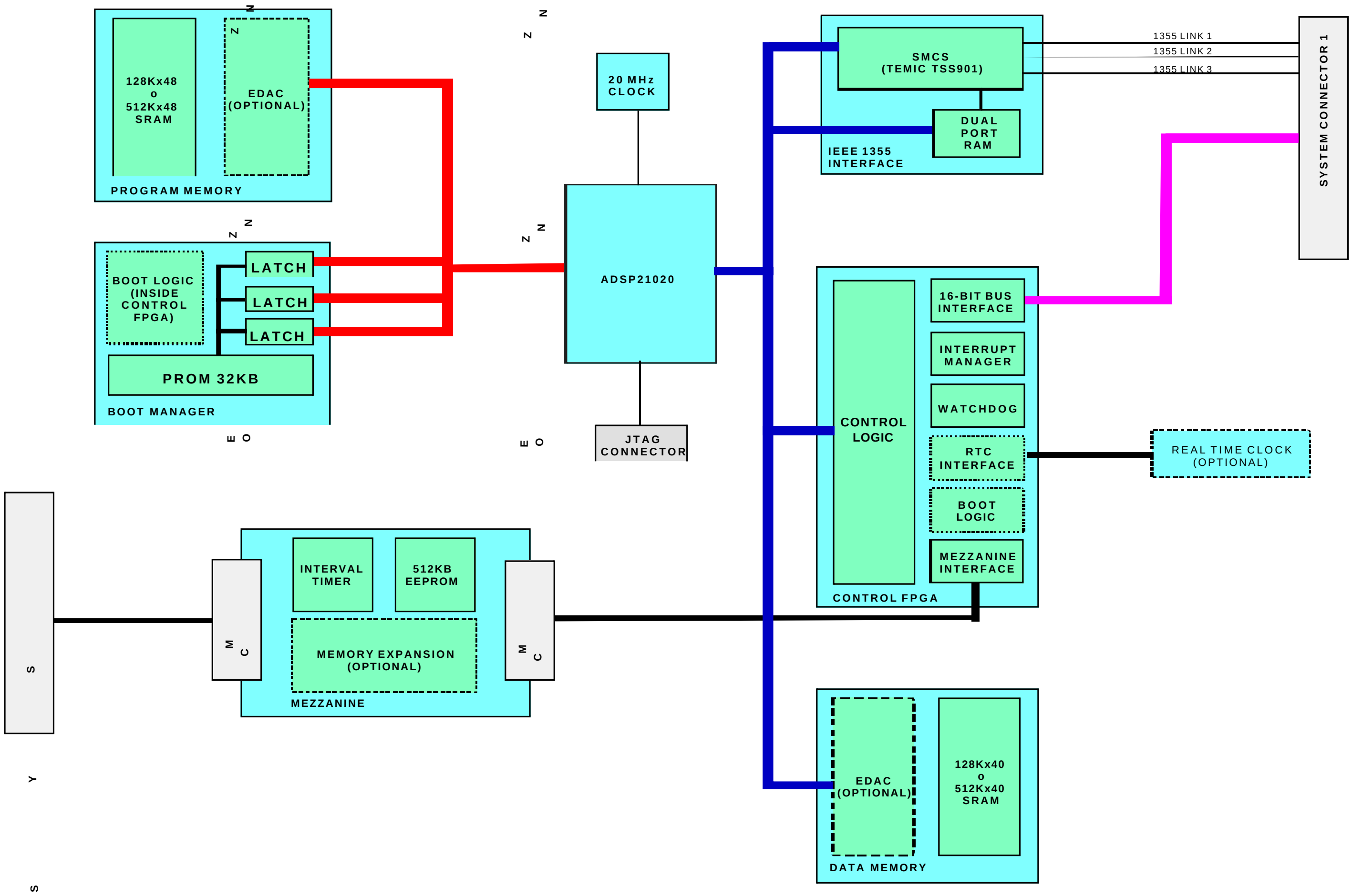

Figure 2-4 CPU board block diagram

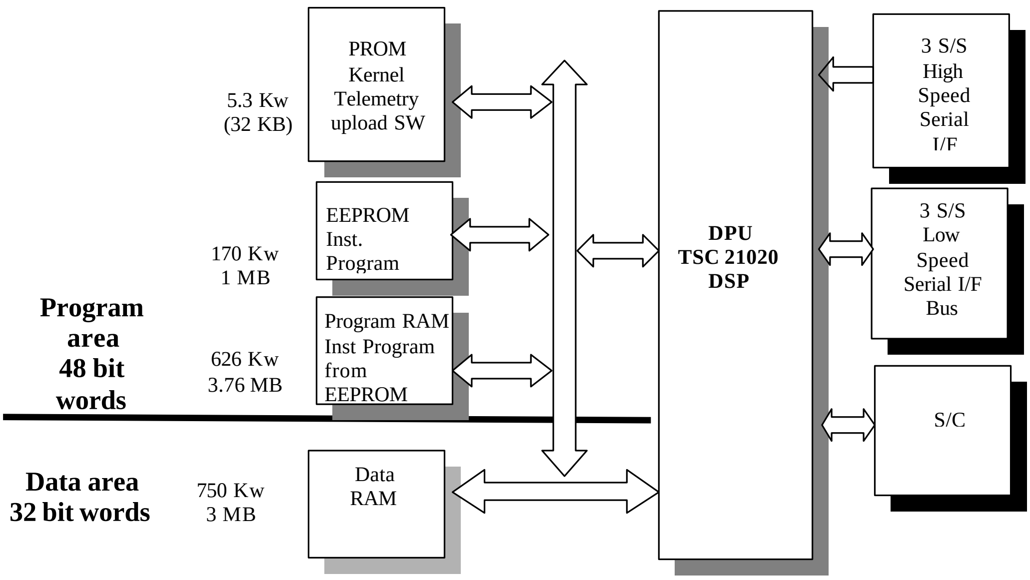

Figure 2-5 CPU memory organisation

In Figure 2.5 the memory organisation of the CPU is shown with the dimensions of the various types of memories. The CPU board will carry (on the PROMs) some basic software containing at least:

1. a driver for the interface circuit with the S/C;
2. a programme loader through the S/C telemetry;
3. a driver for writing the EEPROMs;
4. a function to carry out the EEPROM checksum test.

The DPU interfaces mechanically with the S/C and electrically with the S/C and the various subsystems. The electrical hardware interface with the S/C consists in:

- interface with the S/C Power Distribution System and the 28 V lines;
- interface with the DC/DC synchronisation signal: 131.072 kHz (AD2, section 5.9.6) implemented through a transformer;
- interface with the telemetry and telecommand subsystems.

In figure 2-6 a block diagram of the S/C interface board is shown. The MIL-STD-1553B standard is implemented through one nominal and one redundant transformer in the long stub configuration.

The interface between DPU and DRCU is shown schematically in Figure 2-7; a detailed description of this interface is given in RD1. For the science data link, **three monodirectional fast (1 MHz clock, TBC) synchronous serial input interfaces**, each of which with 8 KW 16 Bit FIFO, are foreseen: the data can be received by the DPU at the same time. The clock, gate and data signals, coming from the subsystems, are as in Figure 2-8.

A serial synchronous bus is foreseen to interface with the control electronics of the focal plane unit subsystems: the bus will be used to transmit commands and receive responses or to control and receive housekeeping information. The baseline clock speed is 0.2 MHz (TBC). In Figure 2-9 the signals are shown: CLK & TX_DAT are coming from DPU and go in parallel with three distinct hardware interfaces to the three DRCU electronics blocks; the three RX_DAT lines are coming each from each of the three blocks and are multiplexed inside the DPU (see RD1).

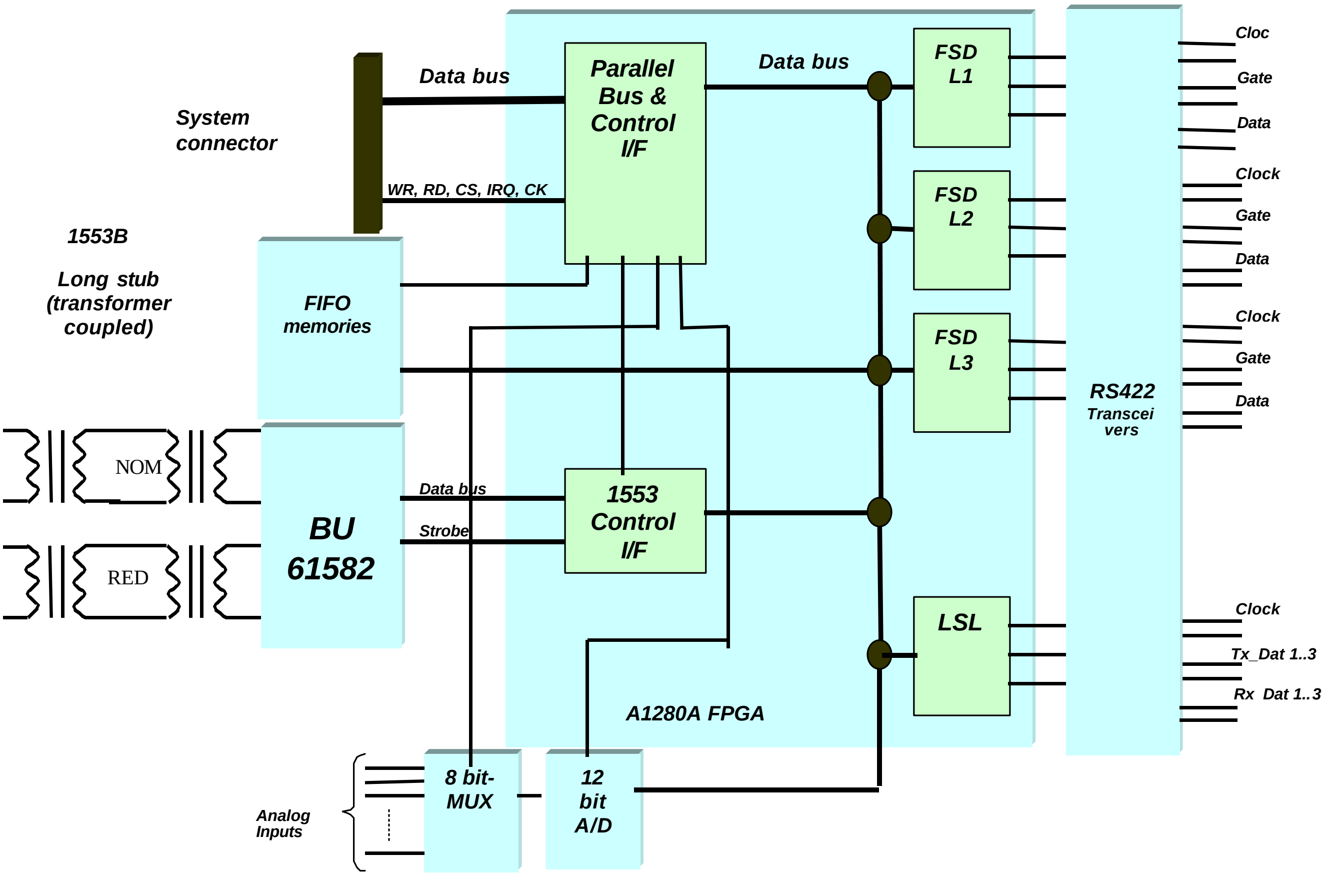

Figure 2-6 Spacecraft Interface Block Diagram

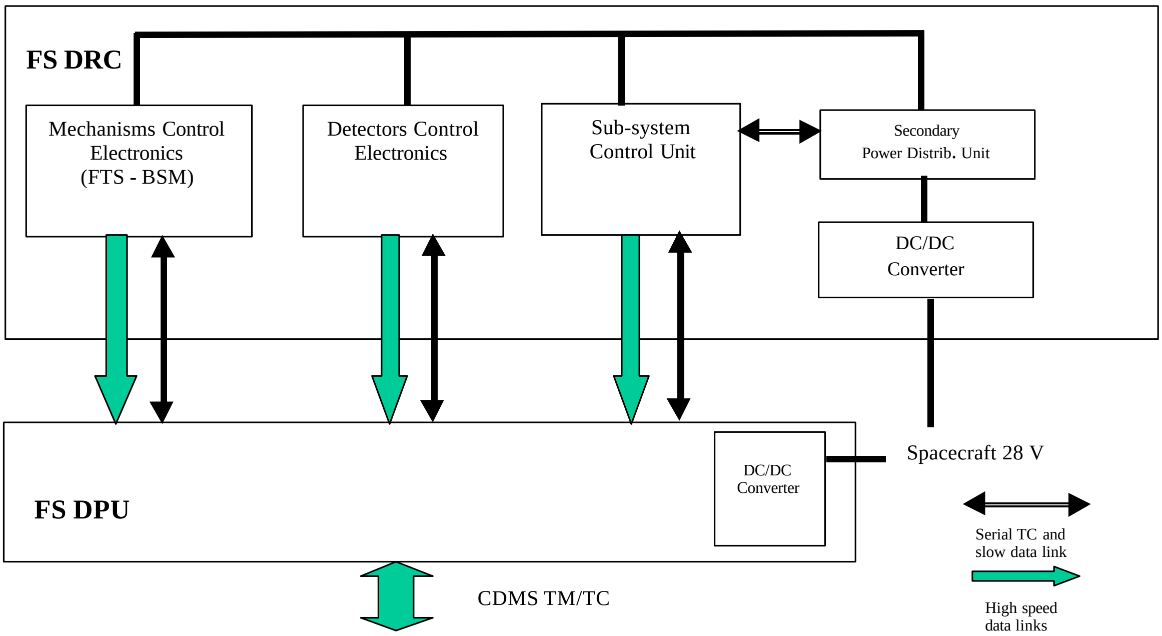

Figure 2-7 FSDPU/FSDRC Interface Block Diagram

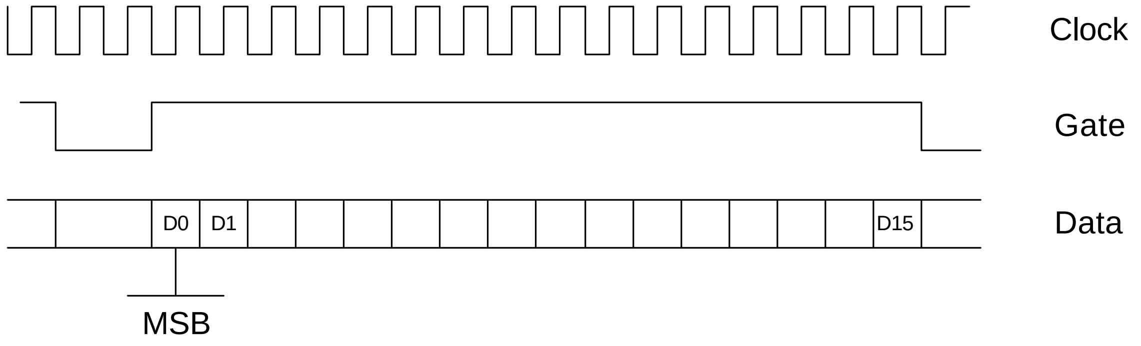

Figure 2-8 High speed interface protocol

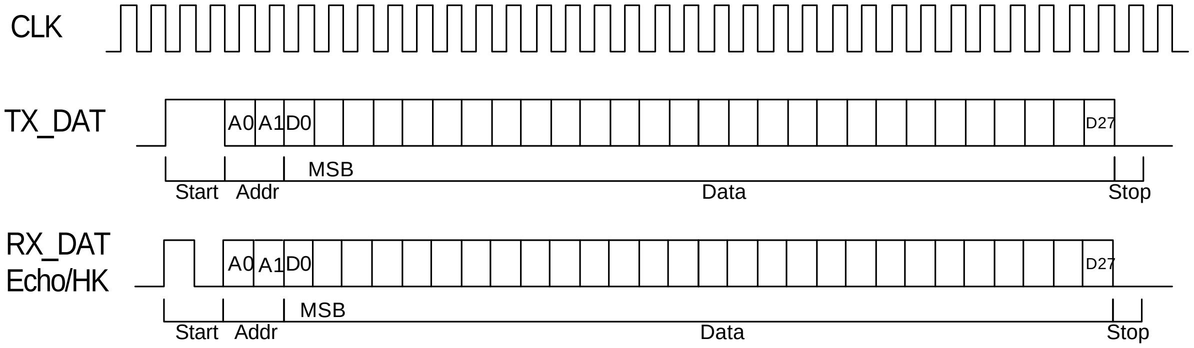

Figure 2-9 FSDPU/FSDRCU Low Speed Interface protocol

All data transactions with the addressed subsystem (addr. In TX_DAT), are initiated by DPU. DPU will send data to all subsystems using one serial data line TX_DAT and can send both commands and HK requests via this line.
Subsystems, if required, will send responses via RX_DAT line.
A **command** is made of 2 start bits, 2 address bits, 28 data bits and 1 stop bit.
A **HK request** is made by setting a dedicated field in the data bits.
A **HK response** will consist of 2 start bits, 2 address bits, 32 data bits and 1 stop bit
The sub-unit address field in the TX command is used to select the input channel RX. No command can be sent to a different sub-unit until the echo/HK RX corresponding to the last command sent is received. Figure 2-10 shows the transmission-reception sequence.

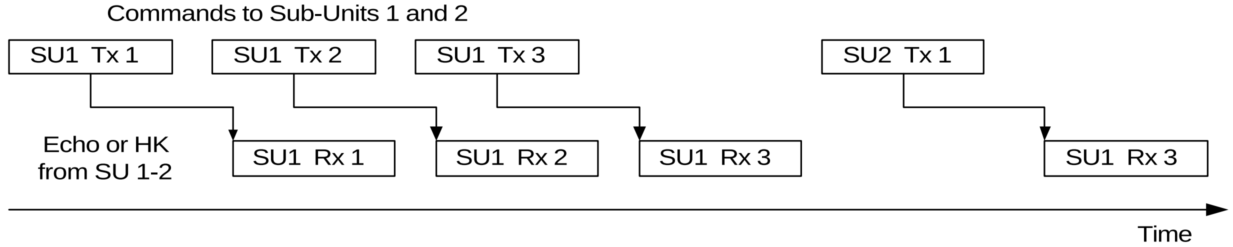

Figure 2-10 Low speed Interface – transmission reception protocol

Clock and TX_DAT are generated by DPU and distributed to all subsystems
For internal reading of analogue signals an A/D converter (12 bit) plus MPX (8 Channels) will be provided in order to digitise the information of an internally conditioned thermistor and of the DC/DC converter voltage and total current.

2.2 Mission Profile

The DPU will be designed to be used for 2 years on the ground, 2 years (TBC) of storage and 4 years in orbit with a probability better than 90% for the single ICU section (prime or redundant).

2.3 Product Tree

The following deliverables are foreseen:

1) DPU-AVM (Avionic Model): no redundancy, neither for the DC/DC converter, nor for the on board computer; only commercial grade components. These are to be used for the spire BBM (breadboard model), see section 2.4 of AD1. **It is anticipated that it will not be possible to comply with what requested in AD2, chapter-page 9-1, paragraph 9.2.2.1, i.e. the AVM components will not be purchased, in general, from the same supplier of the FM/FS parts.** The AVM will be delivered to ESA.
2) DPU-QM (Qualification Model): full redundancy, both for the DC/DC converter, and for the on board computer; only commercial grade components as far as possible within the fit, form and function of the flight model. The printed boards artwork will be the same as for FM/FS. This unit will undergo qualification tests. It is not a deliverable to ESA.
3) DPU-PFM (Proto-Flight Model): full redundant box; SCC level B components for the spacecraft interface, SCC level C for all the other components is the baseline. If it is confirmed by ESA the decision to issue a Common Parts Procurement for which ESA will pay non recurring costs and surcharge costs, then in this case all components will be at SCC level B. This unit will undergo acceptance tests.
4) DPU-FS (Flight Spare): only spare boards (CPU, S/C I/F, SubSytem I/F, DC/DC Conv., mother board): SCC level B components for the spacecraft interface, SCC/C level for all the other components is the baseline, but the same as for the PFM applies. These boards will undergo acceptance tests.

3 Requirements

3.1 Functional requirements

3.1.1 Performance Requirements

Requirement ID	Description	Reference
DPU-FUN-01	The interfaces of the DPU with the DRCU subsystem	

	shall be designed in order to couple with the maximum output data rates of the following subsystems: - FTS mechanism controller; - Beam Steering Mirror; - Photometer detector array, - Spectrometer detector array, - Sorption cooler.	
DPU-FUN-02	The DPU shall be able to acquire all Photometer detector pixels corresponding to a 4'x8' FOV (288 detectors) at a maximum readout frequency of 40 Hz per frame and 16 bits per sample.	
DPU-FUN-03	The DPU shall be able to acquire all Spectrometer detector pixels corresponding to a 2.6'x2.6' FOV (56 detectors) at a maximum readout frequency of 200 Hz per frame and 16 bits per sample.	
DPU-FUN-04	Photometer data: The instantaneous **dynamic range** of the readout of a pixel (feedhorn array) shall be 14 bits (TM), 16 (Sampling)	
DPU-FUN-05	Spectrometer data: The instantaneous **dynamic range** of the readout of a pixel shall be for the Feedhorn: 16 bits (TM) or 15 (with background nulling).	

3.1.2 Technical requirements

DPU-FUN-06	The DPU shall be able to handle the adopted standard MIL-STD-1553B for the interface with the spacecraft, supporting an average telemetry rate of 96 kbps, when the instrument is in prime mode, and of 2kbps otherwise.	AD2 sect. 5.11.4 AD3 sect. 5.11.1
DPU-FUN-07	The DPU shall be able to handle the adopted standard MIL-STD-1553B for the interface with the spacecraft, supporting a maximum telecommand rate of 4 kbps.	AD2 sect. 5.11.4 AD3 sect. 5.11.1
DPU-FUN-08	Maximum DPU power consumption: 15W	AD3 Sect. 5.9.3

3.2 Operational requirements

3.2.1 Operational Safety

Requirement ID	Description	Reference
DPU-SAF-01	Failure of the DPU, or one of its components, shall not affect the health of any other subsystem, the instrument or the interface with the satellite.	IRD-SAFE-R06
DPU- SAF-02	Failure of any component in the DPU shall not damage any redundant or backup component designed to replace that component in the subsystem	IRD-SAFE-R09

DPU- SAF-03	No ASICs or FPGAs shall be capable of affecting instrument operations until they are in a defined state.	
DPU- SAF-04	It shall be possible to break via software all electronic control loops implemented in hardware, provided that the relevant commands are implemented in the FSDRC in agreement with FSDPU.	IRD-REL-R05
DPU- SAF-05	The instrument shall monitor the operational status of the instrument on-board computer and take appropriate action in case of error. (*a watchdog function will be implemented to identify if the on board computer has crashed) TBC*	IRD-AUT-R06
DPU- SAF-06	Cold redundant hardware shall be provided	IRD-REL-R03

3.2.2 Lifetime

Requirement ID	Description	Reference
DPU-OPE-01	The DPU shall be designed to couple with an integrated lifetime of 2 years.	
DPU-OPE-02	The DPU shall be designed to couple with a ground storage lifetime of 2 years (TBC).	
DPU-OPE-03	The DPU shall be designed to couple with an in orbit lifetime of 4 years, with a probability better than 90% for the single DPU section (prime or redundant).	

3.2.3 Operating Modes

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3.2.4 Telemetry

The housekeeping parameters provided by the DPU are (list is TBC):

- DPU Voltage (2bytes)
- DPU Current (2bytes)
- DPU Temperature (2bytes)

3.2.5 Telecommands

The DPU dedicated commands are (list is TBC):

- ***DPU reset***
  Command: DPU_Reset()
  Parameters: Input --- None
  Output --- None
  Action: Set program counter to start address

Remarks: DPU reset has consequences for the other subunits so the response to this command can not be as simple as described. However, the actual actions to be taken will be discussed as part of autonomous functions. Moreover, while the command itself has no return value since the DPU is reset, it is clear that a return value is expected (checksum of memory for instance).

- ***Measurement Reset***
  Command: Msrment_Reset(Restart)
  Parameters: Input --- 1 Byte
  Output --- None
  Action: Restart = 0 --- Stop the measurement
  Restart = 1 --- Stop the measurement and start again the observation

- ***CMD Queue Reset***
  Command: CMD_Queue_Reset()
  Parameters: Input --- None
  Output --- None
  Action: The command queue is reset and the instrument remains waiting for new commands.
  Remarks: It has to be decided if the instruments remains in observing mode or switches to standby mode

- ***Memory Dump***
  Command: Result=Mem_Dmp(Start,Length,Return)
  Parameters: Input --- Start 4 Bytes
  Length 2 Bytes
  Output --- Return 4 Bytes
  Result 1 Byte
  Action: The memory is dumped from the location (Start) to the location (Start+Length-1). The content is then packetized and sent to CDMS.
  Remarks: Result can assume the following values:
  0 : The command has been executed properly (Return has no meaning)
  1 : HW failure (it has not been possible to read memory at the address reported in Return)
  Depending on the address, the command dumps the ROM, the EEPROM or the RAM.

- ***RAM Uplink***
  Command: Result=RAM_Uplink(Start,Length,Data,Return)
  Parameters: Input --- Start 4 Bytes
  Length 2 Bytes
  Data 4 Bytes
  Output --- Return 4 Bytes
  Result 1 Byte
  Action: The content at address Start is substituted for by the content at address Data. The pointers Start and Data are incremented by one and the operation is repeated until Length bytes have been transferred.
  Remarks: Result can assume the following values:
  0 : The command has been executed properly (Return has no meaning)
  1 : HW failure (it has not been possible to read memory at the address reported in Return)

2 : HW failure (it has not been possible to write memory at the address reported in Return)

- ***EEPROM Write***
  Command: Result=EE_Wrt(Start,Length,Data,Return)
  Parameters: Input --- Start 4 Bytes
  Length 2 Bytes
  Data 4 Bytes
  Output --- Return 4 Bytes
  Result 1 Byte
  Action: The content at addres Start is substituted for by the content at address Data. The pointers Start and Data are incremented by one and the operation is repeated until Length bytes have been written.
  Remarks: Result can assume the following values:
  0 : The command has been executed properly (Return has no meaning)
  1 : HW failure (it has not been possible to read memory at the address reported in Return)
  2 : HW failure (it has not been possible to write memory at the address reported in Return)

- ***Subsystem Parameter Table Reset***
  Command: Result=Par_Table_Reset(Return)
  Parameters: Input --- None
  Output --- Return 4 Bytes
  Result 1 Byte
  Action: The parameters table is reset to the values stored in ROM (or EEPROM). It could be needed to reset only a portion of the table, in this case the function will require two additional inputs: start and length of the (sub)table to reset.
  Remarks: Result can assume the following values:
  0 : The command has been executed properly (Return has no meaning)
  1 : HW failure (it has not been possible to read memory at the address in Return)
  2 : HW failure (it has not been possible to write memory at the address reported in Return)

- ***Subsystem Parameter Table Update***
  Command: Result=Par_Table_UpDate(Start,Length,Data,Return)
  Parameters: Input --- Start 4 Bytes
  Length 2 Bytes
  Data 4 Bytes
  Output --- Return 4 Bytes
  Result 1 Byte
  Action: The content at addres Start is substituted for by the content at address Data. The pointers Start and Data are incremented by one an the operation is repeated until Length bytes have been transferred.
  Remarks: Result can assume the following values:
  0: The command has been executed properly (Return has no meaning)
  1 : HW failure (it has not been possible to read memory at the address reported in Return)
  2 : HW failure (it has not been possible to write memory at the address in Return)

- ***Read DPU HK parameters***
  Command: Result=Get_HK(Return)
  Parameters: Input --- None

Output --- Return 6 Bytes
Result 1 Byte

Action: The DPU HK parameters are sampled.
Remarks: Result can assume the following values:
0 : The command has been executed properly and Return contains the HK.
1 : Error in reading DPU voltage
2 : Error in reading DPU current
4 : Error in reading DPU temperature
Result can take on any combination of these values.

3.3 Interface Requirements

The required operating temperatures at the interface of the SVM with FSDPU shall be compliant with AD3, section 5.7.3:

Operating		Start-up	Switch-off	Non-operating	
Min. ^{0}C	Max. ^{0}C	^{0}C	^{0}C	Min. ^{0}C	Max. ^{0}C
-15	+45	-30	+50	-35	+60

With acceptance temperature 5 ^{0}C below min. and 5 ^{0}C above max. operating temperatures. Qualification temperature 10 ^{0}C below min. and 10 ^{0}C above max. operating temperatures.

3.4 Design and Manufacture Requirements

3.4.1 Design requirements

Requirement ID	Description	Reference
	CPU board design	
DPU-DES-01	The CPU board shall be based on the DSP TEMIC TSC21020, at least 20 MHz clock, chip.	
DPU-DES-02	The CPU board shall carry a watch-dog system (TBC).	
DPU-DES-03	The CPU board shall include a programmable timer, with a precision of 1 μs and a max capacity of 100s.	
DPU-DES-04	The CPU board shall carry an EDAC hardware system for on line correction of single errors (TBC). In any case SEU and radiation resistance of memories shall be such as to guarantee no more than one bit error/year on RAM.	
DPU-DES-05	The CPU board shall have at least 32 kbytes of PROM memory with the bootstrap programme and software to face emergency situation and for maintenance.	
DPU-DES-06	The CPU board shall have at least 512 Kbytes of EEPROM memory for the main programme.	
DPU-DES-07	The CPU board should have at least 768 Kbytes of PROGRAMME static RAM.	

DPU-DES-08	The CPU board should have at least 1024 Kbytes of DATA static RAM.	
DPU-DES-09	It shall be possible to modify the EEPROM's content during flight through a maintenance programme resident in PROM and through a software programme coming from the telecommand system.	
DPU-DES-10	All RAM (DRAM) memory (both DATA and PROGRAMME memory) should be either SEU free or protected against SEU by means of a hardware EDAC system. See DPU-DES-04.	
DPU-DES-11	The CPU board shall have a system bus interface working either in master or slave mode. In master mode the board can have access to other digital boards through the bus. In slave mode other master boards (for instance the S/C interface board) can have access to a Dual-Port RAM memory bank, accessible to CPU, to exchange with CPU messages and data blocks.	
DPU-DES-12	The CPU board shall carry on PROM the following basic software: - a loader of a programme from telecommands; - a driver for the spacecraft I/F (MIL-STD-1553B) - a driver for the EEPROM writing. - A function to carry out the EEPROM checksum test Moreover the CPU board shall support the EONIC Virtuoso operating system.	
	Low speed interface design	
DPU-DES-13	All links use the RS 422 standard (balanced line drivers and receivers).	
DPU-DES-14	All the frequencies generated within the DPU shall come from the same oscillator, in order to limit the EMC problems.	
DPU-DES-15	All data transactions with any addressed subsystem (addr. In TX_DAT, see fig. 2-9), are initiated by DPU. DPU shall send data to all subsystems using one serial bus line TX_DAT with three output buffers and can send both commands and HK requests via this line.	
DPU-DES-16	DPU shall be able to accept the subsystems responses via the three RX_DAT lines (see figure 2.7).	
DPU-DES-17	The Clock rate shall be 0.2MHz (TBC).	
DPU-DES-18	Clock and TX_DAT shall be generated by DPU and distributed to all subsystems.	
DPU-DES-19	RX_DAT lines, coming from each subsystem, shall be multiplexed in the DPU.	
DPU-DES-20	For internal reading of analogue signals an A/D converter (12 bit) plus MPX (8 Channels) shall be provided in order to digitise the information of an internally conditioned thermistor and of the DC/DC	

	converter voltages and total DPU current.	
	High speed interface design	
DPU-DES-21	Three fast (1 MHz clock, TBC) synchronous serial input interfaces shall be provided, each of which with 8 KW 32 Bit FIFO. The clock, gate and data signals, coming from the subsystems, are as in Figure 2-8. All data can be received by the DPU at the same time.	
	DC/DC Converter design	
DPU-DES-22	The synchronised DC/DC converter board shall have the following main characteristics: - input DC voltage ranging from 26 to 30 V (TBC), nominal is 28 V within 1%(TBC);	AD2 sect. 5.9.5.2
DPU-DES-23	- max power to the DPU: 15W	AD3 sect. 5.9.3
DPU-DES-24	- efficiency of 70% or better;	
DPU-DES-25	- input filter with EMI-EMC properties (following ESA EMC/EMI specs);	
DPU-DES-26	- overall characteristics in agreement with FIRST IID-A (inrush current etc.).	AD2 sect. 5.9.5.4
DPU-DES-27	- input impedance = 5kOhm in parallel to 200 pF.	AD2 sect. 5.9.5.6
DPU-DES-28	The DC/DC converter shall support a synchronisation signal (squarewave, 5.0 V +/- 20%, ground free, transformer coupled) with a frequency of 131.073 kHz.	AD2 sect. 5.9.5.6
DPU-DES-29	Each of the two DC/DC converters shall be connected to an individual synchronisation signal	AD2 sect. 5.9.5.6.1
DPU-DES-30	In absence of a synchronisation signal, the DC/DC converter shall be free running at the nominal frequency +/- 10% with nominal performance.	AD2 sect. 5.9.5.6.1
	Spacecraft interface design	
DPU-DES-31	The spacecraft interface board shall be compliant with the MIL-STD-1553B standard.	AD3 sect. 5.11.5
	Overall mechanical design	
DPU-DES-32	The total FSDPU mass shall be less than 10 Kg.	AD3 sect. 5.5
DPU-DES-33	The FSDPU dimensions shall be 240x210x194 mm^3	AD3 sect. 5.5
DPU-DES-34	The maximum shock to be sustained in any direction is 5g (TBD).	AD3 sect. 5.15.3.1

3.4.2 Design rules

Requirement ID	Description	Reference
DPU-DES-35	The boards dimensions should preferably be of «double Europe» standard.	
DPU-DES-36	All DPU boards shall carry Rad Tolerant memories and components: - AVM: commercial grade components required; - QM: commercial components or better to match Fit,	

	Form and Functions of the FM/FS units; printed boards artwork shall be the same as FM/FS. - PFM and FS: SCC level B for the S/C I/F SCC level C for all other components (baseline: if CPP confirmed, all components at SCC/C level B).	
DPU-DES-37	External connectors characteristics and mounting shall be compliant with AD2 indications.	AD2 sect. 5.10.1

3.4.3 Manufacture Requirements

Requirement ID	Description	Reference
DPU-DES-32	All the pertinent ESA recommendations for boards manufacturing shall be applied.	

3.5 Logistic Requirements

Normal laboratory conditions will be suitable for the ICU as the FM unit will be enclosed in a plexiglass box with an aluminum plate and it will be possible to have access to the box connectors through appropriate windows. A clean room of at least class 100000 is the preferred environment (see AD3 section 5.15.3.1). Precautions have to be taken in order to avoid ESD damages.

3.6 Environment Requirements

See section 3.5.

3.6.1 Natural environment

See section 3.3 for the in-orbit operating temperatures of the DPU.
See section 3.5 for the storage environment.
Radiation environment: TBW

3.6.2 Operating Environment

See sections 3.3 and 3.6.1 above.

3.7 Verification Requirements

3.7.1 DPU Acceptance And Qualification

According to AD1, section 2.5, the SPIRE instrument will be qualified at unit level (i.e. the Warm electronics units and the cold FPU units).
Adopting the assumptions listed in section 3.3 of AD1, the DPU will undergo the following tests:

Test:	DPU QM	DPU PFM	DPU FS
Vibration:	Q	A	A
Thermal cycle:	Q	A	A
Vacuum cycle	Q	A	A
Lifetime:	-	-	-
Soak/cycle:	X	X	X
Radiation tolerance:	-	-	-
Thermal range:	Q	A	A
Thermal stability:	-	-	-
Microphonics:	-	-	-
Ionising radiation:	-	-	-
EMC (Instrument Level):	X	X	-
EMC (Satellite Level):	X	X	-

Table 3-1 : Test matrix for the FSDPU. Q indicates a test carried out at qualification level for qualification times; A indicates a test carried out at acceptance level. An X indicates that this test is carried out and is a characterisation type test or the level is irrelevant. A dash indicates that no test will be done on this model/unit. Instrument level Qualification

Requirement ID	Description	Reference
DPU-VER-01	To carry out the tests on the FSDPU QM listed in Table 3-1.	IRD-VER-R02
DPU-VER-02	To carry out the tests on the FSDPU PFM listed in Table 3-1.	IRD-VER-R03
DPU-VER-03	To carry out the tests on the FSDPU FS listed in Table 3-1.	IRD-VER-R03

APPENDIX 1: QUALIFICATION TESTS DESCRIPTION

Vibration:	The QM DPU will be vibrated at levels appropriate to its location within the instrument, as defined in AD2.
Thermal-Vacuum cycle:	The DPU will undergo thermal vacuum tests. The number of cycles and the temperatures are defined in AD2.
Lifetime:	NA.
Soak/cycle:	The soak test will be part of the TV test, soak times are defined in AD2.
Radiation tolerance:	All ICU components will be radiation tolerant. A suitable analysis will show that the total dose will not exceed 10 kRad end of life.
Thermal range:	The applicable thermal ranges will be reached during the TV test.
Thermal stability:	NA
Microphonics:	NA
Ionising radiation:	See radiation tolerance above.
EMI:	The sensitivity of the ICU to electromagnetic interference will be characterised.
EMC:	The radiated and conducted electromagnetic emission of a the ICU will be characterised.
Materials conformance:	All materials used in the manufacture of the ICU will be approved for space use by ESA