Hercshel SPIRE

DPU Subsystem Specification Document

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Issue 1.0	0.1	26 Mar 2001	Updated accordingly to new Issues of the Applicable Documents. Low speed interface protocol updated.
Issue 1.2		26 Nov 2001	Grounding Scheme added ; DC/DC Conv. Synch removed + minor changes

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3.2, fig. 3-10	New Low Speed Interface Protocol graphical representation
3.2, fig. 3-4	New CPU memory organisation scheme
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3.4	QM, FM and FS components quality levels
4.23	HK parametres
4.4.1, DPU-DES-32	New DPU mechanical dimensions.
3.3	New Grounding scheme and Box Interface Control Drawing
4.4.1, DPU-DES-12	Updated
4.4.1, DPU-DES-13	Re-phrased
4.4.1, DPU-DES-26	Removed
4.4.1, DPU-DES-27	Synch frequency updated
4.4.1, DPU-DES-28	Removed
4.4.1, DPU-DES-29	Removed
4.4.1, DPU-DES-32	Dimension confirmed
4.4.1, DPU-DES-35	Components quality levels updated

1 Introduction

1.1 Purpose of the document

The Istituto di Fisica per lo Spazio Interplanetario (IFSI) of the Italian Consiglio Nazionale delle Ricerche (CNR) is responsible for the design and manufacturing of the three Digital Processing Units/Instrument Control Units for the three instruments to be flown on board of the ESA satellite FIRST: HIFI, PACS and SPIRE.
This specification defines the requirements applied to the performances, the design and the qualification of the SPIRE Digital Processing Unit (HSDPU subsystem). It is applicable to the AVM, the QM, the PFM and the FS.
The DPU On Board Software specification is given in the DPU/ICU OBS User Requirements Document and DPU/ICU OBS Software Specification Document.

2 Document List

2.1 Applicable Documents

Document Reference	Name	Number/version/date
AD1	SPIRE Instrument Requirements Document	SPIRE/RAL/N/0034 Issue 0.1 23 Nov 2000
AD2	FIRST/Planck Instrument Interface Document Part A	PT-IID-A-04624 Draft 0.3 15 May 2000
AD3	FIRST/Planck Instrument Interface Document Part B Instrument “SPIRE”	SCI-PT-IIDB/PT-SPIRE-02124 Issue 0.1 01 Sep 2000
AD4	Operating Modes for the SPIRE Instrument	SPIRE-RAL-DOC-000320 Issue 0.22 14 June 2000
AD5	FIRST L-2 Radiation Environment	SPIRE-ESA-DOC-000195
AD6	DPU Interface Control Document	SPIRE-IFS-DOC Issue 1.0 2 Apr 2001

2.2 Reference Documents

Document Reference	Name	Number/version
RD1	DPU/DRCU Interface Control Document	SPIRE-SAP-PRJ-000451 Issue 0.2 21 June 2000
RD2	Discussion Note on the DPU/DRCU Operations Protocols- B. Swinyard	22 May 2000

2.3 Acronyms and Glossary

2.3.1 Acronyms

AD	Architectural Design
ATP	Acceptance Test Plan
AVM	Avionic Model
CNR	Consiglio Nazionale delle Ricerche
CPU	Control Processing Unit
CDMS	Computer Data Management System
CPP	Common parts Procurement
CQM	Cryogenic Qualification Model
DCU	Detector Control Unit
DDD	Detailed Design Document
DPU	Digital Processing Unit
DSP	Digital Signal Processor
EEPROM	Electrically Erasable Programmable Read Only Memory
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ESA	European Space Agency
FIRST	Far InfraRed and Submillimeter Telescope
HIFI	Heterodyne Instrument for FIRST
HK	HouseKeeping
HW	HardWare
IBDR	Instrument Baseline Design Review
ICD	Interface Control Document
ICDR	Instrument Critical Design Review
ICU	Instrument Control Unit
IHDR	Instrument Hardware Design Review
IFSI	Istituto di Fisica dello Spazio Interplanetario
ISVR	Instrument Science Verification Review
MCU	Mechanism Control Unit
NA	Not Applicable
OBS	On-Board Software
PA	Product Assurance
PACS	Photoconductor Array Camera and Spectrometer
PROM	Programmable Read Only Memory
RAM	Random Access Memory
SCC	SpaceCraft Components
SCU	Subsystem Control Unit
SEU	Single Event Upset
SPIRE	Spectral and Photometric Imaging Receiver
SVM	Service Module
SW	Software
TBC	To Be Confirmed
TBD	To Be Defined
TBW	To Be Written
TVT	Thermal Vacuum Test

3 Subsystem Description

3.1 General Overview

The DPU of the SPIRE Instrument (HSDPU) interfaces with the Detector readout and Control Unit subsystem (HSDRC) and with the S/C telemetry, telecommand (the on board CDMS, Command and Data Management system) and power systems. In Figure 3-1 the block diagram showing the interfaces of the HSDPU is presented, including the cryo-harness. Conceptually the HSDRC is a single unit. However for accommodation reasons it will be split into two physical units: Instrument Control Unit (FSICU) and Detector Readout Unit (HSDRU).
FSICU contains:

- the electronics for the power conversion and distribution to the DRCU, for the control and readout of the thermometers, the cooler and the calibration sources (Subsystem Control Unit, SCU)
- the electronics for the control and readout of the cold mechanisms (Mechanisms Control Unit, MCU).

HSDRU contains the bias conditioning electronics for the bolometers arrays and JFET units and the lock in amplifiers and readout electronics for all the detector arrays.

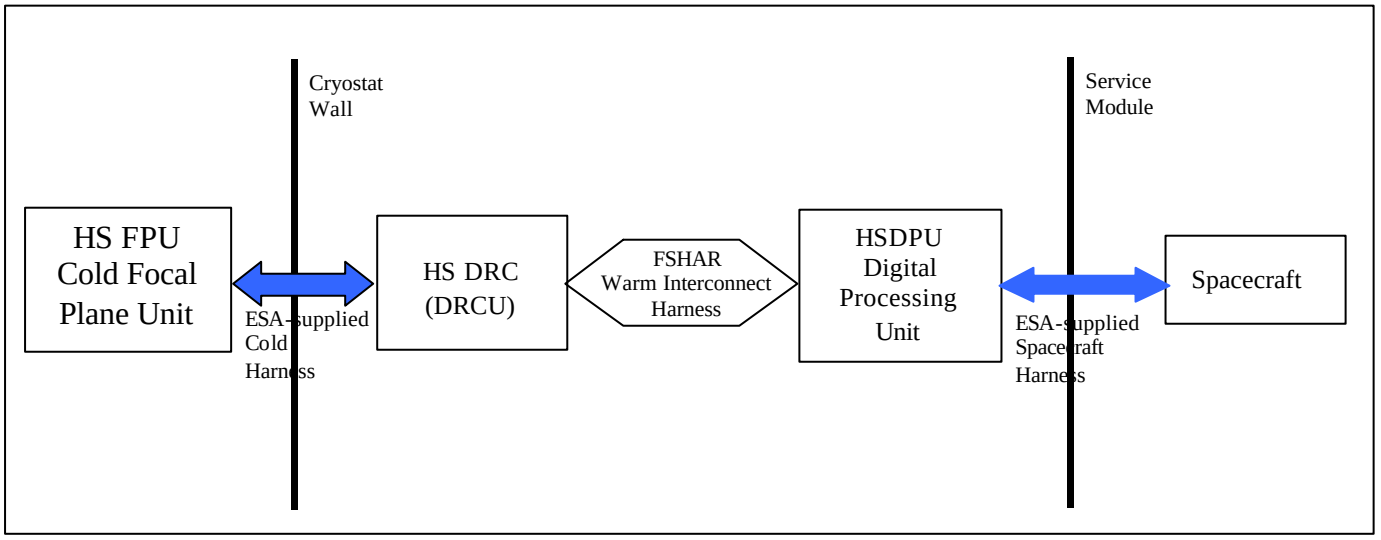

Figure 1-1 SPIRE block diagram

The interface with HSDRC will be composed by three high speed data links for science data collection (two links with HSICU and one link with HSDRU) and one low speed serial bus with three output buffers, for command transmission and housekeeping data collection (two outputs to FSICU and one output to HSDRU). Refer to AD6 for a detailed description of the harness. The interface with the spacecraft shall be able to handle a baseline data rate of 100 kbps, with burst mode transmission up to 300 kbps. The interface shall be compliant with the MIL-STD-

1553B standard, with the HSDPU acting as a remote terminal and the CDMS as the bus controller.

In Figure 3-2 the SPIRE DPU high level block diagram is shown: the HSDPU box is fully hardware redundant, with one DPU ON and the other in cold redundancy. Each of the two redounded computers has its own DC/DC converter, CPU, memory and interfaces both to spacecraft and to the subsystems. Only the Avionic Models (see section 3.4) will have no redundancy, neither for the DC/DC converter, nor for the on board computer.
The main blocks of each of the two redounded DPUs are the CPU, the Spacecraft and subsystems interface and the DC/DC Converter.

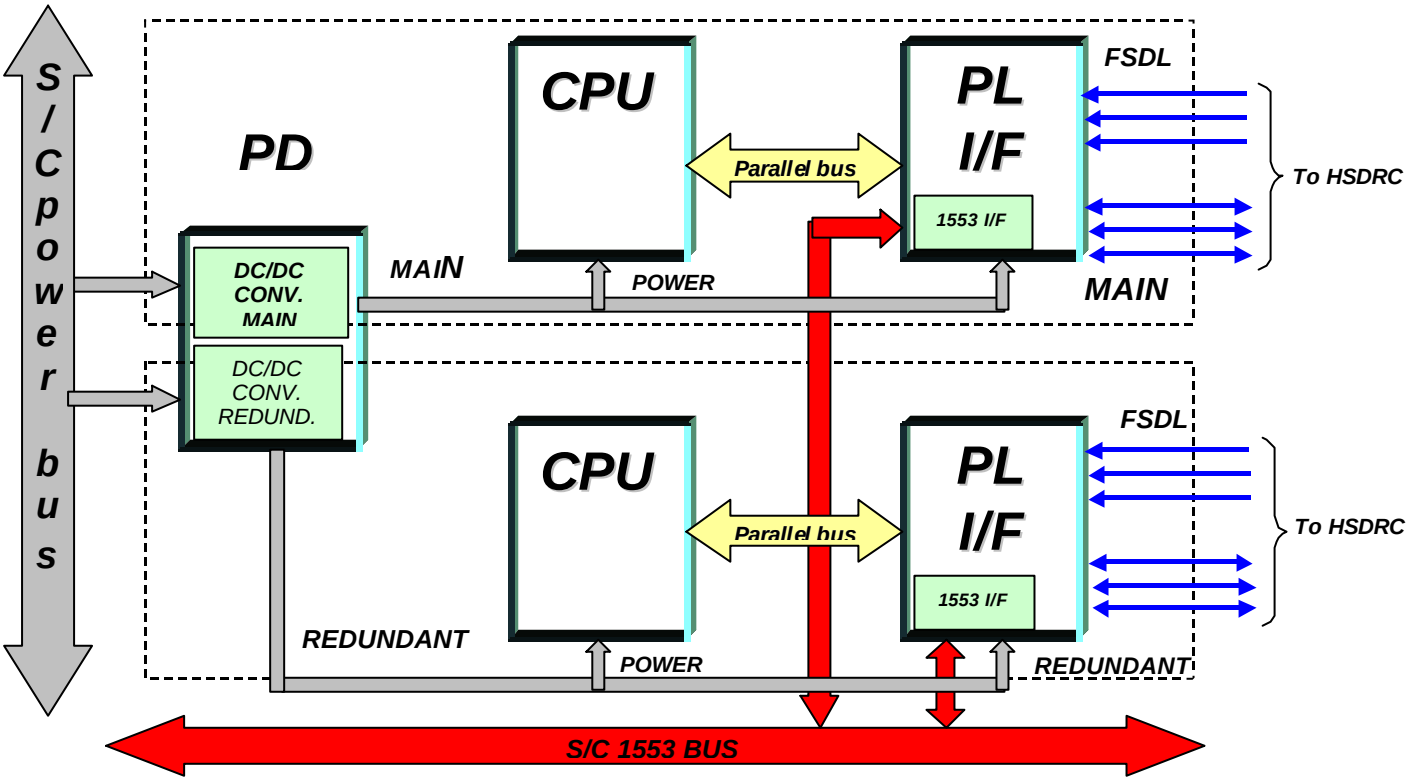

Figure 1-2 HSDPU high level block diagram

3.2 Subsystem Design

The HSDPU subsystem will include a free running (131072 Hz) DC/DC converter with a nominal input DC voltage of 28 V and the overall characteristics in agreement with AD2. In figure 3-3 a block diagram of the DC/DC converter is shown
The adopted CPU is the TEMIC TSC21020, that is a Digital Signal Processor (DSP) unit developed by Analogue Devices and implemented for flight use by TEMIC.
The CPU board will be based on this chip (20 MHz clock), with:

- an appropriate timer for time management and synchronisation purposes
- a watch-dog system that can be hardware disabled through jumper;
- Rad Tolerant memories and components

In Figure 3-4 the main blocks of the CPU board are shown.

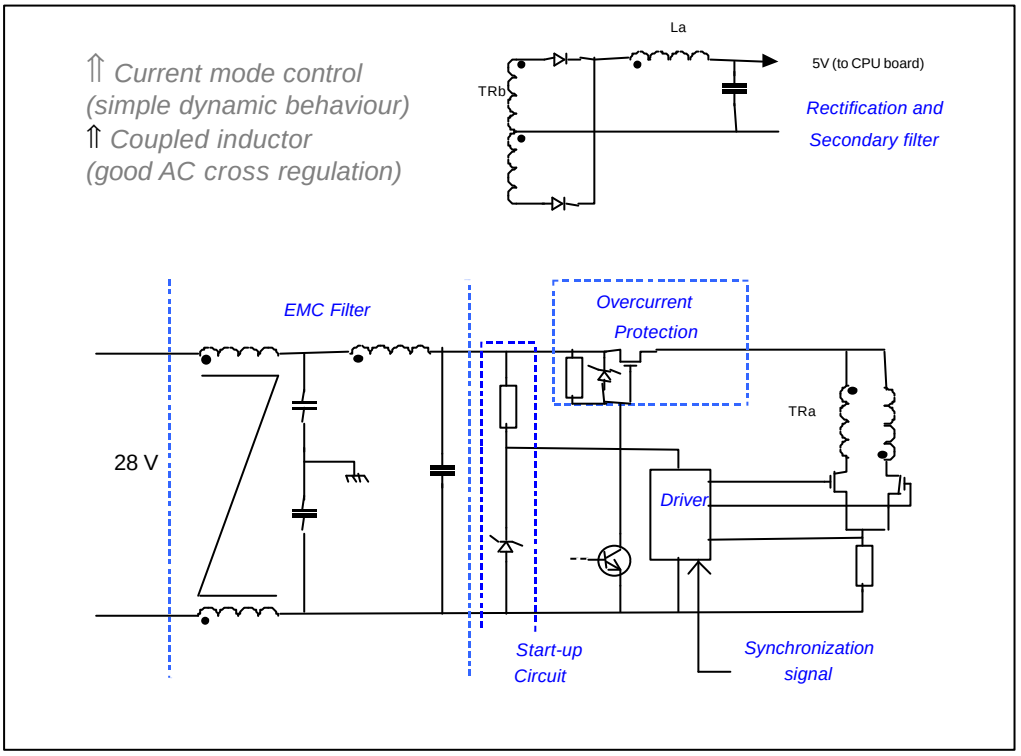

Figure 1-3 DC/DC Converter scheme.

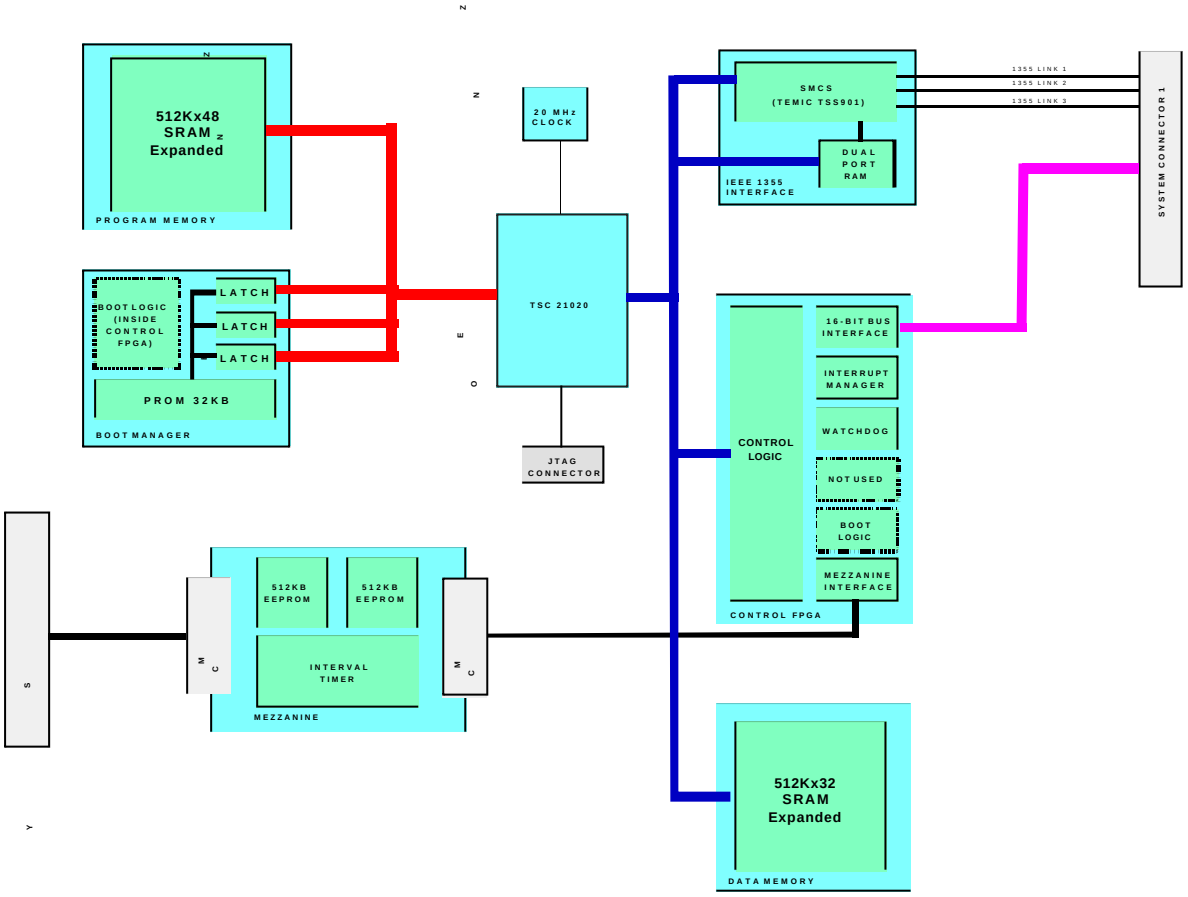

Figure 1-5 CPU Board Block Diagram

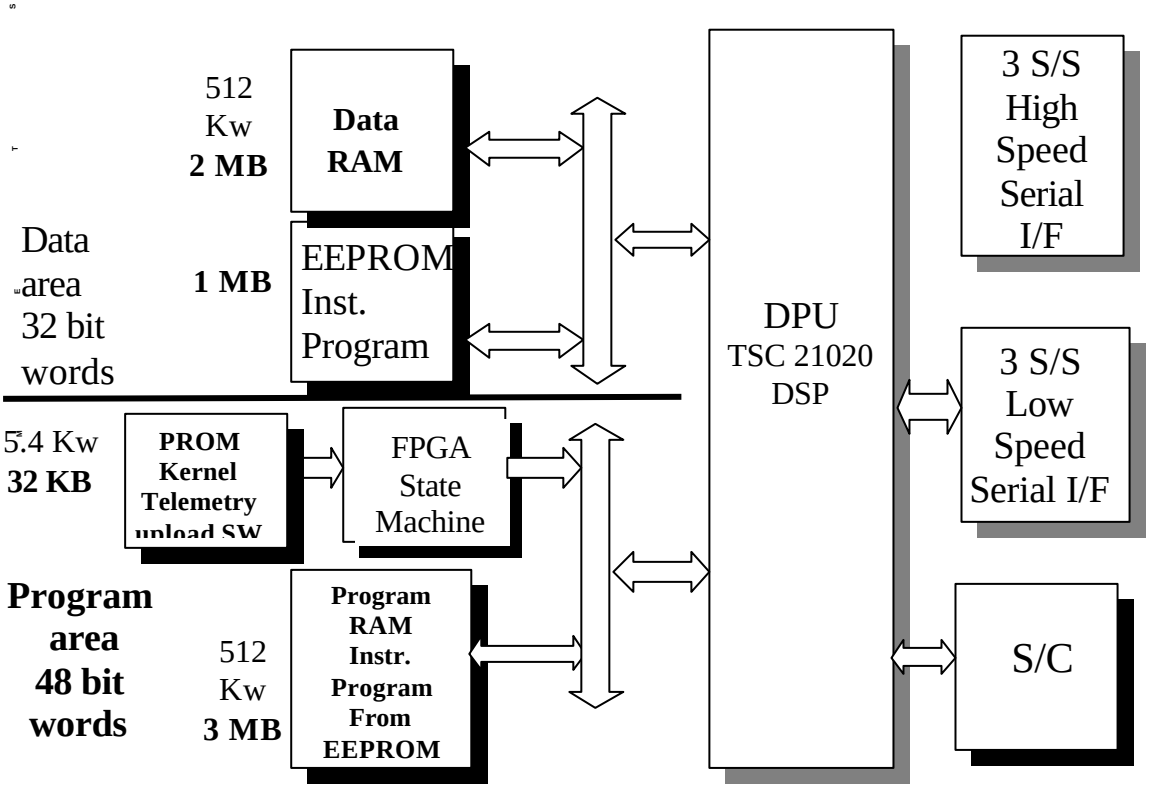

Figure 1-4 CPU Memory Organisation

In Figure 3.4 the memory organisation of the CPU is shown with the dimensions of the various types of memories. The CPU board will carry (on the PROMs) some basic software containing at least:

1. a driver for the interface circuit with the S/C;
2. a programme loader through the S/C telemetry;
3. a driver for writing the EEPROMs;
4. a function to carry out the EEPROM checksum test.

The DPU interfaces mechanically with the S/C and electrically with the S/C and the various subsystems. The electrical hardware interface with the S/C consists in:

- interface with the S/C Power Distribution System and the 28 V lines;
- interface with the telemetry and telecommand subsystems.

In figure 3-5 a block diagram of the S/C interface board is shown. The MIL-STD-1553B standard is implemented through one nominal and one redundant transformer in the long stub configuration.

The interface between DPU and DRCU is shown schematically in Figure 3-7; a detailed description of this interface is given in RD1. For the science data link, **three monodirectional fast (1 MHz clock) synchronous serial input interfaces**, each of which with 8 KW 16 Bit FIFO, are foreseen: the data can be received by the DPU at the same time. The clock, gate and data signals, coming from the subsystems, are as in Figure 3-8.

A serial synchronous bus is foreseen to interface with the control electronics of the focal plane unit subsystems: the bus will be used to transmit commands and receive responses or to control and receive housekeeping information. The baseline clock speed is 0.2 MHz (TBC). In Figure 3-9 the signals are shown: CLK & TX_DAT are coming from DPU and go in parallel with three distinct hardware interfaces to the three DRCU electronics blocks; the three RX_DAT lines are coming each from each of the three blocks and are multiplexed inside the DPU (see RD1).

3.3 Grounding scheme

In fig 1.11 the proposed grounding scheme is shown. It is based on the “Single Point Distributed Grounding Scheme”, i.e. all subsystems have their internal star point to which all the return lines are connected and which in turn is connected to chassis ground with a single connection.

This scheme can be easily transformed in a “Single Point Grounding” if the stars internal to all subsystems are not connected to chassis ground and are connected with a wire to the central star point in turn connected with a single connection to chassis.

During EMC/EMI tests it can be useful to connect the box to the structure with an external strap. To this purpose all warm boxes will foresee a bonding lug implemented according to IID-A 5.10.4.10.

In the following figure 1.12 a preliminary mechanical interface control drawing is shown.

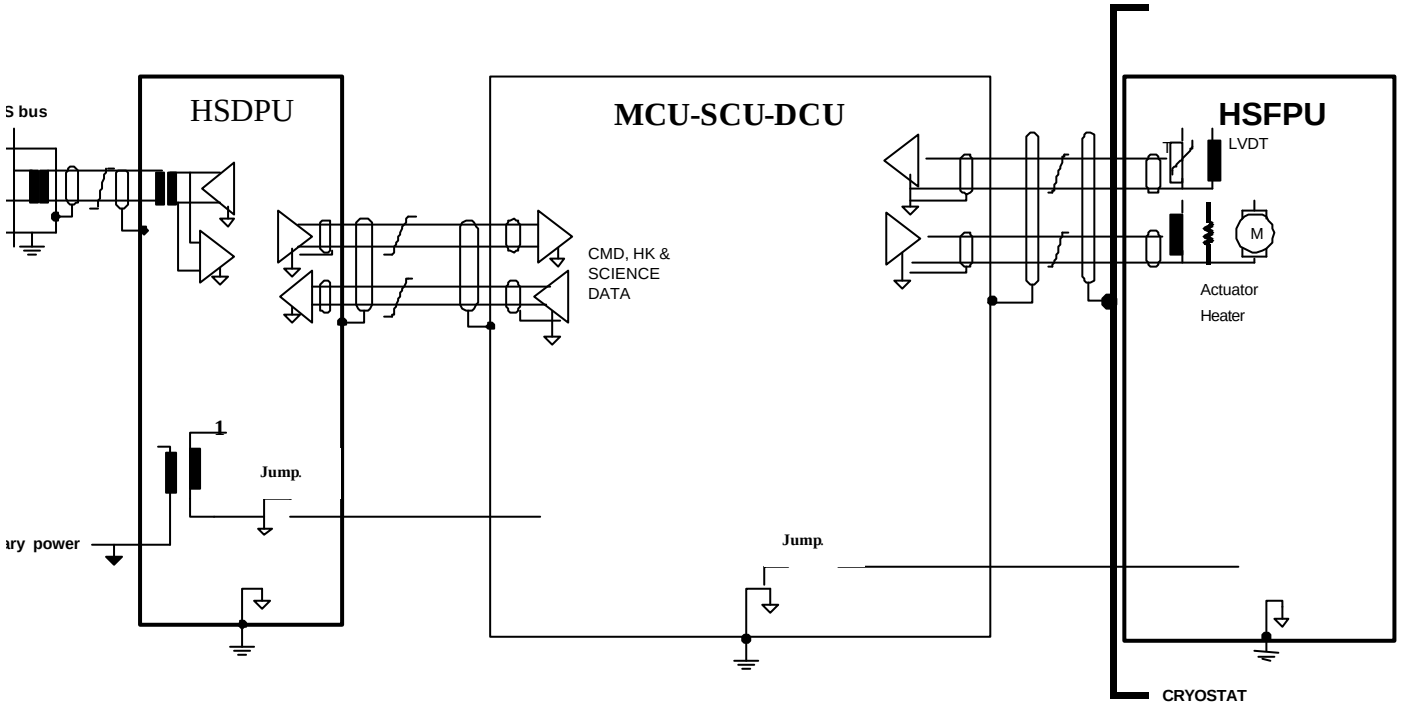

Fig. 1.11 DPU GROUNDING SCHEME

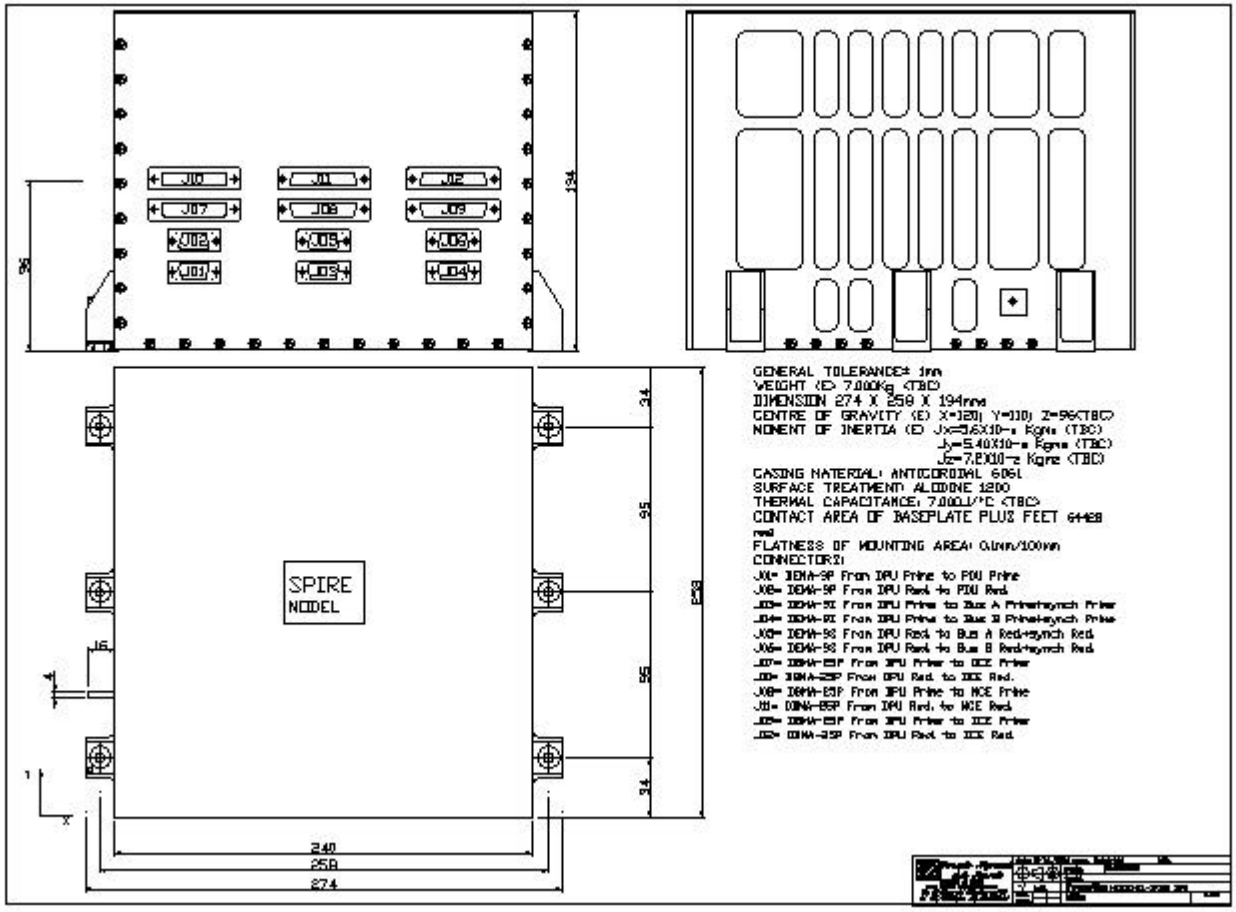

Fig. 1.12 Box Interface Control Drawing

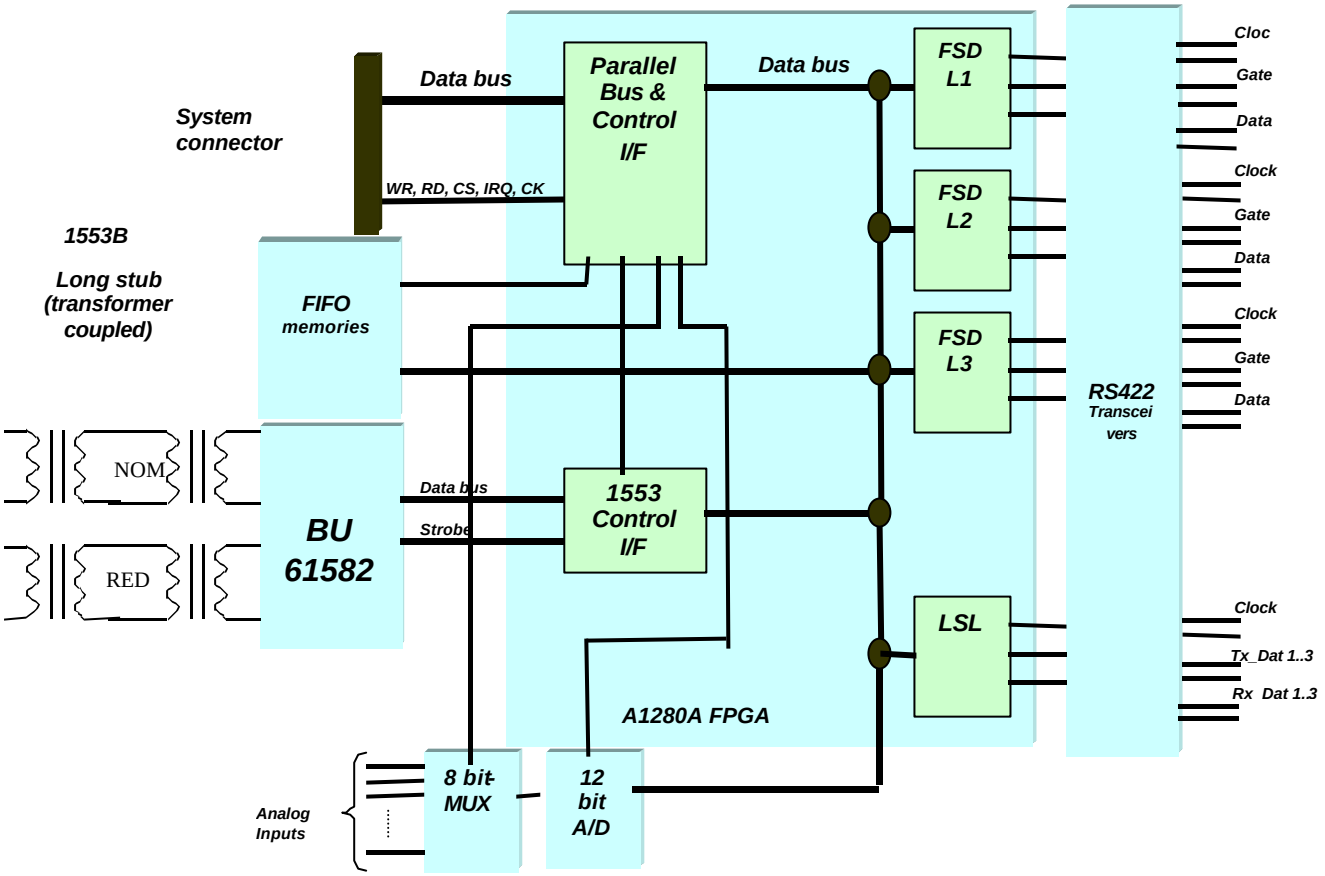

Figure 1-6 Spacecraft Interface Block Diagram

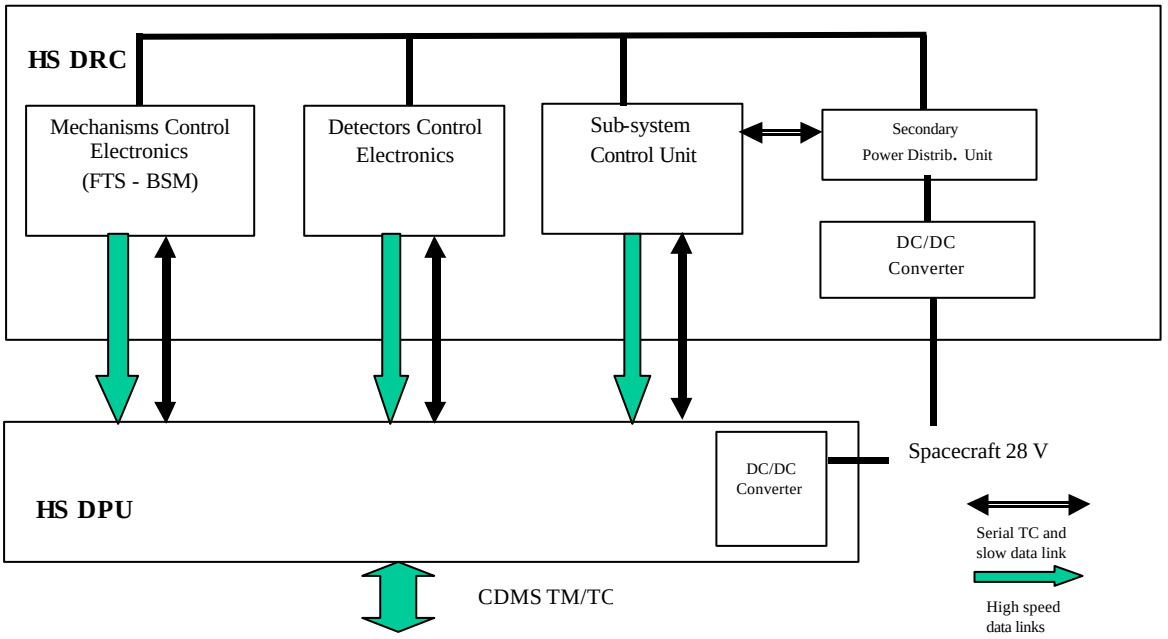

Figure 1-7 HSDPU/HSDRC Interface Block Diagram

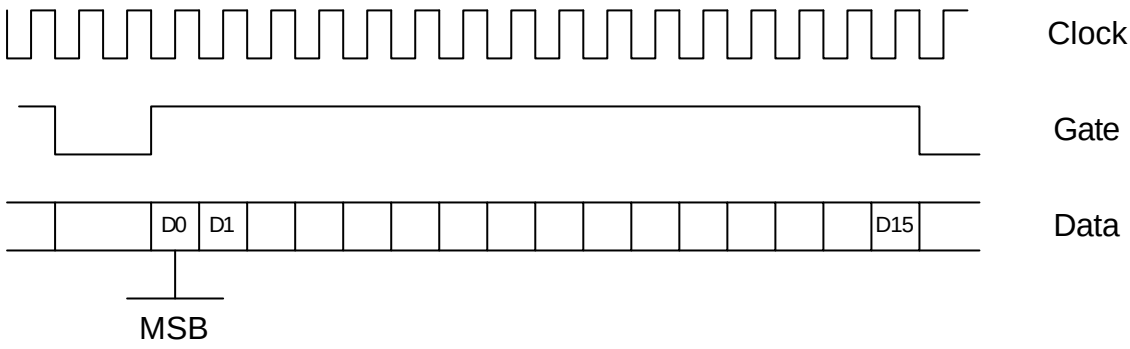

Figure 1-8 High speed interface protocol

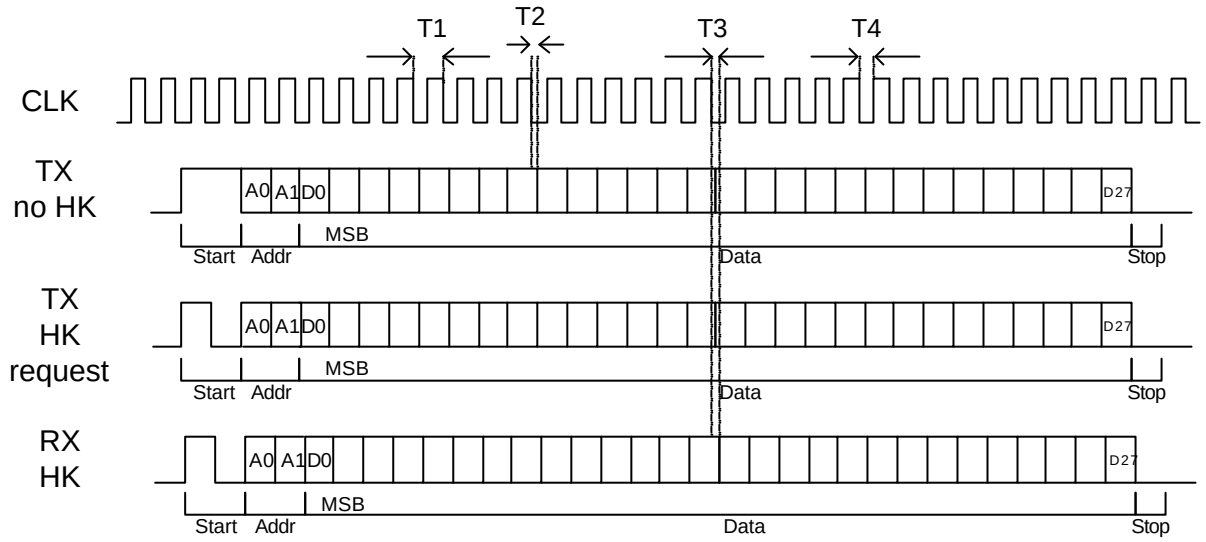

Figure 1-10 HSDPU/HSDRCU Low Speed Interface protocol

All data transactions with the addressed subsystem (addr. In TX_DAT), are initiated by DPU. DPU will send data to all subsystems using one serial data line TX_DAT and can send both commands and HK requests via this line.
Subsystems, if required, will send responses via RX_DAT line.
A **command** is made of 2 start bits, 2 address bits, 28 data bits and 1 stop bit.
A **HK request** is made by setting the second start bit.
A **HK response** will consist of 2 start bits, 2 address bits, 28 data bits and 1 stop bit
The sub-unit address field in the TX command is used to select the input channel RX. No command can be sent to a sub-unit until the echo/HK RX corresponding to the last command sent is received. Figure 3-10 shows the transmission-reception sequence.

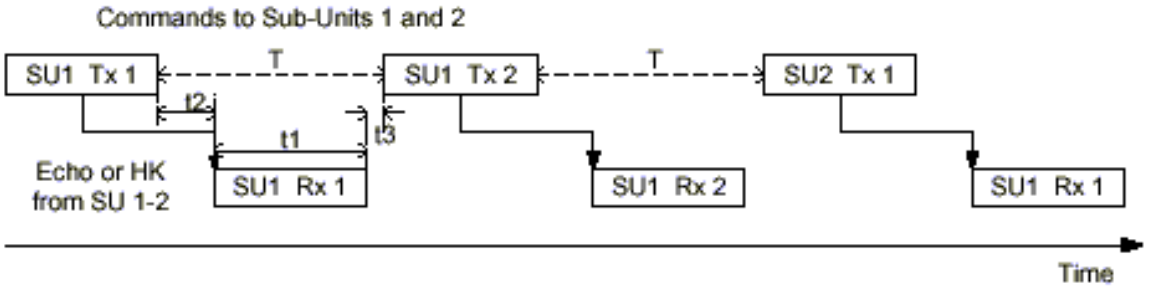

Figure 3-10 Low speed Interface – transmission reception protocol

Clock and TX_DAT are generated by DPU and distributed to all subsystems
For internal reading of analogue signals an A/D converter (12 bit) plus MPX (8 Channels) will be provided in order to digitise the information of an internally conditioned thermistor and of the DC/DC converter voltages.

3.4 Mission Profile

The DPU will be designed to be used for 2 years on the ground, 2 years (TBC) of storage and 4 years in orbit with a probability better than 90% for the single ICU section (prime or redundant).

3.5 Product Tree

The following deliverables are foreseen:

1) DPU-AVM (Avionic Model): no redundancy, neither for the DC/DC converter, nor for the on board computer; only commercial grade components. These are to be used for the spire BBM (breadboard model), see section 2.4 of AD1. **It is anticipated that it will not be possible to comply with what requested in AD2, chapter-page 9-1, paragraph 9.2.2.1, i.e. the AVM components will not be purchased, in general, from the same supplier of the FM/FS parts.** The AVM will be delivered to ESA.
2) DPU-QM (Qualification Model): full redundancy, both for the DC/DC converter, and for the on board computer; as far as possible MIL-C grade components within the fit, form and function of the flight model. The printed boards artwork will be the same as for FM/FS. This unit will undergo qualification tests. It is not a deliverable to ESA.
3) DPU-PFM (Proto-Flight Model): full redundant box; SCC level B components. This unit will undergo acceptance tests.
4) DPU-FS (Flight Spare): only spare boards (CPU, S/C I/F, SubSytem I/F, DC/DC Conv., mother board): SCC level B. These boards will undergo acceptance tests.

4 Specifications

4.1 Functional specifications

4.1.1 Performance specifications

Requirement ID	Description	Reference
DPU-FUN-01	The interfaces of HSDPU with HSDRC shall be designed in order to couple with the maximum output data rates of the subsystems in the Cold Focal Plane: - FTS mechanism controller; - Beam Steering Mirror; - Detector Focal Planes units (3 Photometer arrays and 2 Spectrometer arrays); - Sorption cooler; - Temperature probes; - DRU/ICU housekeeping; - Calibration Sources.	RD2, AD4 Sect. TBD
DPU-FUN-02	The DPU shall be able to acquire all Photometer detector pixels corresponding to a 4'x8' FOV (288 detectors) at a maximum readout frequency of 40 Hz per frame and 16 bits per sample.	RD2, AD4 Sect. TBD
DPU-FUN-03	The DPU shall be able to acquire all Spectrometer detector pixels corresponding to a 2.6'x2.6' FOV (56 detectors) at a maximum readout frequency of 200 Hz per frame and 16 bits per sample.	RD2, AD4 Sect. TBD
DPU-FUN-04	Photometer data: The instantaneous **dynamic range** of the readout of a pixel shall be 16 bits.	AD4 Sect. TBD
DPU-FUN-05	Spectrometer data: The instantaneous **dynamic range** of the readout of a pixel shall be: 15 bits (with background nulling).	AD4 Sect. TBD

4.1.2 Technical specifications

DPU-FUN-06	The DPU shall be able to handle the adopted standard MIL-STD-1553B for the interface with the spacecraft, supporting an average telemetry rate of 96 kbps, when the instrument is in prime mode, and of 2 kbps otherwise.	AD2 sect. 5.11.1 AD3 sect. 5.11.1
DPU-FUN-07	The DPU shall be able to handle the adopted standard MIL-STD-1553B for the interface with the spacecraft, supporting a maximum telecommand rate of 4 kbps.	AD2 sect. 5.11.4

DPU-FUN-08	Maximum DPU power consumption: 15W *Note by IFSI: the actual estimate of the DPU HW manufacturer is 24±6W*	AD3 Sect. 5.9.3

4.2 Operational specifications

4.2.1 Operational Safety

Requirement ID	Description	Reference
DPU-SAF-01	Failure of the DPU, or one of its components, shall not affect the health of any other subsystem, the instrument or the interface with the satellite.	IRD-SAFE-R06
DPU- SAF-02	Failure of any component in the DPU shall not damage any redundant or backup component designed to replace that component in the subsystem	IRD-SAFE-R09
DPU- SAF-03	No ASICs or FPGAs shall be capable of affecting instrument operations until they are in a defined state.	
DPU- SAF-04	It shall be possible to break via software all electronic control loops implemented in hardware, provided that the relevant commands are implemented in the HSDRC in agreement with HSDPU.	IRD-REL-R05
DPU- SAF-05	The instrument shall monitor the operational status of the instrument on-board computer and take appropriate action in case of error. (*a watchdog function will be implemented to identify if the on board computer has crashed) TBC*	IRD-AUT-R06
DPU- SAF-06	Cold redundant hardware shall be provided	IRD-REL-R03

4.2.2 Lifetime

Requirement ID	Description	Reference
DPU-OPE-01	The DPU PFM shall be designed to couple with an integrated lifetime of 2 years.	AD2
DPU-OPE-02	The DPU PFM shall be designed to couple with a ground storage lifetime of 2 years (TBC).	AD2
DPU-OPE-03	The DPU PFM shall be designed to couple with an in orbit lifetime of 4 years, with a probability better than 90% for the single DPU section (prime or redundant).	AD2

4.2.3 Telemetry

The housekeeping parameters provided by the DPU are (list is TBC):

- DPU Voltages (+5, +15, -15, +2.5 V: 8bytes)
- DPU Temperature (2bytes)

4.2.4 Telecommands

The DPU dedicated commands are (list is TBC):

- ***DPU reset***
  Command: DPU_N_Reset(); DPU_R_Reset()
  Parameters: Input --- None
  Output --- None
  Action: Warm reset of the DPU. A warm reset is similar to a reboot without neither a memory test nor a copy of EEPROM into RAM. In this way the following DPU status is like after a switch-on but with its memory content preserved. *This is an immediate command.*

- ***Measurement Reset (TBC)***

- ***Execute a function onboard***
  Command: DPU_N_EXEC_FUNCT (8,3)
  Parameters: Input --- FunctionID 8bits
  N 8bits
  PArameters NX16bits
  Action: Executes a function already stored onboard

- ***Set the telemetry rate***
  Command: DPU_N_SET_TM_RATE (8,3)
  Parameters: Input --- mode 8bits
  Action: Set the telemetry rate: prime, parallel.

- ***Memory check***
  Command: DPU_N_MEM_CHECK (6,9)
  Parameters: Input --- MemID 8bits
  Address 24bits
  Length 16bits
  Action: A checksum is derived for the specified area in memory.

- ***Memory load***
  Command: DPU_N_MEMORY_LOAD (6,2)
  Parameters: Input --- MemID 8bits
  Address 24bits
  Length 16bits
  Data 16Xlength bits
  Action: RAM Memory load (TBC)

- ***Memory dump***
  Command: DPU_N_MEMORY_DUMP (6,5)
  Parameters: Input --- MemID 8bits
  Address 24bits
  Length 16bits

Action: Memory dump applicable to any one of the 3 types of memory, PM, PM, EEPROM (TBC)

- ***Subsystem Parameter Table Update***
  Command: DPU_N_TABLE_UPDATE (6,2)
  Parameters: Input Start 16 bit
  Length 16bit
  Data 16Xlength
  Output --- Return 4 Bytes
  Action: The content at address Start is substituted for by the content at address Data. The pointers Start and Data are incremented by one an the operation is repeated until Length bytes have been transferred. This command updates (part of) the DPU parameters stored onboard in the *s subsystems parameters table*. DATA are stored in Data memory starting from ADDRESS for a total of LENGTH bytes

- ***Set the predefined HK packet to be provided***
  Command: DPU_N_SET_HK_LIST(8,3)
  Parameters: Input --- Mode 8bits
  Output --- Return 6 Bytes
  Result 1 Byte
  Action: sets the predefined list of HK values for the HK packet (the total number of predefined packets depends on the number of operating modes).

- ***Enable packet transmission***
  Command: DPU_N_ENABLE_PACKET_TRANSMISSION(14,1)
  Parameters: Input --- N 8bits
  Type 8bits
  Sub-type 8bits
  SID 8bits
  Action: enables the transmission of telemetry source packets of the specified type and subtype.

- ***Disable packet transmission***
  Command: DPU_N_DISABLE_PACKET_TRANSMISSION(14,2)
  Parameters: Input --- N 8bits
  Type 8bits
  Sub-type 8bits
  SID 8bits
  Action: disables the transmission of telemetry source packets of the specified type and subtype.

- ***All commands related to the time synchronisation (TBC):***
  Command: DPU_N_TIME_SYNC(9,4)
  Command: DPU_N_TIME_VER(9,7)
  Command: DPU_N_TIME_SET(9,4)

- ***Test connection(TBC)***
  Command: DPU_N_TEST_CONN(17,1)

Action: Start the "Are You alive?" procedure.

4.3 Interface Requirements

The required operating temperatures at the interface of the SVM with HSDPU shall be compliant with AD3, section 5.7.3:

Operating		Start-up	Switch-off	Non-operating	
Min. ^{0}C	Max. ^{0}C	^{0}C	^{0}C	Min. ^{0}C	Max. ^{0}C
-15	+45	-30	+50	-35	+60

With acceptance temperature 5 ^{0}C below min. and 5 ^{0}C above max. operating temperatures. Qualification temperature 10 ^{0}C below min. and 10 ^{0}C above max. operating temperatures.

For what concerns the interfaces with the other instrument subsystems, the following requirement is applicable:

Requirement ID	Description	Reference
DPU-IF-01	The interface with FSICU and HSDRU shall be compliant with the description in AD6.	IFSI

4.4 Design and Manufacturing Specifications

4.4.1 Design requirements

Requirement ID	Description	Reference
	CPU board design	
DPU-DES-01	The CPU board shall be based on the DSP TEMIC TSC21020, at least 20 MHz clock, chip.	IFSI
DPU-DES-02	The CPU board shall carry a watch-dog system (TBC).	IFSI
DPU-DES-03	The CPU board shall include a programmable timer, with a precision of 1 μs and a max capacity of 100s.	IFSI
DPU-DES-04	The CPU board shall have at least 32 kbytes of PROM memory with the bootstrap programme and software to face emergency situation and for maintenance.	IFSI
DPU-DES-05	The CPU board shall have at least 512 Kbytes of EEPROM memory for the main programme.	IFSI
DPU-DES-06	The CPU board should have at least 3 Mbytes of PROGRAMME static RAM.	IFSI
DPU-DES-07	The CPU board should have at least 2 Mbytes of DATA static RAM.	IFSI
DPU-DES-08	It shall be possible to modify the EEPROM's content during flight through a maintenance programme resident in PROM and through a software programme coming from the telecommand system.	IRD-CMD-R13 IFSI

DPU-DES-09	All RAM (DRAM) memory (both DATA and PROGRAMME memory) should be SEU free.	IFSI
DPU-DES-10	The CPU board shall have a system bus interface working either in master or slave mode. In master mode the board can have access to other digital boards through the bus. In slave mode other master boards (for instance the S/C interface board) can have access to a Dual-Port RAM memory bank, accessible to CPU, to exchange with CPU messages and data blocks.	IFSI
DPU-DES-11	The CPU board shall carry on PROM the following basic software: - a loader of a programme from telecommands; - a driver for the spacecraft I/F (MIL-STD-1553B) - a driver for the EEPROM writing. - a function to carry out the EEPROM checksum test Moreover the CPU board shall support the EONIC Virtuoso operating system.	
	Low speed interface design	
DPU-DES-12	All links use balanced line drivers and receivers, type 26C31/32.	AD6 Sect. 4.1
DPU-DES-13	All the frequencies generated within the DPU will come as far as possible from the same oscillator, in order to limit the EMC problems.	AD1 Sect. 2.10
DPU-DES-14	All data transactions with any addressed subsystem (addr. In TX_DAT, see fig. 3-9), are initiated by DPU. DPU shall send data to all subsystems using one serial bus line TX_DAT with three output buffers and can send both commands and HK requests via this line.	AD6 Sect. 4.2
DPU-DES-15	DPU shall be able to accept the subsystems responses via the three RX_DAT lines (see figure 3.7).	AD6 Sect. 4.2
DPU-DES-16	The Clock rate shall be at least 0.2MHz (TBC).	IFSI
DPU-DES-17	Clock and TX_DAT shall be generated by DPU and distributed to all subsystems.	AD6 Sect. 4.2, 4.5
DPU-DES-18	RX_DAT lines, coming from each subsystem, shall be multiplexed in the DPU.	AD6 Sect. 4.2
DPU-DES-19	For internal reading of analogue signals an A/D converter (12 bit) plus MPX (8 Channels) shall be provided in order to digitise the information of an internally conditioned thermistor and of the DC/DC converter voltages and total DPU current.	IFSI
	High speed interface design	
DPU-DES-20	Three fast (1 MHz clock, TBC) synchronous serial input interfaces shall be provided, each of which with 8 KW 32 Bit FIFO. The clock, gate and data signals, coming from the subsystems, are as in Figure 2-8. All data can be received by the DPU at the same time.	AD6 Sect. 4.3
	DC/DC Converter design	

DPU-DES-21	The DC/DC converter board shall have the following main characteristics: - input DC voltage ranging from 26 to 30 V (TBC), nominal is 28 V within 1%(TBC);	AD2 sect. 5.9.5.2
DPU-DES-22	- max power to the DPU: 15W *Note by IFSI: the actual estimate of the DPU HW manufacturer is 24±6W*	AD3 sect. 5.9.3
DPU-DES-23	- efficiency of 70% or better;	IFSI
DPU-DES-24	- input filter with EMI-EMC properties (following ESA EMC/EMI specs);	IFSI
DPU-DES-25	- overall characteristics in agreement with FIRST IID-A (inrush current etc.).	AD2 sect. 5.9.5.6
DPU-DES-26	The DC/DC converter will switch at a frequency signal of 131 kHz + - 10%..	AD2 sect. 5.9.5.7
	Spacecraft interface design	
DPU-DES-30	The spacecraft interface board shall be compliant with the MIL-STD-1553B standard.	AD3 sect. 5.11.5 AD2 sect. 5.11.6
	Overall mechanical design	
DPU-DES-31	The total HSDPU mass shall be less than 10 Kg.	AD3 sect. 5.5
DPU-DES-32	The HSDPU dimensions shall be 274x258x194 mm^3	AD3 sect. 5.5 AD6 Sect. 3.1
DPU-DES-33	The maximum shock to be sustained in any direction is 5g (TBC).	AD3 sect. 5.15.3.1

4.4.2 Design rules

Requirement ID	Description	Reference
DPU-DES-34	The boards dimensions should preferably be of «double Europe» standard.	
DPU-DES-35	All DPU boards shall carry Rad Tolerant memories and components: - AVM: commercial grade components required; - QM: at least MIL-C level to match Fit, Form and Functions of the FM/FS units; printed boards artwork shall be the same as FM/FS. PFM and FS: SCC level B .	
DPU-DES-36	External connectors characteristics and mounting shall be compliant with AD2 indications.	AD2 sect. 5.10.1

4.4.3 Manufacture Requirements

Requirement ID	Description	Reference
DPU-DES-37	All the pertinent ESA recommendations for boards manufacturing shall be applied.	IFSI

4.5 Logistic Requirements

Normal laboratory conditions will be suitable for the ICU as the FM unit will be enclosed in a suitable box with an aluminum plate and it will be possible to have access to the box connectors through appropriate windows. A clean room of at least class 100000 is the preferred environment (see AD3 section 5.15.3.1). Precautions have to be taken in order to avoid ESD damages.

4.6 Environment Requirements

See section 4.5.

4.6.1 Natural environment

See section 4.3 for the in-orbit operating temperatures of the DPU.
See section 4.5 for the storage environment.
Radiation environment: described in AD5.

4.6.2 Operating Environment

See sections 4.3 and 4.6.1 above.

4.7 Verification Requirements

4.7.1 DPU Acceptance And Qualification

According to AD1, section 2.5, the SPIRE instrument will be qualified at unit level (i.e. the Warm electronics units and the cold FPU units).
Adopting the assumptions listed in section 3.3 of AD1, the DPU will undergo the following tests:

Test:	DPU AVM	DPU EQM	DPU PFM	DPU FS
Functional Test	X	X	X	X (note2)
Performance Test	X	X	X	X (note2)
Interface Drawing Verification	X *	X	X	NA
Electrical Interface Tests	X	X	X	NA
Vibrations Tests	NA	Q	A	NA
Thermal-.Vacuum Test	NA	Q	A	NA
Radiation tolerance	NA	NA	note 1	note 1
EMI / EMC	NA	Q (note 3)	Partly (TBD)	NA
ESD	NA	X	NA	NA

Table 4-1 : Test matrix for the HSDPU. Q indicates a test carried out at qualification level for qualification times; A indicates a test carried out at acceptance level. An X indicates that this test is carried out and is a characterisation type test or the level is irrelevant. NA indicates that no test will be done on this model/unit. Instrument level Qualification

Items that will be in the Interface Drawing:
- Box dimensions and envelope.
- Mass; Moment of Inertia; Centre of Gravity (*NA for AVM).
- Feet and connector positions..
- Flatness of the mounting surface.
- Box and connectors identification.
- Connector definition.
- Box surface treatment including α and ε values (*NA for AVM).

Note 1: Radiation is included in EEE component selection and S/C sector analysis.
Note 2: Tests on PCB level only.
Note 3: Meaningful EMI/EMC tests should be carried out with subsystems or subsystems simulators.

Requirement ID	Description	Reference
DPU-VER-01	To carry out the tests on the HSDPU QM listed in .	IRD-VER-R02
DPU-VER-02	To carry out the tests on the HSDPU PFM listed in .	IRD-VER-R03
DPU-VER-03	To carry out the tests on the HSDPU FS listed in .	IRD-VER-R03

APPENDIX 1: QUALIFICATION TESTS DESCRIPTION

Vibration:	The QM DPU will be vibrated at levels appropriate to its location within the instrument, as defined in AD2.
Thermal-Vacuum cycle:	The DPU will undergo thermal vacuum tests. The number of cycles and the temperatures are defined in AD2.
Lifetime:	NA.
Soak/cycle:	The soak test will be part of the TV test, soak times are defined in AD2.
Radiation tolerance:	All DPU components will be radiation tolerant. A suitable analysis will show that the total dose will not exceed 10 kRad end of life.
Thermal range:	The applicable thermal ranges will be reached during the TV test.
Thermal stability:	NA
Microphonics:	NA
Ionising radiation:	See radiation tolerance above.
EMI:	The sensitivity of the DPU to electromagnetic interference will be characterised.
EMC:	The radiated and conducted electromagnetic emission of a the DPU will be characterised.
Materials conformance:	All materials used in the manufacture of the DPU will be approved for space use by ESA