DPU/DRCU
ELECTRICAL INTERFACE CONTROL DOCUMENT

	Name and Function	Date	Signature
Prepared by :	C.CARA	21/06/00	
Verified by :			
Approved by :			

Document change record

Issue/Revision	Date	Modified pages
0.1	18/05/00	All : document creation
0.2	21/06/00	§1.1 : reference documents table inserted §1.3 : Figure corrected §1.4.1 : Table 1.4.1-a updated §1.5.1 : parity suppressed §1.5.2 : parity suppressed §2.5.1 : Figures updated §2.5.2 : Figures/Table added §2.5.3 : Figure added

Distribution list

Jean-Louis AUGUÈRES	CEA	
Frederic PINSARD	CEA	
Ken KING	RAL	
Bruce SWINYARD	RAL	
Colin CUNNINGHAM	ROE	
Didier FERRAND	LAM	
Dominique POULIQUEN	LAM	
Patrick LEVACHER	LAM	
Jamie BOCK	JPL	
Jerry LILIENTHAL	JPL	
ESA SPIRE Team	ESA	
Riccardo CERULLI	IFSI	
Renato ORFEI	IFSI	
Goran OLOFSSON	SO	
Hans-Gustav FLOREN	SO	

List of Acronyms

BSM	Beam Steering Mirror
DCE	Detector Control Electronics
DCU	Detector Control Unit
DPU	Data Processing Unit
DRCU	Detector Readout & Control Unit
LIA	Lock-in amplifier
LSB	Less Significant Bit
MCE	Mechanisms Control Electronics
MCU	Mechanisms Control Unit
MSB	Most Significant Bit
SCE	Sub-system Control Electronics
SCU	Sub-system Control Unit
SMEC	Spectrometer Mechanism Control
SMPS	Switch Mode Power Supply
WIH	Warm Interconnect Harnesses

Table of Contents

1. Command Interface

1.1. Reference Documents

RD1	Note IFSI : "DPU/DRCU Interfaces"	SP-RCI-18.5.00

1.2. General Information

The command interface goal is manifold:

- Passing of commands from the DPU to the DRCU subsystems.
- Setting of DRCU Subsystems parameters.
- DRCU Subsystems synchronisation.

It consist in 3 sets of bi-directional links between the DPU and the DRCU (one link per DRCU subsystem) used with a master-slave protocol, the DPU being the master.

It allows to operate independently the 3 DRCU sub-units (DRE, MCE and SCE).

All commands being sent simultaneously to the 3 DRCU subsystems. Dedicated subsystem commands have to be sent in sequence. A broadcast code allows to send the same (broadcast) command simultaneously to the 3 DRCU sub-units.

The command format is fix. It consists in a 32 bit word with 3 fields :

- a DRCU sub-unit address field.
- a command identifier field.
- a parameter field.

DRCU subsystems, if addressed individually replies with an acknowledgement word with the following format:

- a field echoing the sub-unit address and the command identifier field.
- a data field which contains, either the echo of the command parameter field, or a data requested by the command.

In the case of broadcast command, no acknowledgement is sent back by the DRCU subsystems. If the DPU requires acknowledgement it has to be carried out by sending successive acknowledgement request (specific command) to the DRCU sub-units.

1.3. Interface Overall Diagrams

The Command Interface diagram is given in figure 1.2-a. Prime and Redundant interfaces are shown.

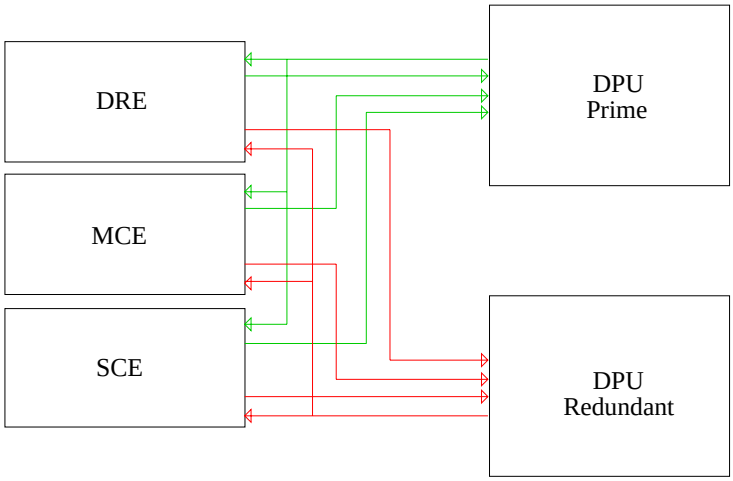


Figure 1.2-a

1.4. Interface Circuit

Each interface is defined by the following signals :

- a command (CMD) line – from DPU to DRE, MCE, SCE sub-units
- a command verification (ACK) line – from each sub-unit to DPU
- a clock (CLK) line for bit synchronisation – from the DPU to DRE, MCE, SCE sub-units.

The interface is a synchronous bi-directional serial link based on two data lines (CMD & ACK) associated to a clock line (CLK) for bit synchronisation.
Each sub-unit implements a complete set of the interface signals : that is the DPU implements 3 electrically independent “Data Interfaces” each having 2 transmitters + 1 receiver.

The interface implements the balanced lines RS422 electrical standard based on 26C31 and 26C32 transmitter and receiver type.
Complete interface functional diagram is given figure 1.3-a.

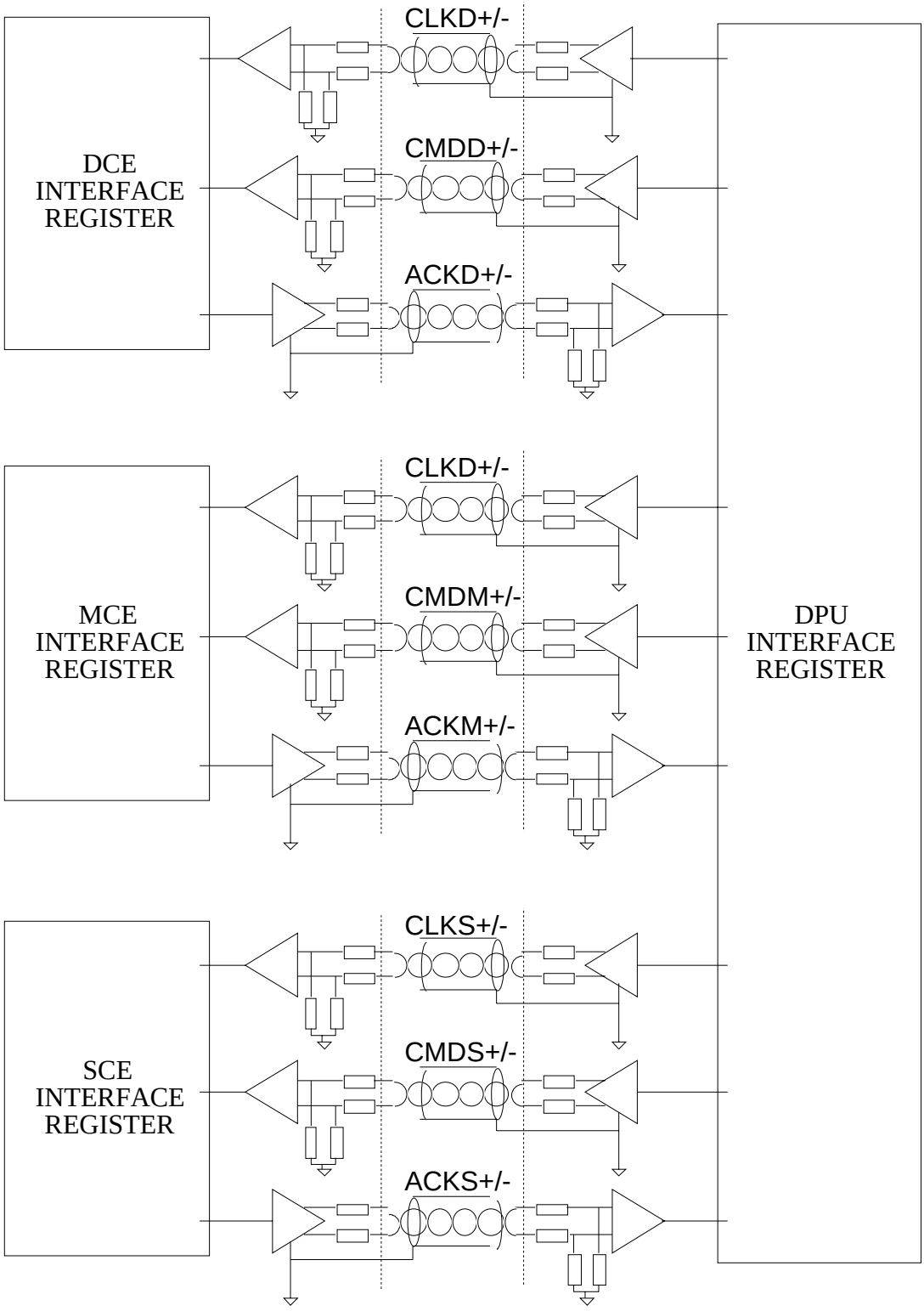


Figure 1.3-a

1.5. Word definition

1.5.1. Command

At any time the DPU can send command words to the DRCU subsystems on the interface CMD line.

The 32-bit command word is divided into 5 fields as defined bellow :

- a 2-bit sync pattern : see table 1.4.1-a for details
- a 2-bit sub-unit address : see table 1.4.1-b for details
- a 8-bit command or command + parameter address : see table 1.4.1-c for details
- a 20-bit parameter when applicable*

* : filled with zero if the command does not require any parameter.

This 5 fields are concatenated as follow to form the 32-bits word :

SYN1-SYN0	SSA1-SSA0	CID7 to CID0	PAR19 to PAR0

Figure 1.4.1-a – Command Word Field Structure

SYN1 - SYN0 : sync. pattern
SSA1 - SSA0 : subsystem address
CID7 to CID0 : command identifier
PAR19 to PAR0 : command parameter

*: filled with zero if no used

Note : • MSB is transmitted first
• SYN1 = MSB
• PAR0 = LSB

SYN1	SYN0	Ack.
1	0	Yes
1	1	No

Table 1.4.1-a – Sync Pattern definition

SSA1	SSA0	Subsystem Name
0	0	DRE
0	1	MCE
1	0	SCE
1	1	*Broadcast Command*

Table 1.4.1-b - Subsystem address allocation

CID7	CID6 to CID0
0	command code (0 of 127)
1	parameter address (0 of 127)

Table 1.4.1-c – Command Identifier Structure

1.5.2. Command Acknowledge

An acknowledge line is included in the command interface to enable command verification (when required) by the DPU. The positive acknowledgement may be required for further command transfer after specific critical commands.
When a command is received the subsystem responds to the DPU by transferring a command acknowledge word on the “ACK” interface line.

The 32-bit command word is divided into 5 fields which are :

- a 2-bit sync pattern (SYN0 & SYN1)
- a 2-bit subsystem address (SSA0 & SSA1)
- a 8-bit command or parameter address (CID7 to CID0)
- a 20-bit parameter (PAR19 to PAR0) / negative acknowledge code

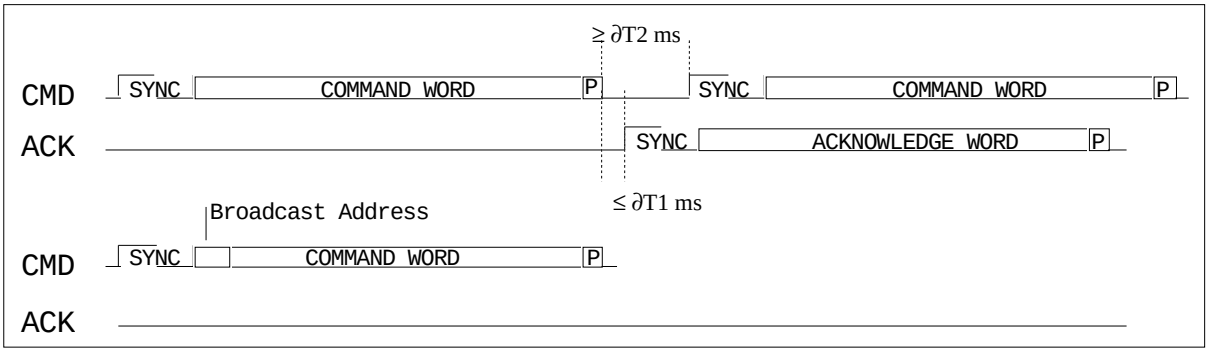
This acknowledge word is nothing else than a echo of the received command in the case of a parameter upload. In the case of a command without parameter the remaining 20-bit field is filled with subsystem status word.
If the subsystem address corresponds to the broadcast address the subsystems does not generate this acknowledge word to avoid collision at the DPU side.

A “negative” acknowledge (specific parameter filed) may result from the following reasons :

- DRCU or DRCU subsystem is off
- A transmission error occurred : receiver does not recognise command identifier
- …

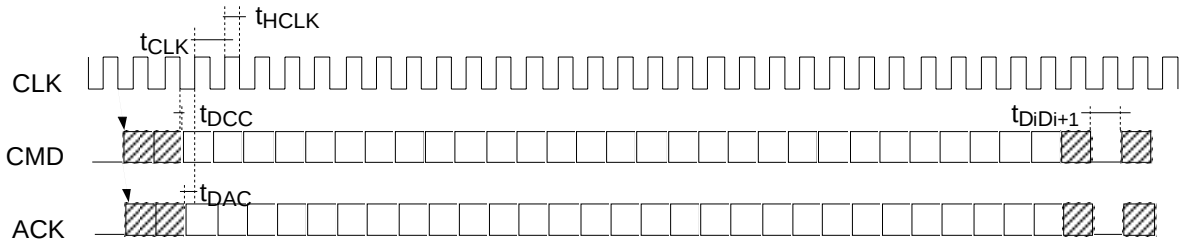
1.6. Protocol

The following figure illustrates the command interface protocol.



1.7. Interface Timing

The interface timing diagram is shown figure 1.6-a



Parameters	Symbol	Limits		Units
		Min	Max	
Clock Period	t_{CLK}	4.95	5.05	µs
Clock High Level	t_{HCLK}	$1/2t_{CLK}$- TBD	$1/2t_{CLK}$+ TBD	µs
Delay Clock Falling Edge & Data Valid	t_{DCC}	-	TBD	µs
Delay between Ack Valid &	t_{DAC}	TBD	-	µs

Clock Falling edge				
Delay between End of Data i and Beginning of Data i+1	t_{DAC}	t_{CLK}	-	µs

Note : CLK is continuously sent

1.8. Timing Performance

The NRZ data rate is fixed at 200 kbit per second.
The command rate including both command word transmission and command acknowledge word transmission is :

Max. command rate = 1 / (5 µs x 32 + ∂T2) ≤ 6250 commands per second.

This value gives the maximum command rate supported by the protocol. Real rate will have to take into account the DPU software performance.

1.9. Command list

1.9.1. DCE command list

TBW

1.9.2. MCE command list

TBW

1.9.3. SCE command list

TBW

2. Data Interface

2.1. General Information

The Data Interface is dedicated to data transfer from subsystem to DPU. Three independent "Data Interface" are required since simultaneous data transfer can occur.
This interface is unidirectional : data are transferred from the DRCU sub-units to the DPU acquisition electronics. Fixed data packet are defined according to sub-unit operating mode.
This data packet contents both scientific data (i.e. bolometer signal) and/or housekeeping parameters.
This implies nominally the housekeeping parameters are sampled at the same rate than the bolometer signal in case of the DCE sub-unit.

2.2. Overall Interface Diagram

The Command Interface diagram is given in figure 2.2. Prime and Redundant interfaces are shown.

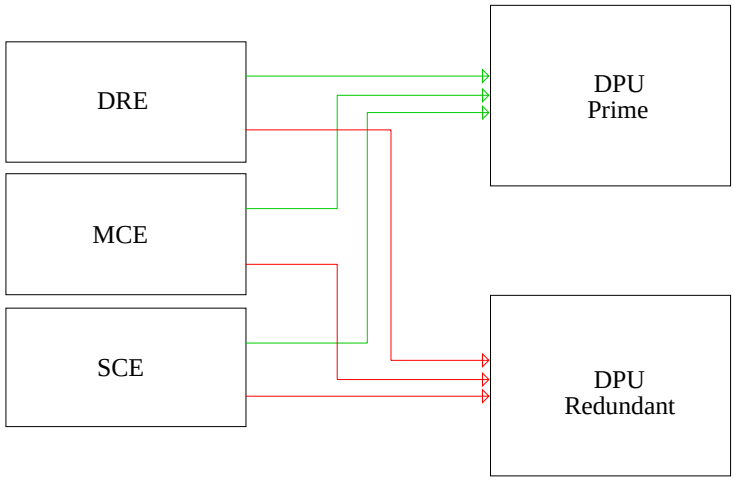
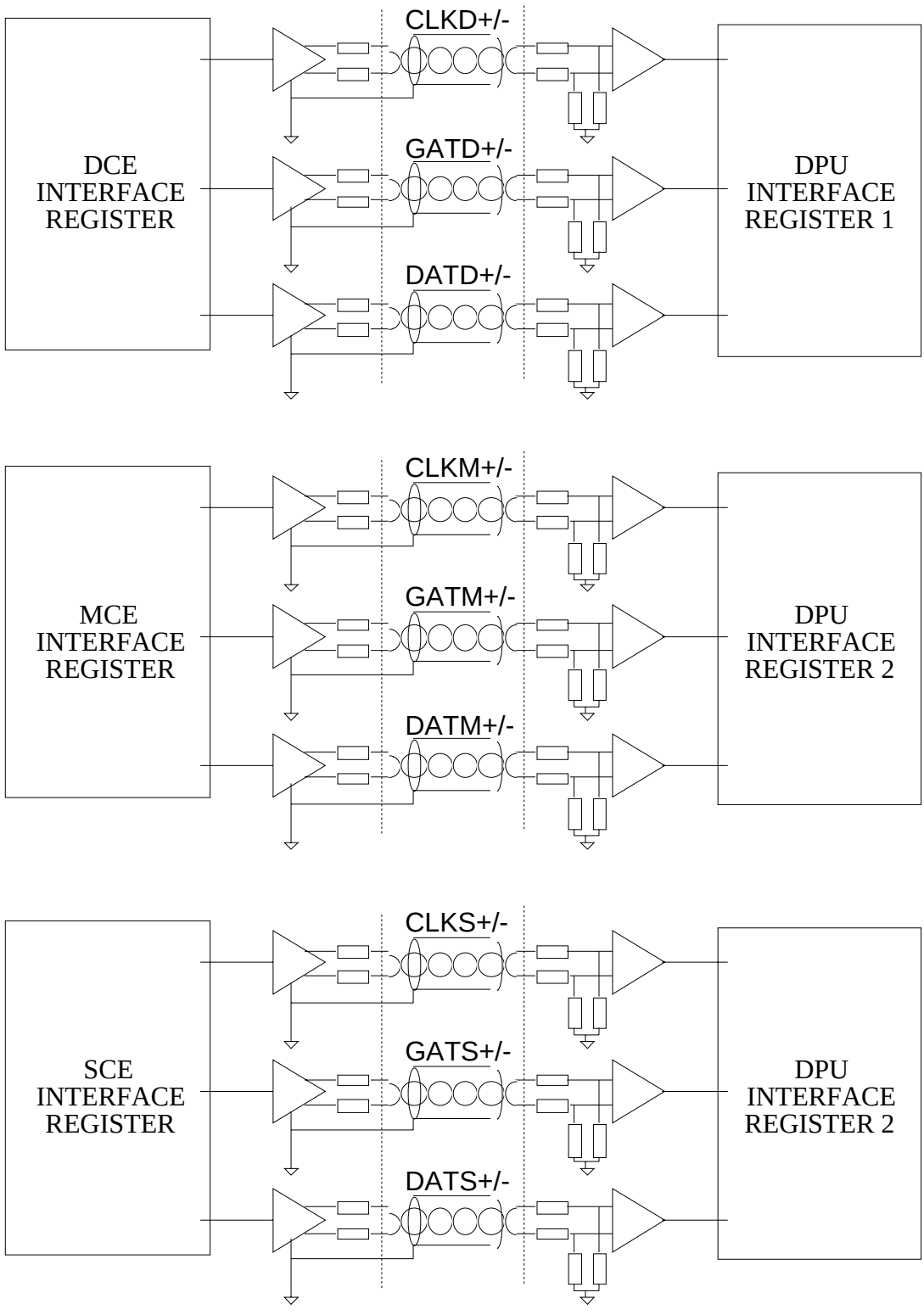


Figure 2.2-a

2.3. Interface Circuit

Each interface is defined by a data line (DTA) a gate line (GAT) and a clock line (CLK).
The interface is a synchronous serial link based on one data line (DTA) associated to a clock line (CLK) for bit synchronisation and a gate line (GAT) for word synchronisation.
Each sub-unit implements a complete set of signals : that is the DPU implements 3 totally independent Data Interfaces each having 3 receivers.

The interface will implement the balanced line RS422 electrical standard based on 26C31 and 26C32 transmitter and receiver type respectively.



2.4. Word definition

Word definition is subsystem dependent. Data are currently 16-bit coded and correspond to bolometer signal, mechanisms motion parameters, instrument temperature and all other housekeeping channels.
In order to deal with the latch-up effect of the analogue to digital converters (see RDxx) which cause the generation of wrong data until the converter recovers full performances, a specific “invalid” data identifier is defined. This avoids the DRCU transfer unpredictable packet length following a cosmic ray impact on the converter and later on-ground misanalysis.

This data words are defined as follow :

DAT15 to DAT0

Figure 2.4-a – Data Word Definition

DAT15 to DAT0 : data

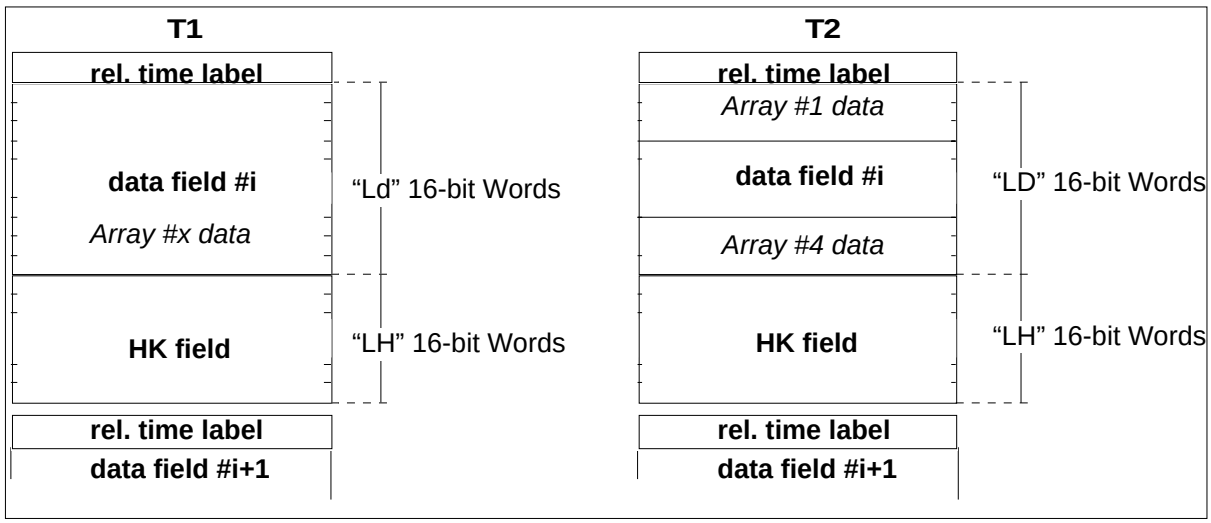
Note : • MSB (DAT15) is transmitted first
• Invalid data : [DAT15:DAT0] = FFFF hexa (TBC)

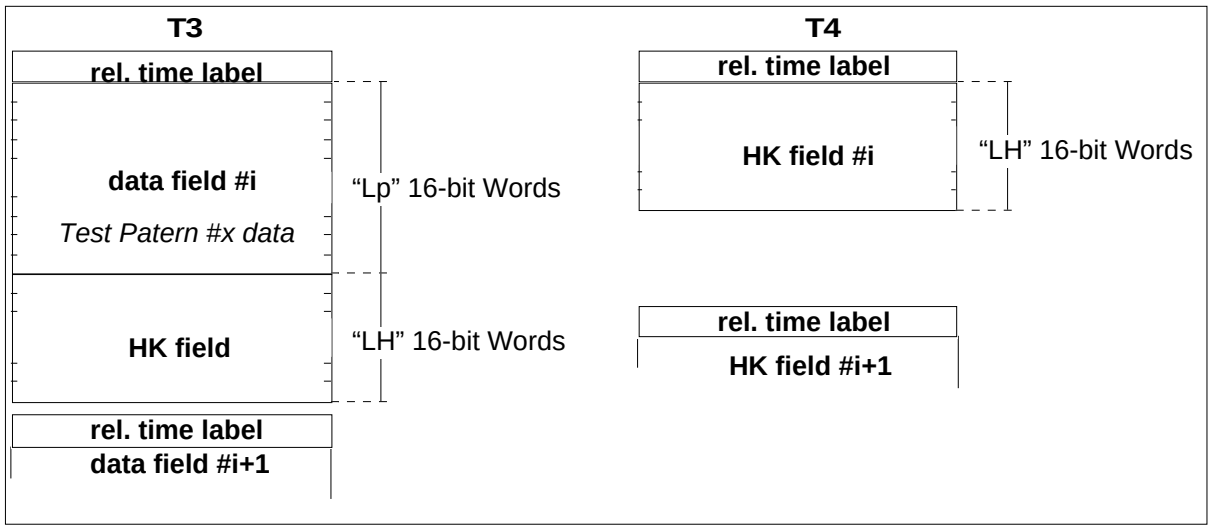
2.5. Packet Definition

Data packet length and structure are defined regarding the DRCU sub-unit and its mode of operation. Since the mode of operation is requested via its command interface the DPU knows the packet length and structure it will have to grab and to process and no packet size parameter is included in the packet definition.

2.5.1. DCE Packet Definition

The packet structures are defined as follow :

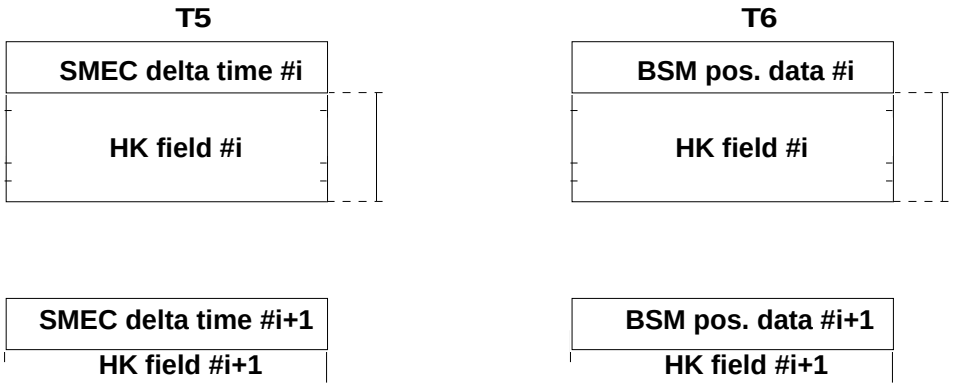




The following cross table shows the corresponding Packet Structure Type for each DCE mode of operation :

Mode of Operation	PST
Photo. Array Subset	T1
Spectro. Array Subset	T1
Photo. Full Array	T2
Spectro. Full Array	T2
Test Pattern	T3
HK Only	T4

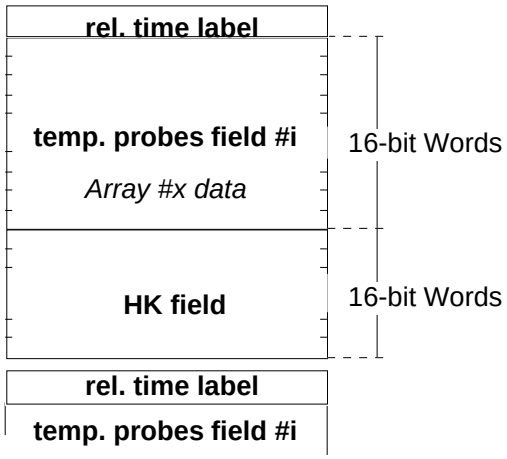
2.5.2. MCE Packet Definition



The following cross table shows the corresponding Packet Structure Type for each MCE mode of operation :

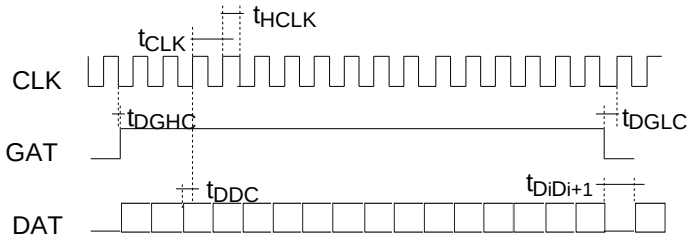
Mode of Operation	PST
Photometer	T6
Spectrometer	T5

2.5.3. SCE Packet Definition



2.6. Interface Timing

The interface timing diagram is shown figure 2.6-a



Parameters	Symbol	Limits		Units
		Min	Max	
Clock Period	t_{CLK}	0.99	1.01	µs
Clock High Level	t_{HCLK}	$1/2t_{CLK}$- TBD	$1/2t_{CLK}$+ TBD	µs
Delay Clock Falling Edge to Gate High	T_{DGHC}	-	TBD	µs
Delay Data Valid to Clock rising edge	T_{DDC}	TBD	-	µs
Delay End of Data i to Beginning of Data i+1	t_{DAC}	t_{CLK}	-	µs

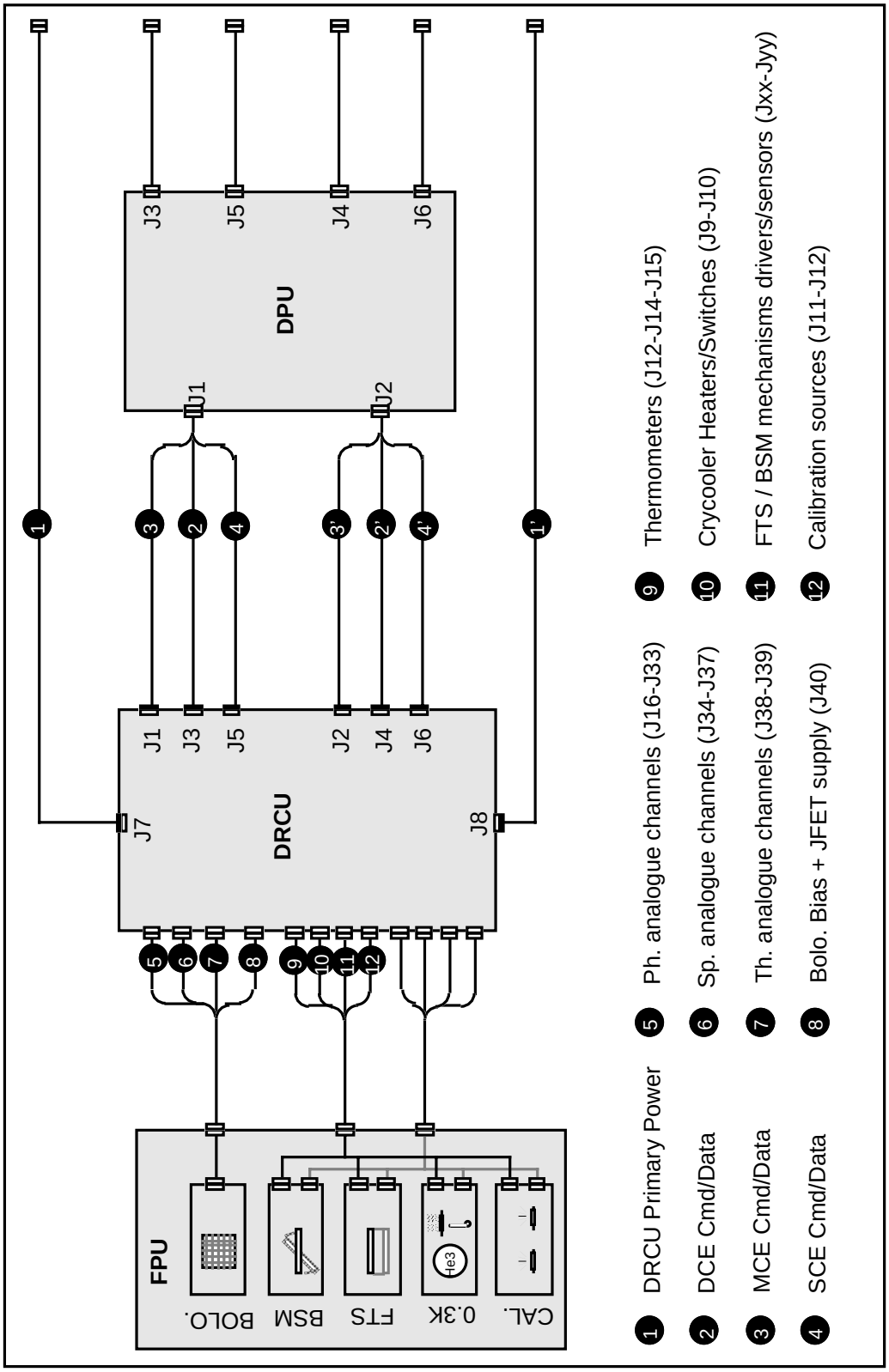
Note : CLK is continuously sent

2.7. Timing Performance

The NRZ data rate is fixed at 1 Mbit per second.

Max data rate = 1 / (1 µs x (16+1)) = 58,823 data per second

3. Connectors and Harness Definition



3.1. Connectors Description

Unit : DRCU
Sub-unit : DCE
Connector Identifier : J01
Connector Type : DBMA25S
Connector Name : DCE_P_J01

J01						
Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_DCE_P+		AWG26	DPU	J01	
3	CMD_DCE_P+		AWG26	DPU	J01	
4	ACK_DCE_P+		AWG26	DPU	J01	
5	ACK_SHD					
6						
7						
8	CLK_DCE_P+		AWG26	DPU	J01	
9	CLK_SHD					
10	DAT_DCE_P+		AWG26	DPU	J01	
11	GAT_DCE_P+		AWG26	DPU	J01	
12	GAT_SHD					
13	-					
14						
15	CLK_DCE_P-		AWG26	DPU	J01	
16	CMD_DCE_P-		AWG26	DPU	J01	
17	ACK_DCE_P-		AWG26	DPU	J01	
18						
19						
20						
21	CLK_DCE_P-		AWG26	DPU	J01	
22	DAT_DCE_P-		AWG26	DPU	J01	
23	DAT_SHD					
24	ACK_DCE_P-		AWG26	DPU	J01	
25	-					

Sub-unit : MCE
Connector Identifier : J03
Connector Type : DBMA25S
Connector Name : MCE_P_J03

J03						
Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_MCE_P+		AWG26	DPU	J01	
3	CMD_MCE_P+		AWG26	DPU	J01	
4	ACK_MCE_R+		AWG26	DPU	J01	
5	ACK_SHD					
6						
7						
8	CLK_MCE_P+		AWG26	DPU	J01	
9	CLK_SHD					
10	DAT_MCE_P+		AWG26	DPU	J01	
11	GAT_MCE_P+		AWG26	DPU	J01	
12	GAT_SHD					
13	-					
14						
15	CLK_MCE_P-		AWG26	DPU	J01	
16	CMD_MCE_P-		AWG26	DPU	J01	
17	ACK_MCE_P-		AWG26	DPU	J01	
18						
19						
20						
21	CLK_MCE_P-		AWG26	DPU	J01	
22	DAT_MCE_P-		AWG26	DPU	J01	
23	DAT_SHD					
24	ACK_MCE_P-		AWG26	DPU	J01	
25	-					

Unit : DRCU
Sub-unit : SCE

Connector Identifier : J05
Connector Type : DBMA25S
Connector Name : SCE_P_J05

J05						
Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_SCE_P+		AWG26	DPU	J01	
3	CMD_SCE_P+		AWG26	DPU	J01	
4	ACK_SCE_P+		AWG26	DPU	J01	
5	ACK_SHD					
6						
7						
8	CLK_SCE_P+		AWG26	DPU	J01	
9	CLK_SHD					
10	DAT_SCE_P+		AWG26	DPU	J01	
11	GAT_SCE_P+		AWG26	DPU	J01	
12	GAT_SHD					
13	-					
14						
15	CLK_SCE_P-		AWG26	DPU	J01	
16	CMD_SCE_P-		AWG26	DPU	J01	
17	ACK_SCE_P-		AWG26	DPU	J01	
18						
19						
20						
21	CLK_SCE_P-		AWG26	DPU	J01	
22	DAT_SCE_P-		AWG26	DPU	J01	
23	DAT_SHD					
24	ACK_SCE_P-		AWG26	DPU	J01	
25	-					

Unit : DRCU
Sub-unit : DCE
Connector Identifier : J02

Connector Type : DBMA25S
Connector Name : DCE_R_J02

J02						
Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_DCE_R+		AWG26	DPU	J01	
3	CMD_DCE_R+		AWG26	DPU	J01	
4	ACK_DCE_R+		AWG26	DPU	J01	
5	ACK_SHD					
6						
7						
8	CLK_DCE_R+		AWG26	DPU	J01	
9	CLK_SHD					
10	DAT_DCE_R+		AWG26	DPU	J01	
11	GAT_DCE_R+		AWG26	DPU	J01	
12	GAT_SHD					
13	-					
14						
15	CLK_DCE_R-		AWG26	DPU	J01	
16	CMD_DCE_R-		AWG26	DPU	J01	
17	ACK_DCE_R-		AWG26	DPU	J01	
18						
19						
20						
21	CLK_DCE_R-		AWG26	DPU	J01	
22	DAT_DCE_R-		AWG26	DPU	J01	
23	DAT_SHD					
24	ACK_DCE_R-		AWG26	DPU	J01	
25	-					

Unit : DRCU
Sub-unit : MCE
Connector Identifier : J04
Connector Type : DBMA25S

Connector Name : MCE_R_J04

J04						
Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_MCE_R+		AWG26	DPU	J01	
3	CMD_MCE_R+		AWG26	DPU	J01	
4	ACK_MCE_R+		AWG26	DPU	J01	
5	ACK_SHD					
6						
7						
8	CLK_MCE_R+		AWG26	DPU	J01	
9	CLK_SHD					
10	DAT_MCE_R+		AWG26	DPU	J01	
11	GAT_MCE_R+		AWG26	DPU	J01	
12	GAT_SHD					
13	-					
14						
15	CLK_MCE_R+		AWG26	DPU	J01	
16	CMD_MCE_R+		AWG26	DPU	J01	
17	ACK_MCE_R+		AWG26	DPU	J01	
18						
19						
20						
21	CLK_MCE_R-		AWG26	DPU	J01	
22	DAT_MCE_R-		AWG26	DPU	J01	
23	DAT_SHD					
24	ACK_MCE_R-		AWG26	DPU	J01	
25	-					

Unit : DRCU
Sub-unit : SCE
Connector Identifier : J06
Connector Type : DBMA25S
Connector Name : SCE_R_J06

J06						
Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1						
2	CLK_SCE_R+		AWG26	DPU	J01	
3	CMD_SCE_R+		AWG26	DPU	J01	
4	ACK_SCE_R+		AWG26	DPU	J01	
5	ACK_SHD					
6						
7						
8	CLK_SCE_R+		AWG26	DPU	J01	
9	CLK_SHD					
10	DAT_SCE_R+		AWG26	DPU	J01	
11	GAT_SCE_R+		AWG26	DPU	J01	
12	GAT_SHD					
13	-					
14						
15	CLK_SCE_R-		AWG26	DPU	J01	
16	CMD_SCE_R-		AWG26	DPU	J01	
17	ACK_SCE_R-		AWG26	DPU	J01	
18						
19						
20						
21	CLK_SCE_R-		AWG26	DPU	J01	
22	DAT_SCE_R-		AWG26	DPU	J01	
23	DAT_SHD					
24	ACK_SCE_R-		AWG26	DPU	J01	
25	-					

Unit : DRCU
Sub-unit : SCE
Connector Identifier : J07
Connector Type : DBMA9P
Connector Name : PWR_P_J07

J07						
Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	PWR_DRCU_28V_P		AWG20	PDU	J0x	
2	PWR_DRCU_28V_P		AWG20	PDU	J0x	
3						
4	PWR_SYNC_P		AWG26	PDU	J0x	
5						
6	PWR_DRCU_RTN_P		AWG20	PDU	J0x	
7	PWR_DRCU_RTN_P		AWG20	PDU	J0x	
8						
9	PWR_SYNC_RTN_P		AWG26	PDU	J0x	

Unit : DRCU
Sub-unit : SCE
Connector Identifier : J08
Connector Type : DBMA9P
Connector Name : PWR_R_J08

J08						
Pin #	Signal Name	EMC Class	Wire	Connected to		
				Unit	Connector	Pin
1	PWR_DRCU_28V_R		AWG20	PDU	J0x	
2	PWR_DRCU_28V_R		AWG20	PDU	J0x	
3						
4	PWR_SYNC_R		AWG26	PDU	J0x	
5						
6	PWR_DRCU_RTN_R		AWG20	PDU	J0x	
7	PWR_DRCU_RTN_R		AWG20	PDU	J0x	
8						
9	PWR_SYNC_RTN_R		AWG26	PDU	J0x	