Minutes of LAM/ATC meeting 15th/16th May 16, 2000

Ian Pain/ Colin Cunningham May 23, 2000

V1.0

Present:

Dominique Pouliquen, Didier Ferrand, Patrick Lavacher, Michel Jevaud
Armand Artinian, Jean-Paul Baluteau, Pascal Dargent (LAM)

Colin Cunningham, Ian Pain (ATC)

Agreements

1) **Architecture**.
   1.1) BSM & SMEC architecture should have a consistent design philosophy regarding parallel redundancy. In the same way that the SMEC is built on two separate " ½ SMEC" boards, two separate " ½ BSM" boards would be implied. This is a **CHANGE** from the previous design assumption and is now considered the baseline BSM architecture. Note:
      (a) The reason this architecture is required, is that if not adopted, then each MAC board must connect to the same BSM, with additional switching to ensure that only 1 MAC board provides instruction and power. This switching is undesirable for reasons of complexity, reduced reliability and the linking of the two independent DSP/MAC/SMEC to a common part.
      (b) Concerns remain in that this architecture requires the ability to provide two separate motor coils. This may be challenging (low power, manufacture).
   1.2) The ½ BSM & ½ SMEC cards may be physically combined or separate as appropriate (depending on size and interface preferences).
   1.3) The baseline is that the MAC will provide power for BMS analogue board

2) **Interface**.
   Interface specification:
   - Position sensors to MAC A/D converters : 12 bits , +- 5V, 15 µs conversion. **TBC**
   - Motor demand MAC D/A output: 16 bits, +- 5V, 10 µs conversion. **TBC**
   - Motor current: (It is not clear why we need this information – the MAC can provide it. Motor voltage would be more useful) **TBD**

3) **Telemetry**.
   The MAC will monitor motor voltage for back emf damping in open loop control – one channel per axis. This will allow a backup mode in the event of position sensor failure where at least vibration damping will be available, even if position is open-loop. We need to decide what needs to be telemetered for diagnostic purposes, and what is needed for processing of bolometer signals, for instance what sampling rate is needed when chopping to allow for synchronisation of chop position and bolometer signal with negligible phase noise.

4) **Position control/Modes.**
   The baseline control mode for BSM sky positions will be by the provision of trajectory variables, which subsequent checks confirm is no change to the current control systems design. Point-by point movements can be commanded, but the trajectory taken between points will be determined by parameters which are set by commands.

   4.1) For engineering purposes, a high resolution step response will be available via DSP FIFO (i.e. The transient settling phenomena of the BSM will be accessible at high resolution to allow control loop tuning to be performed in microgravity).

4.2) Only low time resolution position telemetry will be provided (<100 Hz? **TBD**) in science modes.

5) **Integration**

LAM is responsible for verification of the translation of DSpace to 21020 (demonstrate by 31st Oct)

Actions

1. Control
   1.1. ATC to list all the necessary parameters to define the BSM trajectory & control algorithm
   1.2. ATC to fill out the list of tasks to be done by the DSP & estimated time for BSM control
   1.3. ATC to provide the BSM control loop frequency
   1.4. ATC to sort out the BSM control unit: DPU or MCU?
2. Modes & Telemetry
   2.1. ATC define BSM engineering & science telemetry modes.
   2.2. ATC to list the BSM modes, nominal & backup, and the associated commands required.
   2.3. ATC to list BSM H/K data & telemetry, and assess the need for separate FPGA to control BSM telemetry.
   2.4. ATC check need & precision for BSM motor current monitoring & specify safety actions (eg switch off controller)
3. System Engineering
   3.1. CRC to ask project to approve trajectory mode and " ½ BSM" architecture changes.
   3.2. CRC to ask project what is the need for thermometers mounted on the subsystem & going through the thermometry board (i.e. not directly usable by the subsystem for compensation etc).
4. Architecture
   4.1. ATC evaluate double wound motors for fully parallel redundancy.
   4.2. ATC evaluate Fallback plan for single board redundancy (e.g. switching motors & sensors & selecting correct MAC & PSU).
   4.3. ATC evaluate implications of baseline full parallel redundancy architecture
   4.4. LAM evaluate shared analogue SMEC/BSM board.
   4.5. LAM to incorporate any changes required to accommodate the point-by-point observing mode into design.
5. Electronics Design
   5.1. ATC evaluate LAM power amp for BSM
   (Note: 100mA max current, but can be varied by changing number of transistors)
   5.2. ATC establish required stability of current source.
   5.3. ATC confirm position sensor amplifier band-width
   5.4. ATC specify S/N of Position sensor and amplifier
   5.5. ATC specify maximum wire resistance for motor drives
   5.6. ATC define engineering synch signals, if required
   5.7. ATC check maximum series resistance of switches and wiring for launch damping.
   5.8. ATC evaluate performance of open loop with back emf damping as a reduced performance mode.
   5.9. LAM specify required position sensor precision (tentative 30 um over nominal range).
   5.10. ATC ask MPIA about provision of additional position sensors for LAM to experiment with
   5.11. ATC to complete electronic design and provide by email to Patrick (in pdf format or ORCAD 9.0 compatible file).
      (a) Block diagram
      (b) List of connections
      (c) List of components
6. Documentation
   6.1. LAM provide MCU design description, with blank headings for areas of BSM design (in one week)
   6.2. ATC supply design notes for MCU design description (within 2 weeks) blank headings.

Deliverables

BSM Simulator (Simulink)

Aim - To enable programming of 21020 'Evolution' Board

Form : Electro- Mechanical - crude, but including

- power amps, etc
- Position sensors (including all noise sources & hysteresis)
- DSP control model (V. Important): including command and all parameters (in memory), modes (incl. trajectory, open loop, point-by-point etc).
- 10ms per instruction
- Note that a z-transform coefficient model is needed, not a Laplace-transform model. The sample, trajectory & filters can be modelled and provided in z-form as well , so that LAM may directly programme the Evolution board.

Dates:

- Required for when the LAM Evolution board arrives: (Mid June +)
- ATC aim to deliver simulink model by 1st September
- 1 Month for LAM to programme & then review performance
- LAM output results 31 Oct 00 & trade-off performance

Note - need agreement from project to use trajectory control.

Real Mechanical Model > LAM

Aim:

- Prove electronic & mechanical design are OK
- Green light for development model cards.
- Used in association with SMEC development model – to show can control both & allow optimisation of control parameters

Form: 2 axis, 2 position sensors, all appropriate analogue electronics, , No redundancy.

Dates:

- Required by 15th January
- SMEC development model hardware end of June

Notes:

- No cold tests on development model at LAM (as DSPACE simulators)
- ATC/LAM to provide on-site integration support as required.

Final Analogue BSM Board Design

Aim : freeze manufacturable design

Dates:

Freeze design for manufacture in a BSM-LAM meeting by 31st March 01

CQM BSM board

Aim:

- Warm and cold tests of BSM mechanism and board
- CQM tests of both mechanisms at 20K at LAM then to RAL at 4K.

Dates:

- LAM to deliver board to ATC by 25/12/01
- RAL integration per main project plan
- Remainder of thermal cycling at LAM (begin Jan 02 – end April 15th 02)

Notes:

- ATC/LAM to provide on-site integration support as required.
- We vibrate CQM warm & cold before delivery to LAM
- All tests will be with CQM boards.
- 2 BOARDS REQUIRED:
  - MQ1 Mechanism Qualification
  - MQ2 Warm Electronics Qualification