Detector Electronics Development

The CEA/SAp is in charge of the development and the manufacturing of the warm electronics of the bolometer arrays, which are developed by Caltech/JPL. The final performance depends on the bolometers themselves, but also from the readout electronics, and how it matches with the bolometer characteristics. The interfaces are not simple. All of them are of analog type. In addition, since the bolometers, and their first amplifier stages are within a cryostat, the cryoharness and the grounding scheme of the system should be taken into account in the design phase. This development is a complex area, which will require a good cooperation of the two teams. The development plan should take into account this sharing of tasks, and ensure a clear definition of respective responsibilities.

1 The detector electronics subsystem

The detector electronics subsystem is summarized in the following block diagram. It is composed of two main subsystems: a cold detector unit and a warm electronics unit

1.1 Detector electronics cold unit

The detector electronics cold unit has several components.

1.1.1 Bolometer arrays

There are 5 bolometer arrays, 3 for the photometer, 2 for the FTS. The specifications for the bolometer arrays are described in the Instrument Requirements Documents. The bolometer arrays will be provided by Caltech/JPL. . The bolometer bias voltages, intensities, and their stabilities should be provided by the Caltech/JPL group to the CEA/Saclay

1.1.2 300 mK cryocooler

The bolometer arrays are thermally coupled to the 300 mK cryocooler through thermal straps. While the cryocooler is not part of the detector unit, the detector put requirements on the temperature stability at the end of the cryocooler finger. This has impact on the design of a temperature regulation subsystem. The temperature stability requirement is the responsibility of Caltech/JPL. The cryocoller and the cryocooler control unit, including the temperature regulation is under the responsibility of CEA/Saclay. The overall thermal concept is under the responsibility of the RAL.

1.1.3 JFET Box

The first stage of the amplification chain for the bolometers is based on JFET amplifiers. The JFET are operated at cold temperature, at proximity of the bolometers. They are enclosed in a JFET box thermally connected to the " 10 K " screen. The JFET box, and the harness between the bolometer arrays and the JFET box are under the responsibility of Caltech/JPL, and will be provided by them. The thermal coupling of the JFET box and the cryostat screen is under the responsibility of RAL. From the warm electronics point of view, the JFET box provides the formal interface between the cold unit, under the responsibility of Caltech/JPL, and the warm electronics, under the responsibility of CEA/Saclay.

1.1.4 Cryoharness

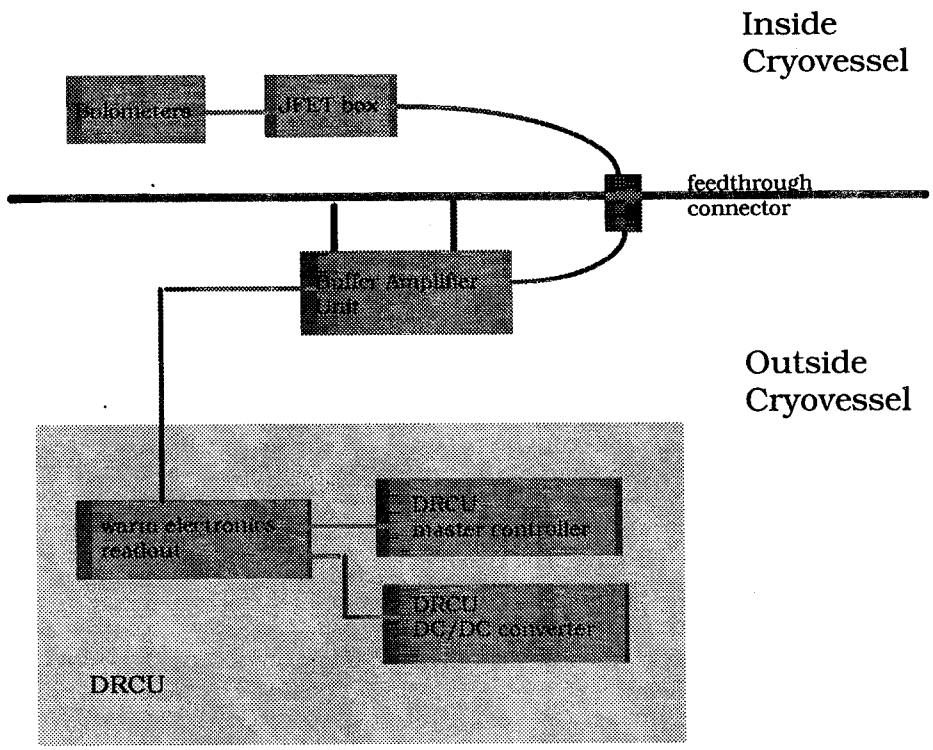
The Cryoharness will be provided by ESA. It would be wise to use the same cryoharness in the Integration and Calibration facility which will be used in RAL. The only requirements placed by the Warm Electronics is that the same harness is used inside the CEA/Saclay test cryostat and in the RAL's Integration and Calibration facility. This harness should be provided by RAL

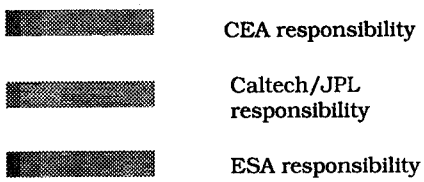
1.1.5 Feedthrough connectors

SPIRE is very demanding in term of feedthrough connectors. The specifications of these feedthrough connectors, in term of mechanical size, and number of pins are under the responsibility of ESA. In a similar way than the cryoharness, it would be wise to use the same type of connectors during the development phases of SPIRE. A joint procurement, through ESA, might be the correct approach. The feedthrough connectors for the CEA/Saclay test cryostat must be identical to the connectors that will be used in the RAL's Integration and Test Facility. They should be provided by RAL

The following table summarized the main responsibilities and the procurement origins of each of these components.

	interfaces with warm electronics	**responsibility**	**origin of procurement**
bolometers	temperature regulation controller bias voltage levels and stability	Caltech/JPL	Caltech/JPL
JFET box	output signal level and noise characteristics power supply levels, intensities, and stabilities	Caltech/JPL	Caltech/JPL
cryoharness	signal degradation induced by the cryoharness must be included in the system performance budget	ESA	ESA for FIRST RAL for tests and integration cryostats
feedthrough connectors	signal degradation induced by the feedthrough connectors must be included in the system performance budget	ESA	ESA for FIRST RAL for tests and integration cryostats





1.2 Detector electronics warm unit

The detector electronics warm unit has several components

1.2.1 Buffer Amplifier Unit

The Buffer Amplifier Unit is an amplifier and filtering unit which is located on the cryovessel. It has an operating temperature of 120 K. Each amplification channel is directly linked with a bolometer. The BAU is under the responsibility and will be procured by CEA/Saclay

1.2.2 Detector Readout Electronics

This unit is located inside the Digital Readout and Control Unit. Its main functions are to transform the analog output signal received from the BAU to a digital signal which will be send to the Master Controller of the DRCU. It provides also the bias voltages to the bolometer arrays and the power supply to the BAU. The interfaces between the Electronics Readout Unit and the Master Controller are analog power supplies, sequencer clocks, and digital signal outputs. The DRE is under the responsibility and will be procured by CEA/Saclay.

1.2.3 Harness

The harness is separated in 3 pieces. The first connect the feedthrough connectors to the BAU. The second connect the BAU to the DRE. The third one directly connect the DRE to a feedthrough connector dedicated to bias supplies for the bolometers. ESA has the responsibility of these 3 harnesses. As for the cryogenic harness, it might be useful to use the same harness type in all integration and test facilities at instrument level. The procurement of the harness of the test cryostat in CEA/Saclay should be provided by RAL, to be identical to the one which will be used in the Integration and Calibration facility in RAL.

The following table summarized the main responsibilities and the procurement origins of each of these components.

	electronics interfaces	**responsibility**	**origin of procurement**
BAU	power supply levels, intensities, and stabilities voltages, intensities, and noise characteristics of input signal	CEA/Saclay	CEA/Saclay
DRE	output signal level and noise characteristics bias voltage levels and stability power supply levels, intensities, and stabilities	CEA/Saclay	CEA/Saclay
harness	signal degradation induced by the cryoharness must be included in the system performance budget	ESA	ESA for FIRST RAL for tests and integration cryostats

2 Development plan

2.1 Model philosophy

In agreement with the general development plan of the Warm Electronics, the development plan of the Detector Readout Electronics is based on 3 phases:

2.1.1 Engineering Model.

This model is a prototype of the final design. It should be based on technology, and components, which can be used with space quality equivalent. It should be validated with a simplified bolometer array and the corresponding JFET box in a dedicated cryostat. The configuration of the array should be large enough to test collective potential problems such as cross-talk. The harnesses might be similar, but not identical to the flight harness. This phase should be performed in a joint effort between Caltech/JPL and CEA/Saclay. Most of the activities will be done in US with CEA personnel working in a team with the JPL engineers. The engineering model will be validated at JPL with a test equipment provided by JPL. This test equipment should reproduce the interfaces within the DRCU. Then the engineering model will be sent to Saclay to be integrated inside the DRCU. After integration and test, it will be delivered to RAL.

2.1.2 Qualification Model.

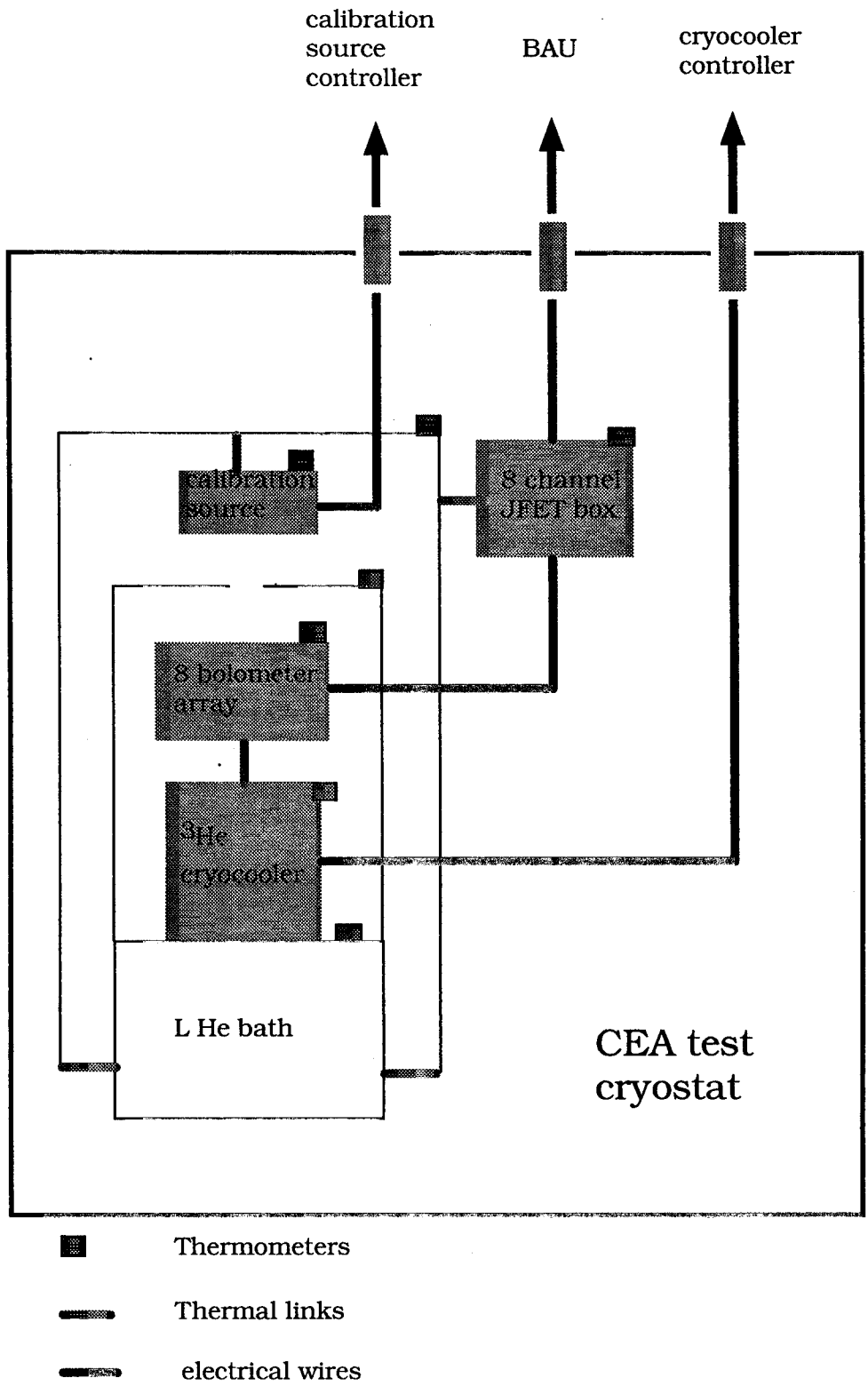
This model is a representative version of the flight model. It will be designed and manufactured in CEA/Saclay. The final acceptance test will be performed in Saclay with test equipment composed, on one side from a cryostat with at least 2 simplified bolometer arrays and their associated JFET boxes, on the other side by a acquisition and data analysis system connected on the DRCU. 2 QM will be manufactured. One will be delivered to RAL for integration in the Cryogenic Model of SPIRE. The second will remain in CEA/Saclay for a qualification with respect to thermal vacuum, EMI/EMC and vibration test.

2.1.3 Flight Model and a Spare Model.

These models are identical. They will be designed and manufactured in CEA/Saclay. Acceptance tests will be performed, before delivery to RAL, with the same equipment, which would have been used for the QM.

2.2 CNES Reviews

Four CNES reviews are planned during this development. The first review will validate the overall development plan and the detector electronics specifications. This review will have to take place before the SPIRE DDR. CNES, and CEA/DSM representatives will be members of the review panels. The success of this review is required to guarantee the CNES and CEA funding for the development of this electronics. 3 reviews, one for the EM, one for the QM and one for the FM, based on the results of the acceptance tests performed in CEA/Saclay will take place before the delivery of these models to RAL. CNES, and CEA/DSM representatives will be members of the review panels.


calibration source controller
BAU
cryocooler controller
calibration source
8 channel JFET box
8 bolometer array
3He cryocooler
L He bath
CEA test cryostat
Thermometers
Thermal links
electrical wires

2.3 Detailed description of the models

2.3.1 Engineering model

2.3.1.1 Model description

This model is composed of a prototype BAU and an DRE. Each of these subsystems is not supposed to contains all the channels which will be present on the flight units. However, they should include a number of channels large enough to studies interference between channels. The printed circuit boards, the technology used (e.g. surface mounted components) should be similar to the final design. Components should be taken within families which offer space qualified version agreed by ESA. The BAU box might be different from the final box. However, it should be compatible with cold test. The harness between the BAU and the DRE might be made with normal wires.

2.3.1.2 Development phases

In the first phase, the BAU and the DRE will be tested by using input simulators. Performances will be measured with these simulators. A dedicated acquisition system will simulate the DRCU interfaces. This phase will take place in JPL. It will be a combined effort of both Caltech/JPL and CEA/Saclay teams.

In the second phase, the BAU and the DRE will be connected to real bolometers and JFET box. Performances with the compared to the results obtained with simulators. This phase will take place in JPL. It will be a combined effort of both Caltech/JPL and CEA/Saclay teams.

In the third phase, the DRE will be integrated with the DRCU. Performances will be measured first with the simulators used in the first phase, then with bolometers and associated JFET box. This phase will take place in Saclay. It will be done by CEA/Saclay people, with a close monitoring from the Caltech/JPL team. The performance test will be done with a DRCU test equipment provided by CEA/Saclay. The bolometers and the JFET box will be set up inside the CEA Test Cryostat, which will be used to validate the functionality and the performances of the warm electronics. The detector array might be delivered in a very simplified mechanical mounting, since it will be bolt directly on he 300 mK fridge. We do not require a mechanical mount identical to the SPIRE system.

2.3.1.3 Test plan

TBW

2.3.1.4 Test equipment

- BAU and DRE input simulator
- BAU cryostat for cold test
- DRE control and acquisition equipment
- JPL test cryostat equipped with one bolometer array of at least 8 (TBC) bolometers and the associated JFET box.
- CEA Test Cryostat
- bolometer array of at least 8 bolometers (TBC) and associated JFET box

2.3.1.5 Deliverable items

2.3.1.5.1 Caltech/JPL

- BAU and DRE input simulator
- JPL test cryostat equipped with a bolometer array and its associated JFET box
- Bolometer array and associated JFET box to be delivered to CEA/Saclay for integration in the CEA test cryostat.
- Detailed description of mechanical, thermal and electrical interfaces of the bolometer array and the JFET box in the CEA Test Cryostat
- Integration procedure for the bolometer array and the JFET box in the CEA Test Cryostat
- Specifications for BAU and DRE
- Test plan for the tests in JPL
- Acceptance test report for the tests performed in JPL
- DRE control and acquisition equipment (To be discussed)

2.3.1.5.2 CEA/Saclay

- Specification for the DRE and DRCU Master Controler interfaces.
- DRCU engineering model
- DRCU test equipment
- BAU cryostat
- CEA Test Cryostat equipped with a 300 mK cryocooler.
- DRE integration procedure.
- Acceptance test report for the tests performed in Saclay.

2.3.1.5.3 RAL

- Feedthrough connectors for the CEA Test Cryostat
- Cryoharness for the CEA Test Cryostat
- System specifications
- Acceptance test procedure
- Acceptance test validation

2.3.1.6 Acceptance tests

Final acceptance tests will be performed in Saclay, according to a procedure defined by RAL, and agreed by Caltech/JPL and CEA/Saclay. Test will be conducted under the responsibility of CEA/Saclay, with Caltech/JPL and RAL people as witness.

2.3.2 Qualification model

2.3.2.1 Model description

This model is composed of a BAU and an DRE. The BAU and the DRE should be fully representative of the flight model, in term of functionality and performances. Mechanical boxes, circuit boards and thermal interfaces should be identical to the Flight Model. Component should be identical to the Flight model, except for the level of quality.

2.3.2.2 Development phases

All the development will take place in CEA/Saclay. In the first phase, the BAU and the Warm Detector Readout will be tested against simulators. In the second phase, they will be tested with actual bolometers inside the CEA Test Cryostat.

2.3.2.3 Test plan

TBW

2.3.2.4 Test equipements

- BAU and DRE input simulator
- BAU cryostat for cold test
- DRE control and acquisition equipment
- JPL test cryostat equipped with one bolometer array of at least 8 (TBC) bolometers and the associated JFET box.
- CEA Test Cryostat
- 2 bolometer arrays of at least 8 bolometers each (TBC) and associated JFET box. One of the bolometer array should have the performances required for the FTS.

2.3.2.5 Deliverable items

2.3.2.5.1 Caltech/JPL

- BAU and DRE simulator (if different from the EM)
- Bolometer arrays and associated JFET box to be delivered to CEA/Saclay for integration in the CEA test cryostat. (at least one more array compliant with FTS performances)
- Detailed description of mechanical, thermal and electrical interfaces of the bolometer array and the JFET box in the CEA Test Cryostat
- Integration procedure for the bolometer array and the JFET box in the CEA Test Cryostat

2.3.2.5.2 CEA/Saclay

- DRCU QM model
- DRCU test equipment
- CEA Test Cryostat equipped with a 300 mK cryocooler.
- Acceptance test report for the tests performed in Saclay.

2.3.2.5.3 RAL

- Additional Feedthrough connectors for the CEA Test Cryostat
- Cryoharness for the CEA Test Cryostat
- QM Acceptance test procedure
- QM Acceptance test validation

2.3.2.6 Acceptance tests

Final acceptance tests will be performed in Saclay, according to a procedure defined by RAL, and agreed by Caltech/JPL and CEA/Saclay. Test will be conducted under the responsibility of CEA/Saclay, with Caltech/JPL and RAL people as witness.

2.3.3 Flight and Spare models

2.3.3.1 Model description

This model is composed of a BAU and a Warm Detector readout Unit.

2.3.3.2 Development phases

The development phase is similar to the development phase of the QM

2.3.3.3 Test plan

TBW

2.3.3.4 Test equipements

FM will be tested with existing test equipment, which would have been validated during the QM phase

2.3.3.5 Deliverable items

2.3.3.5.1 Caltech/JPL

- None

2.3.3.5.2 CEA/Saclay

- Acceptance test report for the tests performed in Saclay.

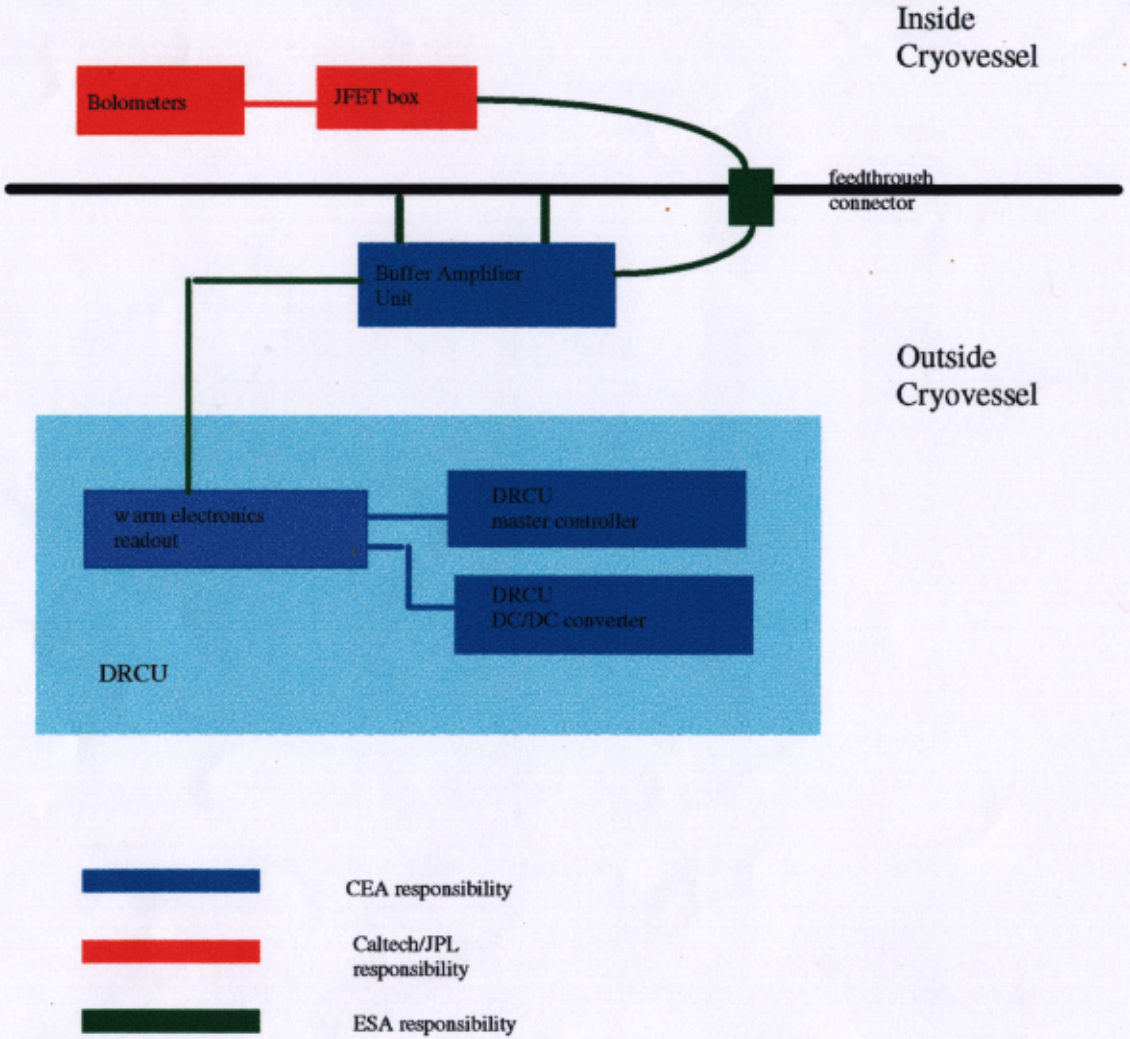
2.3.3.5.3 RAL

- FM Acceptance test procedure
- FM Acceptance test validation

2.3.3.6 Acceptance tests

Final acceptance tests will be performed in Saclay, according to a procedure defined by RAL, and agreed by Caltech/JPL and CEA/Saclay. Test will be conducted under the responsibility of CEA/Saclay, with Caltech/JPL and RAL people as witness.

Detector Electronics Subsystem



CEA Test Cryostat