System-Seam meeting 17 Feb. 2000 MSSL

Berend Winter - MSSL
Colin Cunningha - ROE/ATC
John Coker - MSSL
Dustin Crumb - JPL
Jamie Bock - JPL
Pascal Dargent - L.A.S.
BRUCE SWINYARD - RAL.
Dominique Pouliquen - LAS
Ken King - RAL
PETER HARGRAVE - QMW
COLIN CUNNINGHAM - UK ATC
Kjetil DOHLEN - Obs Marseille
Lionel DUBAM) - CEA SBT
Laurent Vigroux - CEA Saclay
Jean-Louis AUGUERES - CEA Saclay
Martin Fisher - ATC

SPIRE Systems Team Meeting: AGENDA

MSSL Surrey — **17th/18th Feb 00**

			Time (mins)	Leader
Thurs:	9:00	Review Structure/Optics ICD (Splinter)	60	BW
	10:00	Aims of meeting	5	CRC
	9:05	Review Action Items from previous systems team meetings	20	CRC
	9:25	Effects of array selection on systems design - critical issues	120	BMS
	11:25	Report from Cryostat Study (inc Thermal design)	30	BMS
	11:55	Review Opto-mechanical design inc JFET box &shutter	60	BW
	12:55	LUNCH	60	
	13:55	Systems Level Criticality and Reliability Analysis (review doc)	30	CRC
	14:25	Reliability: Cooler and drive electronics	30	BMS
	14:55	Structure/Cooler ICD	45	LD
	15:40	Coffee	15	
	15:55	Structure/FTS ICD	45	BW
	16:40	Review of Actions from WE PDR report	60	BMS
	17:40	END Day 1		

Fri:

10:00	Product Tree - review unnallocated work	30	KK
10:30	Subsystem requirements docs & ICDs & control process	60	BMS/CRC
11:30	Revisions to IID-B in light of array selection	60	CRC
12:30	LUNCH	60	
13:30	Arrays/WE ICD	60	J-L A
14:30	Review ICDs: Splinter Session	60	
	Structure/Arrays		BW
	BSM/WE		MF
15:30	Coffee (BMS/CRC prepare Agreements & ACTION list)	15	
15:45	Preparations for Delta-PDR : Critical systems issues	15	BMS
16:00	List Agreements and ACTION Items	45	CRC
16:45	Review conclusions of meeting	15	MG
17:00	END		

- LIST OF INFORMATION ON S/C IF KK FROM ESA.
- OPERATIONAL CONSTRAINTS KK

COB
- WE REMARKS LV/JB/MG/KK/BS

1st DAY

REVIEW STRUCTURE / OPTICS
ICD (SPLINTER)

B. WINTER

Outcome Workshop

- position focal plane within detect. identified
  - position detectors adjusted accordingly in IDEAS
- Optical Configuration PHT126i following changes/:
  - move PDIC-2 5 mm towards M9
  - move filter support 2K phot. box outwards
  - provide for rattle space fold mirrors (about 3 mm)
  - need for edge-treatment fold-mirrors identified (Bruce will elaborate on this)

Outcome Workshop-cont.

- Filter dimensions nose of the detector
  - thickness less 1 mm (poly-prop.)
  - clamped or bolted, no strict requirements
- Alignment (two stages)
  - 1: mechanical verification (adjustment M6)
  - 2: warm optical verification
  - PMW detector as reference for co-alignment
  - remark : aligment plan for spectrometer?

Outcome Workshop cont.

- Spect. 491
  - lay-out accepted except for small rotation, will be corrected
  - all mirrors fit inside the structure

Outcome Workshop Cont.

- Shutter
  - Location near focal plane 'above' M3
- Outer Cover
  - In principle having a Faraday cage: Common (4K) structure + bellow + JFET box
  - All electrically isolated form cryostat
  - No need for outer cover as RF tight box identified
  - Common structure parts need to elec. cond. Connected (Colin to specify req.)

Outcome Workshop cont.

- Items with respect to RF attenuation identified
  - Clearly specified requirements…..
  - Entry to 4-K structure, filter/cold stop needs to be grounded
  - 4-K panels, Al, need to be allochromed at I/F
  - Maximum sloth length TBD
  - Thermal straps to 4K and 2K need to be isolated

REVIEW ACTION ITEMS
FROM PREVIOUS SYSTEM
TEAM MEETINGS
C. CUNNINGHAM

Outstanding Action Items from Systems Meetings

Due Date:	*Title*		*On:*
21/01/99	AI-ST-0052-23.	**Matt report status of shutter workpackage:** ✓	**MJG::**
~~21/01/99~~ 29/02/00	AI-ST-0052-38.	**Draw up plan of activities leading up to DDR and circulate for comment:**	**KJK:**
~~15/02/99~~ 15/02/00	AI-ST-0599-15	~~**Provide information on frequency plan to GRC**~~ Team Generic PLAN.	**JJB, GV, LR**
12/10/99	AI-ST-0999-05	**Continue leading the ad hoc team to carry out the study as specified in the SPIRE response to the PDR Review Board.**	**BMS** ✓
15/10/99	AI-ST-0999-09	**Provide input to WESRD photometer calibration source (needs relevant part of the Obs. Mode Document)**	**HM** ✓ WE REVIEW
15/10/99	AI-ST-0999-17	**Devise plan for system-level reliability and redundancy analysis**	**CRC/LR**
31/10/99	AI-ST-0599-16	**Provide notes on EGSE, MGSE and OGSE for IID-B to CRC** 3 ACTIONS	**KJK,MSSL,KD**
31/10/99	AI-ST-0599-22	**Write section on EMC for IRD and send to BMS**	**CRC** X
31/10/99	AI-ST-0599-28	**Draw up table of deliverables for subsystems and models**	**Inst PMs**
31/10/99	AI-ST-0999-04	**Devise plan for thermal model development**	**MJG,CRC,BMS,**

Due Date:		*Title*	*On:*	
31/10/99	AI-ST-0999-13	**Ensure that Peter Hamilton's FTS simulations produce recommendation for data compression by October 31.**	**BMS**	DONE → DMJ
28/02/00	AI-ST-0052-30.	**Establish membership and terms of reference of CCB:**	**KK**	
31/03/00	AI-ST-0052-8.	**Recommend light tight aperture design:**	**RAL:**	

EFFECTS OF ARRAY SELECTION ON SYSTEMS DESIGN — CRITICAL ISSUES

B. SWINYARD

Instrument Requirements

- Need to review the requirements on the system as a whole and the sub-systems in light of detector selection and because we've moved on.
- Well lets go.....
- Optics:
  - Straylight control and pupil sizing. Straylight control is somewhat easier with the implementation of feedhorns. The specification of the pupil stop needs looking at as it is likely that the degree of undersize can be relaxed as the edge taper of the Gaussian beams will take care of edge diffraction from the secondary and any spill over onto the "hot bits" in the cryostat and telescope.
  - The focus position for each array needs careful attention. It will be slightly different for each of the arrays depending on the feedhorn design and the Gaussian optics calculations.
  - Dichroic alignment accuracy will need to be looked at due to requirement for co-alignment of pixels in arrays.

Detectors

- Detectors and cold readout electronics:
  - Feedhorn design and implementation needs some attention. The type to be used for the spectrometer needs to be defined and modelled.
  - The JFET box is now a reality – we need to revisit the design of this; its interface to the FIRST optical bench and to the cryostat exhaust line.
  - The issue of RF tightness between the JFET box and the instrument structure and the need (or otherwise) for an outer cover needs urgent attention.

Shutter

- Shutter:
  - No change in basic specification requirements are clear even if the design isn't!
  - Need to operate the shutter in flight – some thoughts on what it could be used for:
    - Determining V-I under predetermined background conditions
    - Flat-fielding with well known source distribution – both photometer and spectrometer
    - Checking for straylight
    - Isolating sources of noise/instability/strange behaviour – i.e. decouples telescope/cryostat sources from internal sources and/or thermal sources.
    - Gives known temperature source into spectrometer for checking calibrator spectral shape.

Beam Steering Mirror

- Beam steering Mirror:
  - With the good low frequency stability of the NTD Ge detectors we can consider lowering the requirement on the BSM chop frequency thus relieving some design constraints – to whit:
    - Lower dissipation
    - Fewer operations – less lifetime testing
    - Less dead-time – easier control loop

Spectrometer

- FTS:
  - No change to mechanism or optical design
  - As we don't need to do decimation we don't need a highly accurate fiducial mark from the Moire fringe device.
  - Natural place for the CRE for the Moire fringe detectors is now inside the JFET box
  - Revisit of focal plane layout is required – can look at using dedicated pixels to optimise long and short wavelength response with individual pass band filters.
  - Need to investigate thoroughly the effect of the loss of the calibrator – J-PB's concerns about the S/N being limited by the position sensor need to be addressed and quantified.

Calibrators

- Calibrators:
  - Again the fact that the NTD Ge detectors have good low frequency stability and they have bias modulation means we can look again at the requirements on the phometer calibrator.
    Do we need to modulate the photometer calibrator at 5 Hz – perhaps only 1 Hz – perhaps not at all?
    If so makes the photometer calibrator specification much easier a basic inverse bolometer style illuminator will be sufficient rather than developing a new fast calibrator
  - FTS calibrator – (see above) - do we need (yet) more redundancy in the FTS calibrator

Cooler

- Cooler:
  - I have concerns here about the total load onto 300 mK. Need to revisit the structure design to make them as light as possible.
    The spectrometer arrays can be made much lighter?
    Also need to look at the 2-0.3 K cable designs?
  - The need for a thermal control circuit could be a design driver for all sorts of sub-systems (i.e. WE and control software – also extra load at 300 mK). Need to identify how and who defines/implements and tests this. Can we have some early test programme or modelling effort to give definitive answer on whether it is really required?
  - Thermal straps – who is going to design and implement these?

OBS/Processors

- On Board Software/Processors:
  - No large amount of on-board data processing is required – selection and data synchronisation and possibly some processing for any peak-up mode.
    Definition of the OBS requirements for each operating mode is now required.
    Can the DPU do this?
    Do we need a high specification processor in the DRCU?
    Are there alternative solutions that will do just as well?
  - If we decide to keep the SPARC can it now do some extra work? – control loop for the BSM; calibrators; thermal stabilisation etc.....

Warm Electronics

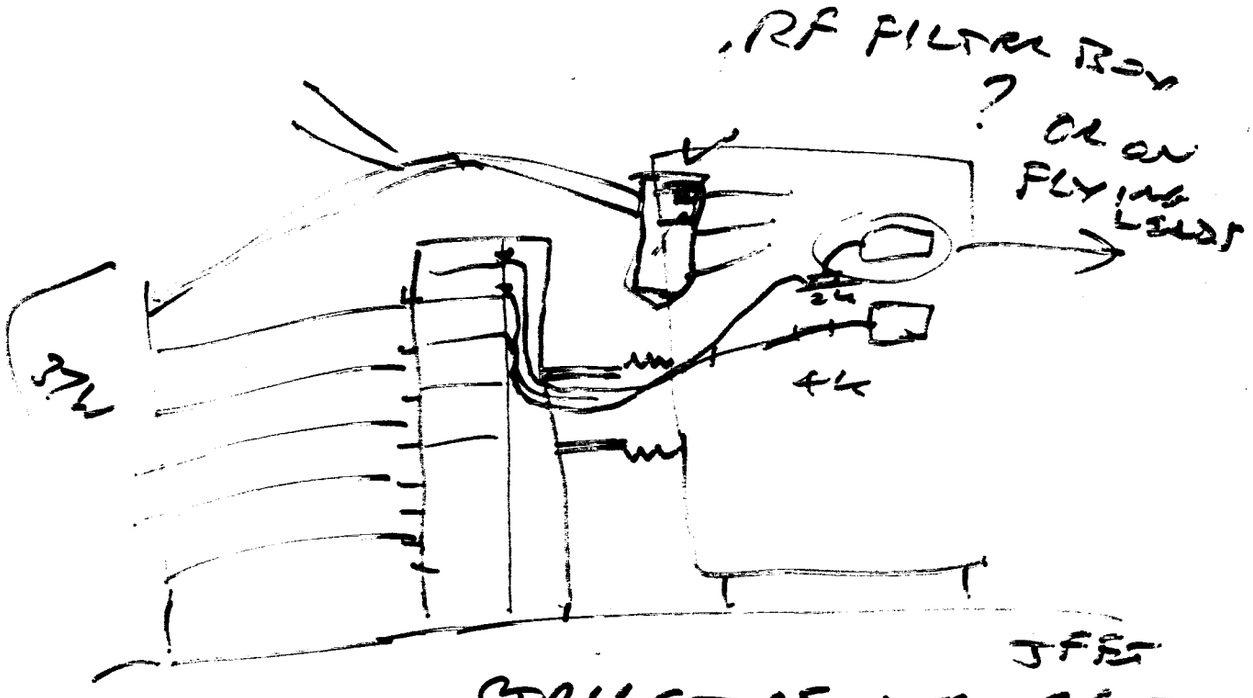
- Warm Electronics:
  - Further definition of the BAU – confirmation of the electrical and thermal design and who is going to build it.
  - Final definition of the readout electronics and the interface to the rest of the DRCU.

Operations

- Operations:
  - We can now start to give some clarity and better definition to the operating modes.
    Can we reduce the number of operating modes?
  - FTS operations are most in need of definition.
    What if the telescope pointing isn't good enough for blind pointing on a point source?
    Need to define peak up mode properly.

REPORT FROM CRYOSTAT
STUDY (incl. THERMAL DESIGN)

B SWINYARD



STRUCTURE INC RF BOX

→ J SL

FILTER MODULES

→ J PL

REVIEW OF ACTIONS
FROM WE PDR REPORT

B. SWINYARD

Things Arising from WE Review

- I've tried to collate the report items by subject (not always successful!)
  - **Operations:**
    - 1 Sorption cooler recycling
      - autonomous or by command? — COMMAND
      - what happens if we miss one? → OPS CONSTRAINT.
    - 3 Switching off safety parameters during commissioning
      - much too early to say what we would do!
    - 4 Difference between standby and observing w.r.t. system config.
      - to be addressed by review of Obs. Mode
    - 5 Definition of peak up mode (ditto)
    - 6 Compression of Data
      - ~~Detector selection makes this much easier to define - there isn't any.~~
    - 7 Burst Mode - ACTION on KJK and BMS to define data transfer sequencing
    - 8 Partner Mode - Matt and Albrecht still need to sort this out. — STILL
    - 15 DRCU nominal operation - we're not allowed to do things when not prime!
    - 27 Instrument Operation and detector selection (ibid #4)

STANDBY → 15 MINUTES FOR EFET WARM UP

FTS REQUIREMENTS

LOSSLESS COMPRESSION

I/F TO ESA — HOOK TO WRITE PARAGRAPH

Things Arising from WE Review

- Cold FPU:
  - 23 FTS Pre-amplifier - where does it go
    - I propose we put this in the JFET box with the others.
  - 25 Thermometry - apparently we are not monitoring FPU temperatures during bakeout
    - Is this true?
    - What about the S/C monitored thermistors? ⇒ WHAT IS THIS ALL ABOUT
  - 26 Shutter Specification
    - No further comment
  - 32 Cooler thermal control
    - Difference in approach between cooler presentation and thermometry presentation
    - As discussed elsewhere in the agenda need to define who is responsible for this area and a plan to discover whether it is actually necessary.
  - 34 BSM Flex pivots
    - Noted as an issue for concern
    - Addressed in BSM development plan?

Things Arising from WE Review

- Detector Selection:
  - 10 Harness capacities - concern over GSFC option - gone
  - 22 BAU - did all options need it - gone
  - 39 RF filtering - ditto - gone

- Interface to S/C
  - 13 Temperature measurements
    - ESA want to know why we need them to monitor WE temperatures - especially as units will be on all the time
    - Fair point - do we change our requirement? → How do we get switched on? Safely?
  - 14 SPIRE Budgets
    - Apparently some inconsistency here - probably arising from detector options?
    - Clarification for Delta PDR
  - 16 Detector Selection - asked for clarification on resource implications - N/A

Things Arising from WE Review

- DRCU:
  - 19 DRCU to DPU communication link
    - Is it necessary to have anything other than 1553B
  - 20 Microprocessor choice
    - ESA don't like having the SPARC (tant pis)
    - However with the reduced processing load - do we still need it?
  - 21 DRCU Conceptual Design Implementation
    - When will it be completed (delta PDR?)
  - 24 DRCU Compatibility with the needs of the FTS
    - Apparently not clear that the FTS electronics and the DRCU system are compatible
    - Addressed by system description and Interface definition?
  - 33 BSM control system
    - How is this to be implemented - can it be done using the DRCU processor
    - To be addressed by system description/requirements for BSM and (then) interface definition
  - 28 OBS - not part of review - when will this be addressed - delta PDR.

NEED FAST LINK SIMPLER THAN 1553 B. GUARANTEED AGREED WITH IFSI.

CLARIFIED AT PDR.

UNDER STUDY. Δ PDR

DISCUSSED AT PDR

COMMANDING FROM DPU - DRCU

DRAFT URD FOR DRCU ← LU'S DOC? WE REVS

DRAFT URD FOR DPU - ISSUED DRAFT

Things Arising from WE Review

- Management and schedule:
  - 9 Model Philosophy
    - we (me) need to clarify what each of our models consists of and what it is to be used for.
  - 11 Delivery of PFM unit
    - Question arising from the presentation of WE schedule showing *prima facie* late delivery of PFM WE
    - a real issue?
    - to be addressed as part of review of AIV.
  - 12 Document Control
    - ESA asked to provide list of up to date documents for instruments to use (Anything happened? Should we do the same?)

Things Arising from WE Review

- Request to ESA:
  - 2 S/C Pointing accuracy during line scanning
    - And the answer is.....?
  - 17 OBDH Interfaces
    - We are supposed to provide "a questionaire" to clarify what information we need - volunteers? ⇒ working a level
    - We should request an industrial study ASAP
  - 29 Grounding scheme, cryoharness definition and EMC
    - We have requested ESA to set up a working party on this - let's keep up the pressure.
  - 31 DC/DC converter synch pulse.
    - We have requested this from the S/C - needs to go into IID-B
    - Is someone keeping a list of IID-B issues?

2nd DAY

PRODUCT TREE –
REVIEW UNALLOCATED
WORK
K. KING

The SPIRE Product Tree

Ken King

Product Tree Issue 1

Forward to first issue:

It is planned to have this document approved, and agreed by all parties, before the end of October 1999 (though some revision will be necessary after detector selection in January 2000). Once agreed, it will form the formal basis of the work breakdown structure to be provided by each institute. Co-investigators, who are responsible for the delivery of the work packages assigned to their institute, should study this document carefully and provide their comments to the SPIRE Project Manager before September 20th.

No comments were received

Product Tree

This document details all hardware and software items to be produced by the SPIRE consortium during development and test of the instrument deliverable models and the SPIRE ICC. The intention is to identify ALL items that shall be delivered from one institute in the SPIRE consortium to another, or to ESA, and to identify the institute responsible for the production and delivery of that item.

The document forms part of the response of the SPIRE consortium to the FIRST Instrument Interface Document Part A (AD1) along with the SPIRE Management Plan (RD1).

This version of the document deals, in detail, only with the items required for the deliverable models of the instrument. It is recognised that there will be other, internal, models of the sub-systems that may require items to be delivered from one institute to another. These will need to be identified as the development plans of each of the sub-systems are finalised and then incorporated into future versions of the document.

Top-Level Breakdown

Product Item	Descriptor	Instrument Model AVM	CQM	PFM	FS	Resp.
Cold FPU			x	x	x	
Warm Electronics		x	x	x	x	CEA
Simulators		x	x	x	x	
Support Items						
Mathematical Models						
Information						
Ground Segment						RAL
Instrument Control Centre						RAL

1.1 Structure

	Structure	STRC		x	x	x	MSSL
	~~Cover (including~~ interface structure to the JFET/Filter box and the FIRST optical bench)	COV		x	x	x	MSSL
	Common 4-K Structure (including supports and any interface structure to the FIRST optical bench)	C4K		x	x	x	MSSL
	Photometer 2-K Structure (including supports)	P2K		x	x	x	MSSL
	Spectrometer 2-K Structure (including supports)	S2K		x	x	x	MSSL
	Internal thermal straps for 4-K and 2-K stages			x	x	x	MSSL
	Thermal interface structure to cryostat 4-K stage			x	x	x	MSSL
	Thermal interface structure to cryostat 2-K stage			x	x	x	MSSL
	Thermal strap from evaporator to detectors (and TCU)			x	x	x	MSSL
	Alignment reference mirrors			x	x	x	MSSL
	Structure thermistors (see separate table) BMS → ALL THERMISTORS	T_P2K_1		x	x	x	MSSL
		T_P2K_2		x	x	x	
		T_S2K_1		x	x	x	
		T_S2K_2		x	x	x	
		T_C4K_1		x	x	x	
		T_C4K_2		x	x	x	
		T_COV_1		x	x	x	
		T_COV_2		x	x	x	
	Structure thermistors harness and connector(s) ? HAVERS			x	x	x	MSSL
	FSFPU Transport containers			x	x	x	MSSL

? connection to harness

for some purchases etc

Optics(1)

Optics			OPT		x	x	x	LAS
	Photometer optical chain and fore optics		OPTP					
		Common instrument input mirror	CPM3		x	x	x	LAS
		Common mirror at pupil (BSM)	CPM4		x	x	x	[redacted]
		Common reimaging mirror	CPM5		x	x	x	LAS
		Field mirror	PM6		x	x	x	LAS
		Optical relay input mirror	PM7		x	x	x	LAS
		Optical relay second mirror	PM8		x	x	x	LAS
		Optical relay output mirror	PM9		x	x	x	LAS
		Plane fold mirror for LW array	PM10		x	x	x	LAS
		Plane fold mirror for SW array	PM11		x	x	x	LAS
		Photometer Mirror mounts			x	x	x	MSSL
	Spectrometer optical train		OPTS					
		Field Pick-Off Mirror	SPOM		x	x	x	LAS
		Input Fold Mirror	SIFM		x	x	x	LAS
		Input Relay Mirror	SIRM		x	x		LAS
		Calibration Source Input Relay Mirror	SCIM		x	x	x	LAS
		Collimator Mirror for arm A or B	SCOM-A SCOM-B		x x	x x	x x	LAS
		Roof-Top Mirror in arm A or B	SRTM-A SRTM-B		x x	x x	x x	LAS
		De-Collimator Mirror in arm A or B	SDCM-A SDCM-B		x x	x x	x x	LAS
		Camera mirror in arm A or B	SCAM-A SCAM-B		x x	x x	x x	LAS
		Output Fold mirror in arm A or B	SOFM-A SOFM-B		x x	x x	x x	LAS
		Spectrometer mirror mounts			x	x	x	MSSL

Optics(2)

Filters; dichroics and beam splitters	**FILT**		x	x	x	QMW
Photometer dichroics						
First dichroic (reflects λ > TBD μm)	PDIC-1		x	x	x	QMW
Second dichroic (reflects λ > TBD μm)	PDIC-2		x	x	x	QMW
Photometer filters						
Input filter on cover	CFIL-1		x	x	x	QMW
Edge filter over entrance to 4-K box	CFIL-2		x	x	x	QMW
Edge filter at 2-K box entrance (pupil)	PFIL-3		x	x	x	QMW
Bandpass filters over SW, MW and LW arrays	PFIL-4S PFIL-4M PFIL-4L		x x x	x x x	x x x	QMW
Blocker filters over SW, MW and LW arrays	PFIL-5S PFIL-5M PFIL-5L		x x x	x x x	x x x	QMW
Photometer filter and dichroic mountings						
Mounting rings			x	x	x	QMW
Mounting structure			x	x	x	MSSL
Spectrometer beam dividers						
Beam Divider 1 (common to both arms)	SBDI-1		x	x	x	QMW
Beam Divider 2 (common to both arms)	SBDI-2		x	x	x	QMW
Beam divider mounting rings			x	x	x	QMW
Beam divider mounting structure			x	x	x	MSSL
Spectrometer Filters						
2-K filters at entrance to 2-K box (pupil)	SFIL-3S SFIL-3L		x x	x x	x x	QMW
Bandpass filters over arrays	SFIL-4S SFIL-4L		x x	x x	x x	QMW
Blocking filters over arrays	SFIL-5S SFIL-5L		x x	x x	x x	QMW
Spectrometer filter and beamsplitter mountings						
Mounting Rings			x	x	x	QMW
Mounting structure			x	x	x	MSSL

Optics (3)

		Baffles	**BAFF**					Note 1
		Photometer and fore-optics optical baffling						
		Baffles (TBD)			x	x	x	Note 1
		Baffle mounts			x	x	x	Note 1
		Spectrometer baffling						
		Baffles (TBD)			x	x	x	Note 1
		Baffle mounts			x	x	x	Note 1

Cooler

Cooler	COOL					CEA
^{3}He Cooler Unit including: pump; evaporator; connection tube; pump and evaporator heat switches and support structure.	COOL		x	x	x	CEA
Cooler thermistors (see separate table)						CEA
CEA/SST	T_CPMP_1 T_CPMP_2 T_CBV_1 T_CBV_1 T_CPHS_1 T_CPHS_2 T_CBHS_1 T_CBHS_2		x x x x x x x x	x x x x x x x x	x x x x x x x x	
Cooler harness and connector(s)			x	x	x	CEA
Cooler mechanical interface structure			x	x	x	MSSL

Photometer Arrays

	Photometer Bolometer Arrays	**DETP**					**Note 2**
	Photometer short wavelength array module	PSW					Note 2
	PSW array; cold readout electronics and support structure			X	X	X	Note 2
	PSW harness and connector(s)			X	X	X	Note 2
	PSW thermal interface structure			X	X	X	Note 2
	PSW mechanical interface structure			X	X	X	MSSL
	Photometer medium wavelength array module	PMW					Note 2
	PMW array; cold readout electronics and support structure			X	X	X	Note 2
	PMW harness and connector(s)			X	X	X	Note 2
	PMW thermal interface structure			X	X	X	Note 2
	PMW mechanical interface structure			X	X	X	MSSL
	Photometer long wavelength array module	PLW					Note 2
	PLW array; cold readout electronics and support structure			X	X	X	Note 2
	PLW harness and connector(s)			X	X	X	Note 2
	PLW thermal interface structure			X	X	X	Note 2
	PLW mechanical interface structure			X	X	X	MSSL
	Photometer array thermistors (see separate table)	T_PSW_1 T_PSW_2 T_PMW_1 T_PMW_2 T_PLW_1 T_PLW_2		X X X X X X	X X X X X X	X X X X X X	Note 2

Spectrometer Arrays

		Spectrometer Bolometer Arrays	**DETS**					**Note 2**
		Spectrometer short wavelength array module	**SSW**					**Note 2**
		SSW array; cold readout electronics and support structure			X	X	X	Note 2
		SSW harness and connector(s)			X	X	X	Note 2
		SSW thermal interface structure			X	X	X	Note 2
		SSW mechanical interface structure			X	X	X	MSSL
		Spectrometer long wavelength array module	**SLW**					**Note 2**
		SLW array; cold readout electronics and support structure			X	X	X	Note 2
		SLW harness and connector(s)			X	X	X	Note 2
		SLW thermal interface structure			X	X	X	Note 2
		SLW interface structure			X	X	X	MSSL
		Spectrometer array thermistors (see separate table)	T_SSW_1 T_SSW_2 T_SLW_1 T_SLW_2		X X X X	X X X X	X X X X	Note 2

Beam Steering Mechanism

Beam Steering Mechanism	**BSM**					**ATC**
BSM motors; mirror support; position pick-offs and structure			x	x	x	ATC
BSM thermistors (see separate table)	T_BSM_1 T_BSM_2		x x	x x	x x	ATC
BSM harness and connector(s) (including provision for calibrator electrical connections)			x	x	x	ATC
BSM interface structure			x	x	x	MSSL

FTS Mechanism

	FTS Mechanism	FTS					LAS
	FTS mechanism carriage and SRTM support			x	x	x	LAS Note3
	FTS mechanism motor(s)			x	x	x	LAS
	FTS mirror position measurement system			x	x	x	LAS
	FTS mechanism thermistors (see separate table)	T_FTS_1 T_FTS_2		x x	x x	x x	LAS
	FTS mechanism harness and connector(s)			x	x	x	LAS
	FTS mechanism interface structure			x	x	x	MSSL

Shutter

Shutter		**SHUT**					**USK**
	Shutter mechanism			x	x	x	USK
	Shutter vane			x	x	x	USK
	Shutter vane thermistors (see separate table)	T_SHUT_1 T_SHUT_2		x x	x x	x x	USK
	Shutter harness and connector(s) — SAVERS			x	x	x	USK
	Shutter interface structure			x	x	x	~~MSSL~~ USK

Calibration Sources

Calibration Sources		**CAL**					**GSFC**
	Photometer Calibration Source	**PCAL**					**GSFC**
	Active element(s)			X	X	X	GSFC
	Integrating cavity and light pipe			X	X	X	GSFC
	PCAL filters			X	X	X	QMW
	PCAL thermistors (see separate table)	T_PCAL_1 T_PCAL_2		X X	X X	X X	GSFC
	PCAL harness and connector(s) [combined with BSM harness and connector(s)]			X	X	X	ATC
	PCAL interface structure			X	X	X	ATC
	Spectrometer Calibration Source	**SCAL**					**GSFC**
	Active element(s)			X	X	X	GSFC
	Integrating cavity and optics			X	X	X	GSFC
	SCAL filters			X	X	X	QMW
	SCAL thermistors (see separate table)	T_SCAL_1 T_SCAL_2		X X	X X	X X	GSFC
	SCAL harness and connector(s)			X	X	X	GSFC
	SCAL interface structure			X	X	X	~~MSSL~~ GSFC

JFET Box

JFET/RF Filter Box	FSFTB					JPL
Box including interface structure to the FIRST optical bench.			x	x	x	JPL
Thermal interface structure			x	x	x	JPL
JFETS and heaters (NTD option only)			x	x	x	JPL
RF filters for all wires into/out of FPU			x	x	x	JPL
FSFTB thermistors (see separate table)	T_FTB_1 T_FTB_2		x x	x x	x x	JPL
Connectors			x	x	x	JPL
Savers			x	x	x	JPL
FSFTB transport container			x	x	x	JPL

Buffer Amplifier Unit

CEA

Buffer Amplifier Unit	FSBAU		x	x		~~JPL~~
Box including interconnect plane and card rack(s)			x	x	x	JPL
Low noise amplifiers			x	x	x	JPL
BAU thermistors (see separate table)	T_BAU_1 T_BAU_2		x x	x x	x x	JPL
Power supplies (if needed)			x	x	x	JPL
Connectors			x	x		JPL
Savers			x	x		JPL
BAU transport container			x	x	x	JPL

FILTER BOX

JPL

Detector Readout and Control

Detector Read Out and Control Unit	**FSDRC**		x	x		CEA
Box including interconnect plane and card rack(s)			x	x		CEA
Detector read out electronics			x	x	x	Note 7
Instrument control electronics			x	x	x	CEA
Beam steering mirror drive electronics			x	x	x	[illegible] Note 8
Spectrometer mechanism drive electronics			x	x	x	LAS
Cooler control electronics			x	x	x	CEA
Calibration source control electronics			x	x	x	CEA
Temperature monitor electronics			x	x	x	CEA
Digital interface to DPU			x	x	x	CEA
Power supplies			x	x	x	CEA
FSDRC thermistors (see separate table)	T_DRCU_1		x	x	x	CEA
	T_DRCU_2		x	x	x	
	T_DRCU_3		x	x	x	
Connectors			x	x		CEA
Savers			x	x		CEA
DRCU transport container			x	x	x	CEA

TBD

shutter electronics

TBD

Digital Processing Unit

Digital Processing Unit	FSDPU					IFSI
Box including interconnect plane and card rack(s)		x	x	x		IFSI
CPU		x	x	x	x	IFSI
Mass memory		x	x	x	x	IFSI
Digital interface to S/C OBDH		x	x	x	x	IFSI
Digital interface to [redacted]DRCU		x	x	x	x	IFSI
Analogue interface to S/C DRCU		x	x	x	x	IFSI
Power supplies		x	x	x	x	IFSI
DPU thermistors (see separate table)	T_DPU_1 T_DPU_2	x x	x	x x	x x	IFSI
Connectors		x	x	x		IFSI
Savers		x	x	x		IFSI
DPU transport container		x	x	x	x	IFSI

Warm Interconnect Harness

Warm Interconnect Harnesses						
DPU to DRCU harness	FSHAR		x	x	x	GEA
DPU to DRCU simulator harness		x				Stock-holm

who pays?

1.1.1 Information

This section identifies specific information packages deliverable between institutes. Much other information is contained in the project documentation, which is not covered by this document.

ID	Product Item	Descriptor	Resp.
	Cooler Electronics Design		CEA
	Detector Electronics Design		[illegible]
	BSM Electronics Design		ATC
	Shutter Electronics Design		[illegible]
	PCAL Electronics Design		GSFC
	SCAL Electronics Design		GSFC

Table 1.2-1 Information Package deliverables

Notes:

1. The responsibility for delivery of the detector electronics design lies with the group whose technology is chosen in the detector selection process.
2. The Canadian Space Agency have been requested to fund this subsystem; in the event that they don't, no shutter will be implemented.

These are all specs

Need design docs also

1.2 Mathematical Models

Mathematical Models	Responsible	Deliverable
Optical		
Instrument Geometrical Optics Model (*Synopsis*)	LAS	No
Straylight Model (*APART; Code V*)	RAL	To Estec
Diffraction analysis (ASAP)	RAL	No
Performance		
Radiometric (*MathCad* and/or *IDL*)	QMW	No
Operations simulations (*IDL*)	ICC	No
Time Estimator (*IDL*)	ICC	To FSC
Engineering		
Structural [redacted] (*IDEAS?*)	MSSL	To Estec
~~Thermal FE [redacted] (Note 1)~~	~~MSSL~~	~~No?~~
Thermal balance (Note 1) Nodal	ATC	To Estec

Structural FEA

Table 1.2-1Mathematical Models No MSSL

Notes:

1. Compilation and maintenance of the thermal models will be organised by the FPU Systems Engineer.

BSM / WE

M. FISHER

SPIRE BSM chop stage simulations.

Power Dissipation (in drive coils only):

$P_d \propto F \times \theta^2 \times J^2 \times f^4$

F = 1/switching time
J = stage inertia
F = Chop frequency
θ = deflection

Simulations give:

For $J = 6.5 \times 10^{-6} kgm^2$; $\theta = \pm 42mrad$ ($\pm 2.4°$); duty cycle 90%

F(Hz)	t_{sw} (msec)	$P_{d\ sin\text{-}acc}$ (mW)	$P_{d\ para\text{-}vel}$ (mW)
10	5	88	53
5	10	5.42	3.25
4	12.5	2.29	1.43
3	16.75	0.87	0.62
2.5	20	0.56	0.44
2	25	0.41	0.36
1	50	0.35	0.34

plus an overhead depending on final damping of system

Low spring rate flexures 0.023Nm/rad ? launch loads

Modes: rigid body $\omega_n \approx 13$ Hz others > 500 Hz

For robust but simple controller design the flexure damping is important. Also some damping expected from interaction of drive magnets and coil assemblies.

Launch loading and flexure stiffness is also a compromise.

So minimise mass and inertia

Controller simulations:

Power dissipation in coils confirmed.

Controller configurations –

- PID and full order state feedback feasible (give good results with with single mode model) but robustness needs to be checked (need assessment of parameter variations) and applied to multi-mode model
- PI-D plus filter and state feedback plus reduced order observer to be assessed as part of robustness issue.

Implementation:

- 2 drive-coil pairs per axis with redundancy built in by driving only one pair if other pair fail.
- 2 sensors per axis (only one powered up, other for redundancy)

Electronics:

- Coil driver circuits.
- Sensor driver/interface circuits.
- Monitoring circuits.
- D/A circuits.
- A/D circuits.
- Controller?

Computing:
Sparc chip-

- Demand waveform shaping and sensor linearisation.
- Redundancy control & configuration
- Flexible parameter controller implementation?

PREPARATION FOR DELTA — PDR: CRITICAL SYSTEMS ISSUES

B. SWINYARD

CRITICAL SYSTEMS ISSUES FOR Δ PDR

- RSM SPEC
- SHUTTER SPEC FLIGHT OR NOT
- COOLER REDUNDANCY PROPOSAL
- QUESTIONS FROM WER.
- DEVELOPMENT PLAN ⇒ CONSOLIDATION OF SCHEDULES.
- WBS + PRODUCT TREE.
- DOCUMENTATION REQUIRED FOR REVIEWS
- LEVEL OF DETAIL.

OTHER

DETECTOR ELECTRONICS

L. VIGROUX

Detector Electronics Development

The CEA/SAp is in charge of the development and the manufacturing of the warm electronics of the bolometer arrays, which are developed by Caltech/JPL. The final performance depends on the bolometers themselves, but also from the readout electronics, and how it matches with the bolometer characteristics. The interfaces are not simple. All of them are of analog type. In addition, since the bolometers, and their first amplifier stages are within a cryostat, the cryoharness and the grounding scheme of the system should be taken into account in the design phase. This development is a complex area, which will require a good cooperation of the two teams. The development plan should take into account this sharing of tasks, and ensure a clear definition of respective responsibilities.

1 The detector electronics subsystem

The detector electronics subsystem is summarized in the following block diagram. It is composed of two main subsystems: a cold detector unit and a warm electronics unit

1.1 Detector electronics cold unit

The detector electronics cold unit has several components.

1.1.1 Bolometer arrays

There are 5 bolometer arrays, 3 for the photometer, 2 for the FTS. The specifications for the bolometer arrays are described in the Instrument Requirements Documents. The bolometer arrays will be provided by Caltech/JPL. . The bolometer bias voltages, intensities, and their stabilities should be provided by the Caltech/JPL group to the CEA/Saclay

1.1.2 300 mK cryocooler

The bolometer arrays are thermally coupled to the 300 mK cryocooler through thermal straps. While the cryocooler is not part of the detector unit, the detector put requirements on the temperature stability at the end of the cryocooler finger. This has impact on the design of a temperature regulation subsystem. The temperature stability requirement is the responsibility of Caltech/JPL. The cryocoller and the cryocooler control unit, including the temperature regulation is under the responsibility of CEA/Saclay. The overall thermal concept is under the responsibility of the RAL.

1.1.3 JFET Box

The first stage of the amplification chain for the bolometers is based on JFET amplifiers. The JFET are operated at cold temperature, at proximity of the bolometers. They are enclosed in a JFET box thermally connected to the " 10 K " screen. The JFET box, and the harness between the bolometer arrays and the JFET box are under the responsibility of Caltech/JPL, and will be provided by them. The thermal coupling of the JFET box and the cryostat screen is under the responsibility of RAL. From the warm electronics point of view, the JFET box provides the formal interface between the cold unit, under the responsibility of Caltech/JPL, and the warm electronics, under the responsibility of CEA/Saclay.

1.1.4 Cryoharness

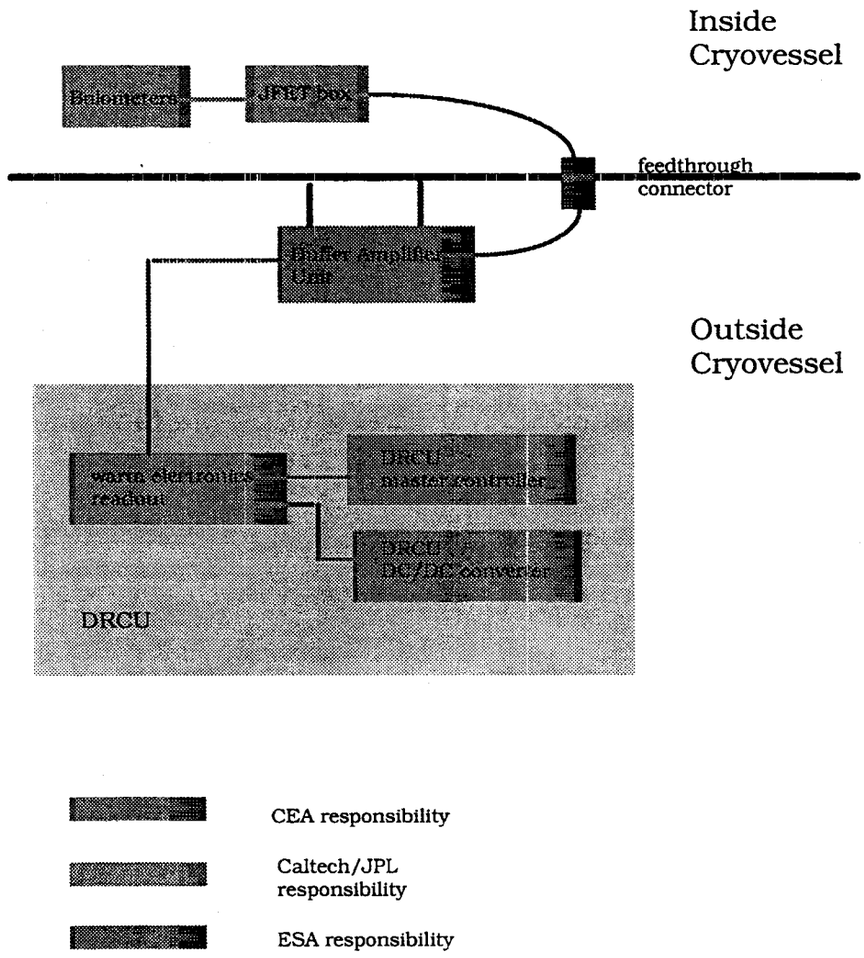
The Cryoharness will be provided by ESA. It would be wise to use the same cryoharness in the Integration and Calibration facility which will be used in RAL. The only requirements placed by the Warm Electronics is that the same harness is used inside the CEA/Saclay test cryostat and in the RAL's Integration and Calibration facility. This harness should be provided by RAL

1.1.5 Feedthrough connectors

SPIRE is very demanding in term of feedthrough connectors. The specifications of these feedthrough connectors, in term of mechanical size, and number of pins are under the responsibility of ESA. In a similar way than the cryoharness, it would be wise to use the same type of connectors during the development phases of SPIRE. A joint procurement, through ESA, might be the correct approach. The feedthrough connectors for the CEA/Saclay test cryostat must be identical to the connectors that will be used in the RAL's Integration and Test Facility. They should be provided by RAL

The following table summarized the main responsibilities and the procurement origins of each of these components.

	interfaces with warm electronics	**responsibility**	**origin of procurement**
bolometers	temperature regulation controller bias voltage levels and stability	Caltech/JPL	Caltech/JPL
JFET box	output signal level and noise characteristics power supply levels, intensities, and stabilities	Caltech/JPL	Caltech/JPL
cryoharness	signal degradation induced by the cryoharness must be included in the system performance budget	ESA	ESA for FIRST RAL for tests and integration cryostats
feedthrough connectors	signal degradation induced by the feedthrough connectors must be included in the system performance budget	ESA	ESA for FIRST RAL for tests and integration cryostats



1.2 Detector electronics warm unit

The detector electronics warm unit has several components

1.2.1 Buffer Amplifier Unit

The Buffer Amplifier Unit is an amplifier and filtering unit which is located on the cryovessel. It has an operating temperature of 120 K. Each amplification channel is directly linked with a bolometer. The BAU is under the responsibility and will be procured by CEA/Saclay

1.2.2 Detector Readout Electronics

This unit is located inside the Digital Readout and Control Unit. Its main functions are to transform the analog output signal received from the BAU to a digital signal which will be send to the Master Controller of the DRCU. It provides also the bias voltages to the bolometer arrays and the power supply to the BAU. The interfaces between the Electronics Readout Unit and the Master Controller are analog power supplies, sequencer clocks, and digital signal outputs. The DRE is under the responsibility and will be procured by CEA/Saclay.

1.2.3 Harness

The harness is separated in 3 pieces. The first connect the feedthrough connectors to the BAU. The second connect the BAU to the DRE. The third one directly connect the DRE to a feedthrough connector dedicated to bias supplies for the bolometers. ESA has the responsibility of these 3 harnesses. As for the cryogenic harness, it might be useful to use the same harness type in all integration and test facilities at instrument level. The procurement of the harness of the test cryostat in CEA/Saclay should be provided by RAL, to be identical to the one which will be used in the Integration and Calibration facility in RAL.

The following table summarized the main responsibilities and the procurement origins of each of these components.

	electronics interfaces	**responsibility**	**origin of procurement**
BAU	power supply levels, intensities, and stabilities voltages, intensities, and noise characteristics of input signal	CEA/Saclay	CEA/Saclay
DRE	output signal level and noise characteristics bias voltage levels and stability power supply levels, intensities, and stabilities	CEA/Saclay	CEA/Saclay
harness	signal degradation induced by the cryoharness must be included in the system performance budget	ESA	ESA for FIRST RAL for tests and integration cryostats

2 Development plan

2.1 Model philosophy

In agreement with the general development plan of the Warm Electronics, the development plan of the Detector Readout Electronics is based on 3 phases:

2.1.1 Engineering Model.

This model is a prototype of the final design. It should be based on technology, and components, which can be used with space quality equivalent. It should be validated with a simplified bolometer array and the corresponding JFET box in a dedicated cryostat. The configuration of the array should be large enough to test collective potential problems such as cross-talk. The harnesses might be similar, but not identical to the flight harness. This phase should be performed in a joint effort between Caltech/JPL and CEA/Saclay. Most of the activities will be done in US with CEA personnel working in a team with the JPL engineers. The engineering model will be validated at JPL with a test equipment provided by JPL. This test equipment should reproduce the interfaces within the DRCU. Then the engineering model will be sent to Saclay to be integrated inside the DRCU. After integration and test, it will be delivered to RAL.

2.1.2 Qualification Model.

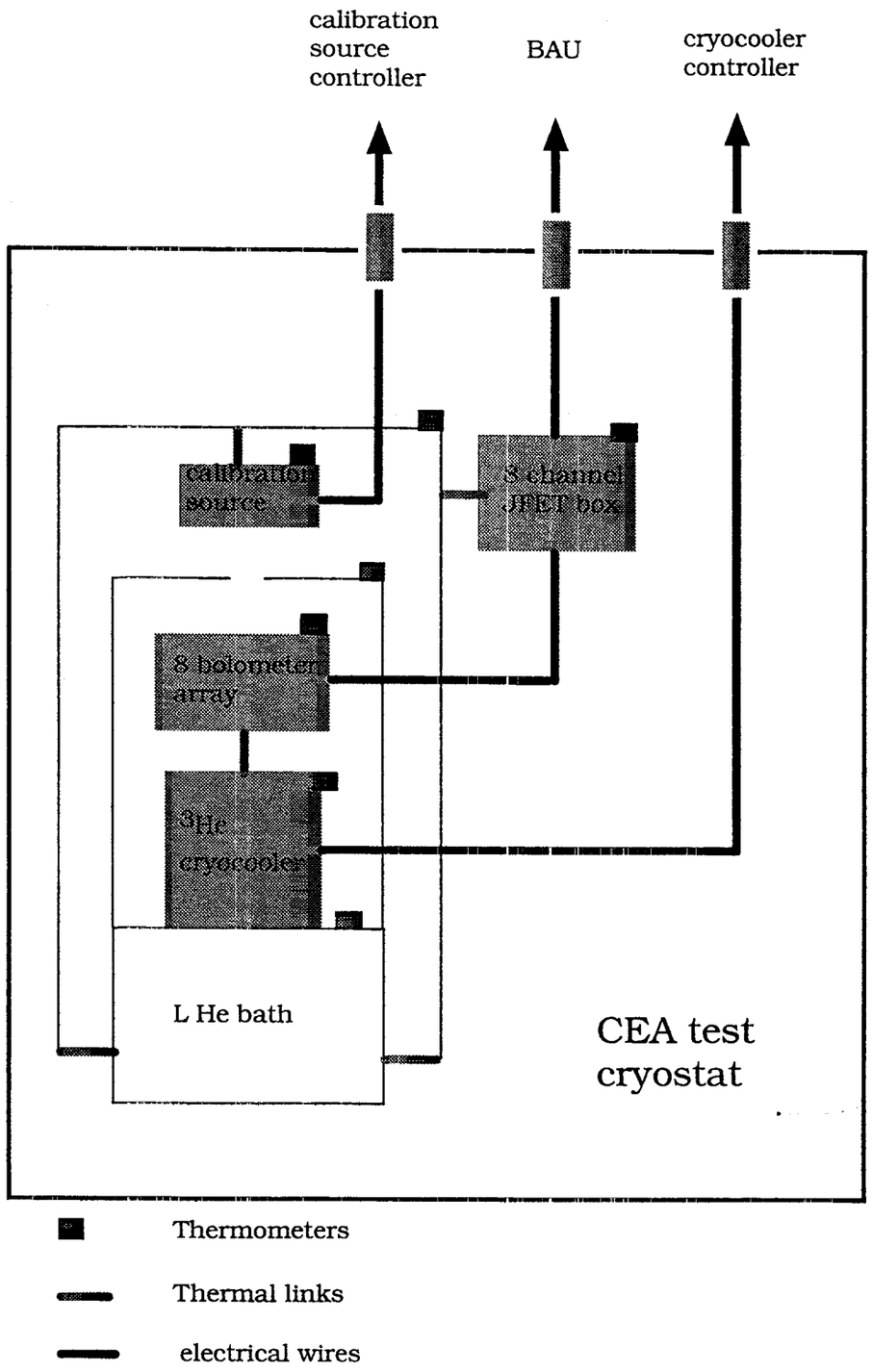
This model is a representative version of the flight model. It will be designed and manufactured in CEA/Saclay. The final acceptance test will be performed in Saclay with test equipment composed, on one side from a cryostat with at least 2 simplified bolometer arrays and their associated JFET boxes, on the other side by a acquisition and data analysis system connected on the DRCU. 2 QM will be manufactured. One will be delivered to RAL for integration in the Cryogenic Model of SPIRE. The second will remain in CEA/Saclay for a qualification with respect to thermal vacuum, EMI/EMC and vibration test.

2.1.3 Flight Model and a Spare Model.

These models are identical. They will be designed and manufactured in CEA/Saclay. Acceptance tests will be performed, before delivery to RAL, with the same equipment, which would have been used for the QM.

2.2 CNES Reviews

Four CNES reviews are planned during this development. The first review will validate the overall development plan and the detector electronics specifications. This review will have to take place before the SPIRE DDR. CNES, and CEA/DSM representatives will be members of the review panels. The success of this review is required to guarantee the CNES and CEA funding for the development of this electronics. 3 reviews, one for the EM, one for the QM and one for the FM, based on the results of the acceptance tests performed in CEA/Saclay will take place before the delivery of these models to RAL. CNES, and CEA/DSM representatives will be members of the review panels.


calibration source controller
BAU
cryocooler controller
calibration source
8 channel JFET box
8 bolometer array
3He cryocooler
L He bath
CEA test cryostat
Thermometers
Thermal links
electrical wires

2.3 Detailed description of the models

2.3.1 Engineering model

2.3.1.1 Model description

This model is composed of a prototype BAU and an DRE. Each of these subsystems is not supposed to contains all the channels which will be present on the flight units. However, they should include a number of channels large enough to studies interference between channels. The printed circuit boards, the technology used (e.g. surface mounted components) should be similar to the final design. Components should be taken within families which offer space qualified version agreed by ESA. The BAU box might be different from the final box. However, it should be compatible with cold test. The harness between the BAU and the DRE might be made with normal wires.

2.3.1.2 Development phases

In the first phase, the BAU and the DRE will be tested by using input simulators. Performances will be measured with these simulators. A dedicated acquisition system will simulate the DRCU interfaces. This phase will take place in JPL. It will be a combined effort of both Caltech/JPL and CEA/Saclay teams.

In the second phase, the BAU and the DRE will be connected to real bolometers and JFET box. Performances with the compared to the results obtained with simulators. This phase will take place in JPL. It will be a combined effort of both Caltech/JPL and CEA/Saclay teams.

In the third phase, the DRE will be integrated with the DRCU. Performances will be measured first with the simulators used in the first phase, then with bolometers and associated JFET box. This phase will take place in Saclay. It will be done by CEA/Saclay people, with a close monitoring from the Caltech/JPL team. The performance test will be done with a DRCU test equipment provided by CEA/Saclay. The bolometers and the JFET box will be set up inside the CEA Test Cryostat, which will be used to validate the functionality and the performances of the warm electronics. The detector array might be delivered in a very simplified mechanical mounting, since it will be bolt directly on he 300 mK fridge. We do not require a mechanical mount identical to the SPIRE system.

2.3.1.3 Test plan

TBW

2.3.1.4 Test equipment

- BAU and DRE input simulator
- BAU cryostat for cold test
- DRE control and acquisition equipment
- JPL test cryostat equipped with one bolometer array of at least 8 (TBC) bolometers and the associated JFET box.
- CEA Test Cryostat
- bolometer array of at least 8 bolometers (TBC) and associated JFET box

2.3.1.5 Deliverable items

2.3.1.5.1 Caltech/JPL

- BAU and DRE input simulator
- JPL test cryostat equipped with a bolometer array and its associated JFET box
- Bolometer array and associated JFET box to be delivered to CEA/Saclay for integration in the CEA test cryostat.
- Detailed description of mechanical, thermal and electrical interfaces of the bolometer array and the JFET box in the CEA Test Cryostat
- Integration procedure for the bolometer array and the JFET box in the CEA Test Cryostat
- Specifications for BAU and DRE
- Test plan for the tests in JPL
- Acceptance test report for the tests performed in JPL
- DRE control and acquisition equipment (To be discussed)

2.3.1.5.2 CEA/Saclay

- Specification for the DRE and DRCU Master Controler interfaces.
- DRCU engineering model
- DRCU test equipment
- BAU cryostat
- CEA Test Cryostat equipped with a 300 mK cryocooler.
- DRE integration procedure.
- Acceptance test report for the tests performed in Saclay.

2.3.1.5.3 RAL

- Feedthrough connectors for the CEA Test Cryostat
- Cryoharness for the CEA Test Cryostat
- System specifications
- Acceptance test procedure
- Acceptance test validation

2.3.1.6 Acceptance tests

Final acceptance tests will be performed in Saclay, according to a procedure defined by RAL, and agreed by Caltech/JPL and CEA/Saclay. Test will be conducted under the responsibility of CEA/Saclay, with Caltech/JPL and RAL people as witness.

2.3.2 Qualification model

2.3.2.1 Model description

This model is composed of a BAU and an DRE. The BAU and the DRE should be fully representative of the flight model, in term of functionality and performances. Mechanical boxes, circuit boards and thermal interfaces should be identical to the Flight Model. Component should be identical to the Flight model, except for the level of quality.

2.3.2.2 Development phases

All the development will take place in CEA/Saclay. In the first phase, the BAU and the Warm Detector Readout will be tested against simulators. In the second phase, they will be tested with actual bolometers inside the CEA Test Cryostat.

2.3.2.3 Test plan

TBW

2.3.2.4 Test equipements

- BAU and DRE input simulator
- BAU cryostat for cold test
- DRE control and acquisition equipment
- JPL test cryostat equipped with one bolometer array of at least 8 (TBC) bolometers and the associated JFET box.
- CEA Test Cryostat
- 2 bolometer arrays of at least 8 bolometers each (TBC) and associated JFET box. One of the bolometer array should have the performances required for the FTS.

2.3.2.5 Deliverable items

2.3.2.5.1 Caltech/JPL

- BAU and DRE simulator (if different from the EM)
- Bolometer arrays and associated JFET box to be delivered to CEA/Saclay for integration in the CEA test cryostat. (at least one more array compliant with FTS performances)
- Detailed description of mechanical, thermal and electrical interfaces of the bolometer array and the JFET box in the CEA Test Cryostat
- Integration procedure for the bolometer array and the JFET box in the CEA Test Cryostat

2.3.2.5.2 CEA/Saclay

- DRCU QM model
- DRCU test equipment
- CEA Test Cryostat equipped with a 300 mK cryocooler.
- Acceptance test report for the tests performed in Saclay.

2.3.2.5.3 RAL

- Additional Feedthrough connectors for the CEA Test Cryostat
- Cryoharness for the CEA Test Cryostat
- QM Acceptance test procedure
- QM Acceptance test validation

2.3.2.6 Acceptance tests

Final acceptance tests will be performed in Saclay, according to a procedure defined by RAL, and agreed by Caltech/JPL and CEA/Saclay. Test will be conducted under the responsibility of CEA/Saclay, with Caltech/JPL and RAL people as witness.

2.3.3 Flight and Spare models

2.3.3.1 Model description

This model is composed of a BAU and a Warm Detector readout Unit.

2.3.3.2 Development phases

The development phase is similar to the development phase of the QM

2.3.3.3 Test plan

TBW

2.3.3.4 Test equipements

FM will be tested with existing test equipment, which would have been validated during the QM phase

2.3.3.5 Deliverable items

2.3.3.5.1 Caltech/JPL

- None

2.3.3.5.2 CEA/Saclay

- Acceptance test report for the tests performed in Saclay.

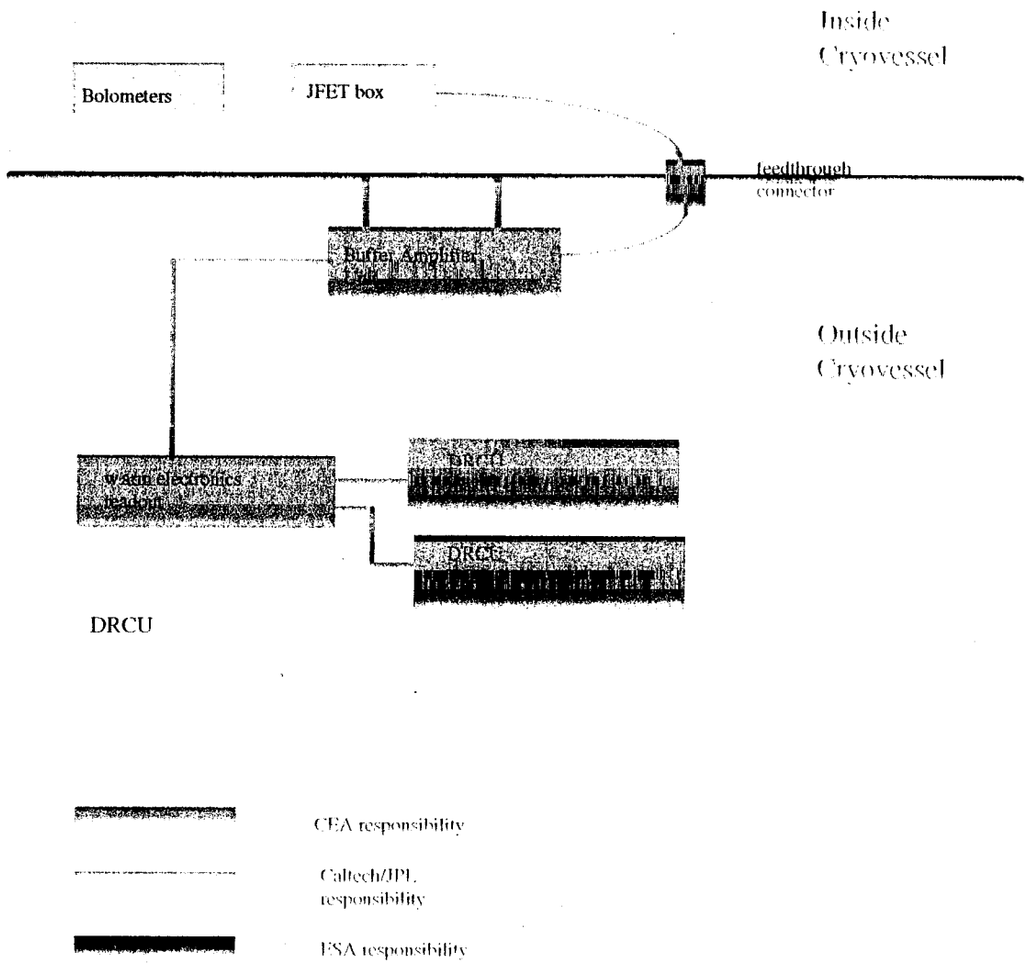
2.3.3.5.3 RAL

- FM Acceptance test procedure
- FM Acceptance test validation

2.3.3.6 Acceptance tests

Final acceptance tests will be performed in Saclay, according to a procedure defined by RAL, and agreed by Caltech/JPL and CEA/Saclay. Test will be conducted under the responsibility of CEA/Saclay, with Caltech/JPL and RAL people as witness.

Detector Electronics Subsystem



CEA Test Cryostat