## Annex A

## Viewgraphs

		SPIRE Bolometer Array Group Meeting Saclay September 29, 30 1999	n yn refer i geref yn i Fri e refer Fri e refer
		AGENDA	
		Day 1: September 29	
1	09.30	Introduction <ul> <li>Meeting logistics</li> <li>Aims of the meeting</li> <li>Review/revision of agenda</li> <li>Status of FIRST and SPIRE</li> </ul>	Vigroux Griffin
2	10.00	SPIRE Review Plan	King
3	10.20	July PDR Review Board report and SPIRE response	Griffin
4	10.40	SPIRE instrument design update	Swinyard
5	11.00	Review of actions	King
6		Progress reports	
	11.30	CEA	Rodriguez
	12.00	GSFC/NIST	Moseley
	12.30	Lunch	
	14.00	JPL/Caltech	Bock
	14.30	QMW (including Array Test Plan update)	Hargrave
7		Electronic system design updates (see note below)	
	15.00	CEA	Cara
	15.30	GSFC/NIST	Moseley
	16.00	JPL/Caltech	Bock
	16.30	Summary/discussion: Preparation for Nov. review	Cara
8	17.00	Splinter meetings: Array Test Plan Warm Electronics	Hargrave Cara
	18.00	End Day 1	
		Day 2: September 30	
9		Simulations	
	09.00	Beam profile and stray light modeling results	Swinyard
	09.30	Instrument operating modes	Griffin
	10.00	Simulations of telescope scanning observations	Oliver
	10.30	Other simulation activities	Vigroux Moseley
	11.30	Discussion: planning of future simulations leading up to detector selection	All

Griffin

. 10 12.00 Summary of meeting and actions

12.30 End of Meeting

MATT GRIFFIN

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· AIMS OF THE MEETING

· STATUS OF FIRST AND SPIRE

## Aims of this meeting

- 1. Review technical status of the array options
  - Test results
  - Readiness for final test phase
  - System design
- 2. Plan the final phase of the array test programme
- 3. Prepare for the Warm Electronics Review in early December
- 4. Review status of instrument modelling and simulation work
  - Major results so far
  - Agree programme leading up to detector selection meeting

This is the last meeting of the Detector Array Group before the Array Selection Meeting in January

## **Status of FIRST and SPIRE**

## **FIRST**

- Available data rate (averaged over 24 hrs) per instrument is now 100 kbs (not as high as the 200 kbs that we hoped for)
- Dornier Cryostat Interface Study has started
  - Limited scope no radical re-examination of the cryostat design
  - Study will examine problems with interfaces associated with the detector options **P** important that we participate
  - Study progress meeting in Munich October 20

## <u>SPIRE</u>

• July PDR Phase 1 was a success overall

Review Board report has been received and SPIRE has responded to it

- PDR plan has been revised (see Ken King's presentation)
- FTS options narrowed down (see Bruce Swinyard's presentation)
- Detailed optical design and layout now available
- Division of focal plane between the three FIRST instruments is now finalised
- Areas in need of urgent attention:
  - Electronic system designs of array options
  - Operating modes and their implications for the warm electronics

## **Schedule of future meetings**

•	Warm Electronics Review (PDR Phase 2)	Dec. 6, 7	Rome
•	Detector Array Selection Meeting	Jan. 31/Feb. 1	RAL
•	PDR Phase 3	March 2000	TBD
•	<b>Detailed Design Review</b>	Sept. 2000	RAL

### Agenda Item 7 Electronic system design updates

### **Detailed information for**

- The Warm Electronics Group and the Systems Team (preparation for the December Warm Electronics Review)
- Cryostat/instrument interfaces study.

## Presentations to include all requirements on and specifications for (and as much detailed design information as possible) on:

- Cryoharness requirements
- Requirements for the grounding scheme
- RF filter box
- BAU
- Detector sampling and synchronisation
- Detector data reduction
  - What needs to be done to convert the raw data stream to the value assumed in the data-rate note?
- Glitch recognition
- Colin's "noise diagram" filled in
- Proposed/suggested warm electronics implementation (block diagrams/circuits/components to be used etc.)
- Warm electronics power
- Anything else that you think may be relevant to the work of the Warm Electronics Group (before it's too late . . . )

### Note on Item 7:

The main purposes of this item are to provide as much and as detailed information as possible for:

- The Warm Electronics Group and the Systems Team to help them define the requirements and outline design for the warm electronics. It is very important to do this in preparation for the November Warm Electronics Review.
- The ESA/Industry study of the cryostat and instrument interfaces which is about to start. The requirements for the cryoharness and the BAU are important here. Much of the relevant material has already been presented at the July PDR and is incorporated into the IID-B - please provide any updates and check for any errors/inconsistencies.

Presentations should include all requirements on and specifications for (and as much detailed design information as possible) on:

- The cryoharness requirements
- Requirements for the grounding scheme
- RF filter box
- The BAU
- Detector sampling and synchronisation
- Detector data reduction ·
  - What needs to be done to convert the raw data stream to the value assumed in the data-rate note?
- Glitch recognition
- Colin's "noise diagram" filled in
- Proposed/suggested warm electronics implementation (block diagrams/circuits/ components to be used etc.)
- Warm electronics power
- Anything else that you think may be relevant to the work of the Warm Electronics Group (if it's not raised soon it might be too late . . . )

Some of these issues and the implications for the warm electronics will be discussed in more detail in the Systems Team meeting immediately afterwards. The agenda will be circulated later by Colin and Louis, but will include:

- Interface Definition and Control
- Warm Electronics (analysis of needs defined by FTS and Detector Groups)
- ESA's industrial study of the FIRST Cryostat
- AIV (outcome of alignment meeting)
- Clarification of subsystem deliverables
- Planning for Warm Electronics internal review in Nov.

## 2. SPIRE REVIEW PLAN

## KEN KING

## SPIRE Review Plans

# Instrument review process takes place in 3 stages:

- Design Reviews
- Preliminary Design Review
- Detailed Design Review

Design approved for manufacture of CQM and AVM

- Development Reviews
- AVM Delivery Review
- CQM Readiness Review
- Critical Design Review

Design approved for manufacture of PFM (and FS)

- Flight Model Delivery Reviews
- PFM Delivery Review
- FS Delivery Review

Detector Group Meeting, Saclay

K.J. King 1

29-30 September 1999

# SPIRE Preliminary Design Review (1)

## **Purpose:**

- To review the instrument design with respect to the scientific goals of the instrument. These goals are defined in the Scientific **Requirements Document.**
- requirements of the mission (spacecraft and ground segment). The requirements are defined in the Instrument Requirements Document To verify that the design conforms to the capabilities and |
- required delivery date. These plans are contained in the Instrument To review the plans for developing such an instrument by the **Development Plan.** |

Detector Group Meeting, Saclay

29-30 September 1999

K.J. King 2

# SPIRE Preliminary Design Review (2)

## The review process is split into four stages following progress in instrument definition

- Review of Cold FPU subsystems Design (July 1999) I
- Scientific Requirements -> Instrument requirements -> subsystem requirements
  - Subsystem designs
- Development Plans
- Review of Warm Electronics Design (December 1999) I

- Warm Electronics Requirements from IRD and subsystems -> WERD.
- DPU, DRCU, Subsystem electronics designs.
- Development Plan.

Detector Group Meeting, Saclay

29-30 September 1999

K.J. King 3

# SPIRE Preliminary Design Review (3)

- Detector Array Selection (Jan-Feb 2000)
- will act as the PDR of the selected detector option.
- Subsystem design, electronics design confirmation

## PDR Delta Review (March 2000)

- will cover items not fully covered before:
- Structure, FTS etc.
- On Board Software (URDs)
- Test and Calibration Facilities
- Support Equipment
- will provide a complete development plan

29-30 September 1999

Detector Group Meeting, Saclay

SPIRE Detailed Design Review

# Purpose: to approve the detailed design of the instrument and release it for manufacture of the AVM and CQM

- Review of instrument detailed design
- System and Subsystems designs (documented)
- Subsystem Interfaces (documented)
- OBS architecture and specification
- Development Plan
- Date: May 2000

requires work to start on detailed design ASAP on subsystems as they are reviewed at PDR level.

29-30 September 1999

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K.J. King 5

## 3. PDR REPORT RESPONSE

MATT GRIFFIN

(SEE NOTE DISTRIBUTED BEFORE THE MEETING

## **Response to PDR Review Board Report**

### 1. Capability to meet science goals

• Effect of pointing errors on scanning mode observations and need for simulations of FTS observations:

Will include in simulations.

Extraction of astronomical spectra from FTS data:
 FTS simulations must be done.

 Need for stray light modelling and experimental measurements

- Build up increasingly detailed APART model.
- Possibly build ground calibration facility early and use as test bed.
- Data rate problems
  - Aim is to avoid any on-board averaging if possible
  - 100 kbs limit may require some compromises
- Urgent need to make progress on the FTS design
  - Already being addressed
  - Working towards full review in March
  - FTS must not distract consortium attention from the photometer
- <sup>3</sup>He cooler redundancy:
  - Study group set up and is working.
  - Assessment and report by end 99
  - Will present proposed scheme to establish high reliability to ESA

## 2. Development Plan

• Structural design, BSM:

Preparing for full PDR in Mar.

• Thermal design:

Full thermal model to be established (will be discussed at Systems Team meeting)

- Shutter:
  - Design can't start in detail until the workpackage has been accepted and funded.
  - Canada only option now; funding status uncertain
  - Cold cryostat lid or retroreflector MGSE should be studied by ESA.
- Detector selection:
  - Agree that it cannot be delayed.

## 4. SPIRE INSTRUMENT

## DESIGN UPDATE

BRUCE SWINYARD

Bruce Swinyard

29/30 Sept 1999

SPIRE Bolometer Array Group Meeting

- No major changes to the opto-mechanical layout
  - Design consolidation and interface specification
  - It all still fits just!
  - Difficult to accommodate the detector arrays (see proposed i/f drawing)
- Attention is now on the detailed design of the FTS
  - A carriage mechanism has been proposed by GSFC
  - This is presently the baseline
  - The Heidenhain Moiré fringe device is baselined for the position sensor
  - The position of the system stop is being finalised

- FTS issues affecting the arrays
  - Decision to keep to two arrays for the FTS
  - Extension to lower wavelengths difficult possible to achieve some sensitivity by profiling filter
  - Sensitivity at longer wavelengths (up to 670 μm) dependent on detector
  - Backup "step and integrate" operation mode will be implemented if possible
  - Envelope is very tight

## Instrument Design Changes

- "External" issues
  - Telescope design has changed now have a thick telescope (~200 mm). F/# and focal position w.r.t. optical bench remain the same (more or less)
  - ESA have started a cryostat study with Dornier to revisit the instrument interfaces.
    - We are asking for the interface temperature to be significantly lower (<6 K) as this would very much simplify the design
    - Dornier fax indicates they won't be radically changing the design
    - They have highlighted the large thermal load from the GSFC wiring they only want to study one detector option
    - We have responded "robustly" to this suggestion

SPIRE Bolometer Array Group Meeting

- Outstanding issues:
  - BAU requirements
  - JFET/Filter box requirements
  - Grounding scheme and EMC requirements
  - Interface definition
    - Electronics/operations N kHz to 40 Hz synchronisation bias and control lines etc...
    - Thermal how do the straps get/on off
    - Mechanical MSSL concerned about the amount of space
    - Accessibility



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## 5. REVIEW OF ACTIONS

## KEN KING

<b>Action Number</b>	Description	Responsible		Due Date Statt
AI-DET-0051-28	Investigate creation of new SPIRE workpackage for a cold shutter	DIM	•	09-Oct-98 .0pen
AI-DET-0051-29	Array splinter meeting actions	AII		Open
AI-DET-0056-07	Design and build 300mK shields for other array options (to be delivered with arrays)	GSFC JPL		Open
AI-DET-0210-33	Investigate availability of illuminators from Jeff Beeman	Hargrave	31/18	o 30-Jun-99 Open
AI-DET-0210-41	Generate nominal beam profiles for 0.5Flambda and 2.0Flambda pixels and provide LV with input map projected through the photometer optics onto the detector focal plane	BMS	N 00237	01-Feb-99 Open
AI-DET-9???-44	To quantify and tabulate geometrical filling factor for ionising radiation (fraction of pixel area that can be struck) for 225, 333 and 500 um arrays	Bock Mos	eley Rodriguez	14-Tun-99 Open
AI-DET-9???-45	To specify array filling factor (fraction of total array area which is sensitive to submm radiation) for 225, 333 and 500 um arrays	Bock Mos	cley	teriun-99 Open
AI-DET-9???-46	To provide Jamie Bock with the latest sensitivity models for SPIRE and discuss the assumptions and methods	₽ DIM	and the first	31-May-99 Open
AI-DET-9???-47	To provide list of non-standard parts that they may wish to use. This will then be provided to ESA for comment.	Bock Mos	eley J-LA	20-Jun-99 Open
AI-DET-9???-48	To comment on the existing draft of the Array Selection Criteria document in as much detail as possible	Bock Mos	eley Vigroux	04-Jun-99 Open
AI-DET-9???-49	To produce a revised draft of the Array Selection Criteria document, which will be distributed as part of the PDR documentation	DIM		14-Jun-99 27em
AI-DET-9???-50	To specify what is required for the Development Plan.	KJK		31-May-99 Open
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28 September 1999

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Action Number	Description	Respons	ble		Due Date Status
AI-DET-9???-51	To review the list of headings for the July PDR viewgraphs/viewgraph sequences and provide Powerpoint template to all subsystem groups	BMS			31-May-99 Open-C
AI-DET-9???-52	To distribute electronmics version of Seb Oliver's viewgraph package to all participants	DIM			27-May-99 Open
AI-DET-9???-53	To comment on Seb Oliver's presentation or any other aspect of SPIRE simulation work	Bock	Moseley	Vigroux See Town	10-Jun-99 Open C
AI-DET-9???-54	To organise a meeting on simulations before the PDR in July (ideal participants: Oliver, Vigroux, Griffin, Gear, Aussel, representatives of Caltech and GSFC).	Vigroux	d.	we have	30-Jun-99 Apen C
AI-DET-9???-55	To comment on the Detector Test Document	Bock	Moseley	Rodriguez	31-May-99 Open C
AI-DET-9???-56	To investigate external filter availability/definitions	Hargrave	PARA		31-May-99 Open C
AI-DET-9???-57	To send BACUS optical design/ZEMAX file to array groups	Hargrave			31-May-99 Open 🤇
AI-DET-9???-58	To send FTS interface details to array groups	Hargrave	PARA	7, 4. prinder	31-May-99 Open C
AI-DET-9???-59	To send QMW shipping agent information to the US groups	Hargrave		9	31-May-99 Open C
AI-DET-9???-60	To refine Letter of Agreement and circulate to GSFC	Gray			04-Jun-99 Open-
AI-DET-9???-61	To investigate and identify any potential shipping problems	Voellmer	Glenn		02-Jul-99 Open C
AI-DET-9???-62	To provide detailed inventory, and list of QMW provided equipment	Bock	Moseley	Rodriguez	04-Jun-99 Open
AI-DET-9???-63	To send QMW email/letter stating lab/bench/office space requirements	Bock	Moseley	Rodriguez	31-May-99 Open <
AI-DET-9???-64	To provide P. Hargrave with QMW test phase schedules	Bock	Moseley	Rodriguez	31-May-99 Open C
AI-DET-9777-65	Revise test document and recirculate	Hargrave			04-tun-99 Open
AI-DET-9???-66	To clarify qualification test/deliverables/schedules at least to CQM.	BMS	Moseley	Rodriguez Hargrave	07-Jun-99 Open

28 September 1999

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PROCRESS REPORTS 6. (a) CEA - Louis RODRIGVEZ (b) GSFC/NIST - HARVEY MOSELEY (c) JPL/CALTECH - JAMIE BOCK (d) QMW - PETER HARGRAVE

\* ARRAYS STATUS CEA DETECTOR Reveret, Vigroux Patrick Agnese, Yann Le Pennec, Louis Rodriguez, Laurent Eric Doumayrou, Vincent Saclay Detector meeting

During the last months we have been working mainly in four directions:

- -We explored also the geometry influence. ( I & Z shapes & channel sizes) Compare thermometers obtained by deep implantation vs mesa technology
- Determine response to a Cold Blackbody on monopixels of 5 x10 pixels arrays built in 98
- Explore the Multiplexing scheme read out (levels, frequencies etc)
  - & determine response to a Cold Blackbody on 16 x 16 arrays.
- **Refine simulation Models**

Of course all that noble tasks have been done once we have solved

- ◆ problems of ESD on MOS readouts.
- problems of adherence of the arrays on the copper plate at cold temperatures.
- & readout circuit contacts on the main chip problems of MUX

VICTOR CONTRACTOR C Saclay Detector meeting

**DETERMINATION OF OPTICAL RESPONSE FOR MONO-BOLOMETERS** 

cold Blackbody for responsivity evaluations (25 cm<sup>2</sup>) "painted" with a multilayer Eccosorb 269 E coating (.5 mm thick), regulated -OFHC Copper plate with pyramidal pattern front surface (2 mm step) in temperature between 2.5 K and 25 K. Manufacture of a "gray"



the 2K shield heated by the parasitic flux coming from Problem to control the placed below BB

## ↑ ↑

shield around the detector. we have built a new 1.5 K

Here estimated load 70 pW



DETERMINATION OF PHYSICAL CARACTERISTICS OF 16 X 16 ARRAYS

Array 99-20 to be tested at QMQ early October

**R/10R** configuration Very resistive sensors : Bridge =900 GOhm at zero Bias @300 mK

@1.2 Volts. **Optimal bias response**  30 Hz @1.4 V 15 Hz at 1.2 V

ŝ ន្តី 50 step 1.2->1.4 V @15 Hz 8 2 22 15 K blackbody 8 0.0 9.0 ģ response to a bias square waveform @ 30Hz ŝ 88 8 22 22 **15 K blackbody** 8 200 9 12 150 step 1.2->1.3 V 0 2 0.5 0 Exemple step 1.2->1.3 V@15 Hz ŝ ្តន្ត 260 300 5 dark conditions Frequency Band 8 Mdu ĝ ŝ 50 0.5 64 өрелоу ofeesto A

A A A A unununununus september 29-30

**N**Saclay Detector meeting

## DETERMINATION OF PHYSICAL CARACTERISTICS OF 16 X 16 ARRAYS: MEASURED RESPONSIVITY





NNSaclay Detector meeting

international and a second second

W/W
**DETERMINATION OF PHYSICAL CARACTERISTICS OF 16 X 16 ARRAYS** 

Noise spectrum @ 1,2 V Bias modulated blackbody and



### 13:49 Sep. 28, 1999 page 1

### Test Report

LEVER

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Système ADWINPRO ; Pré-ampli EPAS : gain = 100, BP = 3.4 KHzRéf.Montage:99\_20 /Réf.Bolomètre:P115\_2.3 Intégré en cryostat : au SAP ; Température : 0.28K Conditions particulières : Bg = CN à 9.6K pW/mm2 ; Filtre :  $\mu$ m -  $\mu$ m (non) Commentaires: Charges externes, VI = 1., offset = 2.745v, Vbias = 1.2 à 1.6v Mode Suiveur ; fréquence trame = 29 Temps d'acquisition par colonne =0 Nombre de moyenne par acquisition =0 Nombre de moyenne par acquisition =0 Nombre d'images successives =255 Valeur du bruit corrélé =0.0104522835903475 Filtrage coupe-bande :1 Cross filtrage : 1 Correction d'offset :10 Nombre de défauts =0 / critère : 0.2

Fichier de sauvegarde : OffsetH:\Porte-documents\acquisition\99\_20\CRYO.SAP\0.3K.25HZ\vin1.2 Fichier de sauvegarde : ImageH:\Porte-documents\acquisition\99\_20\CRYO.SAP\0.3K.25HZ\vin1.2.tcn15 Fichier de sauvegarde : BruitH:\Porte-documents\acquisition\99\_20\CRYO.SAP\0.3K.25HZ\vin1.2 Image de référence; Réponse sous flux; Image de bruit; Signal à bruit Image-offset





DETERMINATION OF PHYSICAL CARACTERISTICS OF 16 X 16 ARRAYS

Figures of Merit

The first 16 X16 array tested with success at Saclay with a probabely pessimistic Hz. A Frequency bandpass controled through the bias input between 15 an 30 calibration source gives very encouraging results:

" The bandpass is actually the electrical bandpass.

"The mean responsivity for a 10 K BB is 1.1 E10 V/W

S. (10 K BB) "The Noise density measured in dark condition & under flux

0.8 E-6 V @ 10 Hz

value of the pMOS readout transistor noise density.

Leading to a Noise Equivalent Power:

NEP mes = 7. E-17 W//Hz

(here BLIP 0.5E-17 V//Hz)

This value, we expect, should be decreased when applying modulation.

which Saclay Detector meeting

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## **PERSPECTIVES FOR THE COMING MONTHS**

Start Next week measurements of the first mesa array in Saclay and the 99-20 detector array at QMW. -Integrate in our test device an InSb source for fast photonic modulation purpose

-Integrate passband filters designed by IAS and already manufactured

Test a new array type every 15 days in each device

(all the measurements done for this presentation are made with a commercial set up sold by Keithley, a preamp by E. Doumayrou and a manual switch box -Test the dedicated electronics we have just received from the manufacturer made by C.Cara).

-Analyse a lot of data produced these two last weeks and not yet exploited.

www.saclay Detector meeting

## GSFC/NIST Detectors

### H. Moseley Sept. 29, 1999

### Progress

- hardware and software, Analysis Algorithms. System development; Test facilities,
- Mechanical design, fabrication, and assembly
- TES production
- Tests of superconducting elements
- Plans for completion of downselect

### BACUS

- electronics are in place for full downselect configured for single array tests, but all The Bacus system has been initally tests.
- Mark II SQUID electronics are functional at GSFC and NIST, seem to work well.
- provides all required capabilities for SQUID mux operation with Mark II electronics. Software has been developed which

### BACUS

- routine. Full housekeeping system makes Operation of the BACUS is cryogenically for easy tracking of system performance. C
- Several items remain to be completed:
- 1 Paddle/shutter installation
- 2 heat switch for faster cooldown of arrays
- 3 complete internal wiring between downselect and breakout board.

## Mechanical System

- Design and Fab are complete for the downselect system.
- successfully on both NIST and GSFC PUDs Detector folding has been carried out
- Assembly of mechanical system has been successfully carried out.

## PUD/TES Production

- PUD's are mechanically reliable
- Never break in folding unless dropped
- position with respect to backshort is being Procedure for achieving accurate PUD developed
- Folded devices are uniform
- New wafers have resulted in better mechanical properties

# PUD/TES Production and Test

- NIST has produced 4 downselect devices, and have tested their electrical and optical characteristics.
- Ag/Al bilayers with shadowmasks
- GSFC has produced photolithographic PUDs with Mo/Au bilayers
- Have wafer of unetched devices with Tc~.460

# Popup Detector Efficiency Measurement



Thruput :  $A^{*}\Omega = 0.0275 \text{ mm}^{2}\text{sr}$ (source diameter and 1/8 of cold aperture)

> Souther Boulder

Measured Efficiency

 $\begin{bmatrix} P_{det}(T_{max}) - P_{det}(T_{s}) \end{bmatrix}$  $\begin{bmatrix} P_{inc}(T_{max}) - P_{inc}(T_{s}) \end{bmatrix}$ 

Source geometry allows some scattered light from source to reach array, increasing measured efficiency.

Tests with redesigned source are now being conducted to improve measurement.



### Souther Bounder

Electrical NEP from Two Tc test popup device



Soulder Boulder



### **PUB Detectors**



The cold plate is lowered, twisted into position with its 'hooks' or 'grooves' at the kevlar straps, and bolted or epoxied to the upper 'C's.

Cold plate epoxied to kevlar straps at each strap set crossing point

Cold plate (alumina)











Amato, Voellmer, Smith 8/99 Epoxy on PUD in folding jig, laser cut, ready to fold (microscope)







## Progress and Status

### of the

# PL/Caltech Feedhorn Option

### Jamie Bock



- Spider bolometer prototype 350µm arrays for SPIRE have achieved up to 90% working pixel yield over the central 1fA and 2f A areas (28/31 pixels) @ room temperature
- 4 arrays have been released with 163/163 spider web pixels intact





### Focal Plane Structure

•Added flexture to use to interface to rest of instrument

Completed structural analysis

•Participated in JPL internal design review

•Added alignment pins, increased spring washer stack height

•Completed fabrication drawings for suspended structure, assembly jig

•Began process of fabricating two engineering models of structure



**BACUS Data Acquisition System** 



- Flexible System for Laboratory Lesting
  Automated DC load curves
  - S<sub>e</sub>(V/W), R(T), DQE
- Software demodulation for chopped sources
- optical time constants, beam maps
- Software demodulation of AC bias
- low frequency noise measurements

**BACUS Readout Electronics** 



Measured end-to-end performance using 200 Hz sine-wave bias and analog lock-in for demodulation







tauoJ



**Bolometer Performance Summary** 

<u>~~</u>

Assumptions:

G = Q/0.1T for margin in optical loading Vn(amp) = 10 nV/VHz C = 1 pJ/K R = 5 M\Omega

- Detectors meet speed and sensitivity requirements
- · Photon-limited sensitivity can be achieved under lower backgrounds with a reduction in speed
- Note: NEP referred to absorbed power 0.7 compling to telescope (assumes background flux is 0.7 times the SPIRE specification resulting in more stringent demands on the detector performance)

Spreadshoet
Sensitivity
tailed
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NEPto		dinar '	ilan ,	<del>~`</del>	<del>.</del>	<del></del>
NEPtot	W/PHHz	9.1E-17	7.2E-17	5.6E-17	1.0E-16	6.1E-17
NEPamp	W/rthe	2.9E-17	2.5E-17	2.2E-17	3.2E-17	2.4E-17
MEPdet	M/ rthe	3.4E-17	3.0E-17	2.6E-17	3.7E-17	2.9E-17
ч	sm	5.7	. 7.2	9.4	4.7	7.8
U	pW/K	134.0	107.2	81.5	162.5	98.8
NEPblip	W / rtHz	8.0E-17	6.0E-17	4.4E-17	8.8E-17	4.9E-17
a	Md	4.0	3.2	2.4	4.9	3.0
	W/m^2sr	2.9E-02	1.2E-02	4.4 4 - 03	2.9E-02	4.4E-03
>	45 5	1200	857	009	1200	600
۲	m	250	350	500	250	200

Ś	Vn(phot)		VmJFET	Vn(BAU)	VmAND	Vinition	a.	Voffset	vemble	Gain	Ę
MIN	althr / Vin		nV / rtHz	NV / THE	NV / PHE	IN / THE	Md	mVrms	NX		nK / rtHz
3.36E+08	26.84	11.26	7.00	5.00	4.38	14.83	7.72	6.21	20.0	284.52	295.4
3.75E+08	22.68	, 1.26	7.00	5.00	3.92	14.70	0.18	··· 5.56	20.0	318.11	291.1
4.30E+08	18.98	11.26	7.00	5.00	3.42	14.58	4.70	4.85	20.0	364.81	295.6
3.05E+08	26.84	11.26	7.00	5.00	4.82	14.97	9.36	6.84	20.0	258.43	268.9
3.91E+08	18.98	11.26	7.00	5.00	3.76	14.66	5.69	5.33	20.0	331.35	269.0

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### Notes: slightly different assumptions than in Griffin et al. MathCad model (e.g.: NEP referred to absorbed power 0.7 coupling to telescope)










- Cryogenic blackbody may be operated between 1.6 K and 35 K using heater and GRT thermometer
- Low straylight for dark characterization
- Modest out-of-band filter requirements (no near-infrared radiation to block)



-

**Optical Coupling Measurements** 



large effective distance

# Summary of Problems and Progress

Cryogenics

12-hour LHe hold time

removed all superinsulation from He stage

Slow cooldowns, 340 mK from <sup>3</sup>He fridge

lightweighted focal plane

replaced Chase <sup>3</sup>He fridge with Duband lab fridge

### Detectors

- · Prototype array demonstrated slow optical time constants (but still in spec) improved release process for demonstration array
  - Lower-than-expected DQE with cryogenic blackbody

carefully checked cavity dimensions interaction with BP filter?

Schedule

- FP structure and JFET prototypes are  $\sim 1$  month behind schedule
- Haven't yet measured optical performance in BACUS

Detectors

- G, R(T) and  $V_n(v)$  satisfactory
- Reasonable yield, optical crosstalk level

Readout Electronics

- Excellent noise performance
- Temperature control electronics not required

### QMW Progress & Array Test Update

#### Progress

- 3 CEA devices tested so far
- Heat switch designed & integrated
- BACUS cool-down cycle well characterised
- Dewar reconfigured for stray light tests
  - Blanked VI's as F(temp.) & noise as F(bias)
  - ISO illuminator tests
  - Stray light tests next week

#### Progress (2)

- Building parts for testing stray light from FTS position sensor (Moire fringe )
- All filters, windows & mounts now built & distributed to groups
- Ruthenium oxide thermometers mounted & calibrated
- Blanking plates complete & distributed test data to be distributed by Raul Hermoso

### Progress (3)

- QMW lab almost completely equipped
- Illuminator tests
  - Stalled due to NASA admin. Four devices were sent 2 months ago, but they are still held up in the shipping dept. - problems with ITAR regulations
  - Ready for integration in BACUS test with NTD pixel.

#### Test Plan Update

- CEA tests continue at QMW
  - Next device to be tested 4/10/99
- GSFC
  - Shipping to QMW 8/11/99
  - Campaign starts 10/11/99 ending 19/12/99
- JPL/Caltech
  - Arriving 1/11/99 for 1 month campaign

#### Test Plan Update (2)

- All dewars now have correct filters/windows to allow "open" operation
- FTS & telescope simulator interfaces & operational modes will be finalised at the splinter meeting

6. ELECTRONIC SYSTEM DESIGN VEDATES (à) CEA - CHRISTOPHE CARA GSFC/NIST - JIM CALDWELL (b)

(C) JPL/CALTECH - VINTOR HRISTOV



DETECTOR SAMPLING AND SYNCHROMISATION

- DETECTOR SAMPLING IS DONE BY SELECTING COLUMNS OF THE ARRAY

- PIXEL OVERSAMPLING IS ACHIEVED BY SWITCHING BUFFER INPUT BETWEEN BOLOMETER SIGNAL AND A REFERENCE BIAS

→ THE WARM ELECTRONICS INCLUDES CLOCK SEQUENCERS :

THE SEQUENCER DESIGN IS COMMON TO PHOTOMETER AND SPECTROMETER SUB-SYSTEMS

 CLOCK SEQUENCES (SIMILAR TO TINY PROGRAMS) ARE SPECIFIC OF SUB-SYSTEM AND ARRAY READOUT MODE (E.G. FRAME RATE)

SEQUENCER GENERATES TEST PATTERN ON REQUEST (TBC)

• H/W PROVIDES : - LOAD/DUMP FEATURES

- EXTERNAL SYNCHRONISATION (INPUT LINE)

- ON/OFF COMMAND (FROM DRCU CONTROLLER)

· IMPLEMENTED ON ANTIFUSE FPGA + RAM

NOTE : ALL THE SEQUENCERS ARE RUNNING SYNCHRONOUSLY WITH A MASTER CLOCK.

		C/OI ITDI ITC .
→ EACH DETECTOR SUB-ARKAT (10X10 FIAEL)	) HAD THE FULLOWING INFUT	S/UUIFUID.
• 5 BIASES		
• 5 SUPPLIES		
• 16 SIGNAL OUTPUTS		
→ EACH ARRAY (3 FOR PHOTOMETER AND 2 F	OR SPECTROMETER) HAS ITS (	<b>WN COLD REDUNDED CLOCK</b>
SPOTIENCER	~	
T ION STACH SUB-ARBAY HAS ITS OWN RIAS VOI 1	AGF GENERATOR (THIS ENABL	ES TO OPTIMIZE FACH SUB-ARRAY
THOLIDOR TAUNAL DAD ANAETEDRY		
LUNCTIONNAL FAMALVETENS)		
$\rightarrow$ IN ORDER TO REDUCE THE WIRING COMPLI	EXITY 2 SUB-ARRAYS SHARE :	
• THE CLOCK LINES		
	L GAIN : 126 LINES !	
<b>RELIABILITY CONSIDERATION :</b>		
FAILURE TYPE:	SOLUTION	COMMENT
CLOCK SEQUENCER	SWITCH TO REDUNDANT	
SUB-ARRAY (INTERNAL)		NO FAILURE PROPAGATION
COMMON LINE SHORTENED	MODIFY CLOCK SEOUENCE	1 SUB-ARRAY LOST
		SUPLLY LINES ARE PROTECTED
BIAS OPENED OR BIAS GENE FAILS		1 SUB-ARRAY LOST
CT OCV OD QUEDEN VDENIED OD CENIE EAIT Q		C C C C C C C C C C C C C C C C C C C
CLUCN UN BUFFLI UFEINEU UN UEINE FAILIS		1 COT CI ENNA-GUC 2
DRCU CONTROLLER	SWITCH TO REDUNDANT	

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ARRAY CLOCK SEQUENCERS CONFIGURATION



3



# **Detector Arrays**

Design Status of the GSFC Electronics J. Caldwell

**GSFC** Detector Array

# Main Design Features

## Functional Description

- Description of the Warm Electronics operation and physical constraints.
- The GSFC/NIST detector system employs SQUIDS to multiplex the data into pairs of wires.
- The system samples each detector at 20,000 frames per second. These are corrupted. The sampling of the data is coordinated with the position data are co-added into a single image. During the co-adding, the pixels are examined for glitches and the data is flagged in the frames which of the FTS and Chopper.
- For both and Photometer and the FTS, the system is synchronized to the start of scan pulses produced by the scan control electronics and to the mirror position sync pulses.

**GSFC Detector Array** 



**GSFC Detector Array** 

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SPIRE TES Package Concept -- Warm Electronics boards



**53 Column Controllers Needed** 

- 3 per Side of 9 Double Sided Circuit Boards
- 2 Double Sided Circuit Boards for all other functions

**GSFC Detector Array** 

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# Column Controller Block Diagram



- System requires 53 Controller Modules (8 + 14 + 31)
- Functions contained within each Column Controller Module
  - Passive Input Filter
- 1 to 2 FPGA's required for each controller
- Loop control is in firmware of the FPGA
- RAM contains the co-added data arrays and A/D and D/A Linearization Tables
  - Bias for TES Detectors.
- Bias for Output Series Array

### **GSFC Detector Array**

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Frame Formatter Controller



- System requires 1 to 2 FFC Modules
- Functions contained within each Module
- Data Tagging -- Error Flags, Error Counts
  - 1 FPGA required for each controller
    - Data and Sync Control Interfaces
      - Data Storage is Ram or FIFO
        - Address Drive for three arrays

**GSFC** Detector Array

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	POV	VER ESTIM	ATE	
	Address Drivers	Column Controller	Bias	BAU (TBD)
Array 1	65 ea OP467 @10 V and 11 mA = 7 15 W	1.3 W per CC x 8 CC = 10.4 W	1 W	8 ea OP467 @10V and 11 mA = 0.88 W
Array 2	65 ea OP467 @10 V and 11 mA = 7.15 W	1.3 W per CC × 14 CC = 18.2 W	1	14 ea OP467 @10V and 11 mA = 1.54 W
Array 3	65 ea OP467 @10 V and 11 mA = 7.15 W	1.3 W per CC x 31 CC = 40.3 W	1 W	31 ea OP467 @10V and 11 mA = 3.41 W
SubTotal	21.45 W	68.9 W	3 W	5.83 W
Total	99.18 W			

**GSFC Detector Array** 







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**GSFC Detector Array** 

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**SPIRE Sep 99 Systems Meeting** 

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**GSFC Detector Array** 





**OPERATION:** 

1st half of sample period - read D/A RAM at address 'row' to get DACdata value for next row. 2nd half of sample period- write D<sub>i</sub> to D/A RAM at address 'row\_delay' for row sampled 'delay' cycles ago. Latch DACdata for next row. 1. i is a sample index, not a cycle (row) index

### **GSFC Detector Array**

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**GSFC Detector Array** 

Detector Array of C columns and R rows with S squids in the series array showing required lines in/out The array size can be adjusted by folding the columns associated with each column controller electronics



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Squid Multiplexor

Physical Arrangement of 500 micron 16x31 Array

8 Column Controllers

TES Bias, SQUID BIAS, MOD, and OUTPUT



**GSFC Detector Array** 

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icro iller ), a	CC31 Pud Ro	W 31P, 1C 31P, 1C	
O I I I	CC30	31P, 1C 31P, 1C 31P, 1C	
S S O N	CC29	31P, 1C 31P, 1C 31P, 1C	?
of 2 AS,	CC28	31P, 1C 31P, 1C 31P, 1C	
BI/		31P, 1C 31P, 1C	
	CC25	31P, 1C 31P, 1C	
ger DU	CC24	31P, 1C 31P, 1C 31P, 1C	
S S S	CC23	31P, 1C 31P, 1C 31P, 1C	
Arra as,	CC22 .	31P, 1C 31P, 1C	5
Bia	CC21	31P, 1C 31P, 1C	
N SI	CC20	31P, 1C 31P, 1C	
ру; Ц Ру;	CC19	31P, 1C 31P, 1C 31B, 1C	
Δ_	CC18	31P, 1C 31P, 1C 31P, 1C	
		31P, 1C 31P, 1C	
	CC15	31P, 1C 31P, 1C	
	CC14	31P, 1C 31P, 1C	
	CC13	31P, 1C 31P, 1C 31P, 1C	
	CC12	31P, 1C 31P, 1C 31P, 1C	
or	CC11	31P, 1C 31P, 1C	
X	CC10	31P, 1C 31P, 1C	
Ĭd	CC9	31P, 1C 31P, 1C	
	CC8	31P, 1C 31P, 1C 31P, 1C	
٧n	CC7	31P, 1C 31P, 1C 31P, 1C	
~	CC6	31P, 1C 31P, 1C 31P, 1C	
n	CC5	31P, 1C 31P, 1C	?
ğ		31P, 1C 31P, 1C	?
0	CC2	31P, 1C 31P, 1C	
		31P, 1C 31P, 1C	

**GSFC Detector Array** 

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	rray		PUT	10p				·				Luca
	Physical Arrangement of FTS 20 × 20 a	7 Column Controllers	TES Bias, SQUID BIAS, MOD, and OUT	10p	<ul> <li>Array has 21 PUD Rows with</li> <li>20 Pixel and 1 Cal SQUID circuits</li> </ul>	A Column Controller Drives     1.5 SQUID Boards	<ul> <li>Super Conducting Wire Interconnect between Boards (where necessary)</li> </ul>	<ul> <li>65 Address Lines +1 Sh</li> <li>8 TES Bias +1 Sh</li> </ul>	14 Feedback +1 Sh	<u>14 Output</u> <u>+1 Sn</u> 101 Lines +4 Sh		
			~	4	Pud Row	20p	3					
b			်႑ိ			20p 20p	51					
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SPIRE Sep 99 Systems Meeting 30 Sep 1999 Saclay	
Squid Multiplexor	Physical Arrangement of FTS 14 x 14 array 4 Column Controllers
- CC1 - CC2 - CC3 - CC4 - CC5 - CC4 - CC5 - CC4 - CC5 - CC5	TES Bias, SQUID BIAS, MOD, and OUTPUT
Pud Row	Array has 21 PUD Rows with     Array has 21 PUD Rows with     20 pixel and 2 Cal SQUID Circuits     (Some Cals are not used.)
14p	<ul> <li>A Column Controller Drives</li> <li>2 SQUID Boards.</li> </ul>
A- 11/17/49/49/17/149/49/17/17/49/49	<ul> <li>Super Conducting Wire Interconnect between Boards where Necessary</li> </ul>
	<ul> <li>65 Address Lines +1 Sh</li> <li>8 TES Bias +1 Sh</li> <li>8 Feedback +1 Sh</li> <li>8 <u>Output</u> +1 Sh</li> <li>89 Lines +4 Sh</li> </ul>
GSFC Detector Array	19




**GSFC** Detector Array



### 21 x 42 Optical 14 x 63 Electrical

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**GSFC Detector Array** 



**GSFC** Detector Array

<u>6</u>

## WIRE COUNT

ŗ						~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	
tal	Shields	4	. 4	4	4	4	20
. To	Wires	105	129	197	101	89	621
AS	Shields	1	1	1	1	1	5
Bl	Wires	8	8	8	8	8	40
DR .	Shields	-	1	-	1	-	5
AC	Wires	65	65	65	65	65	325
8	Shields	-	1	1	1	1	5
FB	Wires	16	28	62	14	8	128
Л	Shields	-	-	-	1	~	5
ō	Wires	16	28	62	14	8	128
SIGNAL	COLS	8	14	31	7	4	64
	Det	500 um	350 um	250 um	FTS	FTS	Totals

**GSFC Detector Array** 

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SQUID MUX ADDRESSING





21

**GSFC** Detector Array



**GSFC Detector Array** 

# WIRE Parameters for Address Line Simulation

- 3 meter length simulation for worst case
- Inductance 0.79e-6H / meter
- Mutual Inductance is 0.1uH / meter
- · Resistance is 26 ohms / meter
- Conductance is 0.0001 mho / meter
- Capacitance is 20 pF / meter

## **TES BIAS Currents**

- 5 mA total current worst case for the 32 column array.
- 156.25 uA Detector bias resistor current worst case.

**GSFC Detector Array** 







**GSFC Detector Array** 





**GSFC Detector Array** 



#### FEATURES:

- RAD-PAK<sup>®</sup> technology hardened against natural space radiation
- Total dose hardness > 100 krad (Si), dependent upon orbit
- Package:
- -16 Pin Rad-Pak® flat pack
- On-resistance,  $<400\Omega$  max
- Transition time, <500ns
- On-resistance match,  $< 10\Omega$
- NO-off leakage current, <20pA at +25°C</li>
- 1.5pC charge injection
- Single-supply operation (+4.5V to +30V) bipolar-supply operation (±4.5V to ±20V)
- Plug-in upgrade for industry-standard DG508A/DG509A
- Rail-to-rail signal handling
- TTL/CMOS-logic compatible

#### DESCRIPTION:

Space Electronics' 338RP (RP for Rad-Pak®) monolithic, CMOS analog multiplexer features a typical 100 kilorad (Si) total dose tolerance. Using Space Electronics' radiation-hardened RAD-PAK® packaging technology, the 338RP is designed to connect one of eight inputs to a common output by control of a 3-bit binary address, and may be used as either a mux or a demux. On-resistance is  $400\Omega$  max, and the it conducts current equally well in both directions. These muxes feature extremely low off leakages (less than 20pA at +25°C), and extremely low on-channel leakages (less than 50pA at +25°C). The new design offers guaranteed low charge injection (1.5pC typ) and electrostatic discharge (ESD) protection greater than 2000V, per method 3015.7. The 338RP operates from a single +4.5V to  $\pm 30V$  supply or from dual supplies of  $\pm 4.5V$  to  $\pm 20V$ . All control inputs (whether address or enable) are TTL compatible (+0.8V to +2.4V) over the full specified temperature range and over the  $\pm 4.5V$  to  $\pm$  18V supply range. Capable of surviving space environments, the 338RP is ideal for satellite, spacecraft, and space probe missions. The patented radiation-hardened Rad-Pak® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing required lifetime in orbit. This product is available up to Class S packaging and screening.

0217.99Rev2

All data sheets are subject to change without notice

(619) 452-4167 - Fax: (619) 452-5499 - www.spaceelectronics.com

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#### Analog Devices, Inc. Space Qualified Parts List

Other Function	5	Electrical		Process
		<u>Grade</u>	Pkg*	Level*
AD2S80A	Variable Resolution Resolver-to-Digital Converter	S	D-40	1,3
AD590	Two Terminal IC Temperature Transducer	K,L	H,F	1,2,3
AD598	LVDT Signal Conditioner	S	D-20	1
AD630	Balanced Modulator/Demodulator	S	D-20	5
AD637	Wideband RMS-to-DC Converter	S	D-14	5
AD9500	Digitally Programmable Delay Generator	S,T	D-24	1,3
ADSP2100A	12.5 MIPS DSP Microprocessor	S	G-100	1,3
MAT01	Matched Dual NPN Transistor	А	Н	1,3
MAT02	Low Noise, Matched Dual NPN Transistor	A,B	H,RC	1
MAT03	Low Noise, Matched Dual PNP Transistor	A,B	H,RC	1
MAT04	Matched Quad NPN Transistor	А	Y	1

#### **Space Products Process Level and Package Information**

- \* 1. Process Level Key
  - 1 Qualified or qualifiable to MIL-STD-883 Level S Para. 1.2.1
  - 2 Qualified, or in qualification as MIL-PRF-38535 QML Level V
  - 3 Available processed to ESA9000 Level B
  - 4 Non-Compliant, Non-QML Devices per MIL-STD-883, Para. 1.2.2
  - SEM only is available in lieu of Wafer Lot Acceptance.
  - 5 Product in qualification

#### \* 2. Package Option Key

CTQFP	44 lead Ceramic Flat Pack (in development)
CSOIC	Ceramic Small Outline IC Package, (in development)
D -	Side Brazed Hermetic DIP
Ε-	Ceramic Leadless Chip Carrier
F -	Ceramic Flat Pack (2-Lead & 16-Lead)
G-100-	Ceramic Pin Grid Array
Н -	Hermetic Metal Can
J -	8-Lead TO-99 Can
L -	10-Lead Flat Pack
М -	14-Lead Flat Pack
N -	24-Lead Flat Pack
F28-	28-Lead Flat Pack
Q -	16-Lead Cerdip (Santa Clara Based Product)
Q -	Cerdip (Other Analog Divisions)
R -	20-Lead Ceramic Dip
RC -	20-Lead Leadless Chip Carrier
TC -	28-Lead Leadless Chip Carrier
Т	28-Lead Ceramic Dip
W	24-Lead Ceramic Dip (Narrow Body)
Х-	18-Lead Ceramic Dip
Υ -	14 Lead Ceramic Dip
Ζ-	8-Lead Ceramic Dip
Z68	68 Pin Gull Wing Package
	CTQFP CSOIC D - E - F - G-100- H - J - L - M - N - F28- Q - Q - R - RC - TC - TC - T W W X - Y - Z - Z68

Product Deletions in 1996, Revision T, U, and Revision X in 1997 These parts are not recommended for new designs. Contact factory for availability

AD587SD,TD AD562SD	AD9696TD AD9022SD	ADC912BW AD9713BTD	OP61AJ,AZ,ARC AMP05BX	OP497AJ,ARC OP64ALAZ ARC	RFF08B7
AD563SD,TD	AD9048SD	AD9720SD	DAC10BX	OP97AJ,AZ,	ICLI UODZ.
AD567SD	AD973SD	AD9721SD	DAC31 2BR	OP260AJ,AZ,ARC	

July 13, 1998

Page 8 of 11.

Radiation Tolerance Category RAD(S)       C       Product       Description         Strategic Levels       SW01       Quad SPST JFET Analog Switch       2         Strategic Levels       SW02       Quad Analog Switch       2         Commercial Space Level       ✓       AD1671       12-Bit 1.25 MSPS ADC         SOK to Meg rad +       ✓       SW02       Quad Analog Switch         Commercial Space Level       ✓       AD571       8/10-Bit ADC         V       AD571       S/10-Bit ADC       With µP Interface         V       AD574       Complete 12-Bit ADC with µP Interface         AD574       Complete 12-Bit ADC with µP Interface         AD580       High Precision 10V Reference         AD581       High Precision 10V Reference         AD582       Internally Trimmed Precision IC Multiplier         AD630       Balanced Modulator / Demodulator         AD632       Internally Trimmed Precision IC Multiplier         AD670       Low Cost Signal Conditioning -Bit ADC         V       AD9002       High Speed Monolithic 8-Bit ADC         V       AD9012       High Speed Monolithic 8-Bit ADC         V       AD9012       High Speed Monolithic 8-Bit ADC         V       AD9010       Precision Instrumentation	Analog Devices, II	IC.	Data Available*	1 Parts List
Category RAD(Si)     G     N     Product     Description       Strategic Levels     SW01     Quad SPST JFET Analog Switch       200K to 1Meg rad +     SW02     Quad Analog Switch       200K to 1Meg rad +     SW06     Quad Analog Switch       200K to 200K rad     AD534     Precision IC Multiplier       50K to 200K rad     AD571     8/10-Bit ADC       V     AD573     Complete 10-Bit ADC with µP Interface       V     AD574     Complete 12-Bit ADC with µP Interface       AD573     Complete 10-Bit ADC with µP Interface       AD574     Complete 12-Bit ADC with µP Interface       AD580     High Precision 10V Reference       AD581     High Precision 10V Reference       AD582     Internally Trimmed Precision IC Multiplier       AD630     Balanced Modulator / Demodulator       AD631     Internally Trimmed Precision IC Multiplier       AD670     Low Cost Signal Conditioning 8-Bit ADC       V     AD767     µProcessor Compatible 12-Bit ADC       V     AD9012     High Speed TTL & Bit ADC       V     AD5910A     12.5 MIPS DSP Microprocessor       V     AD592100A     12.5 MIPS DSP Microprocessor       V     AD9012     High Speed TTL & Bit ADC       V     AD9014     Precision Instrumentation Amplifier	Radiation Tolerance			
Strategic Levels     SW01     Quad SPST JFET Analog Switch       200K to 1Meg rad +     SW02     Quad Analog Switch       200K to 1Meg rad +     SW06     Quad Analog Switch       200K to 1Meg rad +     SW06     Quad Analog Switch       200K to 200K rad     AD1671     12-Bit 1.25 MSPS ADC       50K to 200K rad     AD534     Precision IC Multiplier       V     AD571     8/10-Bit ADC       V     AD573     Complete 10-Bit ADC with µP Interface       AD574     Complete 12-Bit ADC with µP Interface       AD580     High Precision 10V Reference       AD581     High Precision Voltage Reference       AD588     High Precision Voltage Reference       AD580     Balanced Modulator / Demodulator       AD630     Balanced Modulator / Demodulator       AD630     Low Cost Signal Conditioning 8-Bit ADC       V     AD670     Low Cost Signal Conditioning 8-Bit ADC       V     AD767     µProcessor Compatible 12-Bit DAC       V     AD9002     High Speed Monolithic 8-Bit ADC       V     AD5710     I2-S MIPS DSP Microprocessor       V     AD5710     I2-S MIPS DSP Microprocessor       V     AD5710     I2-S MIPS DSP Microprocessor       V     AD761     Matched Dual NPN Transistor       MAT01     Matched Dual NPN	Category RAD(Si)	C	N Product	Description
Status       SW01       Quad Analog Switch         200K to 1Meg rad +       SW02       Quad Analog Switch         Commercial Space Level       AD1671       12-Bit 1.25 MSPS ADC         50K to 200K rad       AD534       Precision IC Multiplier         V       AD571       8/10-Bit ADC         V       AD573       Complete 10-Bit ADC with µP Interface         AD574       Complete 12-Bit ADC with µP Interface         AD580       High Precision IOV Reference         AD581       High Precision IOV Reference         AD588       High Precision IOV Reference         AD589       Precision I.2V Reference         AD530       Balanced Modulator / Demodulator         AD630       Balanced Modulator / Demodulator         AD670       Low Cost Signal Conditioning 8-Bit ADC         V       AD767       µProcessor Compatible 12-Bit DAC         V       AD9002       High Speed Monolitike 8-Bit ADC         V       AD9012       High Speed Monolitike 8-Bit ADC         V       AD52100A       12-S MIPS DSP Microprocessor         V       AD82100A       12-S MIPS DSP Microprocessor         V       AD701       Matched Dual NPN Transistor         MAT01       Matched Dual NPN Transistor	Strategic Levels	U	SW01	
200K to 10kg rad       3 W02       Quad Analog Switch         Commercial Space Level       √       AD1671       12-Bit 1.25 MSPS ADC         50K to 200K rad       √       AD534       Precision IC Multiplier         √       AD571       8/10-Bit ADC       with µP Interface         √       AD573       Complete 10-Bit ADC with µP Interface         √       AD574       Complete 10-Bit ADC with µP Interface         AD581       High Precision 2.5V Reference         AD587       High Precision 10V Reference         AD588       High Precision 10V Reference         AD589       Precision 1.2V Reference         AD532       Internally Trimmed Precision IC Multiplier         AD630       Balanced Modulator / Demodulator         AD632       Internally Trimmed Precision IC Multiplier         AD670       Low Cost Signal Conditioning 8-Bit ADC         √       AD767       µProcessor Compatible 12-Bit DAC         √       AD9002       High Speed Monolithic 8-Bit ADC         √       ADSP100A       12.5 MIPS DSP Microprocessor         √       ADSP100A       12.5 MIPS DSP Microprocessor         √       AD9012       High Speed TTL 8-Bit ADC         √       AD701       Matched Transistor Pair <tr< td=""><td>200K to 1Meg rad i</td><td></td><td>SWUI</td><td>Quad SPST JFET Analog Switch</td></tr<>	200K to 1Meg rad i		SWUI	Quad SPST JFET Analog Switch
Commercial Space Level       √       AD1671       12-Bit 1.25 MSPS ADC         50K to 200K rad       √       AD534       Precision IC Multiplier         √       AD571       &/10-Bit ADC       √         √       AD573       Complete 10-Bit ADC with µP Interface         √       AD574       Complete 12-Bit ADC with µP Interface         √       AD574       Complete 12-Bit ADC with µP Interface         AD580       High Precision 10V Reference         AD581       High Precision 10V Reference         AD588       High Precision 10V Reference         AD589       Precision 1.2V Reference         AD630       Balanced Modulator / Demodulator         AD632       Internally Trimmed Precision IC Multiplier         AD670       Low Cost Signal Conditioning 8-Bit ADC         √       AD9012       High Speed TIL 8-Bit ADC         √       AD9012       High Speed TIL 8-Bit ADC         √       AD9012       High Speed TIL 8-Bit ADC         √       ADSP2100A       12.5 MIPS DSP Microprocessor         √       AMP01       Precision Instrumentation Amplifier         √       CMP04       Low Power Comparator         √       MAT01       Matched Quad NPN Transistor         MAT03	200K to Integ lau +		5 W 02	Quad Analog Switch
Commercial space Level 50K to 200K rad ↓ AD571 AD571 ↓ AD573 Complete 10-Bit ADC ↓ AD573 Complete 10-Bit ADC with µP Interface ↓ AD574 Complete 12-Bit ADC with µP Interface ↓ AD574 AD580 High Precision 10V Reference ↓ AD588 High Precision 10V Reference ↓ AD589 Precision 12V Reference ↓ AD589 ↓ AD570 ↓ AD670 Low Cost Signal Conditioning 8-Bit ADC ↓ AD767 ↓ Processor Compatible 12-Bit DAC ↓ AD9002 High Speed Monolithic 8-Bit ADC ↓ AD9012 High Speed TTL 8-Bit ADC ↓ AD9012 High Speed TTL 8-Bit ADC ↓ AD9012 High Speed Monolithic 8-Bit ADC ↓ AD9012 High Speed Monolithic 8-Bit ADC ↓ AD9012 High Speed Monolithic 8-Bit ADC ↓ AD9012 High Speed TTL 8-Bit ADC ↓ AD9012 High Speed Monolithic 8-Bit ADC ↓ AD9014 Low Power Comparator ↓ OP05 OP004 Dual Precision Instrumentation Amp ↓ OP08 / OP12 Low-Input Bias-Current Op Amp ↓ OP249 Dual Precision Op Amp ↓ OP249 Dual Precision Op Amp ↓ OP37/PM1012 Low-Power Precision Op Amp ↓ PM108 Low-Power Precision Op Amp ↓ PM108 Precision High-Speed Comparator ↓ PM109 Precision High-Speed Comparator	Commercial Space Laurel	<u></u>	<u></u>	Quad Analog Switch
JUN 10 200K rad       V       AD571       8/10-Bit ADC         V       AD571       Complete 10-Bit ADC with µP Interface         AD573       Complete 12-Bit ADC with µP Interface         AD580       High Precision 2.5V Reference         AD581       High Precision 10V Reference         AD582       High Precision 10V Reference         AD583       High Precision Voltage Reference         AD584       High Precision Voltage Reference         AD630       Balanced Modulator / Demodulator         AD632       Internally Timmed Precision IC Multiplier         AD630       Balanced Modulator / Demodulator         AD631       Low Cost Signal Conditioning 8-Bit ADC         V       AD767       µProcessor Compatible 12-Bit DAC         V       AD9012       High Speed Monolithic 8-Bit ADC         V       AD9012       High Speed TTL 8-Bit ADC         V       AD92100A       12.5 MIPS DSP Microprocessor         V       AMP01       Precision Instrumentation Amplifier         V       CMP04       Low Power Comparator         V       MAT01       Matched Quad NPN Transistor         MAT03       Low Noise, Matched Dual PPN Transistor         MAT04       Matched Quad NPN Transistor         MAT04 <td>50K to 200K and</td> <td>N</td> <td>AD1671</td> <td>12-Bit 1.25 MSPS ADC</td>	50K to 200K and	N	AD1671	12-Bit 1.25 MSPS ADC
√       AD571       S/1.4DC         √       AD573       Complete 10-Bit ADC with µP Interface         √       AD574       Complete 12-Bit ADC with µP Interface         △       AD580       High Precision 10V Reference         △       AD581       High Precision 10V Reference         △       AD583       High Precision 10V Reference         △       AD589       Precision 1.2V Reference         △       AD630       Balanced Modulator / Demodulator         △       AD632       Internally Trimmed Precision 1C Multiplier         △       AD670       Low Cost Signal Conditioning 8-Bit ADC         √       AD767       µProcessor Compatible 12-Bit DAC         √       AD9002       High Speed Monolithic 8-Bit ADC         √       ADS2100A       12.5 MIPS DSP Microprocessor         √       ADS2100A       12.5 MIPS DSP Microprocessor         √       ADS2100A       12.5 MIPS Daver Comparator         √       AMP01       Precision Instrumentation Amplifier         √       CMP04       Low Power Comparator         √       MAT01       Matched Quad NPN Transistor         MAT02       Low Noise, Matched Dual NPN Transistor         MAT03       Low Noise, Matched Dual NPN Transistor	JOK 10 200K Tau	Y	AD534	Precision IC Multiplier
√       AD573       Complete 10-Bit ADC with µP Interface         √       AD574       Complete 12-Bit ADC with µP Interface         √       AD580       High Precision 2.5V Reference         △       AD581       High Precision 10V Reference         △       AD587       High Precision 10V Reference         △       AD588       High Precision 10V Reference         △       AD589       Precision 1.2V Reference         △       AD630       Balanced Modulator / Demodulator         △       AD632       Internally Trimmed Precision IC Multiplier         △       AD670       Low Cost Signal Conditioning 8-Bit ADC         √       AD767       µProcessor Compatible 12-Bit DAC         √       AD9002       High Speed Monolithic 8-Bit ADC         √       AD9012       High Speed TTL 8-Bit ADC         √       AD9012       High Speed TTL 8-Bit ADC         √       AD9012       High Speed TTL 8-Bit ADC         √       AD901       Precision Instrumentation Amp         △       AMP05       Fast Settling JFET Instrumentation Amplifier         √       CMP04       Low Power Comparator         √       MAT01       Matched Transistor Pair         MAT02       Low Noise, Matched Dual NPN		N,	AD571	8/10-Bit ADC
√       AD574       Complete 12-Bit ADC with µP Interface         AD580       High Precision 12.5V Reference         AD581       High Precision 10V Reference         AD587       High Precision 10V Reference         AD588       High Precision 12.5V Reference         AD589       Precision 1.2V Reference         AD580       Balanced Modulator / Demodulator         AD630       Balanced Modulator / Demodulator         AD632       Internally Trimmed Precision IC Multiplier         AD670       Low Cost Signal Conditioning 8-Bit ADC         √       AD767       µProcessor Compatible 12-Bit DAC         √       AD9002       High Speed Monolithic 8-Bit ADC         √       AD9012       High Speed TIL 8-Bit ADC         √       AD9012       High Speed Monolithic 8-Bit ADC         √       AD9012       High Speed Monolithic 8-Bit ADC         √       AD872100A       12.5 MIPS DSP Microprocessor         √       AMP01       Precision Instrumentation Amp         AM705       Fast Settling JFET Instrumentation Amplifier         √       CMP04       Low Power Comparator         √       MAT01       Matched Dual NPN Transistor         MAT03       Low Noise, Matched Dual NPN Transistor         MAT0		V	AD573	Complete 10-Bit ADC with µP Interface
AD580       High Precision 2.5V Reference         AD581       High Precision 10V Reference         AD587       High Precision 10V Reference         AD588       High Precision Voltage Reference         AD589       Precision 1.2V Reference         AD630       Balanced Modulator / Demodulator         AD631       Internally Trimmed Precision IC Multiplier         AD670       Low Cost Signal Conditioning 8-Bit ADC         √       AD767         µProcessor Compatible 12-Bit DAC         √       AD9012         High Speed Monolithic 8-Bit ADC         √       AD9012         High Speed Monolithic 8-Bit ADC         √       ADSP2100A         12.5 MIPS DSP Microprocessor         √       ADSP2100A         12.5 MIPS DSP Microprocessor         √       AMP01         Precision Instrumentation Amplifier         √       CMP04         Low Power Comparator         √       MAT01         MAT02       Low Noise, Matched Dual NPN Transistor         MAT03       Low Noise, Current Op Amp         √       OP80 / OP12       Low-Input Bias-Current Op Amp         √       OP200/400       Dual/Quad Low Offset, Low Power Op Amp <td< td=""><td></td><td>V</td><td>AD574</td><td>Complete 12-Bit ADC with µP Interface</td></td<>		V	AD574	Complete 12-Bit ADC with µP Interface
AD581       High Precision 10V Reference         AD587       High Precision 10V Reference         AD588       High Precision 10V Reference         AD589       Precision 1.2V Reference         AD630       Balanced Modulator / Demodulator         AD632       Internally Trimmed Precision IC Multiplier         AD670       Low Cost Signal Conditioning 8-Bit ADC         √       AD767         µProcessor Compatible 12-Bit DAC         √       AD9002         High Speed Monolithic 8-Bit ADC         √       AD9012         High Speed Monolithic 8-Bit ADC         √       ADSP2100A         12.5 MIPS DSP Microprocessor         √       AMP01         Precision Instrumentation Amp         AMP05       Fast Settling JFET Instrumentation Amplifier         √       CMP04       Low Power Comparator         √       MAT01       Matched Transistor Pair         MAT03       Low Noise, Matched Dual PNP Transistor         MAT04       Matched Quad NPN Transistor         √       OP200/400       Dual/Quad Low Offset, Low Power Op Amp         √       OP249       Dual Precision High Speed Op Amp         √       OP250       High Output Current (AVCL*5) Op Amp			AD580	High Precision 2.5V Reference
AD587High Precision 10V ReferenceAD588High Precision Voltage ReferenceAD589Precision 1.2V ReferenceAD630Balanced Modulator / DemodulatorAD632Internally Trimmed Precision IC MultiplierAD670Low Cost Signal Conditioning 8-Bit ADC√AD767µProcessor Compatible 12-Bit DAC√AD9002√High Speed Monolithic 8-Bit ADC√AD9012√High Speed TTL 8-Bit ADC√ADSP2100A12.5 MIPS DSP Microprocessor√AMP01Precision Instrumentation AmpAMP05Fast Settling JFET Instrumentation Amplifier√CMP04Low Power Comparator√MAT01Matched Quad NPN TransistorMAT03Low Noise, Matched Dual NPN TransistorMAT04Matched Quad NPN Transistor√OP200/400√OP249√OP249√OP249√OP27/PM1012√OP37/PM1012√PM108√PM108√PM108√PM111Precision Comparator√PM119Precision High-Speed Comparator	*		AD581	High Precision 10V Reference
AD588High Precision Voltage Reference√AD589Precision 1.2V ReferenceAD630Balanced Moulator / DemodulatorAD632Internally Trimmed Precision IC MultiplierAD670Low Cost Signal Conditioning 8-Bit ADC√AD767µProcessor Compatible 12-Bit DAC√AD9002High Speed Monolithic 8-Bit ADC√AD9012High Speed TTL 8-Bit ADC√ADSP2100A12.5 MIPS DSP Microprocessor√AMP01Precision Instrumentation AmpAMP05Fast Settling JFET Instrumentation Amplifier√CMP04Low Power Comparator√MAT01Matched Transistor PairMAT02Low Noise, Matched Dual NPN TransistorMAT03Low Noise, Matched Dual NPN TransistorMAT04Matched Quad NPN Transistor√OP200/400Dual/Quad Low Offset, Low Power Op Amp√OP200Dual/Quad Low Offset, Low Power Op Amp√OP20High Output Current (AVCL*5) Op Amp√OP50High Output Current (AVCL*5) Op Amp√PM108Low-Power Precision Op Amp√PM108Single / Dual Low Input Bias Current Op Amp√PM108Single / Dual Low Input Bias Current Op Amp√PM111Precision Comparator		•	AD587	High Precision 10V Reference
√       AD589       Precision 1.2V Reference         AD630       Balanced Modulator / Demodulator         AD632       Internally Trimmed Precision IC Multiplier         AD670       Low Cost Signal Conditioning 8-Bit ADC         √       AD767       µProcessor Compatible 12-Bit DAC         √       AD9002       High Speed Monolithic 8-Bit ADC         √       AD9012       High Speed TTL 8-Bit ADC         √       AD9012       High Speed TTL 8-Bit ADC         √       ADS72100A       12.5 MIPS DSP Microprocessor         √       AMP01       Precision Instrumentation Amp         AMP05       Fast Settling JFET Instrumentation Amplifier         √       CMP04       Low Power Comparator         √       MAT01       Matched Transistor Pair         MAT02       Low Noise, Matched Dual NPN Transistor         MAT03       Low Noise, Matched Dual PNP Transistor         MAT04       Matched Quad NPN Transistor         √       OP08 / OP12       Low-Input-Bias-Current Op Amp         √       OP200/400       Dual/Quad Low Offset, Low Power Op Amp         √       OP200/400       Dual/Quad Low Offset, Op Amp         √       OP97/PM1012       Low-Power Precision Op Amp         √       OP97/PM1012 <td></td> <td></td> <td>AD588</td> <td>High Precision Voltage Reference</td>			AD588	High Precision Voltage Reference
AD630Balanced Modulator / DemodulatorAD632Internally Trimmed Precision IC MultiplierAD670Low Cost Signal Conditioning 8-Bit ADC√AD767µProcessor Compatible 12-Bit DAC√AD9002High Speed Monolithic 8-Bit ADC√AD9012High Speed Monolithic 8-Bit ADC√ADSP2100A12.5 MIPS DSP Microprocessor√ADSP2100A12.5 MIPS DSP Microprocessor√AMP01Precision Instrumentation AmpAMP05Fast Settling JFET Instrumentation Amplifier√CMP04Low Power Comparator√MAT01Matched Transistor PairMAT02Low Noise, Matched Dual NPN TransistorMAT03Low Noise, Matched Dual NPN TransistorMAT04Matched Quad NPN Transistor√V OP08 / OP12Low-Input-Bias-Current Op Amp√OP200/400Dual/Quad Low Offset, Low Power Op Amp√OP249Dual Precision High Speed Op Amp√PM108Low-Power Precision Op Amp√PM108Single / Dual Low Input Bias Current Op Amp√PM108Single / Dual Low Input Bias Current Op Amp√PM111Precision Comparator		$\checkmark$	AD589	Precision 1.2V Reference
AD632Internally Trimmed Precision IC MultiplierAD670Low Cost Signal Conditioning 8-Bit ADC√AD767µProcessor Compatible 12-Bit DAC√AD9002√High Speed Monolithic 8-Bit ADC√AD9012√AD912√ADSP2100A12.5 MIPS DSP Microprocessor√AMP01Precision Instrumentation AmpAMP05Fast Settling JFET Instrumentation Amplifier√CMP04Low Power Comparator√MAT01Matched Transistor PairMAT02Low Noise, Matched Dual NPN TransistorMAT03Low Noise, Matched Dual NPN TransistorMAT04Matched Quad NPN Transistor√V OP08 / OP12Low-Input-Bias-Current Op Amp√OP200/400√OP249√OP249√OP249√PM108√PM108√PM108√PM108√PM108√PM111Precision High-Speed Comparator			AD630	Balanced Modulator / Demodulator
AD670Low Cost Signal Conditioning 8-Bit ADC√AD767µProcessor Compatible 12-Bit DAC√AD9002High Speed Monolithic 8-Bit ADC√AD9012High Speed TTL 8-Bit ADC√ADSP2100A12.5 MIPS DSP Microprocessor√AMP01Precision Instrumentation AmpAMP05Fast Settling JFET Instrumentation Amplifier√CMP04Low Power Comparator√MAT01Matched Transistor PairMAT02Low Noise, Matched Dual NPN TransistorMAT03Low Noise, Matched Dual NPN TransistorMAT04Matched Quad NPN Transistor√OP08 / OP12Low-Input-Bias-Current Op Amp√OP200/400Dual/Quad Low Offset, Low Power Op Amp√OP200Dual Precision High Speed Op Amp√OP50High Output Current (AVCL•5) Op Amp√PM108Low-Power Precision Op Amp√PM108Low-Power Precision Op Amp√PM108Low-Power Precision Op Amp√PM111Precision Comparator			AD632	Internally Trimmed Precision IC Multiplier
<ul> <li>√ AD767 µProcessor Compatible 12-Bit DAC</li> <li>√ AD9002 High Speed Monolithic 8-Bit ADC</li> <li>√ AD9012 High Speed TTL 8-Bit ADC</li> <li>√ ADSP2100A 12.5 MIPS DSP Microprocessor</li> <li>√ AMP01 Precision Instrumentation Amp AMP05 Fast Settling JFET Instrumentation Amplifier</li> <li>√ CMP04 Low Power Comparator</li> <li>√ MAT01 Matched Transistor Pair</li> <li>MAT02 Low Noise, Matched Dual NPN Transistor</li> <li>MAT03 Low Noise, Matched Dual PNP Transistor</li> <li>MAT04 Matched Quad NPN Transistor</li> <li>√ OP08 / OP12 Low-Input-Bias-Current Op Amp</li> <li>√ OP249 Dual Precision High Speed Op Amp</li> <li>√ OP50 High Output Current (AVCL+5) Op Amp</li> <li>√ OP50 High Output Current (AVCL+5) Op Amp</li> <li>√ PM108 Low-Power Precision Op Amp</li> <li>√ PM108 Single / Dual Low Input Bias Current Op Amp</li> <li>√ PM111 Precision High-Speed Comparator</li> </ul>			AD670 .	Low Cost Signal Conditioning 8-Bit ADC
√       AD9002       High Speed Monolithic 8-Bit ADC         √       AD9012       High Speed TTL 8-Bit ADC         √       ADSP2100A       12.5 MIPS DSP Microprocessor         √       AMP01       Precision Instrumentation Amp         AMP05       Fast Settling JFET Instrumentation Amplifier         √       CMP04       Low Power Comparator         √       MAT01       Matched Transistor Pair         MAT02       Low Noise, Matched Dual NPN Transistor         MAT03       Low Noise, Matched Dual PNP Transistor         MAT04       Matched Quad NPN Transistor         MAT04       Matched Quad NPN Transistor         √       OP08 / OP12       Low-Input-Bias-Current Op Amp         √       OP200/400       Dual/Quad Low Offset, Low Power Op Amp         √       OP249       Dual Precision High Speed Op Amp         √       OP50       High Output Current (AVCL•5) Op Amp         √       OP97/PM1012       Low-Power Precision Op Amp         √       PM108       Low-Power Precision Op Amp         √       PM108       Low-Power Precision Op Amp         √       PM108       Single / Dual Low Input Bias Current Op Amp         √       PM111       Precision Comparator         √       <		$\checkmark$	AD767	µProcessor Compatible 12-Bit DAC
√AD9012High Speed TTL 8-Bit ADC√ADSP2100A12.5 MIPS DSP Microprocessor√AMP01Precision Instrumentation AmpAMP05Fast Settling JFET Instrumentation Amplifier√CMP04Low Power Comparator√MAT01Matched Transistor PairMAT02Low Noise, Matched Dual NPN TransistorMAT03Low Noise, Matched Dual PNP TransistorMAT04Matched Quad NPN Transistor√V OP08 / OP12Low-Input-Bias-Current Op Amp√V OP200/400Dual/Quad Low Offset, Low Power Op Amp√V OP249Dual Precision High Speed Op Amp√OP50High Output Current (AVCL•5) Op Amp√PM108Low-Power Precision Op Amp√PM108Single / Dual Low Input Bias Current Op Amp√PM111Precision Comparator		$\checkmark$	AD9002	High Speed Monolithic 8-Bit ADC
<ul> <li>ADSP2100A</li> <li>12.5 MIPS DSP Microprocessor</li> <li>AMP01</li> <li>Precision Instrumentation Amp</li> <li>AMP05</li> <li>Fast Settling JFET Instrumentation Amplifier</li> <li>CMP04</li> <li>Low Power Comparator</li> <li>MAT01</li> <li>Matched Transistor Pair</li> <li>MAT02</li> <li>Low Noise, Matched Dual NPN Transistor</li> <li>MAT03</li> <li>Low Noise, Matched Dual NPN Transistor</li> <li>MAT04</li> <li>Matched Quad NPN Transistor</li> <li>MAT04</li> <li>Matched Quad NPN Transistor</li> <li>V OP08 / OP12</li> <li>Low-Input-Bias-Current Op Amp</li> <li>V OP249</li> <li>Dual Precision High Speed Op Amp</li> <li>V OP249</li> <li>Dual Precision Op Amp</li> <li>V OP50</li> <li>High Output Current (AVCL•5) Op Amp</li> <li>OP97/PM1012</li> <li>Low-Power Precision Op Amp</li> <li>PM108</li> <li>Low-Power Precision Op Amp</li> <li>PM108 / PM2108</li> <li>Single / Dual Low Input Bias Current Op Amp</li> <li>PM111</li> <li>Precision High-Speed Comparator</li> </ul>		$\checkmark$	AD9012	High Speed TTL 8-Bit ADC
√AMP01Precision Instrumentation Amp AMP05AMP05Fast Settling JFET Instrumentation Amplifier√CMP04Low Power Comparator√MAT01Matched Transistor PairMAT02Low Noise, Matched Dual NPN TransistorMAT03Low Noise, Matched Dual PNP TransistorMAT04Matched Quad NPN Transistor√√OP08 / OP12Low-Input-Bias-Current Op Amp√√√OP200/400∪ual/Quad Low Offset, Low Power Op Amp√√√OP249∪ual Precision High Speed Op Amp√OP50√High Output Current (AVCL•5) Op Amp√OP97/PM1012√Low-Power Precision Op Amp√PM1008√PM108√PM111Precision Comparator√PM111Precision High-Speed Comparator		$\checkmark$	ADSP2100A	12.5 MIPS DSP Microprocessor
AMP05Fast Settling JFET Instrumentation Amplifier√CMP04Low Power Comparator√MAT01Matched Transistor PairMAT02Low Noise, Matched Dual NPN TransistorMAT03Low Noise, Matched Dual PNP TransistorMAT04Matched Quad NPN Transistor√√ OP08 / OP12√VOP08 / OP12√OP200/400√OP249√OP249√OP50√OP50√OP97/PM1012√Low-Power Precision Op Amp√PM108√PM118√PM111Precision High-Speed Comparator√PM119√Precision High-Speed Comparator			AMP01	Precision Instrumentation Amp
<ul> <li>✓ CMP04</li> <li>Low Power Comparator</li> <li>✓ MAT01</li> <li>Matched Transistor Pair</li> <li>MAT02</li> <li>Low Noise, Matched Dual NPN Transistor</li> <li>MAT03</li> <li>Low Noise, Matched Dual PNP Transistor</li> <li>MAT04</li> <li>Matched Quad NPN Transistor</li> <li>✓ OP08 / OP12</li> <li>Low-Input-Bias-Current Op Amp</li> <li>✓ OP200/400</li> <li>Dual/Quad Low Offset, Low Power Op Amp</li> <li>✓ OP209</li> <li>✓ Dual Precision High Speed Op Amp</li> <li>✓ OP50</li> <li>✓ High Output Current (AVCL•5) Op Amp</li> <li>✓ OP50</li> <li>✓ PM1008</li> <li>Low-Power Precision Op Amp</li> <li>✓ PM108 / PM2108</li> <li>Single / Dual Low Input Bias Current Op Amp</li> <li>✓ PM111</li> <li>Precision Comparator</li> <li>✓ PM119</li> <li>Precision High-Speed Comparator</li> </ul>			AMP05	Fast Settling JFET Instrumentation Amplifier
<ul> <li>MAT01 Matched Transistor Pair</li> <li>MAT02 Low Noise, Matched Dual NPN Transistor</li> <li>MAT03 Low Noise, Matched Dual PNP Transistor</li> <li>MAT04 Matched Quad NPN Transistor</li> <li>√ √ OP08 / OP12 Low-Input-Bias-Current Op Amp</li> <li>√ 0P200/400 Dual/Quad Low Offset, Low Power Op Amp</li> <li>√ 0P249 Dual Precision High Speed Op Amp</li> <li>√ 0P50 High Output Current (AVCL•5) Op Amp</li> <li>√ 0P97/PM1012 Low-Power Precision Op Amp</li> <li>√ PM108 PM2108 Single / Dual Low Input Bias Current Op Amp</li> <li>√ PM111 Precision Comparator</li> <li>√ PM119 Precision High-Speed Comparator</li> </ul>		$\checkmark$	CMP04	Low Power Comparator
MAT02Low Noise, Matched Dual NPN TransistorMAT03Low Noise, Matched Dual PNP TransistorMAT04Matched Quad NPN Transistor√√√OP08 / OP12√OP200/400√OP249√OP250√OP50√OP50√OP97/PM1012↓Low-Power Precision Op Amp√PM1008√PM108 / PM2108√Single / Dual Low Input Bias Current Op Amp√PM111Precision Comparator√PM119Precision High-Speed Comparator		$\checkmark$	MAT01	Matched Transistor Pair
MAT03Low Noise, Matched Dual PNP TransistorMAT04Matched Quad NPN Transistor√√√OP08 / OP12√OP200/400√OP249√OP250√OP50√OP97/PM1012√OP97/PM1012√PM1008√PM108 / PM2108√Single / Dual Low Input Bias Current Op Amp√PM111√PM119√PM119√PM109√PM109√PM109√PM109√PM19√PM19√PM19√PM19			MAT02	Low Noise, Matched Dual NPN Transistor
MAT04Matched Quad NPN Transistor√√OP08 / OP12Low-Input-Bias-Current Op Amp√OP200/400Dual/Quad Low Offset, Low Power Op Amp√√OP249Dual Precision High Speed Op Amp√OP50High Output Current (AVCL•5) Op Amp√OP97/PM1012Low-Power Precision Op Amp√PM1008Low-Power Precision Op Amp√PM108 / PM2108Single / Dual Low Input Bias Current Op Amp√PM111Precision Comparator√PM119Precision High-Speed Comparator			MAT03	Low Noise, Matched Dual PNP Transistor
√√OP08 / OP12Low-Input-Bias-Current Op Amp√OP200/400Dual/Quad Low Offset, Low Power Op Amp√√OP249Dual Precision High Speed Op Amp√OP50High Output Current (AVCL•5) Op Amp√OP97/PM1012Low-Power Precision Op Amp√PM1008Low-Power Precision Op Amp√PM108 / PM2108Single / Dual Low Input Bias Current Op Amp√PM111Precision Comparator√PM119Precision High-Speed Comparator			MAT04	Matched Quad NPN Transistor
√       OP200/400       Dual/Quad Low Offset, Low Power Op Amp         √       √       OP249       Dual Precision High Speed Op Amp         √       OP50       High Output Current (AVCL•5) Op Amp         √       OP97/PM1012       Low-Power Precision Op Amp         √       PM1008       Low-Power Precision Op Amp         √       PM108 / PM2108       Single / Dual Low Input Bias Current Op Amp         √       PM111       Precision Comparator         √       PM119       Precision High-Speed Comparator		$\checkmark$	√ OP08 / OP12	Low-Input-Bias-Current Op Amp
√√OP249Dual Precision High Speed Op Amp√OP50High Output Current (AVCL•5) Op Amp√OP97/PM1012Low-Power Precision Op Amp√PM1008Low-Power Precision Op Amp√PM108 / PM2108Single / Dual Low Input Bias Current Op Amp√PM111Precision Comparator√PM119Precision High-Speed Comparator		$\checkmark$	OP200/400	Dual/Quad Low Offset, Low Power Op Amp
√       OP50       High Output Current (AVCL•5) Op Amp         √       OP97/PM1012       Low-Power Precision Op Amp         √       PM1008       Low-Power Precision Op Amp         √       PM108 / PM2108       Single / Dual Low Input Bias Current Op Amp         √       PM111       Precision Comparator         √       PM119       Precision High-Speed Comparator		$\checkmark$	√ OP249	Dual Precision High Speed Op Amp
√       OP97/PM1012       Low-Power Precision Op Amp         √       PM1008       Low-Power Precision Op Amp         √       PM108 / PM2108       Single / Dual Low Input Bias Current Op Amp         √       PM111       Precision Comparator         √       PM119       Precision High-Speed Comparator		$\checkmark$	OP50	High Output Current (AVCL•5) Op Amp
<ul> <li>✓ PM1008</li> <li>✓ PM108 / PM2108</li> <li>✓ PM108 / PM2108</li> <li>✓ PM111</li> <li>✓ PM111</li> <li>✓ PM119</li> <li>✓ Precision High-Speed Comparator</li> </ul>		$\checkmark$	OP97/PM1012	Low-Power Precision Op Amp
<ul> <li>√ PM108 / PM2108</li> <li>√ PM111</li> <li>√ PM111</li> <li>√ PM119</li> <li>√ Pm119</li> <li>√ Precision High-Speed Comparator</li> </ul>			PM1008	Low-Power Precision Op Amp
PM111Precision Comparator $$ PM119Precision High-Speed Comparator			PM108 / PM2108	Single / Dual Low Input Bias Current Op Amp
√ PM119 Precision High-Speed Comparator		$\checkmark$	PM111	Precision Comparator
		$\checkmark$	PM119	Precision High-Speed Comparator
$\sqrt{\sqrt{PM139}}$ Ouad General Purpose Comparator		$\checkmark$	√ PM139	Quad General Purpose Comparator
$\sqrt{\text{REF43}}$ +2.5V Low Power Precision Reference		$\checkmark$	REF43	+2.5V Low Power Precision Reference

July 13, 1998

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CRITERIA 2. \* : ELECTROMICS\_SBW 2 BOXC\_NOW

HENCE MANIST FREE 2 2: BOULNEW & A



BEREND WINTER



Structure-Detector

Contents:

- Mechanical requirements
- Geometrical requirements





Quasi Static levels	Case 1	Case 2	Case 3	Case 4	
x-direction (ref. sketch)					
Longitudinal		22.5 g	22.5 g	-	-
y-direction (ref. sketch)					
Lateral		<mark>3</mark> g	-	<mark>6</mark> g	-
z-direction (ref. sketch)					
Lateral		-	<mark>3</mark> g	-	<mark>6</mark> g

#### QUALIFICATION (TBC)



Sine vibration levels (all directions)

Frequency range Input at base

5-18 Hz22 mm (peak-peak)18-100 Hz15 g

**QUALIFICATION (TBC)** 



PSD input for qual. random vibration (TBC) RMS 7.4 g







QUALIFICATION (TBC)





#### QUALIFICATION (TBC)

#### Geometrical environment

**MSSL** 





#### Geometrical environment










Detector meeting Saclay 28/29 Sep. 1999

# Conclusions

- Mechanical environment
  - severe sine vibration spec
  - eigenfrequency structure > 120 Hz
  - eigenfrequency detector boxes > 150 Hz
  - eigenfrequency detectors > 300 Hz
  - relaxation of sine spec.



# Conclusions

- Geometrical Environment
- nose of detector < 65 mm diameter

 $\sim$ 

- bottom of detector < 75 mm diameter</li>
- mounting plane through CoG - mounting within this endope ?
- tow About Accoment
- How Abour REI LIGHT TIGHINESS

Detector meeting Saclay 28/29 Sep. 1999

#### **Beam Profile Modelling**

#### **Bruce Swinyard**

29/30 Sept 1999

SPIRE Bolometer Array Group Meeting

#### Beam Profile Modelling

- Telescope design has changed not included in latest model results from Martin
- Tony is concentrating on the FTS design in order to correctly size the exit apertures
- Beam sizes and distortion of field passed to simulations folk as IDL routine and table of positions
- ASAP model now includes real size of detector pixel for bare arrays
- Single Gaussian mode used for simulating feedhorns
  - FWHM 250 17.56 arcsec 350 - 24.73 arcsec 500 - 35.36 arcsec

SPIRE Bolometer Array Group Meeting



29/30 Sept 1999





SPIRE Bolometer Array Group Meeting



29/30 Sept 1999

SPIRE Bolometer Array Group Meeting

#### **Bruce Swinyard**

30 Sept - 1 Oct 1999

SPIRE Systems Team, Saclay

- Operating Modes Document in its infancy
- It will try to define the requirements on the WE; OBS and Ground segment for all operating modes of the SPIRE instrument
- Concentration is on the Observing Mode for the time being
- First draft has 7 (ish) "Observatory Functions" defined for the feedhorn option
- Try to use these to define the "Instrument Functions" and "Data Configurations"
  - These then set the requirements on the WE; OBS and Ground segment.



30 Sept - 1 Oct 1999

SPIRE Systems Team, Saclay



• Observatory functions - examples

• POF1	:	Chop Without Jiggling
• POF2	•	Seven-Point Jiggle Map
POF3	•	Sn-Point Jiggle Map
• POF4	:	Raster Map
• POF5	:	Scan Map Without Chopping
• POF6	:	Scan Map With Chopping
• POF6	:	Photometer Peak-Up
• POF7	:	Operate photometer internal calibrator

Table TBD: Photometer Observatory Function POF2: Seven-Point Jiggle Map							
Instrument Function: Photometer Chop							
No.	Parameter	Range of values	Nominal value	Comments			
1	Prime detector	One of the two	TBD	This position on the array is			
		triple-overlap		aligned on-source for nod			
		positions in the		position 1.			
		centre of the arrays		Common with POF1.			
2	Chop frequency	0.3 (TBC) - 5 Hz	2 (TBC)	Common with POF1.			
3	Chop direction	Any direction in the	Parallel to the	Common with POF1.			
		Y-Z plane	Y-axis				
4	Chop throw	Any value within	126" on the sky	Common with POF1.			
		the BSM range (4	parallel to Y-				
		arcmin. in Y; 0.5	axis				
		arcmin in z)					
Instrument Function: Photometer Jiggle							
1	Jiggle pattern	7-point (central +	$\theta = 6$ arcsec.				
		hexagon) with					
		separation $\theta$					
2	Number of chop	Min = 5	Such as to give				
	cycles/jiggle position	Max = TBD	roughly 1 minute				
			per jiggle cycle				
3	Number of jiggle	N = 1 - TBD	1				
	cycles/nod position						
4	Total integration time	Min = 2 jiggle	None	Only required for nodding OFF			
		cycles					
		Max = TBD					
Telescope Function: Nod							
1	Nodding	ON or OFF	ON	Nodding is optional			
2	Telescope nod	Determined by the	Set to allow one				
	period	time taken for N	jiggle cycle per				
		jiggle cycles	nod position				
3	Nod direction	Same as the chop	Parallel to the				
		direction	Y-axis				
4	Nod throw	Same as the chop	126"				
		throw					
5	Total number of nod	Min = 2	TBD	Specifies total integration time if			
	cycles	Max = TBD		nodding is ON			

#### **Spire Simulations**

Seb Oliver and Neal Todd

#### Overview

Goals

- Overview of Simulation Method
- Current Status
- Latest Results
- Future Steps

SIMULATIONS DONE/IN PROGRESS

250, 350, 500 p

2 λ FILLED ARRAY } 4' \* 8' F.O.V. 2 λ FEED HORNS

3" + 1" MAPS @ 3" SUBPIXEL RESOLUTION

OBSEVATIONS (SIM. DRIFTSCAN) : 1. 5040 × 8 POINTINGS (3° K 45") 2"14 STEP × 4" (60"/s < 28Hz)

10 day To TAL TIME - I he ISM ON EACE BIT OF SKY

2. 5040 × 1 POINTING WITH MAP O 1" SUBPIXEL RESOLUTION.

REQUIREMENTS

450 MHZ PII 256 MB RAM (128 THE SWAP) 3° × 1° MAP PRODUCTION (@ 3"/pix) : 30 MINS. DESCRYATION + ST STAGE REDUCTION : 40 MINS. (UNLOADED MACHINE)

MAP PRODUCTION REQUIRES MINIMUM OF 100MB

$$\underline{Z} \cap (\overline{U}, \overline{U})$$

$$\underline{Z} \cap (\overline{U}, \overline{U})$$

$$\underline{Z} \cap (\overline{U}, \overline{U}) = \underline{Z} \cap (\overline{U}, \overline{U}) + (\overline{U}, \overline{U})$$

$$\underline{Z} \cap (\overline{U}, \overline{U}) + (\overline{U}, \overline{U}) + (\overline{U}, \overline{U})$$

$$\underline{Z} \cap (\overline{U}, \overline{U}) + (\overline{U}, \overline{U})$$

$$\underline{$$

case of notice = 
$$\sigma(\underline{r})$$
  
Min Variane  $W(\underline{r}, \underline{r}_0) = P^{\perp}(\underline{r} - \underline{r}_0) / \sigma^{\perp}(\underline{r})$   
 $\Rightarrow \hat{f}(\underline{r}) = \frac{P(\underline{k}) \frac{S}{\sigma^2}}{P^2 \otimes \frac{1}{\sigma^2}}$   
Give  $\overline{\sigma^2(\underline{r})} \times \overline{\delta(\underline{r})}$   
 $= \frac{P \otimes S}{P^2 \otimes S}$ 

But could choose ...  $\omega(\underline{r},\underline{r}_{\circ}) = \omega'(\underline{r}-\underline{r}_{\circ})/\sigma^{2}(\underline{r})$ eq.  $\omega'(\underline{r}-\underline{r}_{\circ}) = p^{2}(\underline{r}-\underline{r}_{\circ})/2$   $\omega'(\underline{r}-\underline{r}_{\circ}) = \begin{cases} p^{2}(\underline{r}-\underline{r}_{\circ}) & |\underline{r}-\underline{r}_{\circ}| \leq r \\ 0 & |\underline{r}-\underline{r}_{\circ}| \geq r \end{cases}$ 

#### Goals of SPIRE Simulations

Assess Instrument Design Options e.g.

- Filled Arrays vs. Feed Horns
  - Impact on confusion noise
  - Impact on mapping speed
- Filter choice
- Assess Observation modes & Strategies
- Assess Data Reduction Methods and Quality of Data Products

### Simulation Ingredients

- Synthetic Sky
- Instrument Model
- Observing Modes
- Data Reduction
  - Maps
  - Source lists
- Data Assessment

# Synthetic Sky

#### Point Sources

- Model Counts full range of valid models
- Model Colours to test multiλ capabilities
- Model N(z) & P(k) to assess clustering
- Real Sources for observation planning
- Background
  - Cirrus Emission espec. near Galactic plane
  - Zodiacal Light

probably unimportant

#### Instrument Model

#### Beam profile of detector on sky includes coupling of detector to telescope $f(x,y)=I_n(a,d)*B_n$

Power absorbed by detector  $P = f A_{tel} \Delta_n h_{opt} h_{det}$ 

Noise Addition

$$\boldsymbol{s}_{p} = \frac{NEP_{TOT}}{\sqrt{2t}}$$

#### **Current Status**

#### Sky Model

- N(S) models independent across bands
- Low resolution Cirrus
- Instrument/Observing Modes
  - 3 filters 250, 350, 500µm
  - Feed Horn & Filled arrays
  - Single NEP & 2 detector Q. Efficiencies
  - Raster & 64 pt. Jiggle Map
  - Chopped & Un-chopped
  - Scan mapping

# Current Status (ctd.)

#### Data Reduction & Analysis

- Arbitrary map weighting function
- Statistics of intensity map, P(D)
  - Gaussian Fit Gaussian Fit sigma

RMS trimmed at fixed "classical" confusion level

- FWHM
- Itterative Condon s=

$$\mathbf{s} = \sqrt{\int_0^{3\mathbf{s}} \frac{dN}{\int_0^{3\mathbf{s}} dN}}$$

- Intensity in map at position of input sources
- Source extraction, reliability and completeness

#### Limits to Super-Resolution

- With no noise & infinite sampling it is possible to recover infinite resolution
- In practice noise & finte sampling provide constraints
- Leon Lucy has calculated theoretical limits to Super Resolution from photon counting
  - Perfect Instrument: records exact possition of  $\nu$
  - Ideal reconstruction:



# Limits to Super-Resolution (ctd.)

Point Sources vs. Extended Sources

2 Point Sources vs. Extendended Source

 $\underline{\boldsymbol{s}_{Natural}} \propto N^8$ 

 $\boldsymbol{S}_{Super}$ 

 $\frac{\mathbf{S}_{Natural}}{\mathbf{S}_{Natural}} \propto N^4$ 

 $\boldsymbol{S}_{Super}$ 

# Figures of Merit

#### Images

- Measure of dispersion in P(D)
- Must be robhust
- Must be intuative
- Must measure confusion

- Catalogues
  - Completeness
  - Reliability
  - Photometric accuracy
  - Astrometric accuracy



#### 250µm Horn vs Filled Array



#### 250µm Horn Vs Filled Array



#### 250µm Horn Vs Filled Array



# 250µm Un-chopped Vs Chopped



# 250µm Un-chopped Vs Chopped



# 250µm Un-chopped Vs Chopped



# 250µm Beam Vs Square Footprint



# 250µm Beam Vs Square Footprint


# 250µm Beam Vs Square Footprint



## Conclusions

- Little Difference between horns & filled arrays w.r.t. confusion noise
- Chopping significantly worsens confusion noise
- Data reduction techniques crucial
- Trimmed RMS appears to be a reasonable "figure of merit" for confusion noise

## Future Improvements

## Sky Model

- Coherent Source lists at multi-λ
- Generalised Source count models
- Clustering of point sources
- High-resolution Cirrus maps
- Instrument/Observing modes
  - More bands (including PACS)
  - Finer details...

## Future Improvements (Ctd.)

Data Reduction & Analysis

- Hyper-resolution reduction techniques (e.g. CLEAN)
- Assess completeness & reliability of extracted sources
- Refine quality criteria

# Simulations of filled array observations

**Harvey Moseley** 

### Sampling + Dithering.

- Spatial dither patters controls spatial correlation of noise in extracted images
- We are working on developing best scon pattern combining Scanning and dithering with sconminvor.



Derived Gain/True Gain: [1.005,1.015]



,





slice of x = 64



Simulated WIRE Image: (0,0) dither: [8e3,1.2e4]

Derived Gain: [0.8,1.2]



Thick Crust

#### **FIGURE OF MERIT** for dither patterns

$$FOM = V_{p0p0} / \Sigma |V_{ip0}|$$

 $V_{ij}$  = covariance matrix for the detector  $V_{ij}$  = idealized covariance matrix where  $V_{ij}$  = 0 for  $i \neq j$  $p_0$  = selected reference pixel (row or column)

 $0 \le FOM \le 1$ 



F;g. 4

## Gain Errors for Simulated WIRE Date



T :

## NICMOS HDF-S







Derived Gain



Derived Offset





Cal. Flat





#### Matt Griffin Viewgraph Summarising Simulations Discussion

· PRIORITIES:

- SCANNING SPEED CONSTRAINTS AND INFLUENCE OF 1/6 NOISE
- DETAILS OF ARRAY READOUT AND JA
- ANY SIGNIFICANT DIFFERENCES IN OVERHEADS
- KNOW AS ACURATELY AS POSSIBLE THE MAPPING SPEED DIFFERENCES BETWEEN THE 3 OPTIONS INFLUENCE OF TELEMETRY (LIMITS FILLED AREAMS)